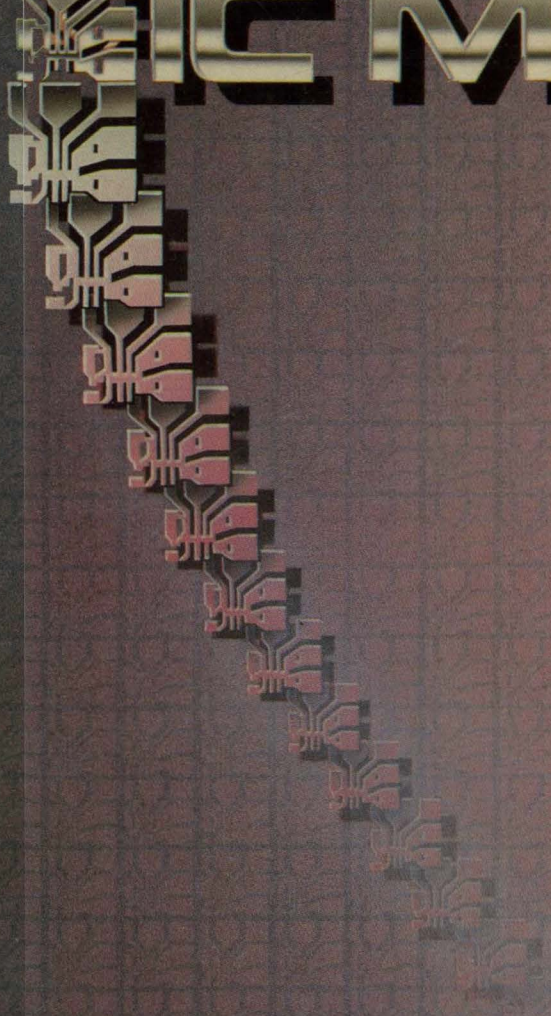
1989

IC MASTER



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HOW TO USE THE IC MASTER

The 1989 edition of the IC MASTER is arranged in three volumes. Each volume serves a specific purpose to help you find the integrated circuit or related product you need. The table of contents on page 1 describes what is in each volume. The table also includes the starting page number for each advertiser.

The IC MASTER is a functional work. You know what you need. The MASTER helps you find it.

Here are typical problems.

Q. What kinds of functions does the MASTER cover?

A. Turn to page 10 in **Volume One**. Here is a complete list of the devices covered. The page and line numbers refer you to the beginning of the Section in which a particular function appears.

Q. Who makes a 16384 x 1 static RAM with an access time of 70 ns or faster? What are my technology choices?

A. Pick up Volume 1. Turn to the MEMORY section. The first page of the section tells you where the listings of your device begins. See this under:

RAMS
Bubble
Dynamic
Static

Turn to the first page of static RAMs. In the first column you see the **Organization**. Browse through the pages until you reach the **16384 x 1** listings. Now look through the listings until you find the access time and characteristics you need. Device numbers are shown by manufacturer. The device numbers of advertisers in the 1989 IC MASTER appear in **bold face**. The page number following the device number is where additional information may be found in **Volume Two**. At the extreme right you will see line numbers. These are the specific lines where a device appears.

Q. Which microprocessors are listed in the MASTER? How do I find the microprocessor I need?

A. All commercially available microprocessors are listed in the MASTER. Start with the **microprocessor** listing in the **Master Selection Guide Index** (starts on page 10). Here you will find the various kinds of products you will need listed according to function and bit size. Turn to the various pages shown and then to the advertiser's page where more detail may be available.

Q. Who makes a Dual, Low Offset Voltage Op Amp?

A. This is a **LINEAR** device. Turn to the LINEAR section in Volume One. The first page of the section shows the starting page for each type of device. Turn to the page where **Dual Units** appear. Look down the list for the device you need. Advertisers' devices are listed in **bold face**. Turn to the page in Volume Two where more information may be available.

Q. I need an IC with Music capability. Which Master Selection Guide should I use?

A. Turn to the **Master Selection Guide Index** starting on page 10. Look through the list until you find **Music**. The page numbers for each kind of device are shown.

Q. I plan to use a digital gate array or some other semicustom ASIC in my next project. Where do I find it in the MASTER? Who makes these things?

A. Turn to Volume Three. Turn to the first page of **ASICs/Custom**. Find Gate Arrays and all of the other devices listed here. Now you can find the device you need. After you find the type of device you need, turn to the proper page and find the manufacturer. Advertisers' pages follow the selection guides in Volume three.

Q. I know the digital IC I need is available. Is it available in a surface mount package?

A. There are two ways to solve this problem. If you know the manufacturer's device number, turn to the Part Number Index in Volume One. Find the basic number and the page number and line where that device is listed in the MASTER. Turn to that page. If the device is available for surface mounting, an open diamond symbol will appear. You can also turn directly to the DIGITAL section and turn to the function of the device you want. The symbol will indicate an SMD is available.

Q. I am looking for an application note on a specific device. Where can I find out if one is currently available?

A. Pick up Volume One. Turn to the Application Note Directory. Here you will find app notes arranged by **function**. Find the function involved and turn to the page where the app note is listed.

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Q. We need a device that meets MIL standards. Where do I look in the MASTER?

A. Turn to the MILITARY Section in Volume One. The Military Device Testing table shows which manufacturers do what kinds of MIL work. Followed by the MIL-STD-1562R directories for microcircuits which contains six tables relating to various standards of classification. The next list is a QPL listing based on the latest Defense Electronics Supply Center (DESC) Qualified Product Listing. Additional Information is often supplied by the advertisers' pages in Volume Two.

Q. I know the basic part number is 2502 and that's all I know. Where do I look?

A. That's easy in the MASTER. Turn to the Part Number Index. All prefixes and suffixes have been stripped away. Turn to the page where 2502 appears. All manufacturers with that kind of number appear in order along with the page and line number where the device is described.

Q. How many manufacturers claim to make a pin-for-pin function-for-function equivalent to a Motorola MC68000?

A. Turn to the Alternate Source Directory in the back of Volume One. Turn to Motorola. Those manufacturers who claim to be equivalent are listed in order. If you have an MS-DOS computer with a hard drive, you can get the 1989 IC MASTER **Alternate Source Directory** on a disk. The disk is Clipper compiled from dBase III + and is delivered compressed by PKARC. This is the complete list of alternate sources and allows you to add notes such as your own part numbers, prices, sources and the like. Call Hearst (516) 227-1300 and ask for Book Sales for further information.

Q. I looked in the Alternate Source Directory. The part I want an alternate source for isn't listed. Why not?

A. Are you sure you looked through the entire listing for the original manufacturer? Some devices may be listed in odd ways depending on how the MASTER's editors receive the information. Then there is the probability that no other manufacturer makes an exact replacement for your part. It is important for you to understand how the Alternate Source Directory is compiled. Manufacturers supply the information that **their** part is an exact replacement for **another** part. The original manufacturer does **not** tell us his part can be replaced by those listed.

Q. I need an $^{8}/_{16}$-bit microcomputer board with an 8 MHz clock frequency and a Multibus support system. Can I find this in the MASTER?

A. Yes! Pick up Volume Three. Turn to the MICROCOMPUTER BOARD Section. Continue to turn pages until the $^{8}/_{16}$ appears in the first column. Then look at all of the available boards to find the board you can use.

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Q. I have a Valid Logic's "Summary" workstation. Which front end tools are compatible? Can I get one with circuit simulation? What capabilities does it have? Who makes it?

A. Pick up Volume Three. Turn to the Design Automation Section. Check the first page. You will see what is available in the Section. Under Design Tools you will find Front End Tools and Circuit Simulators. Read down for your parameters and across for the vendor.

Q. What do the manufacturers' part numbers mean? I have a Signetics N8X02N. What do all the letters and numbers mean?

A. Look in Volume One for the Part Number Guide. Turn to the Signetics portion. Now you know the **N** prefix means, zero to plus seventy degrees Centigrade. The **N** suffix indicates the package style. The numbers and letters in the middle are the device type. Each manufacturer has a different code system. Understanding the system is a great help in comparing devices.

Q. I found the device I want in the MASTER. What are the pinouts? Where can I get more details? Where can I get a price? What is the delivery time?

A. You have just defined exactly what the IC MASTER does. The MASTER is a guide to tell you which devices are available on a commercial basis. After you know this, the next step is to contact the manufacturer, a local sales office or a distributor.

Q. Where can I find the addresses and telephone numbers of manufacturers, local sales offices and distributors?

A. Pick up Volume Two. Turn to the Manufacturers and Distributors Directory. Read the first page. The information on this page will help you understand why the information in the Directory is so important. It will save you time and aggravation.

Q. I just saw a new device advertised in Electronic Products magazine. It isn't listed in the MASTER. Why not? When will it be listed?

A. Preparing the information for the annual IC MASTER is a tremendous undertaking. It requires the cooperation of every single manufacturer. All of the material must be organized, cross referenced and placed in the data base. This data base must be closed off in November in order to meet the publishing date of late January. That is why some devices are not listed. They came on the market too late for the deadline. There are two updates to the annual MASTER. They are called the **IC MASTER UPDATE**. One is issued in the late Spring and the other in early Fall. Be sure to sign up for copies when you get your new IC MASTER. If you are not sure whether or not you have requested the updates, please write to the Circulation Department at the address shown on page 2 of this MASTER. Be sure to indicate which edition of the MASTER you are using.

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ABBREVIATIONS OF COMPANY NAMES

AB Assoc	A.B. Associates, Inc.
ABB HAFO	ABB HAFO Inc.
Abionics	Abionics Inc.
ACASI	American Computer Automated Systems, Inc.
Actel	Actel Corporation
AD	Analog Devices
Adams-Russell	Adams-Russell Electronics Co., Inc.
Adv Analog	Advanced Analog
AdvControl	Advanced Control Systems
AdvDigital	Advanced Digital Corporation
AdvLinear	Advanced Linear Devices
AdvMicroSys	ADVANCED MICRO SYSTEMS, INC.
AI Architects	A. I. Architects, Inc.
AjidaTech	Ajida Technologies, Inc.
Alcyon	Alcyon Corporation
Aldec	Aldec - Automated Logic Design Co.
AllenSys	Allen Systems
Alloy	Alloy Computer Products
AlpsAmerica	Alps America
Altera	Altera Corporation
AMA	American Automation
AMCC	AMCC (Applied Micro Circuits Corporation)
AMD	Advanced Micro Devices, Inc.
AmerMicro	American Micronics, Inc.
Amperex	Amperex Electronic Company
Ampro	Ampro Computers, Inc.
Amtelco	Amtelco
Anadigics	Anadigics
AnalDesTools	Analog Design Tools, Inc.
Analogic	Analogic Corporation
AnalogSys	Analog Systems
Analogy	Analogy Inc.
Anasco	Anasco Corp.
Antona	Antona Corporation
Apex	Apex Microtechnology Corporation
ApplSys	Applied Systems Corporation
AppMicroSys	Applied Microsystems Corporation
Aptek	Aptek Microsystems
Aptos	Aptos Systems
ArrayTech	Array Technology
Aspen	Aspen Semiconductor Corp.
Astro	Astrosystems, Inc.
AT&T	AT&T Technologies, Dept. LT
ATD	Advanced Transducer Devices, Inc.
Atec	Atec, Inc.
Atlanta	Atlanta Signal Processors, Inc.
Atmel	Atmel Corporation
Augat	Augat Inc.
AutoDesk	AutoDesk
AutoSys	Automated Systems Inc.
B&C Micro	B & C Microsystems Inc.
Barvon	Barvon BiCMOS Technolgy Inc.
Basicon	Basicon, Inc.
Bedford	Bedford Control Systems
Berne	Berne Electronics Inc.
BICC-VERO	BICC-VERO Electronics
BinaryTech	Binary Technology, Inc.
Bipolar	Bipolar Integrated Technology
Bishop	Bishop Inc.
Bit3 Comp	Bit 3 Computer Corporation
Brainpower	BrainPower, Inc.
Brooktree	Brooktree Corporation
Buckminster	Buckminster Corp.
Bummer	Bummer Electronics
Burr-Brown	Burr-Brown Corporation
CAD Group	CAD Group Inc.
Cadam	CADAM Inc.
Cadence	Cadence Design Systems, Inc.
Cadic	Cadic, Inc.
Cadisys	Cadisys Corp.
Cadnetix	Cadnetix Corporation
Cadre	Cadre Technologies, Inc.
CAECO	Caeco
Calay	Calay Systems, Inc.
CalDevices	California Devices Inc.
Calmos	Calmos Semiconductor Inc.
Calos	Calos, Inc.
Can-Tron	Can-Tron
CaseTech	Case Technology
Catalyst	Catalyst Research
CentData	Central Data Corporation
Cermetek	Cermetek Microelectronics, Inc.
CharlesRiver	Charles River Data Systems
Cherry Semi	Cherry Semiconductor Corporation
Chips&Tech	Chips and Technologies, Incorporated
Chrislin	Chrislin Industries, Inc.
Ciprico	Ciprico Inc.
Cirrus	Cirrus Logic, Inc.
Clearpoint	Clearpoint, Inc.
CMC Intl	Communication Machinery Corporation (CMC)
CMD ASIC	California Micro Devices Corporation
CMD Micro	California Micro Devices Corporation
Codar	Codar Technology, Inc.
Comark	Comark Corporation
Comlinear	Comlinear Corporation
Commodore	Commodore Semiconductor Group
Compact	Compact Software
Compass	Compass Development, Inc.
CompDyn	Computer Dynamics Sales
CompModules	Computer Modules Inc.
Computrol	Computrol Inc.
CompVision	Computervision
ConnMicro	Connecticut MicroComputer, Inc.
Contemporary	Contemporary Control Systems, Inc.
Context	Context Corp.
ControlData	Control Data
Controlex	Controlex Corporation
Conway	Conway Engineering, Inc.
CreMicro	Creative Micro Systems
Crystal	Crystal Semiconductor Corp.
CTI	Circuit Technology Inc.
Cubit	Cubit Inc.
CustomArrays	Custom Arrays Corp.
Cyberchron	Cyberchron Corporation
Cybernetic	Cybernetic Micro Systems
Cypress	Cypress Semiconductor Corp.
Daisy	Daisy Systems
Dallas	Dallas Semiconductor
Dasoft	Dasoft Designs Systems, Inc.
dataCon	Datacon
Datacube	Datacube Inc.
DataGen	Data General
Datal/O	Data I/O Futurenet
DataLinear	Datalinear
Dataram	Dataram Corp.
DataTrans	Data Translation, Inc.
Datel	Datel, Inc.
Datricon	Datricon Corporation
Davidge	Davidge Corporation
Den/Pas	Densan/Pascot
Dense-Pac	Dense-Pac Microsystems, Inc.
Descartes	Descartes Automation Systems, Inc.
DesignComp	Design Computation
Devtek	Devtek Systems
Dexter	Dexter Research Center, Inc.
Digital RF	Digital RF Solutions Corp.
Digitronics	Digitronics Sixnet
Dionics	Dionics Inc.
DistComp	Distributed Computer Systems
DKL	DKL Technology, Inc.
Douglas	Douglas Electronics
DSB Systems	DSB Systems
DSP-Systems	DSP Systems Corporation
Dual	Dual Systems Corporation
ECI Semi	ECI Semiconductor
EDA Systems	EDA Systems
EDI	Electronic Designs Inc.
EdsunLabs	Edsun Laboratories, Inc.
EES	Electrical Engineering Software, Inc.
EEsof	EEsof Inc.
EG G-Reticon	EG&G Reticon Corporation
Elantec	Elantec, Inc.
ElecConServ	Electronics Consulting Service
ElecDesign	Electro Design, Inc.
Electrologic	Electrologic, Inc.
Elxsi	Elxsi
Enterprise	Enterprise Systems Corp.
EPIC	EPIC Design Technology, Inc.
Ericsson	Ericsson Components
ESP	Electronic Software Products
Essex	
Exar	Exar Corporation
Excelan	Excelan, Inc.
EXEL	EXEL Microelectronics, Inc.
Faraday	Faraday Electronics
Ferranti	Ferranti Electric, Inc.
Force	Force Computers, Inc.
Ford	Ford Microelectronics, Inc.
Fujitsu	Fujitsu Microelectronics, Inc.
Fujitsu A	Fujitsu America
FutureNet	FutureNet

When contacting suppliers, say you saw it in IC MASTER

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GainElec	Gain Electronics Corp.
Galil	Galil Motion Control
Gateway	Gateway Design Automation Corp.
Gazelle	Gazelle Microcircuits, Inc.
GE/Intersil	GE/Intersil, Inc.
GE/RCA	GE/RCA
GenMicro	General Micro Systems Inc.
Gennum	Gennum Corporation
Genoa	Genoa Systems Corp.
GenRad	GenRad Inc.
GENROCO	GENROCO
Gerber	Gerber Scientific Instrument
GigaBit	GigaBit Logic
Golden	Golden Electronics Inc.
GoldStar	GoldStar Semiconductor Ltd.
Gordos	Gordos Arkansas
Gould/AMI	Gould/AMI
GTSys	GT Systems, Ltd.
GW-Three	GW Three Inc.
Harris	Harris Semiconductor
Harris/SciCal	Harris/Scientific Calculations
HEI	HEI Corporation
Hercules	Hercules Computer Technology
Heurikon	Heurikon Corporation
HHB-Sys	HHB Systems
HiLevel	Hilevel Technology, Inc.
Hitachi	Hitachi America, Ltd.
HiTech	HiTech Equipment Corp.
Holt	Holt, Integrated Circuits, Inc.
Honeywell	Honeywell
Honeywell SPT	Signal Processing Technologies
HP	Hewlett-Packard-Logic Systems Division
Hughes	Hughes Aircraft Co.
HybridSys	Hybrid Systems Corporation
HyComp	Hy Comp Inc.
Hytek	Hytek Microsystems, Inc.
Hyundai	Hyundai Electronics America
IBC	IBC
IBM	IBM
IC Designs	IC Designs
IC Editors	IC Editors, Inc.
IC Options	IC Options, Inc.
IC Technology	Integrated Circuit Technology
ICDC	Integrated Circuit Design Centre (PTY) Ltd.
ICI	Integrated Circuits Inc.
ICT	International CMOS Technology
ICT Comp	ICT Computer Drafting Systems, Inc.
IDT	Integrated Device Technology, Inc.
IIC	Industrial Information Controls
Ikon	IKON Corp.
Ikos	IKOS Systems, Inc.
ILC-DDC	ILC Data Device Corp.
iLSi	Integrated Logic Systems Inc.
Imaging	Imaging Technology Inc.
IMI	International Microcircuits, Inc.
IMP	International Microelectronic Products
IndComp	Industrial Computer Designs
IndTech	IndeTech, Inc
Info Research	Information Research Associates
Inmos	Inmos
InnovRes	Innovative Research, Inc.
Inova	Inova Microelectronics Corp.
InrVision	Innervision Computers
IntCirSys	Integrated Circuit Systems, Inc.
Intel	Intel Corporation
Interactive	Interactive Circuits and Systems, Ltd.
Intercept	Intercept Microelectronics
InterconMicro	Intercontinental Microsystems
Interdesign	Ferranti Interdesign, Inc.
Intergraph	Intergraph
Interphase	Interphase Corp.
IntMeasSys	Integrated Measurement Systems
Intronics	Intronics, Inc.
Intusoft	Intusoft
Inventive	Inventive Systems, Inc.
Io Inc	Io Incorporated
IPS	Integrated Power Semiconductors, Ltd.
Ironics	Ironics Inc.
Isocom	Isocom Inc.
ITT	ITT Semiconductors
IXYS	IXYS Corporation
Kern	Kern Systems
Konan	Konan Corporation
Kontron	Kontron Electronics, Inc.
Krueger	Krueger Company
KSystems	K-Systems of Texas, Inc.
Lambda	Lambda Semiconductors
Lansdale	Lansdale Semiconductor
Laserpath	Laserpath Corp.
Lattice	Lattice Semiconductor Corp.
LinearTech	Linear Technology Corporation
LitMach	Little Machines Inc.
LMS	LMS Electronics
Logic Model	Logic Modeling Systems Inc.
LogicalDes	Logical Design Group Inc.
LogicAuto	Logic Automation Incorporated
LogicDev	Logic Devices Inc.
Logicraft	Logicraft
Lomas	Lomas Data Products, Inc.
LPKF-Pacific	LPKF Pacific
LSI Comp	LSI Computer Systems, Inc.
LSI Logic	LSI Logic Corporation
LSTI	Logical Solutions Technology Inc.
LupiData	Lupi Data, Inc.
M2M	M2M Robotics
Magnum	Magnum Opus
Marconi	Marconi Electronic Devices Inc.
Marinco	Marinco Computer Products
Massteck	Massteck Ltd.
Matra	Matra Design Systems
Matra-Harris	Matra-Harris Semiconductors
Matrix	Matrix Corporation
Maxim	Maxim Integrated Products
MCE	MCE Semiconductor
Mentor	Mentor Graphics Corporation
MetaSoft	Meta-Software, Inc.
Metatek	Metatek, Inc.
MetraByte	Metra Byte Corporation
Micom Int	Micom-Interlan, Inc.
MiconSys	Micon Systems Co.
Micra	Micra Corporation
Micrel	Micrel
Micro-Link	Micro-Link Corp.
Micro-Rel	Micro-Rel
MicroAide	Micro-Aide Corporation
Microbar	Microbar Systems Inc.
Microchip	Microchip Technology, Inc.
MicroCompSys	Microcomputer Systems Inc.
Microcosm	Microcosm Inc.
MicroDesigns	Microdesigns, Inc.
MicroElec	Micro Electronic Technologies, Inc.
MicroInds	Micro Industries Corp.
MicroLinear	Micro Linear
MicroNet	Micro Networks Company
Micronix	Micronix Integrated Systems Inc.
MicronTech	Micron Technology
Micropac	Micropac Industries, Inc.
MicroPwr	Micro Power Systems, Inc.
Microsim	MicroSim Corporation
MicroSys	MICRO/SYS
Microvoice	Microvoice Corp.
Mikros	Mikros Systems Corp.
Miller	Miller Technology Inc.
Mimic	Mimic, Inc.
Minc	MINC Incorporated
MiniCompTech	Mini Computer Technology
Minntronics	Minntronics Corporation
Mitchell	Mitchell Electronics
Mitel	Mitel Semiconductor
Mitsubishi	Mitsubishi Electronics America, Inc.
MMI	Monolithic Memories, Inc.
Modula	Modula Corp.
MonSys	Monolithic Systems Corporation
Morrow Tech	Morrow Technologies Corp.
Mosaid	Mosaid Inc.
Motorola	Motorola Semiconductor Products
MTC	Mesa Technology Corp.
Multiwire	Multiwire
Mylex	Mylex Corporation
National	National Semiconductor Corporation
National Inst	National Instruments
NCAI	North Coast Automation Inc.
NCM	NCM Corporation
NCR	NCR Corporation
NCUBE	NCUBE
NEC	NEC Electronics Inc.
NMB	NMB Semiconductor Corporation
Northern	Northern Precision Labs
Novix	Novix Inc.
NthGraphics	Nth Graphics
NTI Group	The NTI Group
Octagon	Octagon Systems Corporation
Octal	Octal
OEI	Optical Electronics Inc.
OKI	OKI Semiconductor, Inc.
Omation	Omation, Inc.
Omnibyte	Omnibyte Corporation
Onset	Onset Computer Corporation
Optek	Optek Technology, Inc.
OrCad	OrCad
Orion	Orion Instruments
OwlComp	Owl Computers Inc.
Oxford	Oxford Computer

CONT.

PacificM	Pacific Microcomputers, Inc.
Panasonic	Panasonic Industrial Company/Electronic Components Division
PC-Office	PC-Office
PCAD	(P-CAD)
PEP-Modular	PEP Modular Computers, Inc.
Peps	Performance Electronic Packaging Services
Perform CAD	Performance CAD
Performance	Performance Semiconductor Corp.
PhaseIIILogic	Phase III Logic
Plessey	Plessey Semiconductors
PLX Tech	PLX Technology, Inc.
PMI	Precision Monolithics Inc.
Polycore	Polycore Electronics Inc.
Pro-Log	Pro-Log Corporation
ProtoCAD	ProtoCAD
Proximity	Proximity Technology Inc.
Quadtree	Quadtree
Qualcomm	Qualcomm Incorporated
Qualogy	Qualogy Corp.
Quantic	Quantic Laboratories, Inc.
RACAL	Racal-Redac
RadstoneTech	Radstone Technology Corp.
Ramtron	Ramtron Corporation
RanchoTech	Rancho Technology Center
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Densan/Pascot

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17981 Skypark Circle, Ste. B
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Dense-Pac

Dense-Pac Microsystems, Inc.
7321 Lincoln Way
Garden Grove, California 92641
714-898-0007
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STG Intl., TEL: 3-561-8231

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EG&G Reticon

EG&G Reticon Corporation
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Camera Product Marketing: EG&G Reticon
Analog Product Marketing: EG&G Reticon
Image Sensor Product Marketing: EG&G Reticon

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Instrumentarium Oy Elektrokiikka, TEL: 358 0 5281

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Enterprise Systems

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EPIC Design Technology

EPIC Design Technology, Inc.
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Ericsson

Ericsson Components
(Formerly RIFA, Inc.)
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Richardson, Texas 75085-3904
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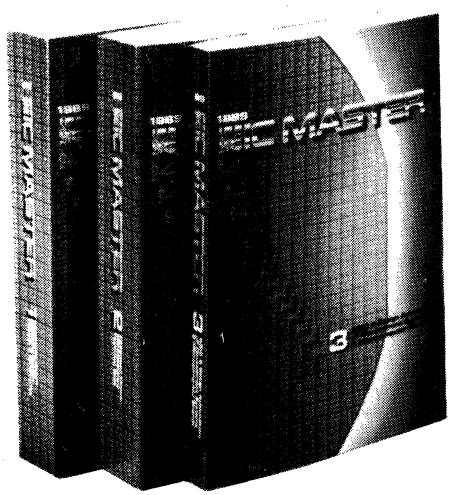

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★ Indicates additional data is provided on the page noted.

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CY7C128-55M	★ 2580 1449-40
CY7C130-25C	★ 2580 1446-75
CY7C130-35C	★ 2580 1446-86
CY7C130-35M	★ 2580 1446-83
CY7C130-45C	★ 2580 1446-97
CY7C130-45M	★ 2580 1446-98
CY7C130-55C	★ 2580 1447-5
CY7C130-55M	★ 2580 1447-8
CY7C131-25C	1446-76
CY7C131-35C	1446-79
CY7C131-35M	1446-80
CY7C131-45C	1446-91
CY7C131-45M	1446-92
CY7C131-55C	1446-109
CY7C131-55M	1446-110
CY7C132-25C	★ 2580 1446-78
CY7C132-35C	★ 2580 1448-81
CY7C132-35M	★ 2580 1446-84
CY7C132-45C	★ 2580 1449-19
CY7C132-45M	★ 2580 1449-20
CY7C132-55C	★ 2580 1449-76
CY7C132-55M	★ 2580 1449-77
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CY7C136-35M	1448-69
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CY7C136-55C	1449-60
CY7C136-55M	1449-61
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CY7C140-35C	★ 2580 1446-85
CY7C140-45C	★ 2580 1446-95
CY7C140-45M	★ 2580 1446-96
CY7C140-55C	★ 2580 1447-3
CY7C140-55M	★ 2580 1447-4
CY7C141-25C	1446-77
CY7C141-35C	1446-81
CY7C141-35M	1446-82
CY7C141-45C	1446-93
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CY7C141-55C	1447-1
CY7C141-55M	1447-2
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CY7C142-35C	★ 2580 1448-72
CY7C142-35M	★ 2580 1448-73
CY7C142-45C	★ 2580 1447-94
CY7C142-45M	★ 2580 1449-12
CY7C142-55C	★ 2580 1449-64
CY7C142-55M	★ 2580 1449-65
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CY7C147-35C	★ 2580 1452-33
CY7C147-35M	★ 2580 1452-34
CY7C147-45C	★ 2580 1452-47
CY7C147-45M	★ 2580 1452-48
CY7C148-25C	★ 2580 1445-55
CY7C148-35C	★ 2580 1445-80
CY7C148-35M	★ 2580 1445-81
CY7C148-45C	★ 2580 1445-106
CY7C148-45M	★ 2580 1445-107
CY7C149-25C	★ 2580 1445-56
CY7C149-35C	★ 2580 1445-82
CY7C149-35M	★ 2580 1445-83
CY7C149-45C	★ 2580 1445-108
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CY7C150-12C	★ 2580 1446-73
CY7C150-15C	★ 2580 1445-33
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CY7C150-25M	★ 2580 1445-69
CY7C150-35C	★ 2580 1445-91
CY7C150-35M	★ 2580 1445-92
CY7C161-20C	★ 2580 1463-23
CY7C161-25C	★ 2580 1463-103
CY7C161-25M	★ 2580 1463-104
CY7C161-35C	★ 2580 1465-36
CY7C161-35M	★ 2580 1465-37
CY7C161-45C	★ 2580 1466-5
CY7C161-45M	★ 2580 1466-6
CY7C161L-25C	★ 2580 1463-105
CY7C161L-35C	★ 2580 1465-38
CY7C161L-45C	★ 2580 1466-7
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CY7C162-25C	★ 2580 1463-106
CY7C162-25M	★ 2580 1463-107
CY7C162-35C	★ 2580 1465-39
CY7C162-35M	★ 2580 1465-40
CY7C162-45C	★ 2580 1466-8
CY7C162-45M	★ 2580 1466-9
CY7C162L-25C	★ 2580 1463-108
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CY7C162L-45	★ 2580 1467-7
CY7C164-20C	★ 2580 1463-3
CY7C164-25C	★ 2580 1463-39
CY7C164-25M	★ 2580 1463-40
CY7C164-35C	★ 2580 1464-77
CY7C164-35M	★ 2580 1464-78
CY7C164-45C	★ 2580 1465-67
CY7C164-45M	★ 2580 1465-68
CY7C164L-25C	★ 2580 1463-41
CY7C164L-35C	★ 2580 1464-79
CY7C164L-45C	★ 2580 1465-69
CY7C166-20C	★ 2580 1463-8
CY7C166-25C	★ 2580 1463-66
CY7C166-25M	★ 2580 1463-67
CY7C166-35C	★ 2580 1464-109
CY7C166-35M	★ 2580 1465-
CY7C166-45C	★ 2580 1465-94
CY7C166-45M	★ 2580 1465-95
CY7C166L-25C	★ 2580 1463-68
CY7C166L-35C	★ 2580 1465-1
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CY7C167-25M	★ 2580 1461-41
CY7C167-35C	★ 2580 1461-60
CY7C167-35M	★ 2580 1461-61
CY7C167-45C	★ 2580 1461-83
CY7C167-45M	★ 2580 1461-84
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CY7C168-25C	★ 2580 1453-75
CY7C168-35C	★ 2580 1454-54
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CY7C168L-25C	★ 2580 1453-76
CY7C168L-35C	★ 2580 1454-56
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CY7C170-35C	⋆ 2580 1454-91
CY7C170-35M	⋆ 2580 1454-92
CY7C170-45C	⋆ 2580 1455-54
CY7C170-45M	⋆ 2580 1455-55
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CY7C171-25	⋆ 2580 1454-1
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CY7C171-35M	⋆ 2580 1454-101
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CY7C172-35M	⋆ 2580 1454-103
CY7C172-45C	⋆ 2580 1455-64
CY7C172-45M	⋆ 2580 1455-65
CY7C172L-25C	⋆ 2580 1453-80
CY7C172L-35C	⋆ 2580 1454-61
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CY7C185-35C	⋆ 2580 1457-47
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CY7C185-45C	⋆ 2580 1457-89
CY7C185-45M	⋆ 2580 1457-90
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CY7C186-25C	⋆ 2580 1457-21
CY7C186-35C	⋆ 2580 1457-50
CY7C186-35M	⋆ 2580 1457-51
CY7C186-45C	⋆ 2580 1457-92
CY7C186-45M	⋆ 2580 1457-93
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CY7C187-45C	⋆ 2580 1471-84
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CY7C194-45M	⋆ 2580 1472-89
CY7C196-25C	⋆ 2580 1472-38
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CY7C196-35M	⋆ 2580 1472-70
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CY7C197-35C	⋆ 2580 1476-42
CY7C197-35M	⋆ 2580 1476-30
CY7C197-45C	⋆ 2580 1476-47
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CY7C198-45M	⋆ 2580 1468-32
CY7C198-55C	⋆ 2580 1468-48
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CY7C199-55C	⋆ 2580 1468-50
CY7C199-55M	⋆ 2580 1468-51
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CY7C225-35M	⋆ 2585 1417-21
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CY7C225-40M	⋆ 2585 1417-29
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CY7C235-30C	⋆ 2585 1418-23
CY7C235-30M	⋆ 2585 1418-20
CY7C235-35M	⋆ 2585 1418-25
CY7C235-40C	⋆ 2585 1418-33
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CY7C245-35C	⋆ 2585 1419-96
CY7C245-35M	⋆ 2585 1419-74
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CY7C245-35WM	⋆ 2585 1419-92
CY7C245-45C	⋆ 2585 1420-19
CY7C245-45M	⋆ 2585 1420-20
CY7C245-45WC	⋆ 2585 1420-21
CY7C245-45WM	⋆ 2585 1420-22
CY7C245A-15C	⋆ 2585 1419-6
CY7C245A-15WC	⋆ 2585 1419-7
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CY7C245A-18WC	⋆ 2585 1419-11
CY7C245A-25C	⋆ 2585 1419-29
CY7C245A-25M	⋆ 2585 1419-30
CY7C245A-25WC	⋆ 2585 1419-31
CY7C245A-25WM	⋆ 2585 1419-24
CY7C245A-35C	⋆ 2585 1419-75
CY7C245A-35M	⋆ 2585 1419-76
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CY7C245AL-35WC	⋆ 2585 1419-61
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CY7C251-55M	⋆ 2585 1425-80
CY7C251-55WC	⋆ 2585 1425-83
CY7C251-55WM	⋆ 2585 1425-84
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CY7C254-55C	⋆ 2585 1425-81
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CY7C254-55WC	⋆ 2585 1425-85
CY7C254-55WM	⋆ 2585 1425-86
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CY7C261-45M	⋆ 2585 1422-79
CY7C261-45WC	⋆ 2585 1422-100
CY7C261-45WM	⋆ 2585 1422-101
CY7C261-55C	⋆ 2585 1423-24
CY7C261-55M	⋆ 2585 1423-25
CY7C261-55WC	⋆ 2585 1423-51
CY7C261-55WM	⋆ 2585 1423-52
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CY7C263-35WC	⋆ 2585 1422-61
CY7C263-40C	⋆ 2585 1422-67
CY7C263-40WC	⋆ 2585 1422-68
CY7C263-45C	⋆ 2585 1422-80
CY7C263-45M	⋆ 2585 1422-81
CY7C263-45WC	⋆ 2585 1422-102
CY7C263-45WM	⋆ 2585 1422-103
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CY7C263-55WM	⋆ 2585 1423-54
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CY7C264-40WC	⋆ 2585 1422-69
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CY7C264-45WM	⋆ 2585 1422-105
CY7C264-55C	⋆ 2585 1423-28
CY7C264-55M	⋆ 2585 1423-29
CY7C264-55WC	⋆ 2585 1423-55
CY7C264-55WM	⋆ 2585 1423-56
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CY7C265-40WC	⋆ 2585 1422-97
CY7C265-50C	⋆ 2585 1423-14
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CY7C281-30C	★ 2585 1418-21
CY7C281-45C	★ 2585 1418-40
CY7C281-45M	★ 2585 1418-41
CY7C282-30C	★ 2585 1418-22
CY7C282-45C	★ 2585 1418-42
CY7C282-45M	★ 2585 1418-43
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CY7C291-35M	★ 2585 1419-53
CY7C291-35WC	★ 2585 1419-63
CY7C291-35WM	★ 2585 1419-93
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CY7C291-50M	★ 2585 1420-29
CY7C291-50WC	★ 2585 1420-38
CY7C291-50WM	★ 2585 1420-39
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CY7C291A-25WC	★ 2585 1419-25
CY7C291A-30M	★ 2585 1419-42
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CY7C291A-35C	★ 2585 1419-81
CY7C291A-35M	★ 2585 1419-82
CY7C291A-35WC	★ 2585 1419-83
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CY7C292-50M	★ 2585 1420-34
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CA158	★ **2647**
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	★ **2653**
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CDP1852C	★ **2644**
	★ **2653**
	639-110
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CDP1853	★ **2644**
	613-107
	856-26
CDP1853C	★ **2644**
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CDP1854A	★ **2644**
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CDP1854AC	★ **2644**
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CDP1855	★ **2644**
	★ **2653**
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CDP1871AC	★ **2644**
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CDP1872C	★ **2644**
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CDP1874C	★ **2644**
	639-112
	856-106
CDP1875C	★ **2644**
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CDP1877	★ **2644**
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CDP1877C	★ **2644**
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CDP1878	★ **2644**
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CDP1879	★ **2644**
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CDP1879C-1	★ **2644**
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CDP1881	★ **2644**
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CDP1881C	★ **2644**
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CDP1882	★ **2644**
	856-100
	856-22
CDP1882C	★ **2644**
	856-101
	856-23
CDP1883	★ **2644**
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CDP1883C	★ **2644**
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CDP6402	★ **2644**
	★ **2653**
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CDP65C51-1	★ **2644**
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CDP65C51-2	★ **2644**
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CDP65C51A	★ **2644**
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CDP68HC05C4	★ **2644**
	★ **2653**
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CDP68HC05D2	★ **2644**
	★ **2653**
	859-5
CDP68HC68A2	★ **2644**
	★ **2653**
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CDP68HC68P1	★ **2644**
	880-65
CDP68HC68R1	★ **2644**
	★ **2653**
	1442-110
CDP68HC68R2	★ **2644**
	★ **2653**
	1444-29
CDP68HC68S1	★ **2644**
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CDP68HC68T1	★ **2644**
	★ **2653**
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CD54ACT534	★ 2643 618-36
CD54ACT540	★ 2643 606-160
CD54ACT541	★ 2643 606-161
CD54ACT563	★ 2643 625-81
CD54ACT564	★ 2643 617-160
CD54ACT573	★ 2643 625-105
CD54ACT623	★ 2643 638-150
CD54ACT646	★ 2643 637-170
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CD54ACT7402	627-157
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CD54AC05	★ 2642 607-118
CD54AC08	★ 2642 620-157
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CD54AC139	★ 2642 614-25
CD54AC151	★ 2642 629-102
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CD54AC374	★ 2643 618-135
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CD54AC534	★ 2643 618-30
CD54AC540	★ 2643 606-151
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CD54HCT153	★ 2640 628-73
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CD54HCT157	★ 2640 ★ 2653 628-149
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CD54HCT165	★ 2640 632-63
CD54HCT166	★ 2640 632-124
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CD54HCT174	★ 2640 617-119
CD54HCT175	★ 2640 617-22
CD54HCT181	★ 2640 603-52
CD54HCT182	★ 2640 603-80
CD54HCT190	★ 2640 612-74
CD54HCT191	★ 2640 609-29
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CD54HCT193	★ 2640 609-30
CD54HCT194	★ 2640 631-96
CD54HCT195	★ 2640 631-162
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CD54HCT243	★ 2640 635-129
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CD54HCT245	★ 2640 ★ 2653 639-6
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CD54HCT32	★ 2640 623-23
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CD54HCT356	★ 2640 630-38
CD54HCT365	★ 2641 606-82
CD54HCT366	★ 2641 606-135
CD54HCT367	★ 2641 606-83
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CD54HCT4017	★ 2641 611-44
CD54HCT4020	★ 2641 610-140
CD54HCT4024	★ 2641 610-7
CD54HCT4040	★ 2641 610-103
CD54HCT4046	★ 2641 634-91
CD54HCT4049	605-119
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CD54HCT4052	★ 2641 ★ 2655 1009-49
CD54HCT4053	★ 2641 ★ 2655 1006-83
CD54HCT4059	★ 2641 613-11
CD54HCT4060	★ 2641 610-179
CD54HCT4066	★ 2641 1003-61
CD54HCT4067	★ 2641 ★ 2655 1011-104
CD54HCT4075	★ 2641 622-170
CD54HCT4094	★ 2641 632-28
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CD54HCT423	630-114
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CD54HCT4511	★ 2641 616-32
CD54HCT4514	★ 2641 615-65
CD54HCT4515	★ 2641 615-66
CD54HCT4516	★ 2641 609-31
CD54HCT4518	★ 2641 612-113

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CD54HCT534	⋆ 2641 618-98
CD54HCT540	⋆ 2641 606-197
CD54HCT541	⋆ 2641 606-198
CD54HCT563	⋆ 2641 626-73
CD54HCT564	⋆ 2641 618-99
CD54HCT573	⋆ 2641 625-167
CD54HCT574	⋆ 2641 619-4
CD54HCT583	⋆ 2641 602-4
CD54HCT597	⋆ 2641 632-76
CD54HCT640	⋆ 2641 638-120
CD54HCT643	⋆ 2641 639-38
CD54HCT646	⋆ 2641 638-7
CD54HCT648	⋆ 2641 637-153
CD54HCT670	⋆ 2641 627-120
CD54HCT688	⋆ 2641 ⋆ 2649 602-123
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CD54HCT7038	⋆ 2641 640-39
CD54HCT7046	⋆ 2642 631-21
CD54HCT73	⋆ 2640 620-62
CD54HCT74	⋆ 2640 616-116
CD54HCT75	⋆ 2640 626-131
CD54HCT85	⋆ 2640 603-115
CD54HCT86	⋆ 2640 624-71
CD54HCT93	⋆ 2640 609-161
CD54HCU04	⋆ 2642 ⋆ 2649 607-138 ¶ 446-26
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CD54HC02	⋆ 2639 623-167
CD54HC03	⋆ 2639 622-1
CD54HC04	⋆ 2639 607-139
CD54HC08	⋆ 2639 620-172
CD54HC10	⋆ 2640 621-91
CD54HC107	⋆ 2640 620-32
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CD54HC299	⋆ 2640 633-13
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CD54HC368	⋆ 2641 606-107
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CD54HC40103	⋆ 2642 610-38
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CD54HC4094	⋆ 2641 632-23
CD54HC42	⋆ 2640 613-124
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CD54HC4514	⋆ 2641 615-52
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CD54HC4516	⋆ 2641 609-5
CD54HC4518	⋆ 2641 612-104
CD54HC4520	⋆ 2641 609-100
CD54HC4538	⋆ 2641 630-79
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CD54HC648	⋆ 2641 637-130
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CD54HC75	⋆ 2640 626-114
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CD54HC86	⋆ 2640 624-46
CD54HC93	⋆ 2640 609-156
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CD74ACT05	⋆ 2642 607-129
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CD74ACT139	⋆ 2642 614-34
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CD74ACT164	⋆ 2642 632-82
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CD74ACT175	⋆ 2642 616-162
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CD74ACT193	⋆ 2642 608-187
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CD74ACT241	⋆ 2642 636-168
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CD74ACT245	⋆ 2642 638-151
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CD74ACT258	⋆ 2642 629-42
CD74ACT273	⋆ 2643 617-168
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CD74ACT283	⋆ 2643 602-29
CD74ACT299	⋆ 2643 633-4
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CD74ACT323	⋆ 2643 632-186
CD74ACT373	⋆ 2643 625-106
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CD74ACT563	⋆ 2643 625-82
CD74ACT564	⋆ 2643 617-161
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CD74ACT646	⋆ 2643 637-171
CD74ACT648	⋆ 2643 637-117
CD74ACT7060	⋆ 2643 610-165
CD74ACT7202	⋆ 2643 628-27
CD74ACT74	⋆ 2642 616-93
CD74ACT7402	627-158
CD74ACT86	⋆ 2642 624-41
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CD74AC158	⋆ 2642 628-156
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CD74AC244	⋆ 2642 607-52
CD74AC245	⋆ 2642 633-123
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CD74AC373	⋆ 2643 625-97
CD74AC374	⋆ 2643 618-137
CD74AC533	⋆ 2643 626-19
CD74AC534	⋆ 2643 618-31
CD74AC540	⋆ 2643 606-153
CD74AC541	⋆ 2643 606-154

¶ Indicates page number in Application Note Directory.
⋆ Indicates additional data is provided on the page noted.

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CD74AC563	★ 2643 625-80
CD74AC564	★ 2643 617-159
CD74AC573	★ 2643 625-98
CD74AC574	★ 2643 618-138
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CD74AC646	★ 2643 637-165
CD74AC648	★ 2643 637-111
CD74AC7060	★ 2643 610-163
CD74AC7202	★ 2643 628-25
CD74AC74	★ 2642 616-87
CD74AC7402	627-156
CD74AC86	★ 2642 624-38
CD74HCT00	★ 2639 ★ 2653 621-169
CD74HCT02	★ 2639 623-189
CD74HCT03	★ 2639 622-6
CD74HCT04	★ 2639 607-164
CD74HCT08	★ 2639 620-193
CD74HCT10	★ 2640 621-110
CD74HCT107	★ 2640 620-63
CD74HCT109	★ 2640 619-138
CD74HCT11	★ 2640 620-136
CD74HCT112	★ 2640 620-12
CD74HCT123	★ 2640 630-146
CD74HCT125	★ 2640 605-76
CD74HCT126	★ 2640 605-77
CD74HCT132	★ 2640 635-160
CD74HCT137	★ 2640 615-26
CD74HCT138	★ 2640 614-158
CD74HCT139	★ 2640 614-70
CD74HCT14	★ 2640 636-34
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CD74HCT154	★ 2640 615-128
CD74HCT157	★ 2640 ★ 2653 628-150
CD74HCT158	★ 2640 628-185
CD74HCT160	★ 2640 611-137
CD74HCT161	★ 2640 608-151
CD74HCT162	★ 2640 611-91
CD74HCT163	★ 2640 608-95
CD74HCT164	★ 2640 632-104
CD74HCT165	★ 2640 632-64
CD74HCT166	★ 2640 632-125
CD74HCT173	★ 2640 617-65
CD74HCT174	★ 2640 617-120
CD74HCT175	★ 2640 617-23
CD74HCT181	★ 2640 603-53
CD74HCT182	★ 2640 603-81
CD74HCT190	★ 2640 612-75
CD74HCT191	★ 2640 609-32
CD74HCT192	★ 2640 611-179
CD74HCT193	★ 2640 609-33
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CD74HCT243	★ 2640 635-130
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CD74HCT245	★ 2640 ★ 2653 639-7
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CD74HCT253	★ 2640 628-106
CD74HCT257	★ 2640 ★ 2653 629-29
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CD74HCT259	★ 2640 626-163
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CD74HCT4024	★ 2641 610-8
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GD4053B	★ **2710** 1006-87
GD4066B	★ **2710** 1004-8
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GD4068B	★ **2710** 622-53
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GD4071B	★ **2710** 623-29
GD4072B	622-139
GD4073B	620-142
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GD4077B	★ **2710** 624-128
GD4078B	★ **2710** 624-24
GD4081B	★ **2710** 620-199
GD4082B	620-98
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GD4086B	★ **2710** 622-127
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GD4104B	★ **2710** 633-108
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GD4511B	★ **2710** 616-37
GD4512B	★ **2710** 629-141
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GD4515B	615-76
GD4516B	★ **2710** 609-49
GD4518B	★ **2710** 612-118
GD4519B	629-89
GD4520B	★ **2710** 609-122
GD4521B	631-8
GD4522B	★ **2710** 612-36
GD4526B	★ **2710** 609-77
GD4527B	635-5
GD4528B	★ **2710** 630-151
GD4532B	★ **2710** 639-132
GD4534B	613-20
GD4538B	630-126
GD4539B	★ **2710** 628-43
GD4543B	615-180
GD4553B	★ **2710** 612-137
GD4555B	★ **2710** 613-171
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GD4561B	604-159
GD4566B	613-47
GD4581B	603-57
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GD4583B	635-69
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GD4703B	★ **2710** 627-126
GD4704B	★ **2710** 602-114
GD4705B	★ **2710** 603-26
GD4706B	★ **2710** 627-131
GD4707B	★ **2710** 602-111
GD4708B	★ **2710** 852-14
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GD4720B	★ **2710** 628-1
GD4721B	★ **2710** 852-33
GD4722B	634-121
GD4723B	★ **2710** 624-178
GD4724B	★ **2710** 626-171
GD4725B	★ **2710** 627-142
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GD4731B	★ **2710** 631-66
GD4734B	616-38
GD4735B	★ **2710** 852-37
GD4736B	★ **2710** 852-36
GD4737B	★ **2710** 610-30
GD4741B	1009-21
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GD74HCT02	★ **2709** 623-190
GD74HCT03	★ **2709** 622-7
GD74HCT04	★ **2709** 607-165
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GD74HCT107	★ **2709** 620-65
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GD74HCT112	★ **2709** 620-13
GD74HCT113	★ **2709** 619-180
GD74HCT123	★ **2709** 630-147
GD74HCT125	★ **2709** 605-85
GD74HCT126	★ **2709** 605-78
GD74HCT132	★ **2709** 635-161
GD74HCT133	★ **2709** 622-76
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GD74HCT138	★ **2709** 614-159
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GD74HCT147	★ **2709** 615-148
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GD74HCT154	★ **2709** 615-133
GD74HCT155	★ **2709** 614-72
GD74HCT157	★ **2709** 628-151
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GD74HCT191	★ **2709** 609-35
GD74HCT192	★ **2709** 611-180
GD74HCT193	★ **2709** 609-36
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GD74HCT221	★ **2709** 630-119
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GD74HCT243	635-131
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GD74HCT258	★ **2709** 629-75
GD74HCT259	★ **2709** 626-164
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GD74HCT27	★ **2709** 623-128
GD74HCT273	★ **2709** 617-195
GD74HCT283	★ **2709** 602-49
GD74HCT298	★ **2709** 629-76
GD74HCT299	★ **2709** 633-31
GD74HCT30	★ **2709** 622-49
GD74HCT32	★ **2709** 623-25
GD74HCT322	★ **2709** 632-126
GD74HCT34	★ **2709** 605-112
GD74HCT354	630-42
GD74HCT356	630-43
GD74HCT365	★ **2709** 606-86
GD74HCT366	★ **2709** 606-139
GD74HCT367	★ **2709** 606-87
GD74HCT368	★ **2709** 606-140
GD74HCT373	★ **2709** 625-170
GD74HCT374	★ **2709** 619-7
GD74HCT377	★ **2709** 618-26
GD74HCT386	★ **2709** 624-73
GD74HCT390	★ **2709** 612-101
GD74HCT393	★ **2709** 609-150
GD74HCT42	★ **2709** 613-143
GD74HCT423	630-120
GD74HCT533	★ **2709** 626-76
GD74HCT534	★ **2709** 618-102
GD74HCT540	★ **2709** 606-201
GD74HCT541	★ **2709** 606-202
GD74HCT563	626-77
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GD74HCT573	625-171
GD74HCT574	619-8
GD74HCT58	★ **2709** 622-124
GD74HCT590	★ **2709** 610-72
GD74HCT640	★ **2709** 638-122
GD74HCT643	★ **2709** 639-40
GD74HCT646	★ **2709** 638-9
GD74HCT648	★ **2709** 637-155
GD74HCT670	★ **2709** 627-122
GD74HCT688	★ **2709** 602-125
GD74HCT73	★ **2709** 620-66
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GD74HC107	★ **2709** 620-36
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GD74HC165	★ 2709 632-47
GD74HC166	★ 2709 632-48
GD74HC173	★ 2709 617-50
GD74HC174	★ 2709 617-103
GD74HC175	★ 2709 617-8
GD74HC190	★ 2709 612-21
GD74HC191	★ 2709 609-9
GD74HC192	★ 2709 611-166
GD74HC193	★ 2709 609-10
GD74HC194	★ 2709 631-82
GD74HC195	★ 2709 631-147
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GD74HC240	★ 2709 636-108
GD74HC241	★ 2709 636-192
GD74HC242	635-89
GD74HC243	635-117
GD74HC244	★ 2709 636-193
GD74HC245	★ 2709 638-177
GD74HC251	★ 2709 629-164
GD74HC253	★ 2709 628-54
GD74HC257	★ 2709 629-16
GD74HC258	★ 2709 629-46
GD74HC259	★ 2709 626-146
GD74HC266	624-111
GD74HC27	★ 2709 623-111
GD74HC273	★ 2709 617-177
GD74HC280	★ 2709 640-49
GD74HC283	★ 2709 602-35
GD74HC298	★ 2709 629-59
GD74HC299	★ 2709 633-15
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GD74HC365	★ 2709 606-59
GD74HC366	★ 2709 606-110
GD74HC367	★ 2709 606-60
GD74HC368	★ 2709 606-111
GD74HC373	★ 2709 625-138
GD74HC374	★ 2709 618-188
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GD74HC42	★ 2709 613-126
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GD74HC51	★ 2709 622-111
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GD74HC643	★ 2709 638-107
GD74HC646	★ 2709 637-185
GD74HC648	★ 2709 637-132
GD74HC670	★ 2709 635-15
GD74HC688	★ 2709 602-165
GD74HC73	★ 2709 620-37
GD74HC74	★ 2709 616-101
GD74HC75	★ 2709 626-116
GD74HC76	★ 2709 619-111
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GD74HC86	★ 2709 624-49
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GD74LS138	★ 2708 659-32
GD74LS139	★ 2708 658-119
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GD74LS163A	★ 2708 655-88
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GD74LS166	★ 2708 675-127
GD74LS17	★ 2708 653-83
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SN54LS170	★ **2943** 671-27
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SN54LS174	★ **2942** 661-94
SN54LS175	★ **2942** 660-176
SN54LS181	★ **2947** 652-36
SN54LS182	652-75
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SN54LS191	★ **2942** 656-60
SN54LS192	★ **2942** 657-134
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SN54LS798	★ **2940** 653-176
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SN54LS85	★ **2946** 651-53
SN54LS86	★ **2938** 668-152
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SN74LS569	★ **2942** 656-76
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SN74LS642	★ **2940** 677-175 1096-41
SN74LS643	678-29
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SN74LS645	★ **2940** 678-106 1096-49
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SN74LS684	⋆ **2946**
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SN74LS685	651-120
SN74LS686	651-135
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SN74LS688	⋆ **2946**
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SN74LS689	651-122
SN74LS716	658-11
SN74LS718	658-6
SN74LS724	680-45
SN74LS73A	⋆ **2941**
	662-177
SN74LS74A	⋆ **2941**
	660-124
SN74LS748	⋆ **2946**
	681-66
SN74LS75	⋆ **2941**
	669-48
SN74LS76A	⋆ **2941**
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SN74LS77	⋆ **2941**
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SN74LS796	⋆ **2940**
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SN74LS797	⋆ **2940**
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SN74LS798	⋆ **2940**
	653-180
SN74LS83A	⋆ **2947**
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SN74LS848	⋆ **2946**
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74F126	★ **3077** 653-46
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74F132	★ **3077** 680-98
74F138	★ **3077** 659-28
74F139	★ **3077** 658-115
74F14	★ **3077** 680-128
74F148	★ **3077** 681-60
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74F162A	★ **3077** 657-40
74F163A	★ **3077** 655-85
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74F174	★ **3077** 661-89
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74F1765	★ **3077** 679-120
74F1765-1	★ **3077** 679-121
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74F1805	676-117
74F1808	676-113
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74F182	★ **3077** 652-73
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74F259	★ **3077** 669-135
74F260	★ **3077** 667-128
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74F280B	★ **3077** 681-98
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74F2953	★ **3077** 679-53
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74F30241	★ **3077** 677-63
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74F541	★ **3078** 677-64 1088-34
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74F544	★ **3078** 678-176
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74F568	★ **3078** 657-91
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74F573	★ **3078** 670-6
74F579	★ **3078** ★ **3093** 657-93
74F583	★ **3078** 651-162
74F588	★ **3078** 677-156
74F595	★ **3078** 675-145
74F597	★ **3078** 675-133
74F598	★ **3078** 675-134

Arranged alphanumerically from left to right.

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74F641-1	* 3078 678-55
74F642	* 3078 677-172
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74F647	* 3078 678-146
74F648	* 3078 * 3084 678-180
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74F654	678-128
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74F656A	* 3078 * 3086 653-164
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74F711-1	* 3078 671-78
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74HCT126	* 3057 605-82
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74HC356	★ 3057 630-31
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Analog-to-Digital Converters
Binary - TTL Outputs

Model	Resolution (bits)	Convert Time (μs)	Linearity Error (Max LSB)	Offset Tempco (PPM/°C)	Gain Tempco (PPM/°C)	Analog Input Range	Output Code	Power Supplies (V@mA)
ADC574A	12	20	±1/2	±5	±10	+10,+20 ±5,±10	BIN OBIN	+5@15 +12/15@15 -12/15@30
ADC674A	12	12	±1/2	±5	±10	+10,+20 ±5,±10	BIN OBIN	+5@15 12/15@15 -12/15@30
ADC84	12	8	±1/2	±3uni ±14bi	±30	+5,+10 ±2.5,±5 ±10	COBIN CBIN 2s COMP	-15@35 +5@38 +15@30
ADC85	12	8	±1/2	±3uni ±7bi	±15	+5,+10 ±2.5,±5 ±10	COBIN CBIN 2s COMP	-15@35 +5@38 +15@30
ADC87	12	8	±1/4	±3	±10	+5,+10 ±2.5,±5 ±10	COBIN CBIN 2s COMP	-15@35 +5@38 +15@25
ADC5200	12	50	±1/2	Note 1	±10	-10	CBIN COBIN	+15@13 -15@15 +5@10
ADC5210	12	13	±1/2	Note 1	±10	-10	CBIN COBIN	+15@13 -15@15 +5@10
ADC5201	12	50	±1/2	Note 1	±10	±5	CBIN COBIN	+15@13 -15@15 +5@10
ADC5211	12	13	±1/2	Note 1	±10	±5	CBIN COBIN	+15@13 -15@15 +5@10
ADC5202	12	50	±1/2	Note 1	±10	±10	COBIN	+15@13 -15@15 +5@10
ADC5212	12	13	±1/2	Note 1	±10	±10	COBIN	+15@13 -15@15 +5@10
ADC5203	12	50	±1/2	Note 1	±3	-10	CBIN	+15@13 -15@15 +5@10
ADC5213	12	13	±1/2	Note 1	±3	-10	CBIN	+15@13 -15@15 +5@10
ADC5204	12	50	±1/2	Note 1	±3	±5	COBIN	+15@13 -15@15 +5@10

Advanced Analog/Intec

MIL-STD-1772 Certified

Advanced Analog
a division of Intech

Model	Resolution (bits)	Convert Time (μs)	Linearity Error (Max LSB)	Offset Tempco (PPM/°C)	Gain Tempco (PPM/°C)	Analog Input Range	Output Code	Power Supplies (V@mA)
ADC5214	12	13	±1/2	Note 1	±3	±5	COBIN	+15@13 -15@15 +5@10
ADC5205	12	50	±1/2	Note 1	±3	±10	COBIN	+15@13 -15@15 +5@10
ADC5215	12	13	±1/2	Note 1	±3	±10	COBIN	+15@13 -15@15 +5@10
ADC5206	12	50	±1/2	Note 1	±10	±10	CBIN	+15@13 -15@15 +5@10
ADC5216	12	13	±1/2	Note 1	±10	±10	CBIN COBIN	+15@13 -15@15 +5@10
ADC5207	12	50	±1/2	Note 1	±3	+10	CBIN	+15@13 -15@15 +5@10
ADC5217	12	13	±1/2	Note 1	±3	+10	CBIN	+15@13 -15@15 +5@10
ADC5245	12	0.9	±1	±10	±20	+5	BIN	+5@120 +15@50 -15@70
ADC5246	12	0.9	±1	±10	±20	±2.5	OBIN	+5@120 +15@50 -15@70
ADC6012	12	0.6	±1	±10	±20	+5	BIN	+5@120 +15@50 -15@70
ADC6013	12	0.6	±1	±10	±20	±2.5	OBIN	+5@120 +15@50 -15@70
ADC6010	12	4	±1/2	±3uni ±14bi	±30	+5,+10 ±2.5,±5 ±10	COBIN CBIN 2s COMP	-15@35 +5@38 +15@30
ADC2714	14	10	±1/2	±5	±10	+5,+10 ±5,±10	BIN OBIN	+5@120/-15@50 -15@50
A8016	16	16	±1/2	±1.5	±6	+10,±10	BIN OBIN 2s COMP	+5@300 +15@40 -15@65
ADC1600-2[2]	16	2	±1/2	±7	±7	±10	OBIN COBIN	±15@260 +5@300
ADC1140[3]	16	35	Note 7	±7	±12	+5,+10 ±5,±10	BIN OBIN	±15@30 +5@150

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Notes:
1. Zero error is ±0.05% FSR (max) for 0 to +70°C.
2. Includes internal sample/hold.
3. .003% FSR.

New 16-bit A/D converter with 35μs conversion rate will be available 1st qtr '89. Unipolar and bipolar versions and will be in a small DIP. Consult factory for details.

DC/DC Converters
Military

Model	Output Voltage	Input Voltage	Output Power	Load Regulaton	Efficiency (%)	Package
PS2805	+5	+28±33%	3.5W	±1.5%	70%	1.1x1.3x0.5
PS2815	±15	+28±33%	7.5W	±1.5%	70%	1.1x1.3x0.5
PS6008	±15,+5	+28±33%	27W	±2.0%	70%	3.0x2.35x0.64
PS6009	±15,+5,+28	+28±33%	80W	±2.0%	70%	3.5x2.42x0.64

Meets or exceeds requirements of MIL-STD-704D for a 28V DC system voltage transient range.

DC/DC Converters
Rugged

Model	Output Voltage	Input Voltage	Output Power	Load Regulaton	Efficiency (%)	Package
A970	+5	+12±10%	1W	±0.1%	50%	1.5 x 2.0 x 0.375
A971	+5	+12±10%	10W	±0.1%	50%	2.5 x 3.5 x 0.875
PS9002	+5	+15±10%	20W	±0.5%	75%	2.5 x 3.0 x 0.375
A972	+12	+28±10%	5W	±0.05%	55%	2.0 x 2.0 x 0.75

Video Digital-to-Analog Converters
Monolithic

Model #	Resolution (Bits)	Settling Time (μs)	Throughput (MHz)	Linearity Error (Max LSB)	Analog Output (V@75Ω)	Input Code	Power Supplies (V@mA)
RGBDAC3400S	4	15	60	±1/2	0 to +1	BIN (TTL)	+5@51
RGBDAC3405S	4	15	60	±1/2	0 to +1	BIN (TTL)	+5@51
VDAC1840	8	15	40	±1	0 to +1	BIN, CBIN (TTL)	+5@20
VDAC1842	8	15	40	±1	0 to +1	BIN, (TTL)	+5@20
VDAC1850	8	15	80	±1	0 to +1	BIN, CBIN (TTL)	+5@30
VDAC1852	8	15	80	±1	0 to +1	BIN (TTL)	+5@30

Video output also contains COMPOSITE SYNC and BLANKING levels. These are added to Analog Output shown.
All have military screening option.

Dual Line Driver

The LD6005 dual line driver accepts TTL inputs and provides balanced 40mA current source outputs to drive terminated twinaxial cable. Enable propagation delay is ≥15ns, rise time and fall time are ≤10ns. The power supply voltage is ±5.0V and input frequency is 0 (min) to 40 (max) MHz. The operating temperature range is -20°C to +85°C. It is designed to meet the requirements of MIL-STD-118-114A type II and III. Military screening.

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Digital-to-Analog Converters
General Purpose - TTL Inputs

Model #	Resolution (Bits)	Settling Time (μs) Iout	Vout	Linearity Error (Max LSB)	Offset Tempco (PPM/°C) UNI	BIP	Gain Tempco (PPM/°C)	Iout (mA)	Analog Outputs Vout (V)	Input Code	Power Supplies (V@mA)
DAC HK*	12	2	3	±1/2	±5	±10	±20	+2	+5, +10, ±2.5 ±5, ±10	BIN OBIN	+15@15 -15@30 +5@65
DAC88	12	-	6	±1/2	-	-	±10	+5	0 to +5 ±5, ±10	BIN OBIN	+15@17 -15@6 +5@30
DAC390	12	-	4	±1/2	-	±5	±5	+5	±10	OBIN	+15@12 -15@75

* The DACHK has tri-state input registers in a hybrid package.

Data Acquisition Systems

Model	Resolution Bits	Linearity Error (Max LSB)	Full Scale Input Range	Channels	Throughput Rate	System Accuracy	Power Supplies (V@mA)
DAS862	12	1/2	-10 to +10V 0 to +-10V	16SE	33kHz	.01%*	+15@18 -15@11 +5@1
DAS863	12	1/2	-10 to +10V 0 to +-10V	8DIF	33kHz	.01%*	+15@18 -15@11 +5@1

* After external offset and gain adjustment.

The DAS862/863 are available in 1" sq. leadless chip carrier or pin grid array.
Military screening.

Sample/Hold Amplifiers

Model	Acquisition Time to 0.01% (μs)	Settling to 0.01% (μs)	Nonlinearity (%)	Aperture Time (ns)	Hold Decay Rate	Input Voltage (V)	Small Signal Bandwidth (Hz)	Output (V@mA)	Power Supplies (V@mA)
A880	1.4	1.4	±0.005	100	1μV/μs	±10	10M	±10@20	±15@60
SH346	2	2	±0.01	30	0.1μV/μs	±10	1.4M	±10@3	+15@20 -15@17
SH347	2.5*	2.5*	±0.03	30	0.5μV/μs	±10	1.4M	±10@3	+15@20 -15@17
SH376	0.2*	0.1*	±0.005	±50ps	0.5μV/μs	±10	16M	±10@20	±15@22 ±5@17

* Acquisition and settling time to 0.05%.
Military screening.

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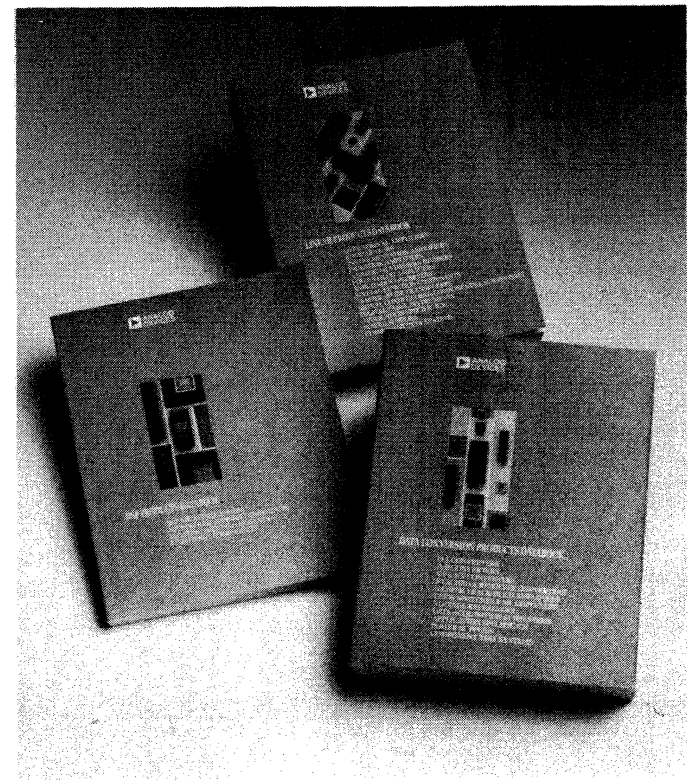
1988 LINEAR PRODUCTS DATABOOK
1988 DATA CONVERSION PRODUCTS DATABOOK
1987 DSP PRODUCTS DATABOOK

Three Volumes with Complete Technical Data on High Performance Amplifiers, Data Converters, Analog Signal Processing, Signal Conditioning, Digital Signal Processing Components, DSP Microprocessors and Related Products

The pages that follow in IC Master are the *Analog Devices Short Form Designers' Guide.* They contain selection guides to all of our product lines with key specifications that will lead you quickly to the optimum device for each application. This Designers' Guide also has block diagrams and descriptions of the latest new products from Analog Devices, particularly in the area of very high speed amplifier and data converter products. This Designers' Guide is a companion to our three comprehensive Databooks on Linear Products, Data Conversion Products and Digital Signal Processing. Listed below are summaries of the product areas covered in each Databook.

Databooks are available free of charge from your nearest Analog Devices sales office or from the Analog Devices Literature Distribution Center at (617)329-4700, Ext. 3392.



LINEAR PRODUCTS
Operational Amplifiers
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Isolation Amplifiers
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RMS-to-DC Converters
Comparators, Special Function Components
Digital Panel Instruments
Multipliers/Dividers, Log/Antilog Amplfiers
Signal Conditioning Components & Subsystems
Analog ASICs
Power Supplies

DATA CONVERSION PRODUCTS
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A/D Converters
Data Acquisition Subsystems
V/F Converters
F/V Converters
Sample/Track-Hold Amplifiers
Voltage References
Multiplexers and Switches
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ANALOG DEVICES

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ANALOG DEVICES

Analog Devices

1988 SHORT FORM DESIGNERS' GUIDE

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1988 SHORT FORM DESIGNERS' GUIDE

This Designers' Guide serves as an update to the Selection Guides in the 1987/1988 Databooks. It also provides the most recent data on specifications and prices as well as the descriptions and block diagrams for many new products.

This Guide is intended to make it easy for users and potential users to become aware of, consider and compare products and product families available from Analog Devices as possible solutions to measurement and control, signal processing and system design problems. Once having arrived at preliminary choices, the user can look up complete information on the products in our Databooks, or else obtain data sheets on newer products by dropping a card in the mail or making a phone call to one of our sales offices (page 66) or to our literature distribution center in Norwood, Massachusetts (617) 461-3392.

This book contains:

- Selection Guides and characteristics tables for comparing features and specifications for all products that are recommended for new designs;
- A comprehensive index to all products;
- New product descriptions, specifications and block diagrams;
- A list of products still in production but not listed in the primary tables because they are not recommended for new designs;
- A list of products no longer available;
- A list of products available to various military standards;
- A description of our Application Specific Integrated Circuit capability;
- Worldwide customer service directory.

1987/1988 PRODUCT DATABOOKS

Analog Devices has recently published a complete set of databooks which contain the data sheets and additional technical information on all of our current products. This Databook set is comprised of three volumes; Data Conversion Products, Linear Products and Digital Signal Processing Products. The products in these Databooks cover the entire range of data acquisition and signal processing requirements. If you have not already received a set of these Databooks, they can be obtained by contacting our main offices or one of our sales offices.

HOW TO USE THIS BOOK

This Volume

This volume is intended to lead the designer to the optimum component to fit a given application with the right mix of performance, features and cost, while also providing up-to-date information on new products. It is to be used in conjunction with our 1987/1988 Databooks and detailed data sheets, and provides source references for more detail.

If You Know the Product Number

Please turn to the product number index on page 68. This will lead you to the selection chart which contains that product and will allow you to compare it with other similar products. The selection chart will also tell you where more detailed data is available.

If You Don't Have a Product Number

If you have a product requirement, start with the table of contents; this will lead you to the proper selection charts of that product class. You can then quickly find a product with the needed mix of specifications.

If You Can't Find It Here . . . Ask!

This book contains all available products from Analog Devices through releases of October, 1988. If you have a product number which is not listed, or if you have a performance requirement which does not seem to be met in the Selection Guides, please call your nearest sales office or Analog Devices at (617) 329-4700, Extension 3596. If you would like a data sheet on a specific product or our complete catalog, ask for Extension 3392.

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Selection Guide Organization (Example)

(1) ANALOG-TO-DIGITAL CONVERTERS

(2) VIDEO ADCs

(3) Model	(4) Res Bits	(5) Throughput Rate MSPS	(6) Full Power . . . BW MHZ . . .	(7) Package Options	(8) Temp Range	(9) Page	(10) Comments	(11) Price

(1) Major product area heading.

(2) Secondary product area heading (a product may be found in more than one area).

(3) Generic part number (without suffixes for performance grades or packages).

(4) Primary specification (first sort criterion).

(5) Secondary sort specification.

(6) Other key specifications. All specifications are min or max unless noted as typical.

(7) Package options — product available in these package styles. Package guide at the bottom of each odd page.

(8) Temperature ranges available — C = Commercial 0 to +70°C; I = Industrial −40°C to +85°C; M = Military −55°C to +125°C.

(9) Page — Indicates detailed data sheet contained in 1987/1988 Databooks with section and page number. D = 1987 DSP Products, C = 1988 Data Conversion Products and L = 1988 Linear Products. If letter designation is preceded by "P," this indicates a preliminary data sheet in the databook. More up-to-date information is now available. SF = new product since databook publication. Block diagram and key features provided in the New Products section of this guide. Detailed data sheet available. N = design-in products not contained in databooks but data sheets are available. Contact your nearest sales office for data sheets on any of the above.

(10) Additional comments on features or applications.

(11) Price — U.S. price in dollars for lowest grade and package in quantities of 100.

Note that products are listed by generic part number only, such as AD9002, without additional suffixes for performance grade and package style (e.g., AD9002AD). In cases where product grades have differing values for a given specification, the range for all grades is given. The individual product data sheets provide the detail specifications on the actual models available, as well as complete ordering information.

PACKAGE OPTIONS

D	Side-Brazed Dual-In-Line Ceramic
E	Leadless Chip Carrier
F	Flat-Pack
G	Pin Grid Array
H	Round Hermetic Metal Can (Header)
M	Metal Hermetic Dual-In-Line
N	Plastic Molded Dual-In-Line
P	Plastic Leaded Chip Carrier (PLCC)
Q	Cerdip
R	Small Outline Plastic (SOIC)
V	Pin-Stake
W	Ceramic/Glass Dual-In-Line, Non-Hermetic
Y	Single-In-Line
Z	Ceramic Leaded Chip Carrier

TEMPERATURE RANGES

C	Commercial — 0 to +70°C
I	Industrial — −40°C to +85°C (Some Older Products −25°C to +85°C)
M	Military — −55°C to +125°C

BOLDFACE TYPE

Boldface entries indicate products recommended for new design.

ASTERISK

*Denotes new product since the publication of the 1987/1988 Databooks.

ANALOG DEVICES

General Introduction

Analog Devices designs, manufactures and sells worldwide sophisticated electronic components and subsystems for use in real-world signal processing. More than six hundred standard products are produced in manufacturing facilities located throughout the world. These facilities encompass all relevant technologies, including several embodiments of CMOS, BiMOS, bipolar and hybrid integrated circuits, each optimized for specific attributes—and assembled products in the form of potted modules, printed-circuit boards and instrument packages.

State-of-the-art technologies have been utilized (and in many cases invented) to provide timely, reliable, easy-to-use advanced designs at realistic prices. Our popular IC products are available in both conventional and surface mount packages (SO, LCC, PLCC), and many of our assembled products employ surface mount technology to reduce manufacturing costs and overall size. More than twenty years of successful applications experience and continuing vertical integration insure that these products are oriented to user needs. The ongoing application of today's state-of-the-art and the invention of tomorrow's state-of-the-art processes strengthen the leadership position of Analog Devices in standard data acquisition and signal processing products and make us a strong contender in high performance, mixed signal ASICs.

NEW PRODUCTS FOR 1988

Analog Devices has made significant investments in the past few years to develop major new process and design technologies which have allowed us to expand our product lines extensively into many new areas such as video displays, digital audio, disk drive data retrieval and telecommunications. These new capabilities have also allowed us to offer higher performance and lower cost products in our traditional data acquisition and signal processing lines. They are all classified and summarized in this Guide, along with existing products which are suitable for new designs. New products will be marked with an "*" in the listings, and those which are not in the 1987/1988 Databooks are described in a special section of this book which includes their major features and a block diagram.

The primary thrust for new products is in the very high speed and video areas with fast new DACs, ADCs and amplifiers directed primarily at display, signal processing, radar, ATE, disk drive and communications applications. Our DSP offerings have also been enchanced greatly by the ADSP-2100A, 12.5 MIPS Microprocessor.

TECHNICAL SUPPORT

Our extensive technical literature discusses the technology and applications of products for precision measurement and control and dynamic signal processing. In addition to tutorial material and comprehensive data sheets, we offer application notes, application guides, technical handbooks and several serial publications; for example, *Analog Productlog* provides brief information on new products being introduced and *Analog Dialogue*, our technical magazine, provides in-depth discussions of new developments in analog and digital circuit technology as applied to data acquisition, signal processing, control and test. In addition to the Databooks and general short form selection guides such as this one, we also publish several short form catalogs on specific product families. Analog Devices also provides in-depth technical support through our sales offices and with a network of applications engineers available at our factory locations to discuss our products and your applications. A call to our central office in Norwood, Massachusetts will be directed to the engineer most closely associated with your interests.

SALES OFFICES

Backing up our design and manufacturing capabilities and our extensive array of publications is a network of sales offices and representatives throughout the United States and most of the world. They are staffed by experienced sales and applications engineers, and many of them maintain a local stock of Analog Devices products. Our Worldwide Service Directory, as of the publication date, appears on pages 66 and 67 at the back of the book.

RELIABILITY

The manufacture of reliable products is a key objective at Analog Devices. We maintain facilities that have been qualified under such standards as MIL-M-38510 for ICs in the U.S. and Ireland, and MIL-STD-1772 for hybrids. More than 14 of our products—both proprietary and second-source—have qualified for JAN part numbers; others are in the process. We have also specified and qualified over 100 products under the DESC and MIL-STD drawing programs. Most of our ICs are available in versions that comply fully with MIL-STD-883C Class B. An up-to-date listing of the products available under all of these programs begins on page 54 of this Designers' Guide. The detail specifications for products available in these various programs are published in our Military Products Databook for designers who specify ICs and hybrids for military contracts (the 1987 issue contains data on nearly 150 available product families). A newsletter, *Analog Briefings*, provides current information about the status of reliability at ADI and the most recent listings of product availability.

Our PLUS program makes available, at a small premium standard devices (commercial and industrial grades, plastic or ceramic packaging) for *any* user with demanding application environments. Subjected to stringent screening, similar to MIL-STD-883 test methods, they are often suffixed "/+" and are available from stock.

PRODUCTS NOT FOUND IN THE SELECTION GUIDES

For maximum usefulness to designers of new equipment, we have limited the contents of selection guides to products most likely to be used for the design of new circuits and systems. If the model number of a product you are interested in is not in the selection guides, turn to page 64 at the back of this volume where you will find a list of older products for which data sheets are available upon request. On page 65, you will find a guide to substitutions for products no longer available.

PRICES

Accurate, up-to-date prices are an important consideration in making a choice among the many available product families. Since prices are subject to change, current price lists and/or quotations are available upon request from our sales offices.

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ANALOG DEVICES

ANALOG DEVICES

Digital-to-Analog Converters

Voltage Output DACs

Model	Res Bits	Settling Time µs typ	Bus Interface Bits[1]	Reference Voltage Int/Ext (M)[2]	Package Options[3]	Temp Range	Page	Comments
AD557	**8**	**0.8**	**8, µP**	**Int**	**N, P**	**C**	**C2–41**	**Lowest Cost 8-Bit DACPORT™. Single +5V Supply**
AD7569	**8**	**1**	**8, µP**	**Int**	**E, N, P, Q**	**C, I, M**	**PC3–195**	**CMOS, Complete 8-Bit DAC/ADC/SHA/ Reference**
AD558	**8**	**3**	**8, µP**	**Int**	**D, E, N, P**	**C, M**	**C2–45**	**10V Out DACPORT. Single or Dual Supply**
AD7224	**8**	**7**	**8, µP**	**2–12.5V, Ext**	**E, N, P, Q**	**C, I, M**	**C2–149**	**CMOS, Low Cost 8-Bit DAC**
HDD-1206	**12**	**2**	**12**	**Int**	**M, W**	**C, M**	**C2–325**	**Deglitched Voltage Output**
AD DAC80-V	12	3	12	6.3V, Int	D	C	C2–309	Improved Industry Standard
AD DAC85-V	12	3	12	6.3V, Int	D	I, M	C2–309	Improved Industry Standard
AD DAC87-V	12	3	12	6.3V, Int	D	I, M	C2–309	Improved Industry Standard
AD667	**12**	**3**	**4/8/12, µP**	**10V, Int**	**D, E, N, P**	**C, I, M**	**C2–105**	**Highest Accuracy Complete 12-Bit DAC**
AD767	**12**	**3**	**12, µP**	**10V, Int**	**D, N**	**C, I, M**	**C2–117**	**Fastest Interface Complete 12-Bit DAC**
***AD7848**	**12**	**4**	**12, µP**	**3V, Int**	**E, N, P, Q**	**C, I, M**	**SF–37**	**CMOS, Complete 12-Bit DAC with DSP Interface**
AD7845	**12**	**5**	**12, µP**	**Ext (M)**	**E, N, P, Q**	**C, I, M**	**PC2–277**	**CMOS, 12-Bit Multiplying DAC with Output Amplifier**
AD7245	**12**	**10**	**12, µP**	**5V, Int**	**E, N, P, Q**	**C, I, M**	**C2–173**	**CMOS, 12-Bit Complete DAC, Parallel Load**
AD7248	**12**	**10**	**8, µP**	**5V, Int**	**E, N, P, Q**	**C, I**	**C2–173**	**CMOS, 12-Bit Complete DAC, Byte Load**
***AD7840**	**14**	**4**	**14/Serial, µP**	**3V, Int**	**E, N, P, Q**	**C, I, M**	**SF–37**	**CMOS, 14-Bit Complete DAC, Parallel or Serial Load**
***AD1856**	**16**	**1.5**	**Serial, µP**	**Int**	**N**	**C**	**SF–39**	**16-Bit PCM Audio DAC**
AD569	**16**	**3**	**8/16, µP**	**±5V, Ext (M)**	**D, N**	**I, M**	**C2–81**	**Monolithic, 16-Bit Monotonic DAC**
AD DAC71-V	16	5	16	6.3V, Int	D, H	C	C2–305	High Resolution 16-Bit DAC
AD DAC72-V	16	5	16	6.3V, Int	D, H	C, I	C2–305	High Resolution 16-Bit DAC
***AD7846**	**16**	**6**	**16, µP**	**Ext (M)**	**D, E, N, P**	**C, I, M**	**SF–37**	**CMOS, 16-Bit Multiplying DAC with Readback Capability**
AD1145	**16**	**6**	**8/16/Serial, µP**	**3–6V, Ext**	**G, PLLCC[4]**	**C**	**C2–131**	
DAC1136	**16**	**8**	**16**	**6V, Int**	**Module**	**I**	**C2–319**	**High Resolution and Accuracy**
AD1147	**16**	**20**	**16, µP**	**10V, Int**	**D**	**I**	**C2–137**	**8-Bit Latched Input DAC for Offset and Gain Adjust**
AD1148	**16**	**20**	**16, µP**	**10V, Int**	**D**	**I**	**C2–137**	**Separate 8-Bit Bus for Offset and Gain Adjust DACs**
***AD1860**	**18**	**1.5**	**Serial, µP**	**Int**	**N**	**C**	**SF–39**	**18-Bit PCM Audio DAC**
DAC1146	18	6	18	10V, Int	Module	C	N	Low Cost, 18-Bit Multiplying DAC
DAC1138	**18**	**10**	**18**	**6V, Int**	**Module**	**C**	**C2–319**	**High Resolution and Accuracy**
AD1139	**18**	**40**	**8, µP**	**–10V, Int**	**D**	**C**	**C2–125**	**True 18-Bit Accuracy**

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Current Output DACs

Model	Res Bits	Settling Time µs typ	Bus Interface Bits[1]	Reference Volt Int/Ext (M)[2]	Package Options[3]	Temp Range	Page	Comments
AD9768	**8**	**0.005**	**8, µP**	**−1.26V, Int**	**D, E**	**C, M**	**C2-301**	**Ultrahigh Speed, ECL Compatible, 20mA Output Current**
AD7524	**8**	**0.1**	**8, µP**	**Ext (M)**	**E, N, P, Q**	**C, I, M**	**C2-187**	**CMOS, Low Cost, 8-Bit Multiplying DAC with Latch**
AD561	**10**	**0.25**	**10**	**Int**	**D, N**	**C, M**	**C2-53**	**Industry Standard 10-Bit DAC, JAN Part Available**
AD7533	**10**	**0.6**	**10**	**Ext (M)**	**E, N, P, Q**	**C, I, M**	**C2-197**	**CMOS, Low Cost 10-Bit Multiplying DAC**
AD568	**12**	**0.035**	**12**	**Int**	**Q**	**C, M**	**C2-69**	**Highest Accuracy 12-Bit Ultrahigh Speed DAC**
HDS-1250	**12**	**0.035**	**12**	**Int**	**D, M**	**C, M**	**C2-345**	**Ultrahigh Speed 12-Bit DAC**
AD668	**12**	**0.05**	**12**	**Ext (M)**	**Q**	**C, M**	**PC2-113**	**Multiplying 12-Bit Ultrahigh Speed DAC**
HDM-1210	**12**	**0.085**	**12**	**Int**	**D**	**I, M**	**C2-339**	**Ultrahigh Speed 12-Bit Multiplying DAC**
AD565A	**12**	**0.25**	**12**	**10V, Int**	**D**	**C, I, M**	**C2-61**	**Industry Workhorse High Speed DAC. JAN Part Available**
AD DAC80-I	12	0.3	12	6.3V, Int	D	C	C2-309	Industry Standard, High Speed Multiplying DAC
AD DAC85-I	12	0.3	12	6.3V, Int	D	I, M	C2-309	Improved Industry Standard
AD DAC87-I	12	0.3	12	6.3V, Int	D	I, M	C2-309	Improved Industry Standard
AD566A	**12**	**0.35**	**12**	**10V, Ext**	**D**	**C, M**	**C2-61**	**High Speed Multiplying DAC**
AD7541A	**12**	**0.6**	**12**	**Ext (M)**	**E, N, P, Q**	**C, I, M**	**C2-227**	**CMOS, 12-Bit Multiplying DAC**
AD7548	**12**	**1**	**8, µP**	**Ext (M)**	**E, N, P, Q**	**C, I, M**	**C2-253**	**CMOS, Byte Load 12-Bit DAC, Specified with Single and Dual Supplies**
AD562	12	1.5	12	Ext	D	C, I, M	C2-57	Industry Standard, JAN Part Available
AD563	12	1.5	12	2.5V, Int	D	C, M	C2-57	Industry Standard
AD7542	**12**	**2.0**	**4, µP**	**Ext (M)**	**D, E, N, P**	**C, I, M**	**C2-233**	**CMOS, Nibble Load 12-Bit Multiplying DAC**
AD7543	**12**	**2.0**	**Serial, µP**	**Ext (M)**	**D, E, N, P, Q**	**C, I, M**	**C2-237**	**CMOS, Serial Load 12-Bit Multiplying DAC**
AD7545	12	2.0	12, µP	Ext (M)	E, N, P, Q	C, I, M	C2-241	CMOS, Parallel Load 12-Bit Multiplying DAC
AD7545A	12	1.0	12, µP	Ext (M)	E, N, P, Q	C, I, M	C2-245	CMOS, Improved AD7545
AD7534	**14**	**1.5**	**8, µP**	**Ext (M)**	**D, N, P**	**C, I, M**	**C2-203**	**CMOS, Byte Load**
AD7535	**14**	**1.5**	**8/14, µP**	**Ext (M)**	**D, E, N, P**	**C, I, M**	**C2-207**	**CMOS, Parallel or Byte Load**
AD7536	**14**	**1.5**	**8/14, µP**	**Ext (M)**	**D, E, N, P**	**C, I, M**	**C2-211**	**CMOS, Parallel or Byte Load, Bipolar Output**
AD7538	**14**	**1.5**	**14, µP**	**Ext (M)**	**N, Q**	**C, I, M**	**C2-219**	**CMOS, Parallel Load**
***AD1856**	**16**	**0.35**	**Serial, µP**	**Int**	**N**	**C**	**SF-39**	**16-Bit PCM Audio DAC**
AD DAC71-I	16	1	16	6.3V, Int	D, H	C	C2-305	High Resolution 16-Bit DAC
AD DAC72-I	16	1	16	6.3V, Int	D, H	C, I	C2-305	High Resolution 16-Bit DAC
***AD1860**	**18**	**0.35**	**Serial, µP**	**Int**	**N**	**C**	**SF-39**	**18-Bit PCM Audio DAC**

[1]This column lists the data format for the bus with "µP" indicating microprocessor capability—i.e., for a 12-bit converter 8/12, µP indicates that the data can be formatted for an 8-bit bus or can be in parallel (12 bits) and is microprocessor compatible.
[2]Ext indicates external reference with the range of voltages listed where applicable. Ext (M) indicates external reference with multiplying capability. Int indicates reference is internal. A voltage value is given if the reference is pinned out.
[3]Package Options: D–Side-Brazed Dual-In-Line Ceramic; E–Leadless Chip Carrier; H–Round Hermetic Metal Can (Header); M–Metal Hermetic Dual-In-Line; N–Plastic Molded Dual-In-Line; P–Plastic Leaded Chip Carrier (PLCC); Q–Cerdip; W–Ceramic/Glass Dual-In-Line, Non-Hermetic; Z–Ceramic Leaded Chip Carrier.
[4]PLLCC = Plastic Leadless Chip Carrier.
Boldface Type: Product recommended for new design.
*New product since the publication of the 1987/1988 Databooks.
†Consult factory for price.

ANALOG DEVICES

Digital-to-Analog Converters

Video DACs

Model	Res Bits	Update Rate MHz min	Settling Time ns max	Reference Voltage Int/Ext[1]	Package Options[2]	Temp Range	Page	Comments
AD9702	4	125	5	Ext	D, W	I	C2–293	RGB Output, TTL or ECL Interface
HDG-0405	4	125	5	Int	D, W	I, M	C2–329	Complete Composite Inputs, Low Glitch Energy, 16 Levels of Gray Scale Output
HDG-0407	4	50	8	Int	D, W	I	C2–335	TTL Compatible Inputs, Low Glitch Energy, 16 Levels of Gray Scale Output
HDG-0605	6	150	8	Int	D, W	I, M	C2–329	Complete Composite Inputs, Low Glitch Energy
*ADV471	6	80, 50, 35			P	C	SF–38	CMOS, Triple 6-Bit Color Palette RAM-DAC
AD9703	8	300	6	Int	D, W	I, M	C2–297	Synchronous Composite Functions, Designed for High Resolution Screens, 300MHz Update Rate
AD9701	8	225	8	Int	E, Q	I, M	C2–287	Low Power, Low Glitch Impulse, Synchronous Composite Functions, 250MHz Update Rate
HDG-0805	8	150	9	Int	D, W	I, M	C2–329	−5.2V Power Supply
AD9700	8	100	12	Ext	D, W	I, M	C2–281	Single −5.2V Power Supply, On-Chip Reference
*ADV478	8	80, 50, 35			P	C	SF–38	CMOS, Triple 8-Bit Color Palette RAM-DAC
*ADV453	8	66, 40			N, P		SF–38	CMOS, Triple 8-Bit Color Palette RAM-DAC
HDG-0807	8	50	14	Int	D, W	I	C2–335	TTL-Compatible Inputs

LOGDACs™

Model	Res dB	Full Scale Range dB	Accuracy dB	Package Options[2]	Temp Range	Page	Comments
AD7111	0.375	88.5	0.17	E, N, Q	C, I, M	C2–143	Low Distortion

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Multiple DACs

Model	Res Bits	Out Mode V/I	Settling Time µs typ	Bus Interface Bits[3]	Reference Volt Int/Ext[1]	# DACs	Package Options[2]	Temp Range	Page	Comments
*AD7669	8	V	1	8, µP	Int	2	N, P	C, I, M	SF–43	CMOS, Complete 8-Bit Dual DAC/ADC/SHA/Reference
AD7225	8	V	5	8, µP	2–12.5V, Ext	4	E, N, P, Q	C, I, M	C2–153	CMOS, Separate Reference for Each DAC
AD7228	8	V	5	8, µP	2–10V, Ext	8	E, N, P, Q	C, I, M	C2–165	CMOS, Specified with Single and Dual Supplies, Skinny 20-Pin Package
AD7226	8	V	7	8, µP	2–12.5V, Ext	4	E, N, P, Q, R	C, I, M	C2–159	CMOS, No User Trims, Specified with Single and Dual Supplies
AD392	12	V	4	12, µP	Int	4	M	C	C2–19	Fast Bus Access Time (<40ns), Data Readback Capability
AD390	12	V	8	12, µP	+10V, Int	4	D	C, M	C2–11	Factory Trimmed Gain and Offset
AD664	12	V	10	12, µP	±14.5V, Ext (M)	4	D, E, N, P	C, I, M	C2–93	Readback, Reset, Low Power Quad DAC
AD394	12	V	15	12, µP	±11V, Ext (M)	4	D	C, M	C2–25	Four Independent Reference Inputs, Precision Amps for Bipolar Output
AD395	12	V	15	12, µP	±11V, Ext (M)	4	D	C, M	C2–25	Four Independent Reference Inputs, Precision Amps for Unipolar Output
AD396	14	V	15	8, µP	±11V, Ext (M)	4	D	C, M	C2–33	Four Independent Reference Inputs, Bipolar Output, Simultaneous Update
AD7528	8	I	0.2	8, µP	Ext (M)	2	E, N, P, Q, R	C, I, M	C2–193	CMOS, +5V to +15V Operation, TTL Compatible at V_{DD} = 5V
AD7628	8	I	0.35	8, µP	Ext (M)	2	E, N, P, Q	C, I, M	C2–273	CMOS, +12V to +15V Operation, TTL Compatible at V_{DD} = 12V to 15V
AD7537	12	I	1.5	8, µP	Ext (M)	2	E, N, P, Q	C, I, M	C2–215	CMOS, Byte Load, Double Buffered
AD7547	12	I	1.5	12, µP	Ext (M)	2	E, N, P, Q	C, I, M	C2–249	CMOS, Parallel Load
AD7549	12	I	1.5	4, µP	Ext (M)	2	D, E, N, P	C, I, M	C2–265	CMOS, Nibble Load, Double Buffered

[1]Ext indicates external reference with the range of voltages listed where applicable. Ext (M) indicates external reference with multiplying capability. Int indicates reference is internal. A voltage value is given if the reference is pinned out.
[2]Package Options: D–Side-Brazed Dual-In-Line Ceramic; E–Leadless Chip Carrier; M–Metal Hermetic Dual-In-Line; N–Plastic Molded Dual-In-Line; P–Plastic Leaded Chip Carrier (PLCC); Q–Cerdip; R–Small Outline Plastic (SOIC); W–Ceramic/Glass Dual-In-Line, Non-Hermetic.
[3]This column lists the data format for the bus with "µP" indicating microprocessor capability—i.e., for a 12-bit converter 8/12, µP indicates that the data can be formatted for an 8-bit bus or can be in parallel (12 bits) and is microprocessor compatible.
Boldface Type: Product recommended for new design.
*New product since the publication of the 1987/1988 Databooks.
†Consult factory for price.

ANALOG DEVICES

Analog-to-Digital Converters

Sampling ADCs

Model	Res Bits	Conv Time µs max	SHA BW kHz typ[1]	Reference Volt Int/Ext[2]	Bus Interface Bits[3]	Package Options[4]	Temp Range	Page	Comments
AD7821	8	0.66	100	0–5V, Ext	8, µP	N, P, Q	C, I	PC3–295	CMOS, Bipolar or Unipolar Operation
AD7569	8	2	200	Int	8, µP	E, N, P, Q	C, I, M	PC3–195	CMOS, Complete I/O Port with DAC, ADC, SHA, AMPs, & Reference
*AD7669	8	2	200	Int	8, µP	N, P	C, I, M	SF–43	CMOS, Complete I/O Port with 2 DACs, ADC, SHA, AMPs, & Reference
AD7820	8	2	7	0–5V, Ext	8, µP	E, N, P, Q, R	C, I, M	C3–283	CMOS, 8-Bit Sampling ADC
AD7824	8	2.5	10	0–5V, Ext	8, µP	N, Q	C, I, M	C3–305	CMOS, 4 Channel, 8-Bit Sampling ADC
AD7828	8	2.5	10	0–5V, Ext	8, µP	E, N, P, Q	C, I, M	C3–305	CMOS, 8 Channel, 8-Bit Sampling ADC
AD7575	8	5	50	1.23V, Ext	8, µP	E, N, P, Q	C, I, M	C3–223	CMOS, Low Cost
AD7579	10	18.5	25	2.5V, Ext	8, µP	E, N, P, Q	C, I, M	C3–237	CMOS, Low Cost 10-Bit Sampling ADC
AD7580	10	18.5	25	2.5V, Ext	10, µP	E, N, P, Q	C, I, M	C3–237	CMOS, Low Cost 10-Bit Sampling ADC
*AD9005	12	0.1	38000	Int	12	M	C, M	SF–41	Complete 12-Bit ADC with T/H, Reference and Timing Circuitry
CAV-1205	12	0.2	15000	Int	12	Card	C	C3–415	12-Bit, 5MSPS Eurocard
CAV-1202	12	0.5	5000	Int	12	Card	C	C3–411	12-Bit, 2MSPS Eurocard
MOD-1205	12	0.5	15000	Int	12	Card	C	C3–443	12-Bit, 5MSPS Video ADC
AD9003	12	1	10000	Int	12	M	C	C3–345	12-Bit, 1MSPS ADC, Single 40-Pin DIP
HAS-1201	12	1	2000	Int	12	M	C, M	C3–423	12-Bit, 1MSPS ADC
HAS-1204	12	2	7000	Int	12	M	C, M	C3–433	12-Bit 500kHz. ADC Single 40-Pin DIP
AD678	12	4	500	5V, Int	8/12, µP	D, N, P	C, M	PC3–123	BiMOS, High Impedance High Bandwidth Sampling Input, 10V Range
*AD1678	12	4	500	Int	8/12, µP	D, N, P	C	SF–42	BiMOS, 12-Bit Sampling ADC, ac Characterized
AD1332	12	8	125	−5V, Int	12, µP	D	I	PC3–175	Complete 12-Bit 125kHz Sampling ADC for Digital Signal Processing
AD7870	12	8	500	3V, Int	8/12/Serial, µP	N, P, Q	C, I, M	PC3–317	CMOS, 100kHz Throughput Rate
AD7878	12	8	500	3V, Int	12, µP	E, N, P, Q	C, I, M	PC3–323	CMOS, 100kHz Throughput, On-Chip FIFO
*AD1334	12	15	235	−5V, Int	12, µP	D	I	SF–41	Four Channel 65kHz 12-Bit Sampling ADC for Digital Signal Processing
AD368	12	15	40–1000	6.3V, Int	12	D	I, M	C3–13	Complete 12-Bit ADC with Programmable Gains of 1, 8, 64, 512
AD369	12	15	40–1000	6.3V, Int	12	M	I	C3–13	Complete 12-Bit ADC with Programmable Gains of 1, 10, 100, 500
AD363	12	40	X	10V, Int	12, µP	D	C, M	C9–5	16-Channel, 12-Bit DAS
AD364	12	50	X	10V, Int	12, µP	D	C, M	C9–5	High Speed, 16-Channel, 12-Bit DAS with Three-State Buffered Output

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Model	Res Bits	Conv Time µs max	SHA BW kHz typ[1]	Reference Volt Int/Ext[2]	Bus Interface Bits[3]	Package Options[4]	Temp Range	Page	Comments
HAS-1409	**14**	**9**	**200–800**	**Int**	**14**	**M**	**C**	**C3–437**	**125kHz Word Rates; Includes T/H**
AD679	**14**	**10**	**500**	**5V, Int**	**8, µP**	**D, N, P**	**C, M**	**PC3–135**	**BiMOS, High-Impedance High-Bandwidth Sampling Input, 10V Input Range**
***AD1679**	**14**	**10**	**500**	**5V, Int**	**8, µP**	**D, N, P**	**C**	**SF–42**	**14-Bit BiMOS Sampling ADC, ac Characterized**
***AD7871**	**14**	**10**	**X**	**3V, Int**	**8/14/Serial, µP**	**D, E, P**	**C, I, M**	**SF–43**	**CMOS, 14-Bit, 100kHz Sampling ADC**
DAS1152	**14**	**40**	**X**	**10V, Int**	**14**	**D**	**I**	**C9–23**	**14-Bit High Accuracy Sampling ADC**
DAS1157	**14**	**55**	**X**	**10V, Int**	**14**	**D**	**I**	**C9–27**	**Low Power, 14-Bit Sampling ADC**
DAS1153	**15**	**50**	**X**	**10V, Int**	**15**	**D**	**I**	**C9–23**	**15-Bit High Accuracy Sampling ADC**
DAS1158	**15**	**55**	**X**	**10V, Int**	**15**	**D**	**I**	**C9–27**	**Low Power, 15-Bit Sampling ADC**
AD1380	**16**	**20**	**900**	**Int**	**16/Serial**	**D**	**C**	**C3–187**	**Low Cost, 16-Bit Sampling ADC. Operation Over −55°C to +85°C Temperature Range**
DAS1159	**16**	**55**	**X**	**10V, Int**	**16**	**D**	**I**	**C9–27**	**Low Power, 16-Bit Sampling ADC**

Multiplexed ADCs

Model	Res Bits	# Chan	Conv Time µs	SHA BW kHz	Reference Volt Int/Ext[2]	Bus Interface Bits[3]	Package Options[4]	Temp Range	Page	Comments
AD7824	**8**	**4**	**2.5**	**10**	**0–5V, Ext**	**8, µP**	**N, Q**	**C, I, M**	**C3–305**	**CMOS, On-Chip Track-Hold**
AD7828	**8**	**8**	**2.5**	**10**	**0–5V, Ext**	**8, µP**	**E, N, P, Q**	**C, I, M**	**C3–305**	**CMOS, On-Chip Track-Hold**
AD7581	8	8	66.7		−5V—(−15V), Ext	8, µP	D, N	C, I	C3–253	CMOS
AD363	**12**	**16**	**40**		**10V, Int**	**12, µP**	**D**	**C, M**	**C9–5**	**High Speed, 16-Channel, 12-Bit DAS**
AD364	**12**	**16**	**50**		**10V, Int**	**12, µP**	**D**	**C, M**	**C9–5**	**16-Channel, 12-Bit DAS with Three-State Buffers**
AD7582	**12**	**4**	**100**		**4V–6V, Ext**	**12, µP**	**D, E, N, P**	**C, I, M**	**C3–261**	**CMOS, 1LSB Total Unadjusted Error**

[1]X indicates that the internal SHA bandwidth is not specified in kHz.
[2]Ext indicates external reference with the range of voltages listed where applicable. Ext (M) indicates external reference with multiplying capability. Int indicates reference is internal. A voltage value is given if the reference is pinned out.
[3]This column lists the data format for the bus with "µP" indicating microprocessor capability—i.e., for a 12-bit converter 8/12, µP indicates that the data can be formatted for an 8-bit bus or can be in parallel (12 bits) and is microprocessor compatible.
[4]Package Options: D–Side-Brazed Dual-In-Line Ceramic; E–Leadless Chip Carrier; M–Metal Hermetic Dual-In-Line; N–Plastic MoldedDual-In-Line; P–Plastic Leaded Chip Carrier (PLCC); Q–Cerdip;R–Small Outline Plastic (SOIC).
Boldface Type: Product recommended for new design.
*New product since the publication of the 1987/1988 Databooks.
†Consult factory for price.

ANALOG DEVICES

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General Purpose ADCs

Model	Res Bits	Conv Time µs	Int SHA BW kHz[1]	Reference Voltage Int/Ext[2]	Bus Interface Bits[3]	Package Options[4]	Temp Range	Page	Comments
AD7821	**8**	**0.66**	**100**	**0–5V, Ext**	**8, µP**	**N, P, Q**	**C, I**	**PC3–295**	**CMOS, Bipolar or Unipolar Operation**
AD7569	**8**	**2**	**200**	**Int**	**8, µP**	**E, N, P, Q**	**C, I, M**	**PC3–195**	**CMOS, Complete I/O Port with DAC, ADC, SHA, Amps and Reference**
***AD7669**	**8**	**2**	**200**	**Int**	**8, µP**	**N, P**	**C, I, M**	**SF–43**	**CMOS, Complete I/O Port with 2 DACS, ADC, SHA, Amps and Reference**
AD7820	**8**	**2**	**7**	**0–5V, Ext**	**8, µP**	**E, N, P, Q, R**	**C, I, M**	**C3–283**	**CMOS, 8-Bit Sampling ADC**
AD7824	**8**	**2.5**	**10**	**0–5V, Ext**	**8, µP**	**N, Q**	**C, I, M**	**C3–305**	**CMOS, 4 Channel, 8-Bit Sampling ADC**
AD7828	**8**	**2.5**	**10**	**0–5V, Ext**	**8, µP**	**E, N, P, Q**	**C, I, M**	**C3–305**	**CMOS, 8 Channel, 8-Bit Sampling ADC**
AD7575	8	5	50	1.23V, Ext	8, µP	E, N, P, Q	C, I, M	C3–223	CMOS, Low Cost
AD670	**8**	**10**		**Int**	**8, µP**	**D, E, N, P**	**C, I, M**	**C3–93**	**Single Supply, Including In-Amp and Reference**
AD7576	8	10		1.23V, Ext	8, µP	E, N, P, Q	C, I, M	C3–227	CMOS, Low Cost
AD570	8	25		Int	8	D	C, M	C3–39	
AD673	8	30		Int	8, µP	D, N, P	C, M	C3–105	
AD7581	8	66.7		−5V—(−15V), Ext	8, µP	D, N	C, I	C3–253	CMOS 8-Bit ADC
AD579	**10**	**1.8**		**10V, Int**	**10/Serial**	**D, N**	**C, I**	**C3–87**	
AD7579	**10**	**18.5**	**25**	**2.5V, Ext**	**8, µP**	**E, N, P, Q**	**C, I, M**	**C3–237**	**CMOS, Low Cost 10-Bit Sampling ADC**
AD7580	**10**	**18.5**	**25**	**2.5V, Ext**	**10, µP**	**E, N, P, Q**	**C, I, M**	**C3–237**	**CMOS, Low Cost 10-Bit Sampling ADC**
AD571	**10**	**25**		**Int**	**10**	**D**	**C, M**	**C3–39**	
AD573	**10**	**30**		**Int**	**8/10, µP**	**D, N, P**	**C, M**	**C3–53**	
AD575	**10**	**30**		**Int**	**Serial**	**D, N**	**C, M**	**C3–73**	
***AD9005**	**12**	**0.1**	**38000**	**Int**	**12**	**M**	**C, M**	**SF–41**	**Complete 12-Bit ADC with T/H, Reference and Timing Circuitry**
CAV-1205	**12**	**0.2**	**15000**	**Int**	**12**	**Card**	**C**	**C3–415**	**12-Bit, 5MSPS Eurocard**
CAV-1202	**12**	**0.5**	**5000**	**Int**	**12**	**Card**	**C**	**C3–411**	**12-Bit, 2MSPS Eurocard**
MOD-1205	**12**	**0.5**	**15000**	**Int**	**12**	**Card**	**C**	**C3–443**	**12-Bit, 5MSPS Video ADC**
AD9003	**12**	**1**	**10000**	**Int**	**12**	**M**	**C**	**C3–345**	**12-Bit, 1MSPS ADC. Single 40-Pin DIP**
HAS-1201	**12**	**1**	**2000**	**Int**	**12**	**M**	**C, M**	**C3–423**	**12-Bit, 1MSPS ADC**
HAS-1202A	**12**	**1.6**		**Int**	**12**	**D**	**C, I, M**	**C3–429**	**12-Bit, 641kHz ADC**
HAS-1204	**12**	**2**	**7000**	**Int**	**12**	**M**	**C, M**	**C3–433**	**12-Bit, 500kHz ADC. Single 40-Pin DIP**
HAS-1202	**12**	**2.9**		**Int**	**12**	**D**	**C, I, M**	**C3–429**	**12-Bit, 349kHz ADC**
AD578	**12**	**3**		**10V, Int**	**12**	**D, N**	**C, M**	**C3–81**	**Complete, 3µs, 12-Bit ADC**
AD7672	**12**	**3**		**−5V, Ext**	**12, µP**	**E, N, P, Q**	**C, I, M**	**C3–267**	**CMOS, Unipolar or Bipolar, −12V, +5V Supply**
AD678	**12**	**4**	**X**	**5V, Int**	**12, µP**	**D, N, P**	**C**	**PC3–123**	**BiMOS, High-Impedance, High-Bandwidth Sampling Input, 10V Range**

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Model	Res Bits	Conv Time µs	Int SHA BW kHz[1]	Reference Voltage Int/Ext[2]	Bus Interface Bits[3]	Package Options[4]	Temp Range	Page	Comments
***AD1678**	**12**	**4**	**500**	**Int**	**8/12, µP**	**D, N, P**	**C**	**SF–42**	**BiMOS, 12-Bit Sampling ADC, ac Characterized**
AD5240	12	5		6.3V, Int	12	D	C, I	C3–391	Industry Standard
AD7572	**12**	**5**		**−5.25V, Int**	**12, µP**	**E, N, P, Q**	**C, I, M**	**C3–211**	**CMOS 12-Bit ADC**
AD1332	**12**	**8**	**125**	**−5V, Int**	**12, µP**	**D**	**I**	**PC3–175**	**Complete 12-Bit 125kHz Sampling ADC for Digital Signal Processing**
AD7870	**12**	**10**	**X**	**3V, Int**	**8/12/Serial, µP**	**E, N, P, Q**	**C, I, M**	**PC3–317**	**CMOS, 100kHz Throughput—**
AD7878	**12**	**10**	**X**	**3V, Int**	**12, µP**	**E, N, P, Q**	**C, I, M**	**PC3–323**	**CMOS, 100kHz Throughput, On-Chip FIFO. Serial, Parallel or Byte Output**
***AD7772**	**12**	**10**	**X**	**5.25, Int**	**Serial, µP**	**E, N, P, Q**	**C, I, M**	**SF–42**	**CMOS, Serial Output 12-Bit ADC**
***AD1334**	**12**	**15**	**235**	**−5V, Int**	**12, µP**	**D**	**I**	**SF–41**	**Four Channel 65kHz 12-Bit Sampling ADC for Digital Signal Processing**
AD ADC84	12	10		6.3V, Int	12	D	C	C3–391	Industry Standard
AD ADC85	12	10		6.3V, Int	12	D	C, I	C3–391	Industry Standard
AD5210	12	13		−10V, Int/Ext	12	D	I, M	C3–189	Industry Standard
AD674A	**12**	**15**		**10V, Int**	**12, µP**	**D**	**C, M**	**C3–113**	**Complete 12-Bit ADC**
AD368	**12**	**15**	**40–1000**	**6.3V, Int**	**12**	**D**	**I, M**	**C3–13**	**Complete 12-Bit ADC with Programmable Gains of 1, 8, 64, 512**
AD369	**12**	**15**	**40–1000**	**6.3V, Int**	**12**	**M**	**I**	**C3–13**	**Complete 12-Bit ADC with Programmable Gains of 1, 10, 100, 500**
AD572	12	25		10V, Int	12	D, M	I, M	C3–45	12-Bit Successive Approximation ADC
AD ADC80	12	30		6.3V, Int	12	D	I	C3–383	Industry Standard
AD574A	**12**	**35**		**10V, Int**	**8/12, µP**	**D, E, N, P**	**C, M**	**C3–61**	**Complete ADC with Reference and Clock**
AD363	**12**	**40**	**X**	**10V, Int**	**12, µP**	**D**	**C, M**	**C9–5**	**High Speed 16-Channel, 12-Bit DAS**
AD364	**12**	**50**	**X**	**10V, Int**	**12, µP**	**D**	**C, M**	**C9–5**	**16-Channel, 12-Bit DAS with Three-State Buffered Output**

[1]X indicates that the internal SHA bandwidth is not specified in kHz.
[2]Ext indicates external reference with the range of voltages listed where applicable. Ext (M) indicates external reference with multiplying capability. Int indicates reference is internal. A voltage value is given if the reference is pinned out.
[3]This column lists the data format for the bus with "µP" indicating microprocessor capability—i.e., for a 12-bit converter 8/12, µP indicates that the data can be formatted for an 8-bit bus or can be in parallel (12 bits) and is microprocessor compatible.
[4]Package Options: D–Side-Brazed Dual-In-Line Ceramic; E–Leadless Chip Carrier; M–Metal Hermetic Dual-In-Line; N–Plastic Molded Dual-In-Line; P–Plastic Leaded Chip Carrier (PLCC); Q–Cerdip; R–Small Outline Plastic (SOIC).
Boldface Type: Product recommended for new design.
*New product since the publication of the 1987/1988 Databooks.
†Consult factory for price.

ANALOG DEVICES

Analog-to-Digital Converters

General Purpose ADCs

Model	Res Bits	Conv Time µs	Int SHA BW kHz[1]	Reference Voltage Int/Ext[2]	Bus Interface Bits[3]	Package Options[4]	Temp Range	Page	Comments
AD5200	12	50		−10V, Int/Ext	12	D	I, M	C3–189	Industry Standard
AD7578	12	100		5V, Ext	12, µP	D, N	C, I, M	C3–231	**CMOS, 1LSB Total Unadjusted Error**
AD7582	12	100		5V, Ext	12, µP	D, E, N, P	C, I, M	C3–261	**CMOS, 1LSB Total Unadjusted Error**
HAS-1409	14	9	200–800	Int	14	M	C	C3–437	**14-Bit, 125kHz ADC. Single 40-Pin DIP**
AD679	14	10	X	5V, Int	14, µP	D, N, P	C	C3–135	**BiMOS, High Impedance, High Bandwidth Sampling Input, 10V Input Range**
***AD1679**	14	10	500	5V, Int	8/14, µP	D, N, P	C	SF–42	**14-Bit BiMOS Sampling ADC, ac Characterized**
***AD7871**	14	10	X	3V, Int	8/14/Serial, µP	E, N, P, Q	C, I, M	SF–43	**CMOS, 14-Bit, 100kHz Sampling ADC**
ADC1131	14	12		Int	14	Module	C	C3–399	**14-Bit, High Speed ADC**
ADC1130	14	25		Int	14	Module	C	C3–399	**14-Bit, High Speed ADC**
DAS1152	14	40	X	10V, Int	16	Module	I	C9–23	**14-Bit High Accuracy Sampling ADC**
DAS1157	14	55	X	10V, Int	16	Module	I	C9–27	**Low Power, 14-Bit Sampling ADC**
DAS1153	15	50	X	10V, Int	16	Module	I	C9–23	**15-Bit High Accuracy Sampling ADC**
DAS1158	15	55	X	10V, Int	16	Module	I	C9–27	**Low Power, 15-Bit Sampling ADC**
***AD1377**	16	10	X	Int	16, Serial	D	C	SF–41	**Complete 16-Bit Converter. Industry Standard Pin Out**
AD376	16	15		Int	16	M	C	C3–31	**Complete, High Speed 16-Bit ADC**
AD1376	16	15		Int	16, Serial	V	C	C3–179	**Complete, High Speed 16-Bit ADC Operation over −25°C to +85°C**
AD1380	16	20	900	Int	16, Serial	D	C	PC3–187	**Low Cost, 16-Bit Sampling ADC Operation over −55°C to +85°C Temperature Range**
ADC1140	16	35		10V, Int	16	Module	C	C3–403	**16-Bit ADC, Operates over −25°C to +85°C Temperature Range**
ADC1143	16	70		10V, Int	16	Module	C	N	Low Power 10-Bit ADC
AD ADC71	16	50		6.3V, Int	16	D, M	C	C3–375	Industry Standard
AD ADC72	16	50		6.3V, Int	16	D, M	C, I	C3–375	Industry Standard
DAS1159	16	55	X	10V, Int	16	D	I	C9–27	**Low Power, 16-Bit Sampling ADC**
AD1170	18	1000		5V, Int	24	D	C	C3–155	**7 to 22-Bit Programmable Integrating ADC**
ADi175K	22	50ms		6.95V, Int/Ext	24	Module	C	PC3–167	**High Accuracy, 22-Bit Integrating ADC**

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Video ADCs

Model	Res Bits	Throughput Rate MSPS min	Full Power BW MHz typ	Reference Voltage Int/Ext[2]	Bus Interface Bits[3]	Package Options[4]	Temp Range	Page	Comments
AD9688	**4**	**175**	**100**	**0.16–6V, Ext**	**4**	**E, Q**	**I, M**	**C3–369**	**Second Source to AM688, Overrange Bits, Stackable to 8 Bits**
***AD9006**	**6**	**470**	**250 (min)**	**±1V, Ext**	**6, μP**	**E, Z**	**C, M**	**SF–40**	**470MSPS, 6-Bit ADC. 8.5pF Input Capacitance**
***AD9016**	**6**	**470**	**250 (min)**	**±1V, Ext**	**6, μP**	**E, Z**	**C, M**	**SF–40**	**470MSPS, 6-Bit ADC with On-Board Demultiplexing Circuitry**
AD9000	**6**	**50**	**20**	**0.5–2V, Ext**	**6**	**D, E**	**C, M**	**C3–331**	**MIL-STD-883, Rev. C, Devices Available. Low Error Rate**
AD770	**8**	**200**	**250**	**±2V, Ext**	**8**	**D**	**C, M**	**PC3–147**	**High Bandwidth, Error Correction**
AD9002	**8**	**125**	**115 (Sm. Sig.)**	**0.1—(−2.1) Ext**	**8**	**D, E**	**I, M**	**C3–339**	**Single Supply, Low Power, Low Input Capacitance, MIL-STD-883, Rev. C Device Available**
***AD9011**	**8**	**100**	**80**	**Int**	**8**	**M**	**C, M**	**SF–40**	**8-Bit, 100MSPS ADC with On-Board Amp and Reference, Multiple Gain Selection**
AD9012	**8**	**75**	**180**	**−2V, Ext**	**8**	**Q, E**	**I, M**	**C3–353**	**TTL Compatible Outputs**
***AD9048**	**8**	**35**	**15**	**−2V, Ext**	**8, μP**	**N, P, Q, Z**	**C, M**	**SF–40**	**35MSPS, 8-Bit Video ADC, 16pF Input Capacitance**
AD9502	**8**	**13**	**7.5**	**Int**	**8**	**M**	**I**	**C3–361**	**RS-170 Video Frame Grabber. Digitizes RS-170, NTSC, PAL Signals**
CAV-1040	10	40	20	Int	10	Card	C	C3–407	Excellent Dynamic Performance over Frequency
CAV-1040A	**10**	**40**	**40**	**Int**	**10**	**Card**	**C**	**C3–407**	**Higher Input Bandwidth Version of CAV-1040**
CAV-1220	**12**	**20**	**35**	**Int**	**12**	**Card**	**C**	**C3–419**	**Fastest 12-Bit A/D Converter Available**

[1]X indicates that the internal SHA bandwidth is not specified in kHz.
[2]Ext indicates external reference with the range of voltages listed where applicable. Ext (M) indicates external reference with multiplying capability. Int indicates reference is internal. A voltage value is given if the reference is pinned out.
[3]This column lists the data format for the bus with "μP" indicating microprocessor capability—i.e., for a 12-bit converter 8/12, μP indicates that the data can be formatted for an 8-bit bus or can be in parallel (12 bits) and is microprocessor compatible.
[4]Package Options: D–Side-Brazed Dual-In-Line Ceramic; E–Leadless Chip Carrier; M–Metal Hermetic Dual-In-Line; N–Plastic Molded Dual-In-Line; P–Plastic Leaded Chip Carrier (PLCC); Q–Cerdip; V–Pin-Stake; Z–Ceramic Leaded Chip Carrier.
Boldface Type: Product recommended for new design.
*New product since the publication of the 1987/1988 Databooks.
†Consult factory for price.

ANALOG DEVICES

V/F and F/V Converters

Voltage-to-Frequency Converters

Model	Full-Scale Frequency MHz	Linearity % max	FS Calib Error % typ	Output Format	Input Range V	Package Options[1]	Temp Range	Page	Comments
AD652	**2**	**0.005–0.05**	**0.25–0.5**	**Pulse Train**	**0 to 10 0 to −10 ±5**	**Q, P**	**C, I, M**	**C4–25**	**Synchronous, Multiple Input Ranges, Low Nonlinearity**
AD650	**1**	**0.005–0.1**	**5–10**	**Pulse Train**	**−10 to 0**	**D, N, P**	**C, I, M**	**C4–13**	**Low Nonlinearity**
AD654	**0.5**	**0.1–0.4**	**10**	**Square Wave**	**0 to (V_S–4)**	**N, R**	**C**	**C4–41**	**Single Supply, Low Cost**
ADVFC32	0.5	0.01–0.2	5	Pulse Train	0 to 10	H, N	C, I, M	C4–49	Industry Standard
AD537	0.15	0.07–0.25	5	Square Wave	$-V_S$ to ($+V_S$–4)	D, H	C, M	C4–5	

Frequency-to-Voltage Converters

Model	Input Range kHz	Linearity % max	Response Time ms typ	Package Options[1]	Temp Range	Page	Comments
451	0 to 10	0.03–0.008	4	Module	I	C4-53	Complete, No External Components
453	0 to 100	0.03–0.008	0.8	Module	I	C4-53	Complete, No External Components

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Synchro, Resolver, Inductosyn‡ and LVDT-to-Digital Converters

Model	Res Bits	Input Format[2]	Accuracy arc mins	Tracking Rate Options revs/sec[3]	Reference Frequency Options Hz	Input Isol	Package Options[1]	Temp Range	Page	Comments
SDC/RDC1741	12	S, R	± 15.3	18	400, 2.6k	Yes	D	C, E	C5–19	Tristate, Latched Output Internal Transformer Isolation
SDC/RDC1742	12	S, R	± 8.5	18	400, 2.6k	Yes	D	C, E	C5–19	Tristate, Latched Output Internal Transformer Isolation
1S20	12	I, R	± 8.5	50, 90, 170	400→2.6k, 2.6k→5k, 5k→10k	No	D	C, E	C5–33	High Tracking Rate with Velocity, Error, Ripple Carry and Direction Outputs. Latched, Tristate Output. Low Cost
2S81	**12**	**I, R**	**± 30[4]**	**260**	**400–20k**	**No**	**D**	**C**	**C5–71**	**Monolithic, User Selectable Dynamic Characteristics High Tracking Rate, Quality Velocity Output**
SDC/RDC1740	14	S, R	± 5.3	12	400, 2.6k	Yes	D	C, E	C5–19	Tristate, Latched Output Internal Transformer Isolation
1S40	14	I, R	± 5.3	12.5, 22.5, 42.5	400→2.6k, 2.6k→5k, 5k→10k	No	D	C, E	C5–33	High Tracking Rate with Velocity Ripple Carry and Direction Outputs. Latched, Tristate Output. Low Cost
2S54	14	LVDT	± 0.03[5]	360LSB/ms[6]	360→5k	No	D	C, E	C5–51	Direct Ratiometric Conversion of LVDT Signal, Selectable Input Gain. No External Trims
1S60	16	I, R	± 4.0, ± 2.6[4]	3, 5.5, 10.5	400→2.6k, 2.6k→5k, 5k→10k	No	D	C, E	C5–33	High Tracking Rate with Velocity, Error, Ripple Carry and Direction Outputs. Latched, Tristate Output. Low Cost
1S61	16	I, R	± 10, ± 4.0[4]	3, 5.5, 10.5	400→2.6k, 2.6k→5k, 5k→10k	No	D	C, E	C5–33	Lower Accuracy Version of 1S60. Low Cost
2S56	16	LVDT	± 0.03[5]	360LSB/ms[6]	360→5k	No	D	C, E	C5–51	Direct Ratiometric Conversion of LVDT Signal, Selectable Input Gain. No External Trims
2S80	**16, 14, 12, 10[7]**	**I, R**	**± 2, ± 4, ± 8**	**1040[8]**	**50–20k**	**No**	**D**	**C, E**	**C5–59**	**Monolithic, User Selectable Dynamic Characteristics, and Resolution High Tracking Rate and Quality Velocity Output**
2S82	**16, 14, 12, 10[7]**	**I, R**	**± 2, ± 4, ± 8**	**1040[8]**	**50–20k**	**No**	**E, P**	**C, E**	**PC5–83**	
2S50	11	LVDT	0.1[5]	200LSB/ms[6]	400, 1k→10k	No	D	C, E	C5–49	Direct Conversion of LVDT Signal, No External Trims Required, Tristate Output

NOTES
[1]Package Options: D–Side-Brazed Dual-In-Line Ceramic; E–Leadless Chip Carrier; H–Round Hermetic Metal Can (Header); N–Plastic Molded Dual-In-Line; P–Plastic Leaded Chip Carrier (PLCC); Q–Cerdip; R–Small Outline Plastic (SOIC).
[2]S = Synchro; R = Resolver; I = Inductosyn.
[3]Revs/sec equivalent to pitches/sec in the case of an Inductosyn; in general higher reference frequency options have higher tracking rates.
[4]Consult Data Sheet.
[5]LVDT Converter Accuracy given as % Full Scale.
[6]Slew Rate (min).
[7]Resolution is User Selectable.
[8]Depends on Resolution Selected.
Boldface Type: Product recommended for new design.
*New product since the publication of the 1987/1988 Databooks.
†Consult factory for price.
‡Inductosyn is a registered trademark of Farrand Industries, Inc.

ANALOG DEVICES

ANALOG DEVICES

Synchro and Resolver Converters

Digital-to-Synchro and Resolver Converters

Model	Res Bits	Output Format[1]	Accuracy arc mins	Load Driving Capability	Reference Frequency Options Hz	Reference Input Volt Options V rms	Signal Output Volt Options V rms	Transformer Output Isolation	Package Options[2]	Temp Range	Page	Comments
DRC1745	14	R	±2, ±4[3]	2.0VA[4]	dc→2600	0→3.4	0→6.8	Use Ext. STM1680 and STM1683 Transformer	D	M	C5-7	Digital-to-Resolver Converter with Int. 2VA Power Amplifier. Optional Int. TransZorb‡ Protection. 2 Byte Latched Inputs.
DRC1746	16	R	±2, ±4[3]	2.0VA[4]	dc→2600	0→3.4	0→6.8	Use Ext. STM1680 and STM1683 Transformer	D	M	C5-7	16-Bit Version of DRC1745

Input Transformers

Model	Description	Frequency Hz	Accuracy arc mins	Input Voltage Options V rms[5]	Package Options	Package Size Inches (mm)	Page
5S72	Ref Isolation for 1S14/24/44/64/74 and 1S20/40/60/61	360 to 3000	N/A	11.8, 26, 115	Module	1.12 × 1.12 × 0.4 (28.5 × 28.5 × 10.2)	C5-85
5S70	Signal Input for 1S14/24/44/64/74 and 1S20/40/60/61	360 to 3000	±0.33 (typ) ±1.5 (max)	11.8, 26, 90	Module	2.25 × 1.12 × 0.4 (57.0 × 28.5 × 10.2)	C5-85

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Model	Specified Accuracy %	Acquisition Time µs max	Aperture Time ns typ	Aperture Jitter ns typ	Droop Rate µV/µs max	Package Options[2]	Temp Range	Page	Comments
AD389	**0.003**	**2.5**	**30**	**0.4**	**0.1**	**D**	**C, I**	**C6–11**	**High Resolution Track-and-Hold Amplifier**
SHA1144	0.003	8	50	0.5	2	Module	C	N	High Resolution Track-and-Hold Amplifier
HTC-0300A	**0.01**	**0.1**	**6**	**0.05**	**0.5**	**D**	**I, M**	**C6–33**	**Ultrahigh Speed Track-and-Hold Amplifier**
AD683	**0.01**	**0.5**	**5**	**0.05**	**0.01**	**P, Q**	**I, M**	**PC6–29**	**Very High Speed, Precision. Same Pin Out as AD681**
AD681	**0.01**	**0.9**	**5**	**0.05**	**0.01**	**P, Q**	**I, M**	**PC6–29**	**Pin-Compatible with HA-5330, One Half the Power**
***AD684**	**0.01**	**1.0**	**25**	**0.2**	**0.001**	**P, Q**	**C, I, M**	**SF–44**	**Quad, Monolithic 1µs SHA**
AD346	0.01	2.0	60	0.4	0.5	D	C, M	C6–5	High Speed Sample-and-Hold
AD585	**0.01**	**3.0**	**35**	**0.5**	**1**	**E, P, Q**	**C, I, M**	**C6–23**	**High Speed, Precision. On-Board Hold Cap**
AD583	0.01	5.0	50	5		D	C	C6–21	5µs SHA
HTS-0010	**0.01**	**0.014**	**2**	**0.005**		**D**	**C, I**	**C6–37**	**Ultrahigh Speed Track-and-Hold Amplifier**
HTS-0025	**0.01**	**0.025**	**5**	**0.02**		**D**	**C, I**	**C6–43**	**Ultrahigh Speed Track-and-Hold Amplifier**
AD582	0.1	6.0	200	15		D, H	C, M	C6–17	Low Cost, 25µs

[1]R = Resolver.
[2]Package Options: D–Side-Brazed Dual-In-Line Ceramic; E–Leadless Chip Carrier; H–Round Hermetic Metal Can (Header); P–Plastic Leaded Chip Carrier (PLCC); Q–Cerdip.
[3]Depends on option.
[4]Can be used with pulsating power supply for reduced dissipation.
[5]Synchro and resolver format available on all models.
Boldface Type: Product recommended for new design.
*New product since the publication of the 1987/1988 Databooks.
†Consult factory for price.
‡TransZorb is a trademark of General Semiconductor Industries, Inc.

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ANALOG DEVICES

Analog Switches & Multiplexers

CMOS Switches

Model	Function	Leakage Current nA max	R_{ON} Ω max	Latched	Package Options[1]	Temp Range	Page	Comments
*ADG201HS	Quad SPST	1	50		E, N, P, Q, R	C, I, M	SF–44	CMOS, High-Speed Quad Switch. 44V Supply Maximum Ratings
ADG201A	Quad SPST	1–2	90		E, N, P, Q, R	C, I, M	C7–17	CMOS, 44V Supply Maximum Ratings
ADG202A	Quad SPST	1–2	90		E, N, P, Q, R	C, I, M	C7–17	CMOS, 44V Supply Maximum Ratings
ADG221	Quad SPST	1–2	90	X	E, N, P, Q, R	C, I, M	C7–25	CMOS, Latched Input, 44V Supply Maximum Ratings
ADG222	Quad SPST	1–2	90	X	E, N, P, Q	C, I, M	C7–25	CMOS, Latched Input, 44V Supply Maximum Ratings
AD7510DI	Quad SPST	5–10	100		E, N, P, Q	C, M	C7–9	DiCMOS, Dielectrically Isolated
AD7511DI	Quad SPST	5–10	100		E, N, P, Q	C, M	C7–9	DiCMOS, Dielectrically Isolated
AD7590DI	Quad SPST	5	90	X	E, N, P, Q	C, I, M	C7–13	DiCMOS, Latched, Dielectrically Isolated
AD7591DI	Quad SPST	5	90	X	E, N, P, Q	C, I, M	C7–13	DiCMOS, Latched, Dielectrically Isolated
ADG211A	Quad SPST	5	115		N, P, R	C	C7–21	CMOS, Low Cost, 44V Supply Maximum Ratings
ADG212A	Quad SPST	5	115		N, P	C	C7–21	CMOS, Low Cost, 44V Supply Maximum Ratings
AD7512DI	Dual SPDT	5–10	100		E, N, P, Q	C, M	C7–9	DiCMOS, Dielectrically Isolated
AD7592DI	Dual SPDT	5	90	X	E, N, P, Q	C, M	C7–13	DiCMOS, Latched, Dielectrically Isolated

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Analog CMOS Multiplexers

Model	Function	Leakage Current nA max	R_{ON} Ω max	Latched	Package Options[1]	Temp Range	Page	Comments
ADG506A	**16:1**	**1**	**280**		**E, N, P, Q**	**C, I, M**	**C7–29**	**Superior Second Source to DG506A**
ADG526A	**16:1**	**1**	**280**	**X**	**E, N, P, Q**	**C, I, M**	**C7–41**	**Superior Second Source to DG526A**
AD7506	16:1	1–5	400		D, E, N	C, M	C7–7	
ADG507A	**Dual 8:1**	**1**	**280**		**E, N, P, Q**	**C, I, M**	**C7–29**	**Superior Second Source to DG507A**
ADG527A	**Dual 8:1**	**1**	**280**	**X**	**E, N, P, Q**	**C, I, M**	**C7–41**	**Superior Second Source to DG527A**
AD7507	Dual 8:1	1–5	400		D, E, N	C, M	C7–7	
ADG508A	**8:1**	**1**	**300**		**E, N, P, Q, R**	**C, I, M**	**C7–37**	**Superior Second Source to DG508A**
ADG528A	**8:1**	**1**	**300**	**X**	**E, N, P, Q, R**	**C, I, M**	**C7–49**	**Superior Second Source to DG528A**
AD7501	8:1	1-5	300		E, N, Q	C, M	C7–5	
AD7503	8:1	1–5	300		E, N, Q	C, M	C7–5	
ADG509A	**Dual 4:1**	**1**	**300**		**E, N, P, Q, R**	**C, I, M**	**C7–37**	**Superior Second Source to DG509A**
ADG529A	**Dual 4:1**	**1**	**300**	**X**	**E, N, P, Q, R**	**C, I, M**	**C7–49**	**Superior Second Source to DG529S**
AD7502	Dual 4:1	1–5	300		E, N, Q		C7–5	

Video Multiplexers

Model	Function	Full Power BW MHz min	Crosstalk Rejection F = 10MHz dB	Package Options[1]	Temp Range	Page	Comments
***AD9300**	**4:1**	**30**	**75**	**E, Q**	**C, M**	**SF–44**	**Wideband Video Mux**

[1]Package Options: D–Side-Brazed Dual-In-Line Ceramic; E–Leadless Chip Carrier; N–Plastic Molded Dual-In-Line; P–Plastic Leaded Chip Carrier (PLCC); Q–Cerdip; R–Small Outline Plastice (SOIC).
Boldface Type: Product recommended for new design.
*New product since the publication of the 1987/1988 Databooks.
†Consult factory for price.

ANALOG DEVICES

Voltage References

Model	Ouput Voltage V	Initial Accuracy % F.S. max	Temp Stability ppm/°C max	Package Options[1]	Temp Range	Page	Comments
AD589	**+1.235**	**1.2–2.8**	**10–100**	**H**	**C, M**	**C8–51**	**Two Terminal, 1.2V Reference**
AD580	**+2.5**	**0.4–3**	**10–85**	**H**	**C, M**	**C8–5**	**Precision, Three Terminal, 2.5V Reference**
AD1403	+2.5	0.4–1	25–40	N	C	C8–63	Second Source, 2.5V Reference
AD586	**+5**	**0.05–0.4**	**5–25**	**Q, R**	**C, M**	**C8–23**	**Precision, Buried Zener 5V Reference**
ADREF02	+5	0.3–0.5	8.5–25	Q	C, M	C8–79	Second Source, 5V Reference
AD689	**+8.129**	**0.05–0.2**	**5–25**	**Q**	**C, M**	**C8–55**	**Precision, 8.192 Volt Reference**
AD2700	+10	0.025–0.05	3–10	D	C, M	C8–67	Very High Precision 10V Reference
AD581	+10	0.05–0.3	5–30	H	C, M	C8–9	Three Terminal 10V Bandgap Reference
AD587	**+10**	**0.05–0.1**	**5–20**	**Q, R**	**C, M**	**C8–31**	**Precision Buried Zener 10V Reference**
ADREF01	+10	0.3–0.5	8.5–25	Q	C, M	C8–75	Second Source 10V Reference
AD2710	**+10**	**0.01**	**1–5**	**N**	**C**	**C8–71**	**Ultrahigh Precision 10V Reference**
AD2712	**±10**	**0.01**	**1–5**	**N**	**C**	**C8–71**	**Ultrahigh Precision ±10V Reference**
AD2702	**±10**	**0.025–0.05**	**3–10**	**D**	**C, M**	**C8–67**	**Very High Precision ±10V Reference over Full Military Temp Range**
AD2701	**−10**	**0.025–0.05**	**3–10**	**D**	**C, M**	**C8–67**	**Very High Precision −10V Reference**
AD588	**Selectable**	**0.01–0.03**	**1.5–4**	**D**	**I, M**	**C8–39**	**Ultrahigh Precision, Monolithic Programmable Reference**
AD584	**Selectable**	**0.05–0.3**	**5–30**	**E, H**	**C, M**	**C8–15**	**Precision, Programmable Bandgap Reference**

Comparators

Model	Prop Delay ns max	Logic	V_{OS} mV max	Package Options[1]	Temp Range	Page	Comments
AD96685	**3.5**	**ECL**	**2**	**E, H, P, Q**	**I, M**	**L3–17**	**Ultrafast**
AD96687	**3.5**	**ECL**	**2**	**E, P, Q**	**I, M**	**L3–17**	**Dual AD96685**
AD9685	3	ECL	5	D, E, H	I, M	L3–9	
AD9687	4	ECL	5	D, E	I, M	L3–9	Dual AD9685
AD9686	**7 (typ)**	**TTL**	**2**	**E, H, Q**	**I, M**	**L3–13**	**Complementary TTL Outputs**
AD790	**35**	**TTL**	**0.5–1**	**N, Q, R**	**C, I, M**	**PL3–5**	**Fast, Precise Single Supply**

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Low Cost, General Purpose Amplifiers

Model	V_{OS} mV max	V_{OS} TC µV/°C max	I_B nA max	BW MHz typ[2]	SR V/µs typ	Settling Time µs 0.01% typ	Noise µV p-p 0.1–10Hz typ	Package Options[1]	Temp Range	Page	Comments
AD707	**0.015–0.09**	**0.1–1**	**1–2.5**	**0.9**	**0.15**	**—**	**0.23**	**H, N, Q, R**	**C, I, M**	**PL2–103**	**Very High dc Precision**
AD OP-07	**0.025–0.15**	**0.6–2.5**	**3–12**	**0.6**	**0.17**	**—**	**0.35-0.38**	**H, N, Q, R**	**C, M**	**L2–223**	**Improved Industry Standard**
AD711	**0.25–2**	**3–20**	**0.025–0.05**	**4**	**20**	**1**	**2**	**H, N, Q, R**	**C, I, M**	**L2–107**	**Excellent Combination of ac and dc Performance at Very Competitive Prices**
AD548	**0.25–2**	**2–20**	**0.01–0.02**	**1**	**1.8**	**8**	**2**	**H, N, Q, R**	**C, I, M**	**L2–55**	**Low Power, HighPerformance**
AD542	0.5–2	5–20	0.025–0.05	1	3	—	2	H	C, M	L2–47	High Performance BiFET
AD544	0.5–2	5–20	0.025–0.05	2	13	—	2	H	C, M	L2–47	High Performance BiFET
AD741	3–6	20	200–500	1	0.5	—	—	H, N	C, I, M	L2–133	Improved Second Source

Low Input Current Amplifiers

Model	I_B pA max	Input Impedance Differential Ω||pF typ	Input Impedance Common-Mode Ω||pF typ	CMRR dB f = 1kHz typ	V_{OS} mV max	V_{OS} TC µV/°C max	BW MHz typ[2]	Package Options[1]	Temp Range	Page	Comments
AD549	**0.06–0.25**	**10^{13}||1**	**10^{15}||0.8**	**62**	**0.25–1**	**5–20**	**1**	**H**	**C, M**	**L2–63**	**Monolithic, Lowest I_B**
AD515A	0.075–0.3	10^{13}||1.6	10^{15}||0.8	62	1–3	15–50	1	H	C	L2–35	Lower Cost AD515 Replacement
AD515	0.075–0.3	10^{13}||1.6	10^{15}||0.8	87	1–3	15–50	0.35	H	C	N	FET-Input Electrometer Op Amp
*AD545A	1–2	10^{13}||1.6	10^{15}||0.8	62	0.25–1	3–25	1	H	C	N	Lower Cost AD545 Replacement
AD545	1–2	10^{13}||1.6	10^{15}||0.8	87	0.25–1	3–25	0.7	H	C	N	Low Drift FET Input Op Amp
AD548	**10–20**	**10^{12}||3**	**3×10^{12}||3**	**84**	**0.25–2**	**2–20**	**1**	**H, N, Q, R**	**C, I, M**	**L2–55**	**Low Power, Low Cost**
AD547	25–50	10^{12}||6	10^{12}||3	60	0.25–1	1–5	1	H	C, M	L2–47	Low Drift
AD711	**25–50**	**3×10^{12}||5.5**	**3×10^{12}||5.5**	**62**	**0.025–2**	**3–20**	**4**	**H, N, Q, R**	**C, I, M**	**L2–107**	**Low Cost BiFET, Excellent ac and dc Performance**

[1]Package Options: D–Side-Brazed Dual-In-Line Ceramic; E–Leadless Chip Carrier; H–Round Hermetic Metal Can (Header); N–Plastic Molded Dual-In-Line; P–Plastic Leaded Chip Carrier (PLCC); Q–Cerdip; R–Small Outline Plastic (SOIC).
[2]Unity gain small signal bandwidth.
Boldface Type: Product recommended for new design.
*New product since the publication of the 1987/1988 Databooks.
†Consult factory for price.

ANALOG DEVICES

Operational Amplifiers

High Speed Amplifiers

Model	GBW MHz typ	SR V/μs typ	Settling Time ns to % typ	A_{CL} min V/V	V_{OS} mV typ	I_{OUT} mA min	Supply Current mA typ	Package Options[1]	Temp Range	Page	Comments
AD5539	**1400**	**600**	**12–1**	**5**	**2**	**20**	**14**	**N, Q**	**C, M**	**L2–183**	**Improved Replacement for SE/NE5539. Designed for Video/R_F Applications**
AD849	**750**	**300**	**65–0.1**	**25**	**0.5**		**5**	**N, Q, R**	**C, I, M**	**PL2–181**	**Stable Driving Cap. Loads High Speed, Low Power A_{VCL}>25**
AD846	**450**	**450**	**100–0.01**	**1**	**0.025**	**50**	**5**	**N, Q**	**I, M**	**PL2–165**	**High Precision, Current Feedback**
AD840	**400**	**400**	**100–0.01**	**10**	**0.2**	**50**	**10**	**N, Q**	**C, M**	**PL2–157**	**Wideband, Fast Settling, A_{VCL}>10**
AD9611	**280**	**1900**	**13–0.1**	**1**	**0.5**	**40**	**21**	**H**	**I, M**	**L2–207**	**Ultrafast Settling, Wide Bandwidth Current Feedback**
***AD9615**	**200**	**1400**	**13–0.1**	**1**	**0.25**	**45**	**69**	**H**	**I, M**	**SF–45**	**Ultrafast, Precision Current Feedback**
AD848	**175**	**300**	**80–0.1**	**5**	**0.5**		**5**	**N, Q, R**	**C, I, M**	**PL2–179**	**High Speed, Low Power, Stable Driving Capactive Loads A_{VCL}>5**
AD9610	**100**	**3500**	**18–0.1**	**1**	**0.3**	**50**	**21**	**H**	**I, M**	**L2–199**	**Fast Settling, Wide Bandwidth Current Feedback**
HOS-050	100	300	80–0.1	1	10–45	100	20	H	I, M	L2–245	Fast Settling Video Amp
HOS-060	100	300	80–0.1	1	0.5	100	20	H	M	L2–251	Low Offset, Fast Settling Video Amp
AD842	**80**	**375**	**100–0.01**	**2**	**0.5**	**100**	**12**	**H, N, Q**	**C, M**	**PL2–161**	**Fast Settling, High Output Current A_{VCL}>2**
ADLH0032	0	500	300–0.1	1	2–5	50	18	H	I, M	L2–215	Improved Second Source
***AD844**	**60**	**2000**	**100–0.1**	**1**	**0.2–0.5**	**60**	**6.5**	**N, Q**	**I, M**	**SF–45**	**High Slew Rate, Current Feedback**
AD847	**50**	**300**	**120–0.1**	**1**	**0.5**		**5**	**N, Q, R**	**C, I, M**	**PL2–177**	**High Speed, Low Power Unity Gain Stable Excellent Driving Cap. Loads**
AD841	**40**	**300**	**110–0.01**	**1**	**0.5**	**50**	**10**	**H, N, Q**	**C, M**	**PL2–159**	**Wideband, Unity Gain Stable Fast Settling**
AD380	**40**	**330**	**250–0.01**	**1**	**1**	**60**	**12**	**H**	**C, M**	**L2–15**	**Wideband, FET Input**
***AD843**	**35**	**250**	**130–0.01**	**1**	**0.5**	**50**	**12**	**N, Q**	**C, I, M**	**SF–45**	**Fast Settling, FET Input**
AD507	35	35	900–0.1	10	3	20	4	H	C, M	L2–27	
AD509	20	120	500–0.1	3	4–5		6	H	C, M	L2–31	
AD845	**16**	**100**	**300–0.01**	**1**	**0.1–0.7**	**50**	**10**	**N, Q**	**C, I, M**	**PL2–163**	**Exceptional Performance JFET Input, High Speed**
AD744	**13**	**75**	**500–0.01**	**1**	**0.25**	**10**	**3.5**	**H, N, Q**	**C, I, M**	**L2–137**	**Precision, Fast Settling Custom Compensation**
AD381	5	30	750–0.1	1	0.5	10	5	H	C, M	L2–21	Low Drift, FET Input
AD382	5	30	750–0.1	1	0.5	50	6	H	C, M	L2–21	Low Drift, FET Input

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Precision Amplifiers

Model	V_{OS} μV max	V_{OS} TC μV/°C max	Noise μV p-p 0.1–10Hz typ	BW MHz typ[2]	Slew Rate V/μs typ	I_B nA max	CMRR dB f=1kHz typ	Package Options[1]	Temp Range	Page	Comments
AD707	**15–90**	**0.1–1**	**0.23**	**0.9**	**0.3**	**1–2.5**	**100**	**H, N, Q, R**	**C, I, M**	**PL2-103**	**Highest dc Precision, Low Cost**
AD OP-07	**25–150**	**0.6–2.5**	**0.35**	**0.6**	**0.17**	**2–12**	**95**	**H, N, Q, R**	**C, M**	**L2-223**	**Improved Industry Standard**
AD OP-27	**25–100**	**0.6–1.8**	**0.08**	**8.0**	**2.8**	**40–80**	**123**	**H, N, Q**	**I, M**	**L2-229**	**Ultralow Noise**
AD OP-37	**25–100**	**0.6–1.8**	**0.08**	**63 (GBP)**	**17**	**40–80**	**123**	**H, N, Q**	**I, M**	**L2-237**	**Combination of Precision and Speed. $A_{VCL} \geq 5$**
AD517	50–150	1.3–3	2	0.25	0.10	0.25–2	94	H	C, M	L2-41	
AD821	**250–1000**	**3–10**		**1.3**	**3**	**0.02–0.03**		**N, Q, R**	**C, I, M**	**PL2-153**	**Single Supply, Low Power, FET Input**
AD548	**250–2000**	**2–20**	**2**	**1**	**1.8**	**0.003–0.005**	**83**	**H, N, Q, R**	**C, I, M**	**L2-55**	**Low Power BiFET**
AD547	250–1000	1–5	2	1	3	0.025–0.05	60	H	C, M	L2-47	Low Drift

Unity Gain Buffers

Model	−3dB BW MHz typ	SR V/μs min	I_{OUT} mA min	V_{OS} mV typ	I_{SS} mA max	Package Options[1]	Temp Range	Page	Comments
HOS-200	**200**	**1000**	**100**	**12**	**16**	**H**	**I, M**	**L2-257**	**Wideband, High Speed**
HOS-100	**125**	**1000**	**100**	**5–10**	**16–20**	**H**	**I, M**	**L2-255**	**Wideband, High Speed**
ADLH0033	**100**	**1000**	**100**	**5–12**	**20–21**	**H**	**I**	**L2-219**	**Improved Second Source**

[1]Package Options: H–Round Hermetic Metal Can (Header); N–Plastic Molded Dual-In-Line; Q–Cerdip; R–Small Outline Plastic (SOIC).
[2]Unity gain small signal bandwidth.
Boldface Type: Product recommended for new design.
*New product since the publication of the 1987/1988 Databooks.
†Consult factory for price.

ANALOG DEVICES

Operational Amplifiers

Dual Operational Amplifiers

Model	V_{OS} mV max	V_{OS} TC µV/°C max	I_B nA max	BW MHz typ[1]	Slew Rate V/µs typ	Settling Time to 0.01% µs typ	Package Options[2]	Temp Range	Page	Comments
AD708	**0.03–0.1**	**0.3–1.0**	**1–2.5**	**0.9**	**0.3**		**H, N, Q**	**C, I, M**	**PL2–105**	**Highest dc Precision. Excellent Matching Between Amps, Dual AD707**
AD712	**0.3–3**	**5–20**	**0 .05–0.075**	**4**	**20**	**1**	**H, N, Q, R**	**C, I, M**	**L2–119**	**Excellent ac and dc Performance Dual AD711**
AD746	**0 .25–1**	**3–20**	**0 .15**	**13**	**75**	**0.5**	**H, N, Q**	**C, I, M**	**PL2–149**	**Precision, Fast Settling, Dual AD744**
AD647	0.25–1	2.5–10	0.035–0.075	1	3		E, H	C, M	L2–87	Dual AD547
AD648	**0.3–2**	**3–20**	**0.01–0.02**	**1**	**1.8**	**8**	**H, N, Q**	**C, I, M**	**L2–93**	**Low Power, BiFET, Dual AD548**
AD642	0 .5–2		0.035–0.075	1	3		H	C, M	L2–75	Dual AD542
AD644	0.5–2		0.035–0.075	2	13		H	C, M	L2–81	Dual AD544

Quad Operational Amplifiers

Model	V_{OS} mV max	V_{OS} TC µV/°C max	I_B pA max	BW MHz typ[1]	Slew Rate V/µs typ	Settling Time to 0.01% µs typ	Package Options[2]	Temp Ranges	Page	Comments
AD713	**0 .5–1.5**	**20**	**75–150**	**4**	**20**	**1**	**N, Q**	**C, I, M**	**PL2–131**	**Superior ac and dc Performance, Quad AD711**

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Instrumentation Amplifiers

Model	Gain Ranges	Gain Error % max	Gain TC ppm/°C max	BW MHz typ[1]	Package Options[2]	Temp Range	Page	Comments
AD524	**1, 10, 100, 1000**	**0.02–2.0**	**5–100**	**1.0**	**D, E**	**I, M**	**L4–25**	**Pin Programmable, Input Protection**
AD526	**1, 2, 4, 8, 16**	**0.01–0.15**	**2–5**	**4.0**	**D, N**	**C, I, M**	**L4–37**	**Software Programmable, μP Interface**
AD624	**1, 100, 200, 500, 1000**	**0.02–1.0**	**5–25**	**1.0**	**D**	**I, M**	**L4–49**	**Pin Programmable**
AD625	**1–10,000**	**0.02–0.05**	**5**	**0.65**	**D, N**	**C, I, M**	**L4–61**	**Resistor Programmable, Low Cost**
AD365	1, 10, 100, 500	0.05–0.1	5–10	0.8	M	I	L4–7	Digitally Programmable with T/H
AD521	0.1–1000	(±0.25–0.004G)	±(3±0.05G)	>2	D	C, M	L4–15	Resistor Programmable
AD522	1–10,000	0.05–1.0	2–50	0.3	D	I, M	L4–21	Resistor Programmable

Isolation Amplifiers

Model	Peak Volt Iso V pk	Gain Range V/V	Gain Nonlin % max	Freq Resp kHz	Package Options[2]	Temp Range	Page	Comments
284J	2500	1–10	0.05	1	Module	C	L5–33	Medical, Single Channel, Low Cost
286J	2500	1–100	0.05-0.2	1	Module	C	L5–39	Medical, Multichannel, Low Cost
289	**2500**	**1–100**	**0.012–0.05**	**20**	Module	**C**	**L5–45**	**Precision, Wide Bandwidth, Synchronized**
290A	**1500**	**1–100**	**0.1–0.25**	**2.5**	Module	**I**	**L5–51**	**Single Channel, General Purpose**
292A	**1500**	**1–100**	**0.1–0.25**	**2.5**	Module	**I**	**L5–51**	**Multichannel, General Purpose**
AD202	**1000–2000**	**1–100**	**0.025–0.05**	**2**	**N, Y**	**C**	**L5–7**	**Lowest Cost, Small Size, Single Channel, −40°C TO +85°C**
AD204	**1000–2000**	**1–100**	**0.025-0.05**	**5**	**N, Y**	**C**	**L5–7**	**Lowest Cost, Small Size, Multichannel, −40°C to +85°C**
AD210	**3500**	**1–100**	**0.012–0.025**	**20**	**N**	**I, C**	**L5–19**	**Precision, 3-Port Isolation, Wide Bandwidth**
AD295	**2500**	**1–1000**	**0.012–0.05**	**4.5**	**Module**	**I**	**L5–27**	**−40°C to +100°C, Low Drift, 3-Port Isolation**
281					Module	C	L5–39	External Oscillator for 286J and 292A Isolation Amplifiers
AD246					N, Y	C	L5–7	External Oscillator for AD204 Isolation Amplifier

[1]Unity gain small signal bandwidth.
[2]Package Options: D–Side-Brazed Dual-In-Line Ceramic; E–Leadless Chip Carrier; H–Round Hermetic Metal Can (Header); M–Metal Hermetic Dual-In-Line; N–Plastic Molded Dual-In-Line; Q–Cerdip; Y–Single In-Line Package.
Boldface Type: Product recommended for new design.
*New product since the publication of the 1987/1988 Databooks.
†Consult factory for price.

ANALOG DEVICES

Multipliers/Dividers

Model	BW MHz typ[1]	Total Error % FS max	Accuracy vs Temp %/°C typ	Package Options[2]	Temp Range	Page	Comments
AD834	**500**	**2**	**TBD**	**Q, R**	**C, M**	**PL6–43**	**Very High Speed 4-Quad Mult/Div**
AD539	**60**	**1.5–2.5**	**1–2% (T_{min}–T_{max})**	**D, N**	**C, M**	**L6–31**	**High Speed 2-Channel, 2-Quad Mult/Div**
AD534	**1**	**0.25–1.0**	**0.0008–0.022**	**D, E, H**	**C, M**	**L6–13**	**High Accuracy 4 Quad Mult/Div**
AD632	**1**	**0.5–1.0**	**0.01–0.02**	**D, H**	**I, M**	**L6–39**	**High Accuracy Replacement for AD532**
AD532	1	1–2	0.01–0.04	D, H	C, M	L6–7	Accurate 4-Quad Mult/Div
AD538	**0.4**	**0.5–1.0**		**D**	**I, M**	**L6–23**	**Simultaneous Mult/Div/Exponentiator**
AD535	**0.02**	**0.5–5.0**	**0.01–0.05**	**D, H**	**C**	**N**	**Dedicated Divider**

RMS-to-DC Converters

Model	Conversion Accuracy mV ±%Read max	Full-Scale Range V rms	dB Output Error dB max	Package Options[2]	Temp Range	Page	Comments
AD737	**(0.2±0.3)–(0.4±0.5)**	**0.2**		**N, Q, R**	**C, I**	**PL8–29**	**Low Cost, Low Power, No Output Buffer**
AD736	**(0.3±0.3)–(0.5±0.5)**	**0.2**		**N, Q, R**	**C, I**	**PL8–25**	**General Purpose, Low Cost, Low Power**
AD636	**(0.2±0.3)–(0.5±0.6)**	**0.2**	**0.2–0.5**	**D, H**	**C**	**L8–11**	**Low Power**
AD637	**(0.5±0.2)–(1±0.5)**	**7**	**1 (typ)**	**D, Q**	**C, M**	**L8–17**	**High Accuracy, Wide Bandwidth**
AD536A	**(2±0.2)–(5±0.5)**	**7**	**0.3–0.6**	**D, E, H**	**C, M**	**L8–5**	**General Purpose**

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Log/Antilog Amplifiers

Model	Input Range	Log Conformity % RTI	BW kHz	Package Options[2]	Temp Range	Page	Comments
755	1nA–1mA	0.5	10	Module	I	L7–11	Complete, Current and Voltage, 6 Decade, High Accuracy
757	1nA–1mA	0.5	25	Module	I	L7–15	Complete, Log/Antilog Ratio, 6 Decade, High Accuracy
759	20nA–0.2mA	1.0	200	Module	I	L7–11	Complete, Current and Voltage, 4 Decade, Lowest Cost
AD9521	0.4V p-p	±1dB	10–250MHz	E, H	C, M	L7–7	Wideband Amplifier with Logarithmic Detected Output
*AD640	0.75mV–200mV		120MHz	D, E	I, M	SF–46	120MHz, 45dB, SDLA

Special Function Components

Model	Description	Package Options[2]	Temp Range	Page
AD345	High Speed Pin Driver with Inhibit Mode	Y	C	L9–5
AD630	Balanced Modulator/Demodulator	D, E, N	C, I, M	L9–9
AD639	Universal Trigonometric Function Converter	D	I	L9–17
AD890	Precision Wideband Channel Processing Element	P, Q	C	PL9–29
AD891	Rigid Disk Data Channel Qualifier	P, Q	C	PL9–35
*AD7341	Voiceband Transmission Filter for 14-Bit DAC	N, P	C	SF–47
*AD7371	Voiceband Receive Filter for 14-Bit ADC	N, P	C	SF–47
AD9500	Digitally Programmable Delay Generator	E, P, Q	I, M	L9–41
*AD9901	Digital Phase/Frequency Discriminator	E, Q	C, M	SF–46

[1]Small signal bandwidth.
[2]Package Options: D–Side-Brazed Dual-In-Line Ceramic; E–Leadless Chip Carrier; H–Round Hermetic Metal Can Header; N–Plastic Molded Dual-In-Line; P–Plastic Leaded Chip Carrier (PLCC); Q–Cerdip; R–Small Outline Plastic (SOIC); Y–Single In-Line Package.
Boldface Type: Product recommended for new design.
*New product since the publication of the 1987/1988 Databooks.
†Consult factory for price.

Signal Conditioning Components & Subsystems

Model	V/I Transmitters Loop Power	Local Power	Isolated	Sensor Excitation	Sensor Type(s)	IC	Hybrid Package	Module	Page
AD594/AD595					**TC**	**X**			**L11–5**
AD596/AD597					**TC**	**X**			**L11–13**
AD693	**X**	**X**		**X**	**mV: All**	**X**			**L11–19**
1B21	**X**		**X**					**X**	**L11–31**
1B22		**X**	**X**					**X**	**PL11–35**
1B31				**X**	**Strain Gage**		**X**		**L11–37**
1B32				**X**	**Strain Gage**		**X**		**L11–45**
1B41			**X**	**X**	**RTD**			**X**	**PL11–53**
1B51			**X**		**TC, mV**			**X**	**PL11–55**
2B20		X						X	L11–59
2B22		X	X					X	L11–63
2B23		X	X					X	L11–67
2B24	X		X					X	L11–87
2B30					Strain Gage, RTD			X	L11–71
2B31				X	Strain Gage, RTD			X	L11–71
2B50			X		TC, mV			X	L11–77
2B52	X		X		TC, mV			X	L11–87
2B53	X				TC, mV			X	L11–87
2B54/2B55			**X**		**mV, 4-Channel**			**X**	**L11–81**
2B57	**X**			**X**	**Solid State (AD590)**			**X**	**L11–87**
2B58				X	3-Wire RTD			X	L11–87
2B59	X			X	2-Wire RTD			X	L11–87
3B Series			**Modular Signal Conditioning Subsystem**						**L11-89**
4B Series			Alarm Limit Subsystem						L11-93
5B Series			**Modular Signal Conditioning Subsystem, Lowest Cost**						**L11-95**
***6B Series**			**Modular Digital Transmitters, Low Cost**						**SF-48**

Temperature Transducers

Model	I_{OUT} µA/K	Cal Error °C max	Nonlin °C max	Package Options[1]	Temp Range	Page	Comments
AC2626	1	0.5–5	0.3–1.5	3/16″ Stainless Steel Sheath	C, M	L10–5	General Purpose Temperature Probe 4″ and 6″ Length
AD590	1	0.5–5	0.3–1.5	F, H	M+	L10–7	Wide Temperature Range, Accurate
AD592	1	0.5–2.5	0.15–0.35	N	I+	L10–17	Low Cost, Accurate

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Digital Panel Meters

Model	Digits	F.S. Range	Data Output	Display Type	Page	Comments
AD2026-1	3	−99mV to +999mV	N/A	LED	L12–13	+5V Power
AD2010	3 1/2	±199.9mV	BCD	LED	L12–9	+5V Power
AD2021	3 1/2	±199.9mV, ±1.999V, ±19.99V	Serial	LED	L12–11	+5V Power
AD2026-2	3	−99mV to +999mV	N/A	LED	L12–13	Line Power

Digital Temperature/Transducer Meters

Model	Interface	Readout	Digital Data Output	Page	Comments
AD2050	Thermocouple	LED 3 1/2 Digits	7-Bit Character Serial ASCII	L12–15	Self-Calibrated, User Specified Thermocouple
AD2051	Thermocouple	LED 3 1/2 Digits	7-Bit Character Serial ASCII	L12–15	Self-Calibrated, Switch Selected Thermocouple
AD2060	RTD/Thermister	LED 3 1/2 Digits	7-Bit Character Serial ASCII	L12–17	Self-Calibrated, User Specified RTD/Thermister
AD2061	RTD/Thermister	LED 3 1/2 Digits	7-Bit Character Serial ASCII	L12–17	Self-Calibrated, Switch Selected RTD/Thermister
AD2070	Thermocouple	LED 4 1/2 Digits	7-Bit Character Serial ASCII	L12–19	Self-Calibrated, Autoranging Thermocouple
AD2071	Thermocouple	LED 4 1/2 Digits	7-Bit Character Serial ASCII	L12–19	Self-Calibrated, Autoranging Thermocouple

[1]Package Options: F–Flat Pack; H–Round Hermetic Metal Can (Header); N–Plastic Molded Dual-In-Line.
Boldface Type: Product recommended for new design.
*New product since the publication of the 1987/1988 Databooks.
†Consult factory for price.

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ANALOG DEVICES

Digital Signal Processing Components

Fixed Point Multipliers

Word Size	Model	Multiplication Time, ns[1] Clocked Comm	Clocked MIL	Unclocked Comm	Unclocked MIL	I_{DD}[2] Comm	I_{DD}[2] MIL	Data Formats Twos Comp	Unsign Mag	Mixed Mode	Pins	Package Options[3]	Logic Type	Page
8×8	ADSP-1080A	J=45 K=33	S=55 T=45	N/A	N/A	45	55	X			40	D, E, N[4]	TTL	D5–5
8×8	ADSP-1081A	J=45 K=33	S=55 T=45	N/A	N/A	45	55		X		40	D, E, N[4]	TTL	D5–11
12×12	ADSP-1012A	J=75 K=50	S=90 T=60	J=105 K=80	S=125 T=95	60	70	X	X	X	64 68	D, N E, G	TTL	D5–15
16×16	ADSP-1016A	J=85 K=70	S=95 T=80	J=105 K=90	S=120 T=105	45	55	X	X	X	64 68	D, N E, G	TTL	D5–21
24×24	**ADSP-1024A**	**J=120 K=95**	**S=150 T=120**	**N/A**	**N/A**	**70**	**90**	**X**			**84**	**G**	**TTL[5]**	**D5–61**

Multiplier/Accumulators

Word Size	Model	Multiplication Accumulate Time[1] Comm	Multiplication Accumulate Time[1] MIL	Accum Size	Accum	I_{DD}[2] Comm	I_{DD}[2] MIL	Pins	Package Options[3]	Page
8×8	ADSP-1008A	J=60 K=50	S=75 T=60	19	1	40	45	48	D, N	D5–27
12×12	ADSP-1009A	J=85 K=70	S=100 T=85	27	1	70	75	64 68	D, N E, G	D5–33
16×16	ADSP-1010A	J=85 K=75	S=100 T=90	35	1	80	100	64 68	D, N E, G	D5–39
16×16	**ADSP-1101**	**J=90 K=80**	**S=105 T=95**	**40**	**2**	**75**	**75**	**100**	**G**	**D5–83**
16×16	**ADSP-1110A**	**J=100 K=85**	**S=120 T=100**	**40**	**1**	**70**	**80**	**28**	**D, E, N, P**	**D5–69**

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Floating Point Components

Model	Grade	Number of Ports	Pipelined Throughput (ns) 32-Bit	Pipelined Throughput (ns) 64-Bit	Latency (ns) 32-Bit	Latency (ns) 64-Bit	IEEE Exact Divide (μs) 32-Bit	IEEE Exact Divide (μs) 64-Bit	IEEE Exact Square Root (μs) 32-Bit	IEEE Exact Square Root (μs) 64-Bit	Page
ADSP-3211 Multiplier	**L**	3	50	200	140	315					**D4–5**
	K	3	100	400	240	590					
	J	3	125	500	300	738					
	U	3	70	280	190	400					
	T	3	125	500	300	738					
	S	3	150	600	360	885					
ADSP-3210 Multiplier	**L**	2	60	240	190	370					**D4–5**
	K	2	100	400	290	590					
	J	2	125	500	363	738					
	U	2	75	300	238	463					
	T	2	125	500	363	738					
	S	2	150	600	435	885					
ADSP-3221 ALU	**K**	3	100	100	240	290	1.6	3	2.9	5.8	**D4–5**
	J	3	125	125	300	363	2	3.75	3.63	7.25	
	T	3	125	125	300	363	2	3.75	3.63	7.25	
	S	3	150	150	360	435	2.4	4.5	4.35	8.7	
ADSP-3220 ALU	**K**	3	100	100	240	290					**D4–5**
	J	3	125	125	300	363					
	T	3	125	125	300	363					
	S	3	150	150	360	435					
ADSP-3201 Single-Precision Multiplier	**K**	3	100	100	240						**D4–51**
	J	3	125	125	300						
	T	3	125	125	300						
	S	3	150	150	360						
ADSP-3202 Single-Precision ALU	**K**	3	100	100	240		1.6		2.9		**D4–51**
	J	3	125	125	300		2		3.63		
	T	3	125	125	300		2		3.63		
	S	3	150	150	360		2.4		4.35		
ADSP-3212	**K**	3	50	50	130	155	0.300	0.600			**PD4–85**
ADSP-3213 Multiplier/ Divider	**J**	3	60	60	157	187	0.360	0.720			**PD4-85**
***ADSP-3222**	**K**	3	50	50	130	155			1.45	2.90	**SF–49**
ADSP-3223 ALU	**J**	3	60	60	157	187			1.74	3.48	**PD4–85**
***ADSP-3264 Integrated ALU, Multiplier/ Divider & Register File**	**K**	2	64	64			0.384	0.768	1.86	3.70	**SF–50**
	J	2	80	80			0.480	0.960	2.32	4.64	

[1]ns max @ T_A = +70°C Commercial, T_A = +125°C Military.
[2]mA max, f_{CLK} = max, V_{DD} = +5V @ T_A = +70°C Commercial, +125°C Military.
[3]Package Options: D–Side-Brazed Dual-In-Line Ceramic; E–Leadless Chip Carrier; G–Pin Grid Array; N–Plastic Molded Dual-In-Line; P–Plastic Leaded Chip Carrier (PLCC).
[4]Contact factory.
[5]TTL levels of 0.8V and +2.2V.

Boldface Type: Product recommended for new design.
*New Product since the publication of the 1987/1988 Databooks.
†Consult factory for price.

ANALOG DEVICES

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Digital Signal Processing Components

Microcoded Support Components

ADSP-1410 ADDRESS GENERATOR

		Data Memory Address Size Single-Precision	Data Memory Address Size Double-Precision	Clock-to-Address Valid Delay[1]	Minimum Cycle Time	# of Address Registers	Total # of Registers	I_{DD}[2]	Package Options[1]	Logic Type	Page
Commercial	J	16 Bits / 64K Words	30 Bits / 1 Gigaword	35ns	100ns	16	30	75mA	D, N, P	TTL	D3–25
	K	16 Bits / 64K Words	30 Bits / 1 Gigaword	30ns	90ns	16	30	75mA	D, N, P	TTL	D3–25
Military	S	16 Bit / 64K Words	30 Bits / 1 Gigaword	45ns	125ns	16	30	100mA	D	TTL	D3–25
	T	16 Bits / 64K Words	30 Bits / 1 Gigaword	35ns	100ns	16	30	100mA	D	TTL	D3–25

ADSP-1401 PROGRAM SEQUENCER

		Program Address Size	Clock-to-Address Valid Delay[2]	Minimum Cycle Time	Stack Depth	Number of Interrupts	I_{DD}[3]	Package Options[1]	Logic Type	Page
Commercial	J	16 Bits / 64K Words	35ns	90ns	64 Words	10	75mA	D, N, P	TTL	D3–5
	K	16 Bits / 64K Words	25 ns	70ns	64 Words	10	75mA	D, N, P	TTL	D3–5
Military	S	16 Bits / 64K Words	45ns	110ns	64 Words	10	100mA	D	TTL	D3–5
	T	16 Bits / 64K Words	35 ns	90ns	64 Words	10	100mA	D	TTL	D3–5

*ADSP-1402 PROGRAM SEQUENCER

		Program Address Size	Clock-to-Address Valid Delay	Minimum Cycle Time	Stack Depth	Number of Interrupts	Event Counters	Package Options	Logic Type	Page
Commercial	J	16 Bits / 64K Words	15ns	65ns	64 Words	10	4	G	TTL	SF–51
	K	16 Bits / 64K Words	12ns	50ns	64 Words	10	4	G	TTL	SF–51

*ADSP-3128A REGISTER FILE

Model	Word Size Bits	Cycle Rate ns	# of 16 Bit Ports	Bandwidth Bits/μs	# of Transfers Cycles	Bidirectional Port	Technology	Package Options	Comments	Page
*ADSP-3128A	128 × 16 or 64 × 32	50	5	3,200	6	1	CMOS	G	Cascadable	SF–52

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ADSP-2100/ADSP-2100A

Model	Cycle Time (ns)	Speeds (MHz)	Temperature Ranges	Package Options[1]	Page
ADSP-2100	166	6.144	0 to +70°C	F, G	D2–15
	125	8.192	−55°C to +125°C		
***ADSP-2100A**	**100**	**10.24**	**0 to +70°C**	**F, G**	**SF–53**
	80	**12.50**	**−55°C to +125°C**		

The ADSP-2101/2, a microcomputer version of the ADSP-2100A, was recently announced. Consult your local sales office for further information.

ADSP-2100/ADSP-2100A DEVELOPMENT TOOLS

Model	Description
ADDS-2110	Cross-Software and Simulator (VAX/VMS)
ADDS-2121	Cross-Software (IBM PC/DOS)
ADDS-2122	Simulator (IBM PC/DOS)
ADDS-2123-C	Cross-Software and Simulator (Sun 2/3/Unix BSD 4.2)
ADDS-2130	C Compiler, Cross-Software and Simulator (VAX/VMS)
ADDS-2131	C Compiler, Cross-Software and Simulator (IBM PC/DOS)
ADDS-2133-C	C Compiler, Cross-Software and Simulator (Sun 2/3/Unix BSD 4.2)
ADDS-2150A	ADSP-2100A In-Circuit Emulator (110V)
ADDS-2150AE	ADSP-2100A In-Circuit Emulator (220V)
ADDS-2151A	ADSP-2100A In-Circuit Emulator (110V) with Trace Board
ADDS-2151AE	ADSP-2100A In-Circuit Emulator (220V) and Trace Board
ADDS-2157	Upgrade from ADDS-2150 In-Circuit Emulator to ADDS-2150A In-Circuit Emulator (either 110V or 220V)
ADDS-2161	Trace Board Upgrade to ADDS-2150 or ADDS-2150E
ADDS-2160	ADSP-2100A Evaluation Board
ADDS-2190	Three Day ADSP-2100 Workshop
ADDS-2169	University Package (ADDS-2131 and ADDS-2160)

[1]Package Options: D–Side-Brazed Dual-In-Line Ceramic; G–Pin Grid Array; N–Plastic Molded Dual-In-Line; P–Plastic Leaded Chip Carrier (PLCC).
[2]Maximum at +70°C for Commercial, +125°C for Military.
[3]mA maximum, f_{CLK} = max, over full V_{DD} range, at +70°C for Commercial, +125°C for Military.
Boldface Type: Product recommended for new design.
*New product since the publication of the 1987 1988 Databooks.
†Consult factory for price.

ANALOG DEVICES

ANALOG DEVICES

Data Acquisition Subsystems

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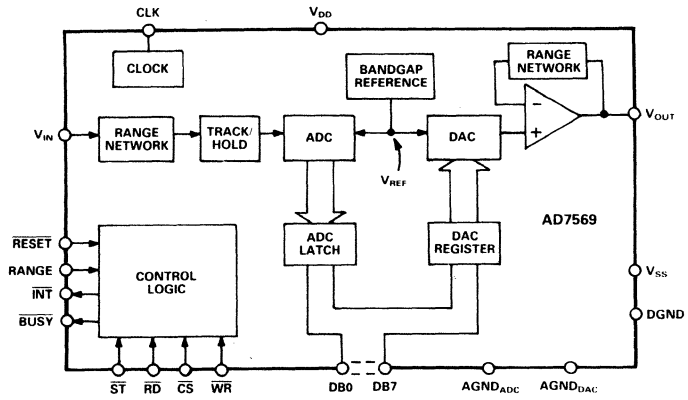
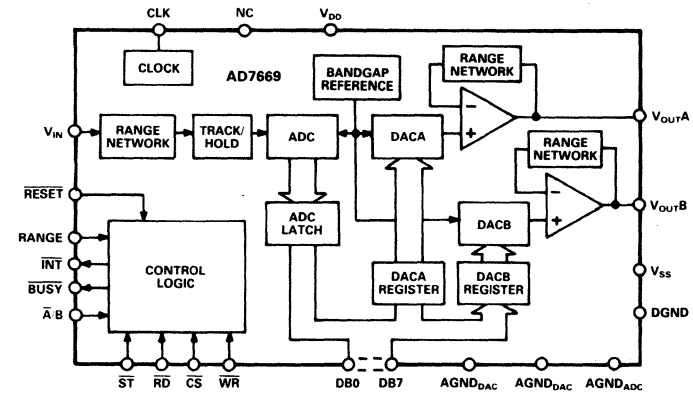
LC²MOS Complete, 8-Bit Analog I/O System





AD7569/AD7669

2μs ADC with Track/Hold
1μs DAC with Output Amplifier
AD7569, Single DAC Output
AD7669, Dual DAC Output
On-Chip Bandgap Reference
Fast Bus Interface
Single or Dual 5V Supplies
Additional Information:

Model	Page
AD7569	PC3-195
AD7669	SF-43

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Complete 16-Channel 12-Bit Data Acquisition Systems

AD362/AD363/AD364

AD362

16-Channel Data Acquisition Input Stage with:

- **Digitally Controlled Channel Selection/Mode Control**
- **16 Single-Ended or 8 Differential Channels**
- **High Common-Mode Rejection**
- **10μs Acquisition Time to 12-Bit Accuracy (0.01%)**

AD363

16-Channel Data Acquisition Input Stage with:

- **Digitally Controlled Channel Selection/Mode Control**
- **16 Single-Ended or 8 Differential Channels**
- **25kHz Throughput Rate**
- **Guaranteed No Missing Codes Over Temperature**

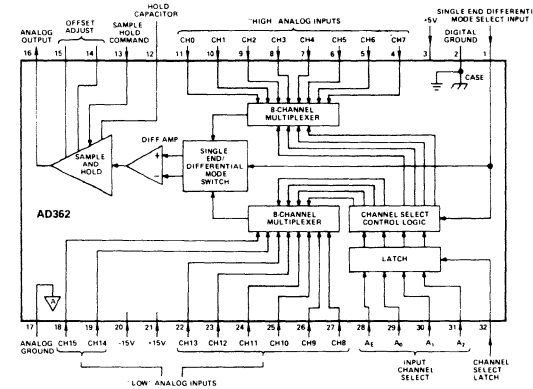
AD364

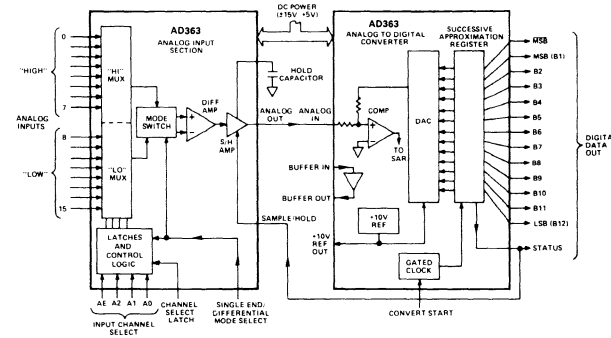
16-Channel Data Acquisition Input Stage with:

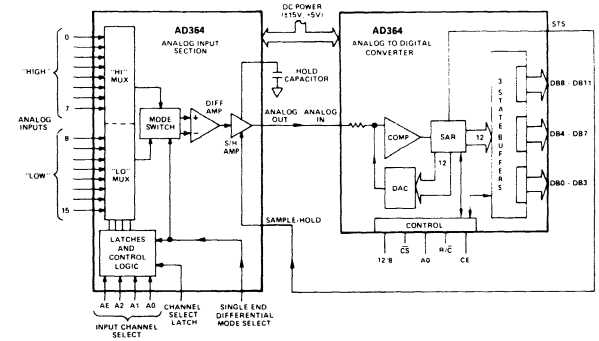
- **Digitally Controlled Channel Selection/Mode Control**
- **16 Single-Ended or 8 Differential Channels**
- **20kHz Throughput Rate**
- **Guaranteed No Missing Codes Over Temperature**
- **Three-State Buffered Digital Output**

Additional Information:

Model	Page
AD362	C9-5
AD363	C9-5
AD364	C9-5



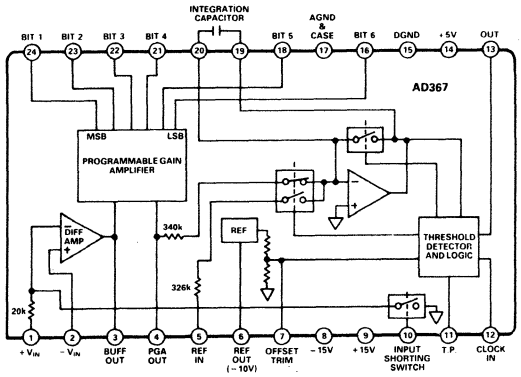




ANALOG DEVICES

Data Acquisition Subsystems

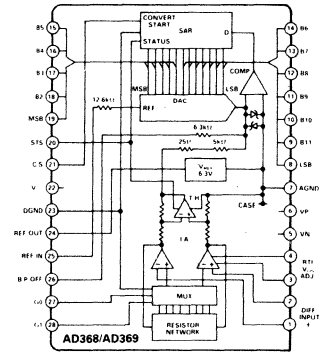
High Resolution Programmable Gain DAS



AD367

- Differential Input – Programmable Gain Amplifier
- 6-Bit (1 or 64) Gain Control
- Internal – 10V Reference
- 15-Bit Integral Nonlinearity
- ±305μV Resolution
- 10ms Conversion Time
- External Integration Capacitor Programmable Conversion Time
- Additional Information:
  - Page
  - C9-17

Complete 12-Bit A/D Converter with Programmable Gain

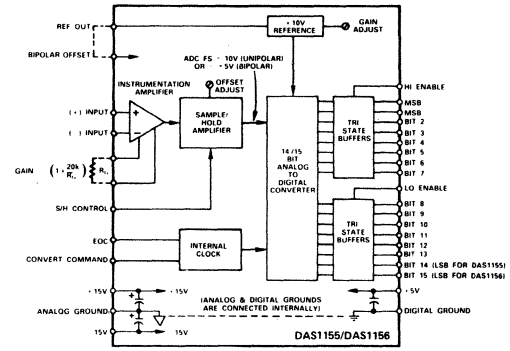


AD368/AD369

- Low Cost Data Acquisition Systems Including:
  - Programmable Gain Instrumentation Amplifier
  - Track-and-Hold Amplifier
  - 12-Bit A/D Converter
- Digitally Controlled Gains:
  - AD368 Gains = 1, 8, 64, 512
  - AD369 Gains = 1, 10, 100, 500
- 50kHz Throughput Rate
- Small Size: 28-Pin Hermetic Double DIP
- Guaranteed No Missing Codes Over Specified Temperature
- True 12-Bit Linear; Error ≤1/2LSB (B Grade)
- Unipolar or Bipolar Operation
- Additional Information:

Model	Page
AD368	C3-13
AD369	C3-13

Complete Low Level 14-Bit & 15-Bit Data Programmable Gain DAS



DAS1155/DAS1156

- 14-Bit & 15-Bit Low Level Data Acquisition System
- Functionally Complete:
  - Includes Instrumentation Amplifier, Sample/ Hold Amplifier and Analog-to-Digital Converter
- Differential Nonlinearity:
  - ±0.002% FSR Maximum (DAS1156)
- Guaranteed Nonlinearity:
  - ±0.005% FSR (DAS1155)
  - ±0.003% FSR (DAS1156)
- High Common-Mode Rejection:
  - 80dB (up to 500Hz)
- High Feedthrough Rejection: 96dB
- Resistor Programmable Gain: 1V/V to 1000V/V
- 25kHz Throughput Rate (DAS1155)
- Internal Gain and Offset Potentiometers
- Additional Information:

Model	Page
DAS1155	N
DAS1156	N

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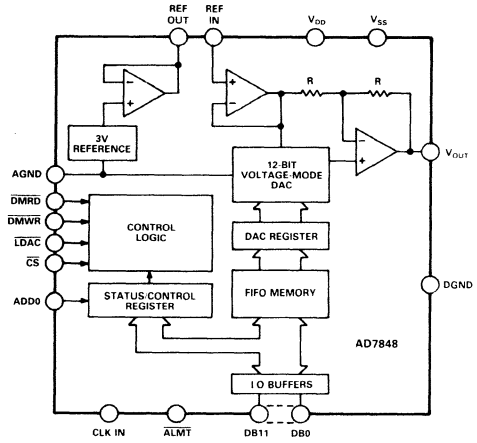
LC²MOS Complete 12-Bit DAC with DSP Interface

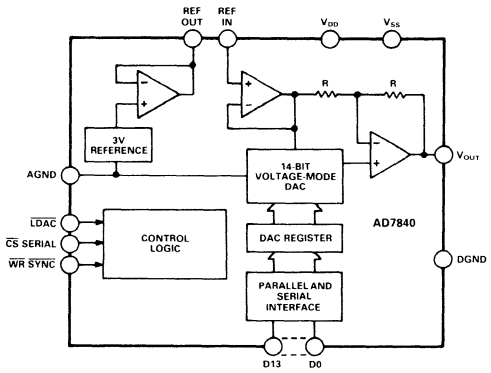


AD7848

Complete DAC with DSP Interface, Comprising:
- **12-Bit Voltage-Mode DAC**
- **3V Zener Reference**
- **Output Buffer Amplifier with 4μs Settling Time**
- **8-Word FIFO and Interface Logic**

70dB SNR at 10kHz Output Frequency
Interfaces to High Speed DSP Processors e.g., ADSP-2100, TMS32010, TMS32020
46ns Minimum $\overline{WR}$ Pulse Width
Low Power 75mW Maximum

LC²MOS Complete 14-Bit DAC

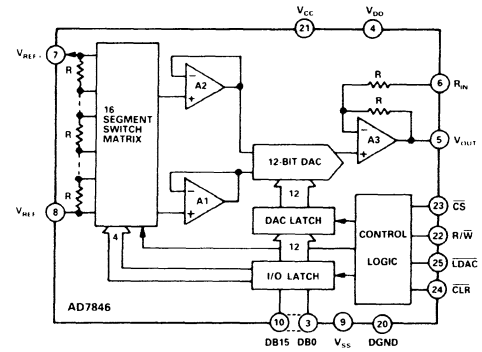


AD7840

Complete 14-Bit DAC Comprising:
- **14-Bit Voltage-Mode DAC**
- **3V Zener Reference**
- **Output Buffer Amplifier with 4μs Settling Time**
- **Parallel and Serial Interface Capability**

84dB SNR at 10kHz Output Frequency
Interfaces to High Speed DSP Processors e.g., ADSP-2100, TMS32010, TMS32020
40ns Minimum $\overline{WR}$ Pulse Width
Low Power 75mW Maximum

LC²MOS 16-Bit Voltage Output DAC



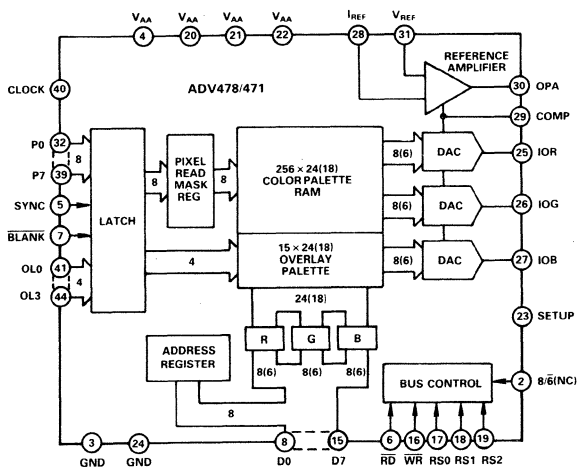
AD7846

16-Bit Monotonicity Over Temperature
±2 LSBs Integral Linearity Error
Microprocessor Compatible with Readback Capability
Unipolar or Bipolar Output
Multiplying Capability
Low Power 100mW Typical

ANALOG DEVICES

New Products

CMOS 80MHz Monolithic 256 × 24(18) Color Palette RAM-DAC

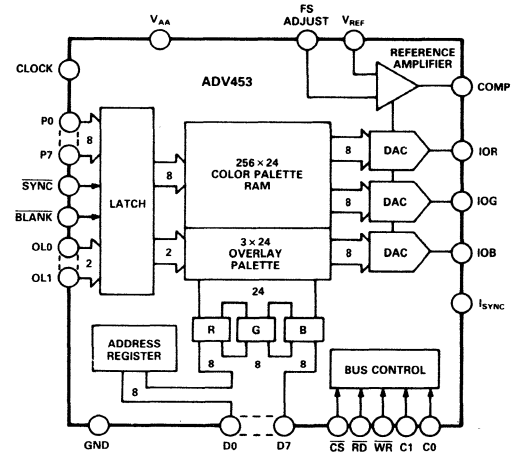


NOTES
1. NUMBERS IN PARENTHESIS INDICATE PIN NAMES FOR THE ADV471.
2. NC = NO CONNECT

ADV478/ADV471

Personal System/2* Compatible
80MHz Pipelined Operation
Triple 8-Bit (6-Bit) D/A Converters
256 × 24(18) Color Palette RAM
15 × 24(18) Overlay Registers
RS-343A/RS-170 Compatible Outputs
Sync on All Three Channels
Programmable Pedestal (0 or 7.5 IRE)
External Voltage or Current Reference
Standard MPU Interface
+5V CMOS Monolithic Construction
44-Pin PLCC Package
Power Dissipation: 800mW

CMOS 66MHz Monolithic 256 × 24 Color Palette RAM-DAC



ADV453

66MHz Pipelined Operation
Triple 8-Bit D/A Converters
256 × 24 Color Palette RAM
3 × 24 Overlay Registers
RS-343A/RS-170 Compatible Outputs
+5V CMOS Monolithic Construction
40-Pin DIP or Small 44-Pin PLCC Package
Power Dissipation: 1000mW

*Personal System/2 is a trademark of International Business Machines Corp.

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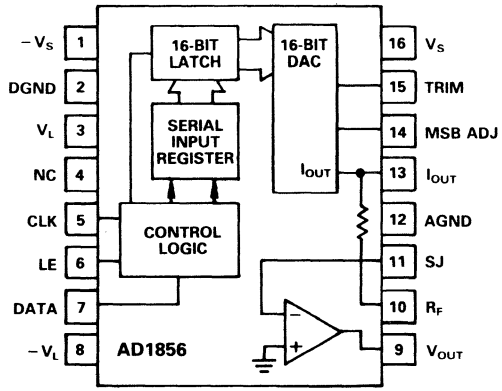
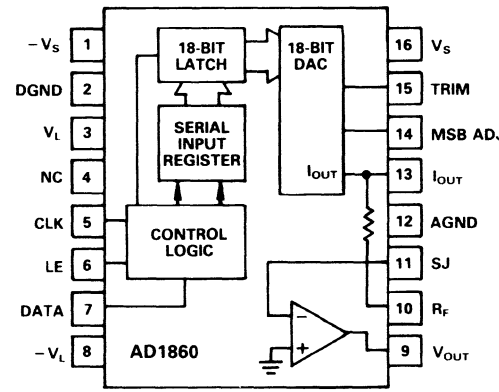
16-Bit PCM Audio DAC



AD1856

0.0025% THD
Fast Settling Permits 2×, 4× or 8× Oversampling
±3V Output
Optional Trim Allows Superlinear Performance
±5V to ±12V Operation
16-Pin Plastic DIP Package
Serial Input
Industry Standard Pinout

18-Bit PCM Audio DAC



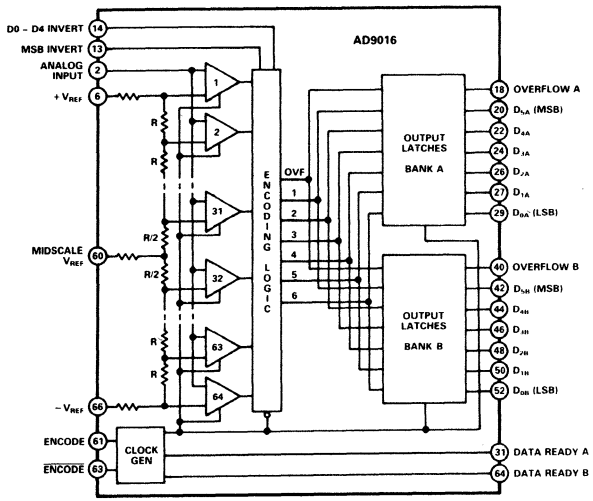
AD1860

0.001% THD
Fast Settling Permits 2×, 4× or 8× Oversampling
±3V Output Swing
Optional Trim Allows Superlinear Performance
±5V to ±12V Operation
16-Pin Plastic DIP Package
Serial Input
Industry Standard Pinout

ANALOG DEVICES

New Products

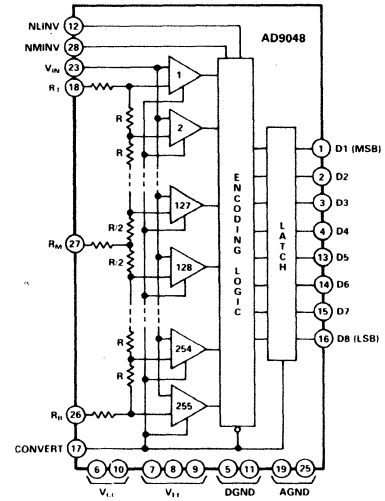
High Speed, 6-Bit A/D Converter



AD9006/AD9016

470MSPS Encode Rate
Very Low Input Capacitance – 8.5pF
30dB SNR @ 200MHz Analog Input
MIL-STD-883 Available
Bipolar Input Range (±1V)
Demultiplexed Outputs (AD9016)

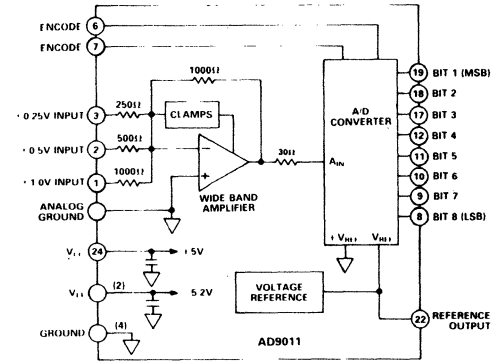
Monolithic 8-Bit Video A/D Converter



AD9048

35MSPS Encode Rate
16pF Input Capacitance
350mW Power Dissipation
Industry Standard Pinouts

8-Bit, 100MSPS A/D Converter



AD9011

On-Board Amplifier and Reference
100MSPS Encode Rate
Internal Input Clamping Circuit
Multiple Gain Selection
Bipolar Inputs

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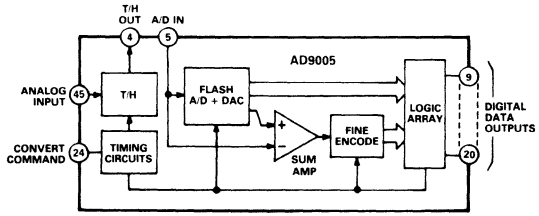
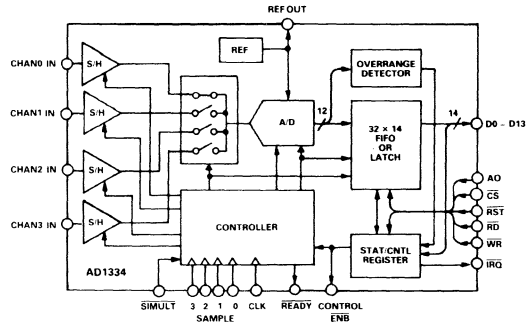
12-Bit, 10MHz A/D Converter



AD9005

Complete 12-Bit A/D Converter
Includes Track and Hold, Reference and Timing Circuitry
Bipolar Inputs
Up to 10MHz Sampling Rate
Low Power Dissipation – 3.4W
Low Harmonic Distortion

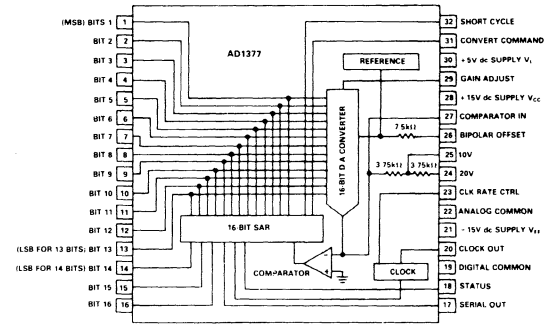
Four Channel 12-Bit Sampling A/D Converter for Digital Signal Processing



AD1334

Four-Channel A/D System for DSP Includes:
Simultaneous or Independent Channel Sampling Capability
12-Bit Accurate A/D Converter
32-Word Deep FIFO Memory
Fully Asynchronous High Speed, Digital Interface
Single-Channel Sample Rate up to 65kHz
Four-Channel Simultaneous Sample Throughput up to 28kHz
Entire System is Dynamically Characterized
Minimal Aperture Delay Time Mismatch from Channel-to-Channel & Device-to-Device
15ns Data Access Time Allows "No Wait State"
Interface to: ADSP-2100 (A), TMS320C25 DSP56000, NECμPD77230
Low Power – 250mW/Channel Maximum

Complete High Speed 16-Bit A/D Converter



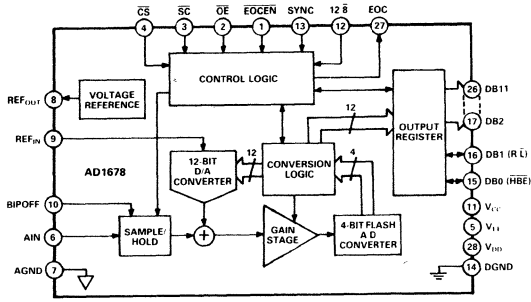
AD1377

Complete 16-Bit Converter with Reference and Clock
Fast Conversion Time – 10μs (16 Bits)
No Missing Codes to 14 Bits (0 to +70°C)
±0.003% Maximum Nonlinearity
Short Cycle Capability
Parallel and Serial Outputs
Industry Standard Pinout

ANALOG DEVICES

New Products

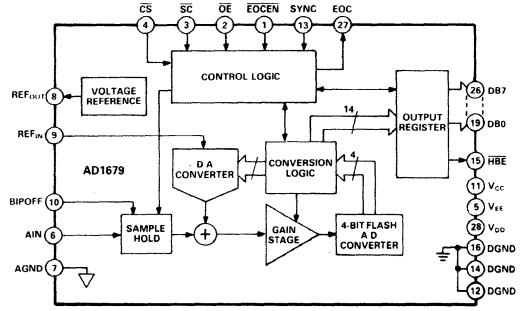
12-Bit 200 KSPS Sampling ADC



AD1678

AC Characterized
500kHz Full Power Bandwidth
72dB S/N + D (K Grade)
On-Board Reference and Clock
8-Bit and 16-Bit Bus Interface
10V Unipolar or Bipolar Input Range

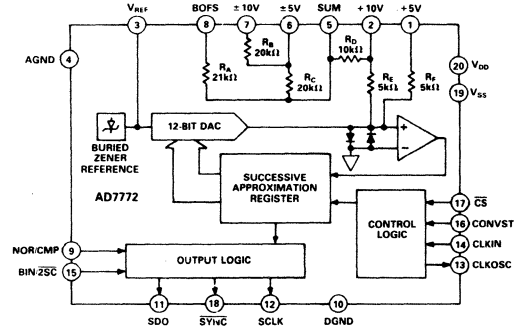
14-Bit 100 KSPS Sampling ADC



AD1679

AC Characterized
500kHz Full Power Bandwidth
80dB S/N + D (K Grade)
On-Board Reference and Clock
8-Bit and 16-Bit Bus Interface
10V Unipolar or Bipolar Input Range

LC²MOS Serial Output 12-Bit ADC



AD7772

12-Bit Resolution and Accuracy
Fast Conversion Time: 10µs
Serial Output
Complete with On-Chip Reference
Low Power
Unipolar or Bipolar Input Ranges
Small 0.3", 20-Pin DIPs and 20-Terminal Surface Mount Package

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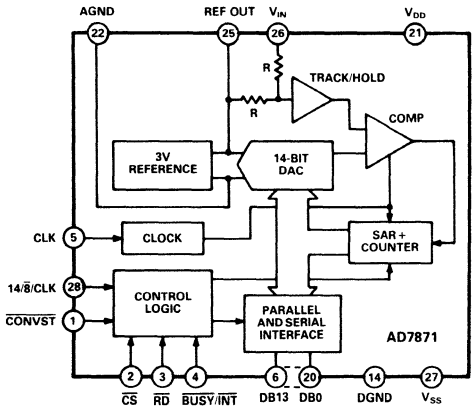
LC²MOS Complete, 14-Bit, 100kHz Sampling ADC

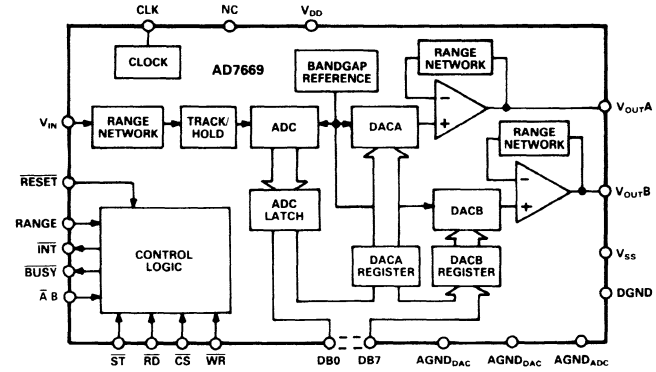


AD7871

Complete Monolithic 14-Bit ADC with:
- **2μs Track/Hold Amplifier**
- **8μs A/D Converter**
- **On-Chip Reference**
- **Laser Trimmed Clock**
- **Parallel, Byte and Serial Digital Interface**

82dB SNR at 10kHz Input Frequency
60ns Data Access Time
Low Power – 60mW Typical

ADC LC²MOS Complete, 8-Bit Analog I/O System



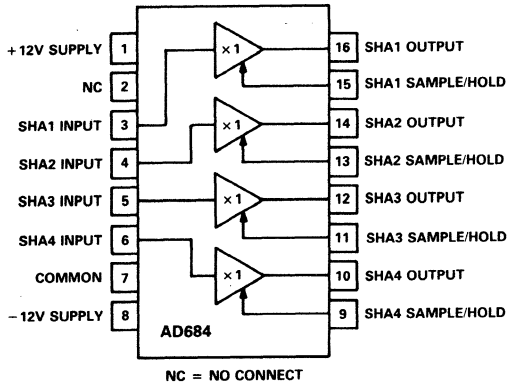
AD7669

2μs ADC with Track/Hold
Dual 1μs DAC with Output Amplifiers
On-Chip Bandgap Reference
Fast Bus Interface
Single or Dual 5V Supplies

ANALOG DEVICES

New Products

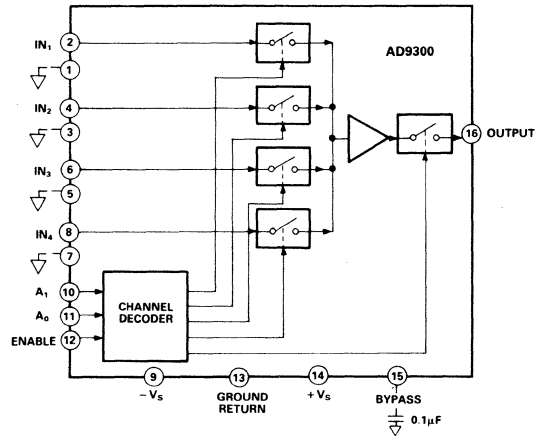
4-Channel Sample-and-Hold Amplifier



AD684

Four Independent Sample-and-Hold Amplifiers
Monolithic with Internal Hold Capacitors
Fast Acquisition Time: 800ns to 0.01%
Low Droop Rate: 0.001μV/μs
Aperture Jitter: 100ps
Low Power Dissipation: 360mW
0.3″ Skinny DIP Package

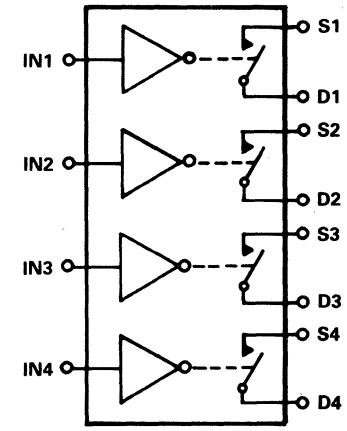
4 × 1 Wideband Video Multiplexer



AD9300

34MHz Full Power Bandwidth
±0.1dB Gain Flatness to 8MHz
75dB Crosstalk Rejection @ 10MHz
0.05°/0.05% Differential Phase/Gain
Cascadable for Switch Matrices

LC²MOS High Speed Quad SPST Switch



ADG201HS

50ns Maximum Switching Time Over Full Temperature Range
Low R_{ON} (30Ω Typical)
Single Supply Specifications for +10.8V to +16.5V Operation
Extended Plastic Temperature Range (–40°C to +85°C)
Break-Before-Make Switching
Low Leakage (100pA Typical)
44V Supply Maximum Rating
ADG201HS (K, B, T) Replaces HI-201HS
ADG201HS (J, A, S) Replaces DG271

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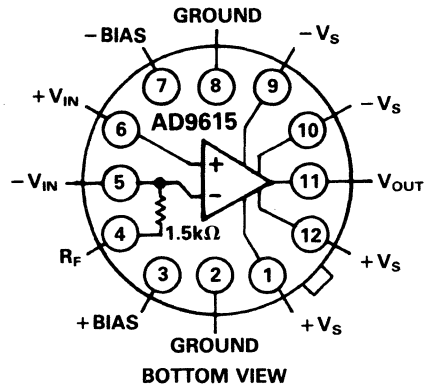
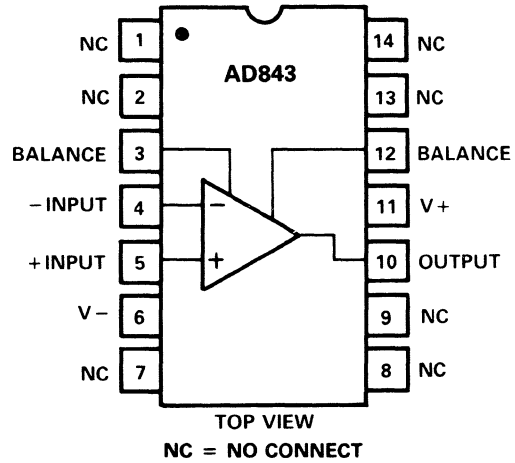
Ultrafast, Precision Operational Amplifier



AD9615

Low Distortion
Small Signal Bandwidth 200MHz
Full Power Bandwidth 190MHz
Settling: 13ns to 0.1%
Offset Voltage ±0.25mV; 3μV/°C
Bias Current ±500nA; 20nA/°C
Power Dissipation Independent of Load

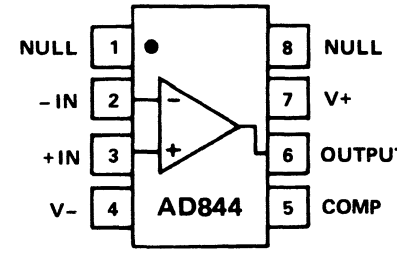
35MHz, CBFET Fast Settling Op Amp



AD843

AC PERFORMANCE:
Unity-Gain Bandwidth: 35MHz
Fast Settling: 130ns to 0.01%
Slew Rate: 300V/μs
Unity-Gain Stable
Full Power Bandwidth: 4.8MHz
DC PERFORMANCE:
Input Offset Voltage: 1mV Maximum
Input Bias Current: 120pA Typical
Input Voltage Noise: 13nV/$\sqrt{Hz}$
Open-Loop Gain: 50V/mV into a 500Ω Load
Output Current: 50mA Minimum
Supply Current: 12mA Maximum

2000V/μs Slew Rate Operational Amplifier



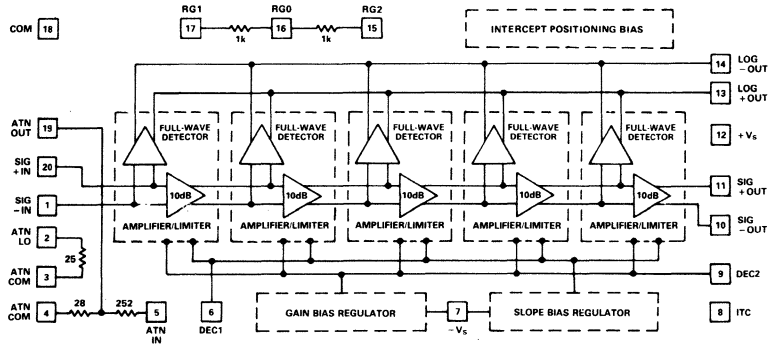
AD844

AC PERFORMANCE:
Fast Settling: 100ns to 0.1% (10V Step)
Small Signal Bandwidth: 60MHz (Gain = –1)
40MHz (Gain = –10)
Slew Rate: 2000V/μs
Full Power Bandwidth: 20MHz (V_O = 20V p-p)
Constant Rise Time over Input Amplitude
DC PERFORMANCE:
Input Offset Voltage: 200μV Maximum
Input Offset Drift: 2μV/°C
Input Voltage Noise: 2nV/$\sqrt{Hz}$ (100Hz – 10MHz)
Open Loop Transresistance: 2.8MΩ
Output Current: 50mA Minimum into 50Ω
Quiescent Supply Current: 6.5mA

ANALOG DEVICES

New Products

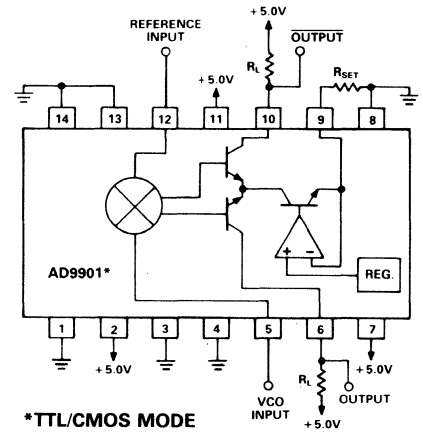
DC-Coupled Demodulating Logarithmic Amplifier



AD640

Complete, Fully Calibrated Monolithic System
Five 10dB Stages, DC-120MHz Bandwidth
Stable Logarithmic Intercept and Slope vs. Temperature and Supply Variations
Very Low Input Offset Voltage (25μV Typical)
Dual-Polarity Current Outputs of 1mA/Decade
Voltage Slope Options Using On-Chip Application Resistors
Low Power Operation (Typically 220mW @ ±5V)

75MHz Phase/Frequency Discriminator



*TTL/CMOS MODE

AD9901

DC-75MHz Input Range
ECL/TTL/CMOS Compatible
Linear Transfer Function
No "DEAD ZONE"

APPLICATIONS
Low Phase Noise Reference Loops
Fast Tuning "Agile" IF Loops
Secure "Hopping" Communications
Coherent Radar Transmit/Receive Chains

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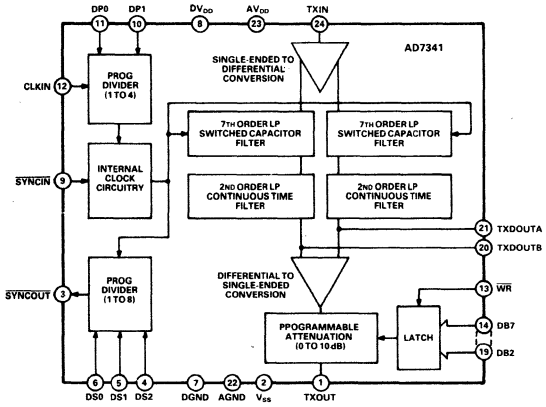
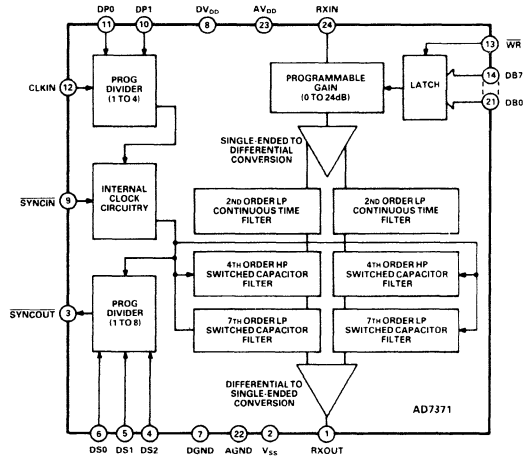
LC²MOS Modem Transmit & Receive Filter Set

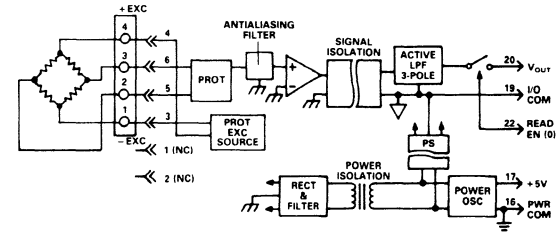




AD7341/AD7371

AD7341 – Transmit (Reconstruction) Filter for 14-Bit DAC (AD7840)
– Programmable Attenuation Range (0dB to −38dB)
AD7371 – Receive Filter for 14-Bit ADC (AD7371)
– Programmable Gain Range (0dB to 24dB)
70dB Stopband Attenuation
75dB In-Band Signal-to-Noise Ratio
−75dB Total Harmonic Distortion
CCITT V.32 & V.33 Compatible
Small, 0.3", 24-Pin Plastic Package & 28-Pin PLCC Package

5B38 Strain Gage Input Module



5B38

Accommodates Full and Half Bridges
Internal Half Bridge Completion
+10.0V and 3.333V Excitation
Bridge Resistances from 100Ω to 10kΩ
10kHz Bandwidth for Dynamic Signals

5B FAMILY FEATURES
Transformer Based Isolation: 1500V rms Common Mode
Small Size: 2.25" × 2.25" × 0.60"
No Potentiometer Adjustments
±0.05% Accuracy Typical
Custom Ranging Available
Mix and Match Capability

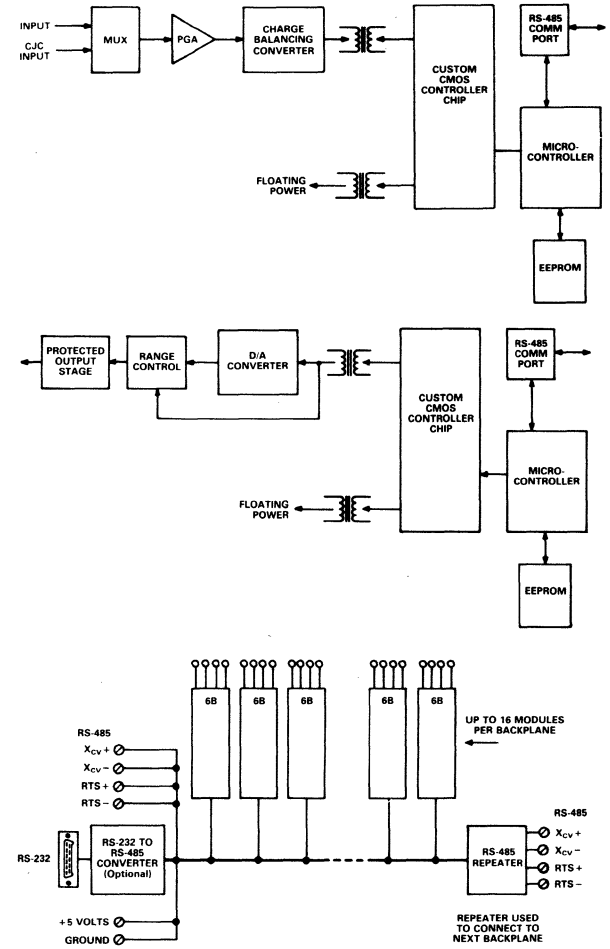
ANALOG DEVICES

ANALOG DEVICES

Smart Digitizing Signal Conditioners

6B SERIES

Sensor-to-Computer Conditioning and Digitizing, Complete Data Acquisition System in Each Module
Inputs: Thermocouples, RTDs, Millivolt, Volt, Process Current
Output: RS-485
Backplane Option of RS-232 or RS-485 Interface to Host
Field Configuration via Software
Autocalibrating, High Performance Integrating Converter
Linearized Outputs in Engineering Units
On-Board Microcontroller Converts Digitized Data to Standard Units
Input to Output Isolation: 1500V rms
Designed to Meet IEEE Standard for Transient Voltage Protection (IEEE-STD 472)
Mix and Match Module Capability
Small Package: 2.3″ × 3.1″ × 0.75″
Modules Plug into Backplane for High Channel Density



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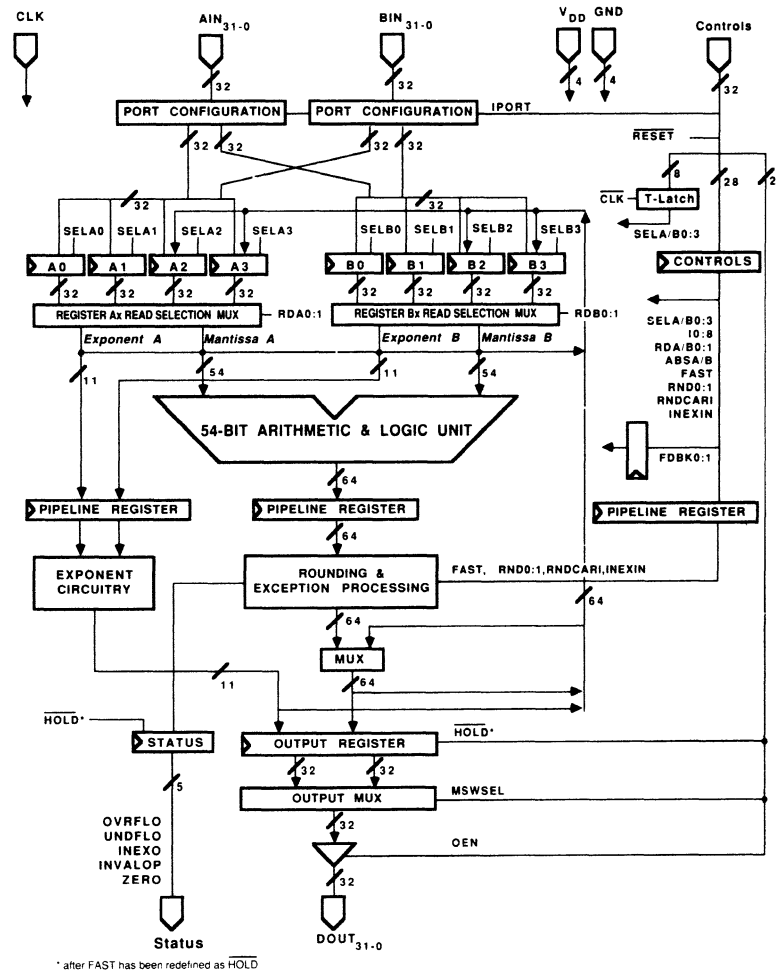
64-Bit IEEE Floating Point ALU

ADSP-3222

Complete 20 MFLOPS Floating Point ALU
Fully Compatible with IEEE Standard 754
Arithmetic Operations on Four Data Formats:
32-Bit Single-Precision Floating Point
64-Bit Double-Precision Floating Point
32-Bit Twos-Complement Fixed Point
32-Bit Unsigned-Magnitude Fixed Point
Only One Internal Pipeline Stage
20 MFLOPS Pipelined Throughput for Standard ALU Operations
Low Latency for Scalar Operations
130ns for 32-Bit Standard ALU Operations
155ns for 64-Bit Standard ALU Operations
Exact Square Root Instruction
1W Maximum Power Dissipation with 1.0μm CMOS Technology
144-Lead Pin Grid Array
Available Specified to MIL-STD-883, Class B
Pin-Compatible Upgrade from ADSP-3221

APPLICATIONS
High Performance Digital Signal Processing
Engineering Workstations
Floating Point Accelerators
Array Processors
Mini-Supercomputers
RISC Processors



* after FAST has been redefined as $\overline{\text{HOLD}}$

ANALOG DEVICES

New Products

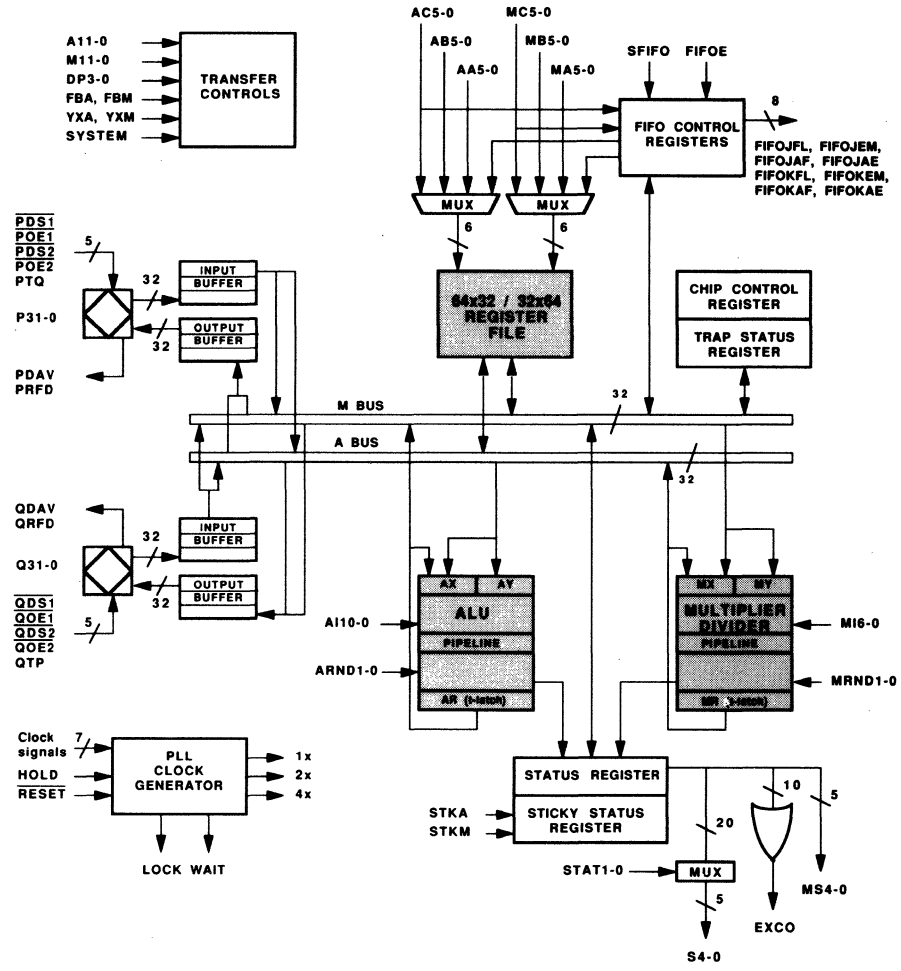
64-Bit Floating Point Arithmetic Unit (FPAU)

ADSP-3264

Floating Point ALU, Floating Point Multiplier/Divider and 64×32/32×64 Register File All On One Chip
Fully Compatible with IEEE Standard 754
31.2 MFLOPS Single- and Double-Precision Pipelined Throughput for Multiplication and Standard ALU Operations
Arithmetic Operations on Four Data Formats
- **32-Bit Single-Precision Floating Point**
- **64-Bit Double-Precision Floating Point**
- **32-Bit Twos-Complement Fixed Point**
- **32-Bit Unsigned Magnitude Fixed Point**

Exact Division: 360ns Single Precision and 720ns Double Precision
Exact Square Root Instruction
Left and Right Shifts
Buffered I/O Ports: One 64-Bit Port or Two 32-Bit Ports
I/O Ports Synchronous or Asynchronous with Optional Data-Driven Operation
Flexible, High Bandwidth Internal Data Transfers on Four-Way Time-Multiplexed Buses
Hardware Support for Arithmetic and I/O Exceptions; Requires No External Circuitry When Used with ADSP-1402 Program Sequencer
280-Lead Pin Grid Array (199 Signal Pins)
4 Watts Maximum

APPLICATIONS
High Performance Digital Signal Processing
Engineering Workstations
Floating Point Accelerators
Array Processors
Mini-Supercomputers
Graphics Processors



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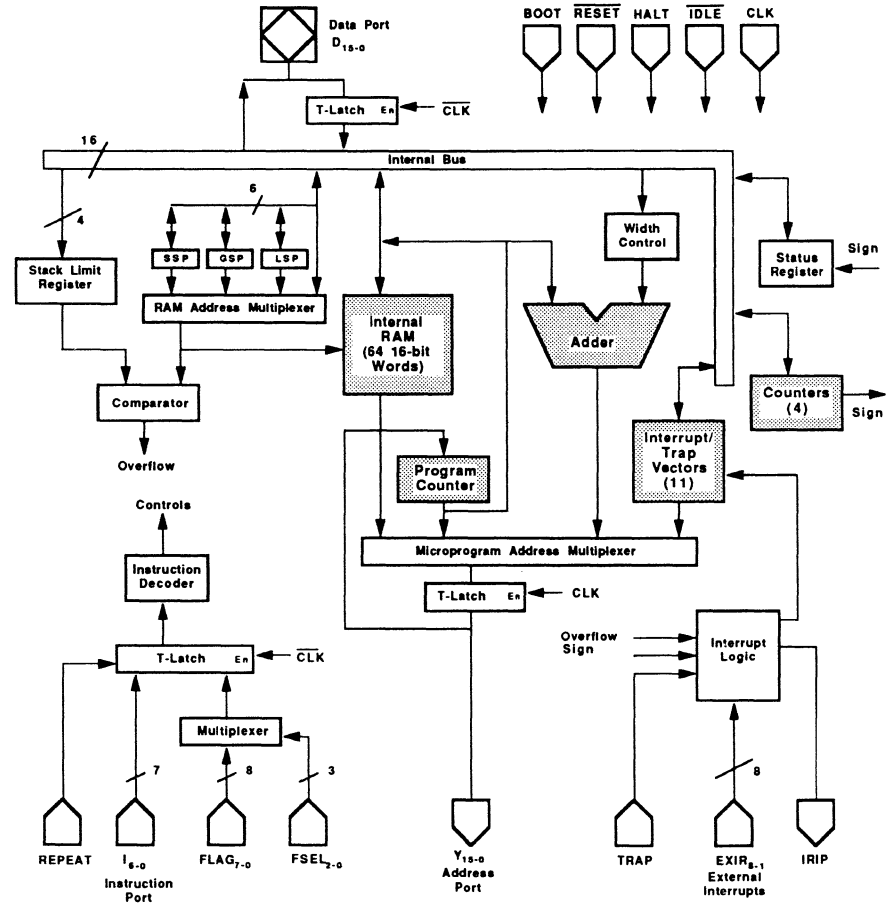
Program Sequencer

ADSP-1402

16-Bit Microcode Addressing Capability
Look-Ahead™ Pipeline
Extensive Interrupt Processing with Eleven On-Chip Interrupt Vectors
Four Event Counters to Support Looping
Absolute, Relative and Indirect Addressing
50ns Cycle Time; 12ns Clock-to-Address Delay
64-Word RAM for Storing:
- **Subroutine Linkage**
- **Jump Addresses**
- **Counters**
- **Status Register**

1μm CMOS Technology
84-Pin Grid Array Package



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Multiport Register File

ADSP-3128A

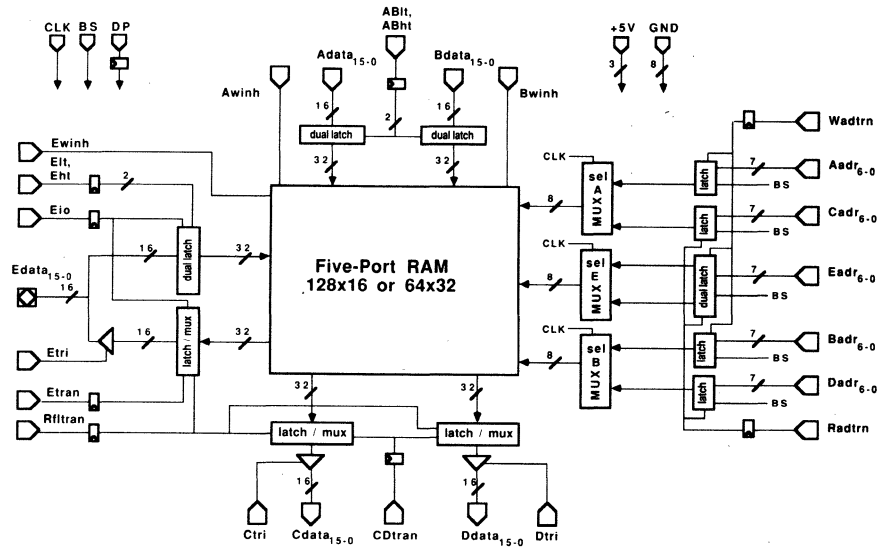
128 × 16 or 64 × 32 Register File Organization
Flexible "Crossbar" Data Routing via Five Ports
- **Two Input**
- **Two Output**
- **One Bidirectional**

Cascadable Horizontally and Vertically
Supports 20MHz Operation from Single 1 × Clock
- **18ns Clock-to-Valid-Output (Registered)**
- **30ns Address-to-Valid-Output (Transparent)**

Flexible Latching Modes at Address and Data Ports: Transparent, Latched, Registered
Prioritized Write Ports
Write Inhibit Control on Each Write Port
Automatically Pipelined Bank Select and Port Select
Register-to-Register Transfers
Three-State Outputs
Fully Static Operation
2W Power Dissipation in Low Power, TTL-Compatible 1.0μm CMOS
145-Pin Grid Array

APPLICATIONS
High Speed Temporary Data Storage in
- **Digital Signal Processing**
- **Numeric Processing**
- **Graphics**

Floating Point and Fixed Point



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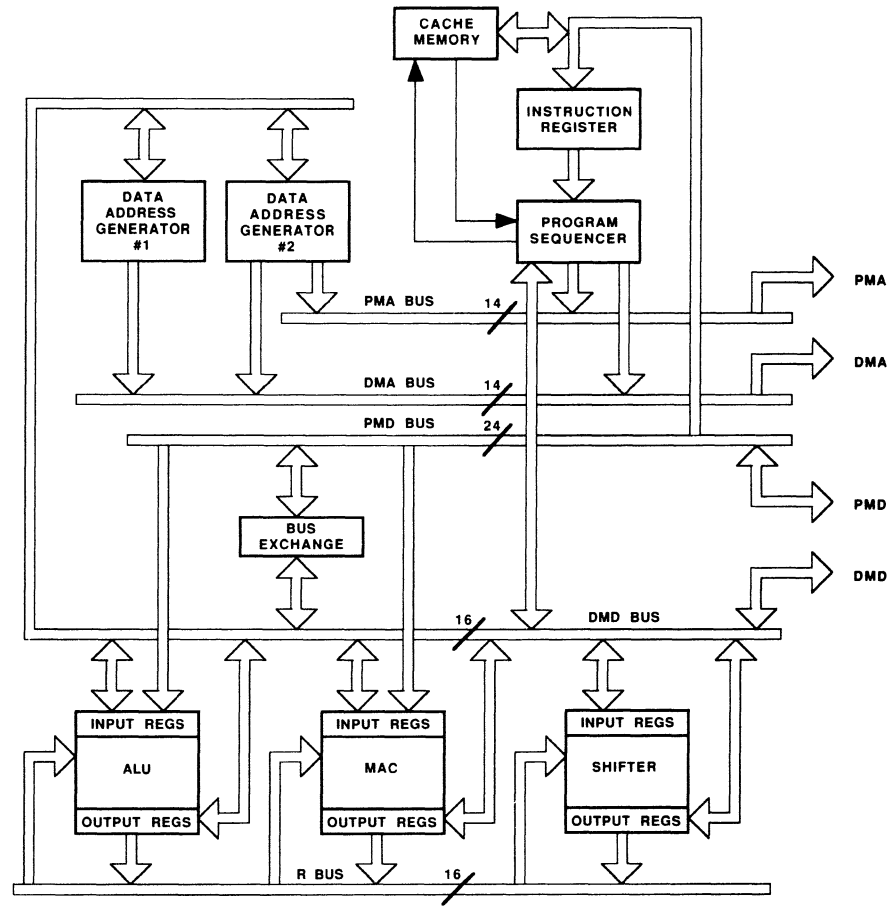
12.5 MIPS DSP Microprocessor

ADSP-2100A

Pin and Code Compatible with ADSP-2100 DSP Microprocessor
ADSP-2100A, Fabricated in 1.0 Micron CMOS
Separate Program and Data Buses, Extended Off-Chip
Single-Cycle Direct Access to 16K × 16 of Data Memory
Single-Cycle Direct Access to 16K × 24 (Expandable to 32K × 24) of Program Memory
Dual Purpose Program Memory for Both Instruction and Data Storage
Three Independent Computational Units: ALU, Multiplier/Accumulator and Barrel Shifter
Two Independent Data Address Generators
Powerful Program Sequencer
Internal Instruction Cache
Provision for Multiprecision Computation and Saturation Logic
Single-Cycle Instruction Execution
Multifunction Instructions
Four External Interrupts
80ns Cycle Time
790mW Maximum Power Dissipation (ADSP-2100A, J and K Grades)
100-Pin Grid Array, 100-Lead PQFP

APPLICATIONS

Optimized for DSP Algorithms Including
Digital Filtering
Fast Fourier Transforms
Applications Include
Image Processing
Radar, Sonar
Speech Processing
Telecommunications



ANALOG DEVICES

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Military Products

Products Available to Standard Military Drawings

Analog Devices' IC and hybrid products are supplied with processing to the three major levels of military screening, JAN QPL, Standard Military Drawing (SMD) and MIL-STD-883B (Revision C). These products are all produced in facilities which are fully qualified to MIL-M-38510 for integrated circuits, or MIL-STD-1772 for hybrids. In addition to these listings, we also publish a *Military Products Databook* which contains the specification details for designers who specify components for military contracts. The listings here are up-to-date and accurate as of the publication date (9/88), but there is ongoing development in this area by ADI and military procurement agencies. For status of specific parts, please contact your local salesperson. This list will also be updated and published every six months in *Analog Briefings* and in this *Short Form Designers' Guide*.

SMD Part Number	Generic Part Number	Description
5962-8512701XA	AD574AUD/883B	Complete 12-Bit ADC**
5962-8512702XA	AD574ATD/883B	Complete 12-Bit ADC**
5962-8759101LX	AD7572SQ12/883B	Complete 12-Bit 12μs ADC**
5962-87591013X	AD7572SE12/883B	Complete 12-Bit 12μs ADC**
5962-8759102LX	AD7572TQ12/883B	Complete 12-Bit 12μs ADC**
5962-87591023X	AD7572TE12/883B	Complete 12-Bit 12μs ADC**
5962-8759103LX	AD7572UQ12/883B	Complete 12-Bit 12μs ADC**
5962-87591033X	AD7572UE12/883B	Complete 12-Bit 12μs ADC**
5962-8759104LX	AD7572SQ05/883B	Complete 12-Bit 5μs ADC**
5962-87591043X	AD7572SE05/883B	Complete 12-Bit 5μs ADC**
5962-8759105LX	AD7572TQ05/883B	Complete 12-Bit 5μs ADC**
5962-87591053X	AD7572TE05/883B	Complete 12-Bit 5μs ADC**
5962-8759106LX	AD7572UQ05/883B	Complete 12-Bit 5μs ADC**
5962-87591063X	AD7572UE05/883B	Complete 12-Bit 5μs ADC**
5962-8861501XA	AD674AUD/883B	Complete 12-Bit ADC**
5962-8861502XA	AD674ATD/883B	Complete 12-Bit ADC**
5962-8850501RA	AD573SD/883B	10-Bit ADC
5962-8680202VA	AD571SD/883B	Complete 10-Bit ADC
5962-8680201VA	AD570SD/883B	Complete 8-Bit ADC
5962-8776201VX*	AD7575SQ/883B	8-Bit ADC with T/H
5962-8776202VX*	AD7575TQ/883B	8-Bit ADC with T/H
5962-87762012X*	AD7575SE/883B	8-Bit ADC with T/H
5962-87762022X*	AD7575TE/883B	8-Bit ADC with T/H
5962-8763501RA	AD670SD/883B	Signal Conditioning 8-Bit ADC**
5962-8850502RA	AD673SD/883B	8-Bit ADC
5962-8865001RX*	AD7820TQ/883B	8-Bit 2μs ADC with T/H
5962-88650012X*	AD7820TE/883B	8-Bit 2μs ADC with T/H
5962-8865002RX*	AD7820UQ/883B	8-Bit 2μs ADC with T/H
5962-88650022X*	AD7820OUE/883B	8-Bit 2μs ADC with T/H
8300201JC	AD DAC87/883B	12-Bit Hybrid DAC
8300301JA	AD DAC87/883B	12-Bit Monolithic DAC
5962-8776301LX	AD7537SQ/883B	12-Bit Dual Multiplying DAC**
5962-87763013X	AD7537SE/883B	12-Bit Dual Multiplying DAC**
5962-8776302LX	AD7537TQ/883B	12-Bit Dual Multiplying DAC**
5962-87763023X	AD7537TE/883B	12-Bit Dual Multiplying DAC**
5962-8776303LX	AD7537UQ/883B	12-Bit Dual Multiplying DAC**
5962-87763033X	AD7537UE/883B	12-Bit Dual Multiplying DAC**
5962-877020IRX	AD7545SQ/883B	12-Bit Multiplying DAC**
5962-8770202RX	AD7545TQ/883B	12-Bit Multiplying DAC**
5962-8770203RX	AD7545UQ/883B	12-Bit Multiplying DAC**
5962-8770204RX	AD7545GUQ/883B	12-Bit Multiplying DAC**
5962-87702012X	AD7545SE/883B	12-Bit Multiplying DAC**
5962-87702022X	AD7545TE/883B	12-Bit Multiplying DAC**
5962-87702032X	AD7545UE/883B	12-Bit Multiplying DAC**
5962-87702042X	AD7545GUE/883B	12-Bit Multiplying DAC**
5962-8780101XA*	AD567SD/883B	12-Bit High Speed DAC**
5962-8865901JA*	AD667SD/883B	12-Bit Dual Buffered DAC**
5962-8850901X	AD390SD/883B	12-Bit Quad DAC
5962-8850902X	AD390TD/883B	12-Bit Quad DAC
5962-8851001X	AD394SD/883B	12-Bit Quad DAC
5962-8851002X	AD394TD/883B	12-Bit Quad DAC
5962-8851003X	AD395SD/883B	12-Bit Quad DAC
5962-8851004X	AD395TD/883B	12-Bit Quad DAC
5962-8770001EX	AD7524SQ/883B	8-Bit DAC**
5962-8770002EX	AD7524TQ/883B	8-Bit DAC**
5962-8770003EX	AD7524UQ/883B	8-Bit DAC**
5962-87700012X	AD7524SE/883B	8-Bit DAC**
5962-87700022X	AD7524TE/883B	8-Bit DAC**
5962-87700032X	AD7524UE/883B	8-Bit DAC**

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SMD Part Number	Generic Part Number	Description
5962-8770101RX	AD7528SQ/883B	8-Bit Dual Buffered DAC**
5962-87701012X	AD7528SE/883B	8-Bit Dual Buffered DAC**
5962-8770102RX	AD7528TQ/883B	8-Bit Dual Buffered DAC**
5962-87701022X	AD7528TE/883B	8-Bit Dual Buffered DAC**
5962-8770103RX	AD7528UQ/883B	8-Bit Dual Buffered DAC**
5962-87701032X	AD7528UE/883B	8-Bit Dual Buffered DAC**
5962-8778901EA*	AD558SD/883B	8-Bit DACPORT™**
5962-8778902EA*	AD558TD/883B	8-Bit DACPORT™**
5962-8780201RX	AD7226TQ/883B	8-Bit Quad DAC with Amps**
5962-87802012X	AD7226TE/883B	8-Bit Quad DAC with Amps**
5962-8866301LX*	AD7228TQ/883B	8-Bit Octal Voltage Out DAC**
5962-88663013X*	AD7228TE/883B	8-Bit Octal Voltage Out DAC**
5962-886602LX*	AD7228UQ/883B	8-Bit Octal Voltage Out DAC**
5962-8866023X*	AD7228UE/883B	8-Bit Octal Voltage out DAC**
5962-8503001XC	AD2700SD/883B	Precision +10V Reference
5962-8503002XC	AD2700UD/883B	Precision +10V Reference
5962-8503003XC	AD2702SD/883B	Precision ±10V Reference
5962-8503004XC	AD2702UD/883B	Precision ±10V Reference
5962-8686101XC	AD580SH/883B	Precision +2.5V Reference
5962-8686102XC	AD580TH/883B	Precision +2.5V Reference

SMD Part Number	Generic Part Number	Description
5962-8757101XC	AD590JF/883B	Temp. Transducer 1μA/°K
5962-8757101YC	AD590JH/883B	Temp. Transducer 1μA/°K
5962-8757102XC	AD590KF/883B	Temp. Transducer 1μA/°K
5962-8757102YC	AD590KH/883B	Temp. Transducer 1μA/°K
5962-8757103XC	AD590LF/883B	Temp. Transducer 1μA/°K
5962-8757103YC	AD590LH/883B	Temp. Transducer 1μA/°K
5962-8757104XC	AD590MF/883B	Temp. Transducer 1μA/°K
5962-8757104YC	AD590MH/883B	Temp. Transducer 1μA/°K
5962-80013	ADLH0032/883B	High Speed Op Amp
5962-80014*	ADLH0033/883B	High Speed Buffer Amp
5962-8754001CA	AD585SQ/883B	High Speed S/H Amp
5962-87719*	AD625/883B	Instrumentation Amp
5962-88539*	AD524/883B	Instrumentation Amp
5962-88579*	HOS-050A, 060SH/883B	Video Op Amp
7705201EX	ADG508ATQ/883B	8-Channel Analog MUX
5962-8671601EX	ADG201HSTQ/883B	Quad SPST Fast Switch
5962-86716012X	ADG201HSTE/883B	Quad SPST Fast Switch
5962-8773501	ADSP-2100SG/883B	6MHz Digital Signal μP
5962-8773502	ADSP-2100ASG/883B	8MHz Digital Signal μP**
5962-8773503	ADSP-2100ATG/883B	10MHz Digital Signal μP**

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ANALOG DEVICES

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Military Products

MIL-STD-883 Class B Products

AD346	AD532	AD572	AD637	AD5200 Series	AD7522	AD7578	ADG222	ADSP-1401/10
AD362	AD534	AD573	AD642	AD5210 Series	AD7524	**AD7579**	**ADG506A/507A**	**ADSP-2100**
AD376	AD536A	AD574A	AD644	AD5240	AD7528	**AD7580**	**ADG508A/509A**	ADSP-3210/20
AD380	AD537	AD575	AD647	AD5539	AD7533	AD7582	**ADG526A/527A**	ADVFC32
AD381	AD538	AD578	AD648	AD7111	AD7534	AD7590/1DI	**ADG528A/529A**	**HDS-1250**
AD382	AD539	AD579	AD650	AD7118	**AD7535**	AD7592DI	ADLH0032	HOS-050A/060SH
AD390	AD542	AD580	AD651	AD7224	AD7536	**AD7672**	ADLH0033	HTC-0300A
AD394	AD544	AD581	**AD652**	AD7225	AD7537	AD7820	AD OP-07	
AD395	AD547	AD582	AD667	AD7226	AD7541 & A	AD7824	AD OP-27	
AD396	AD548	AD584	AD670	AD7501	AD7542	AD7828	AD OP-37	
AD506	AD558	AD585	AD673	AD7502	AD7543	**AD9000**	**ADREF01**	
AD507	AD561	**AD586**	**AD674A**	AD7503	AD7545	**AD9002**	**ADREF02**	
AD509	AD562	**AD587**	AD711	AD7506	AD7547	**AD9048**	ADSP-1008A	
AD510	AD563	**AD589**	AD712	AD7507	AD7548/49	**AD9610**	ADSP-1009A	
AD517	AD565A	AD590	AD741	AD7510DI	**AD7569**	AD ADC85/7	ADSP-1010A	
AD518	AD566A	AD624	**AD744**	AD7511DI	AD7572	AD DAC87	ADSP-1012A	
AD521	AD567	AD625	AD2700	AD7512DI	AD7574	ADG201A	ADSP-1016A	
AD522	AD570	AD630	AD2702	AD7520	AD7575	ADG202A	ADSP-1024A	
AD524	AD571	AD632	AD3860	AD7521	AD7576	ADG221	ADSP-1080A/81A	

Boldface indicates new MIL-STD-883 Class B Product availability since publication of 1987/1988 Databooks. For status of specific parts, please contact your local salesperson. Due to the nature of slash sheet and MIL drawing development, the availability of parts is difficult to predict. This list will be updated and published in *Analog Briefings* every six months.

JAN QPL Products

JAN Part Number	Generic Part Number	Description	JAN Part Number	Generic Part Number	Description
JM38510/14001BXA*	AD574AUD	Complete, 12-Bit ADC**	JM38510/13901BIA	AD534TH	Analog Multiplier, Prog. Scale
JM38510/14002BXA*	AD574ATD	Complete, 12-Bit ADC**	JM38510/13901BCA	AD534TD	Analog Multiplier, Prog. Scale
JM38510/12101BJC	AD562SD	12-Bit Current Output DAC	JM38510/13902BCA	AD534SD	Analog Multiplier, Prog. Scale
JM38510/12103BJC	AD565D	12-Bit Current Output DAC	JM38510/13902BIA	AD534SH	Analog Multiplier, Prog. Scale
JM38510/12702BEC	AD7520UD	10-Bit Multiplying DAC	JM38510/13903BIA	AD532SH	Analog Multiplier, Fixed Scale
JM38510/13301BEA	AD561DD	10-Bit DAC, I-Out	JM38510/13903BCA	AD532SD	Analog Multiplier, Fixed Scale
JM38510/12801BGC, A	AD584SH	Multi-Tap Reference			
JM38510/12802BGC, A	AD584TH	Multi-Tap Reference			

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Analog Devices offers a full spectrum of capabilities in application specific integrated circuits (ASICs). These chip-level systems can implement designs with 12-bit accuracy and 16-bit resolution that formerly required board-level solutions.

Analog Devices can incorporate most of the functions of its standard monolithic parts in full-custom and semicustom ICs. Full-custom parts optimize performance and space requirements, while cell-based semicustom parts reduce development time and engineering expense. Development costs can be cut further by tailoring a predefined system-on-a-chip known as a Linear System Macro to your application.

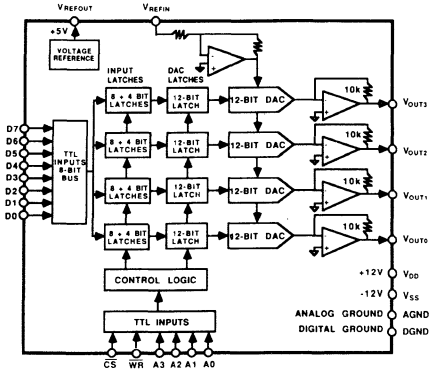
Analog's experienced design engineers work with powerful computer-aided design tools to design and lay out your circuit. Design centers are currently in Massachusetts, California and England.

Multiple locations for fabrication, assembly and testing ensure a ready supply of production parts. Products can be processed in full MIL-38510 certified facilities.

DESIGN EXAMPLES

Analog Devices has created a variety of customer-specific and function-specific ASIC parts. Described here are two Linear System Macros, a custom chip set and a semicustom chip.

AD75004 QUAD DAC



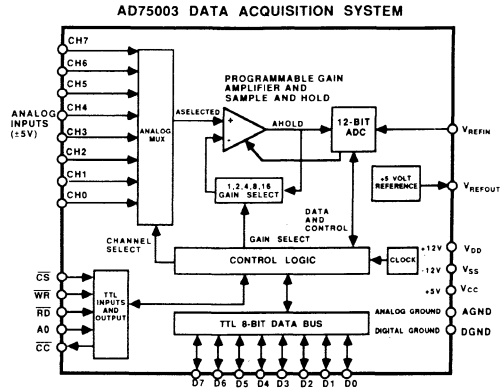
AD75004 Quad DAC

This circuit contains four separate 12-bit D/A converters with amplifiers for voltage output and an on-board reference. Double-buffering latches interface with an 8-bit parallel bus and permit updating of all four channels individually or simultaneously.

AD75003 Data Acquisition System

This DAS converts analog signals on 8 input channels to 12-bit values and interfaces via an 8-bit parallel bus. The chip integrates an 8-channel multiplexer, programmable-gain amplifier, sample-and-hold and 12-bit A/D converter with internal voltage reference.

AD75003 DATA ACQUISITION SYSTEM



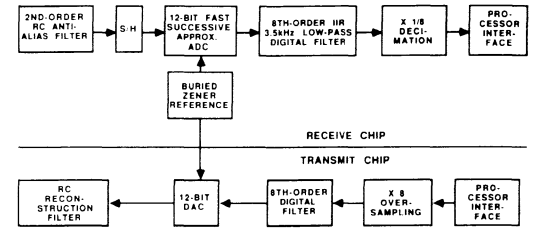
Derivative Circuits

The circuits outlined above can be modified to suit a specific customer's application. One such device is a semicustom, serial-interface DAS. The AD75003 design was altered to have programmable gains of 1 to 20 instead of 1 to 16, and a serial UART instead of an 8-bit parallel interface. In addition to the AD75003 functions, this part contains a precision instrumentation amplifier, a programmable line-frequency notch filter, a 7-bit trim DAC and a temperature sensor.

Modem Chip Set

Library cells can be combined to form macro building blocks for high speed modems. This two-chip design concept filters and converts data to interface a digital signal processor with the analog circuitry of a 9600-baud modem. On one chip, the received signal passes through an antialiasing filter, sample-and-hold, 12-bit A/D converter, 8th-order digital filter and decimation. On the other chip, transmit data is 8× oversampled, then goes to an 8th-order filter, a 12-bit DAC and an active reconstruction filter.

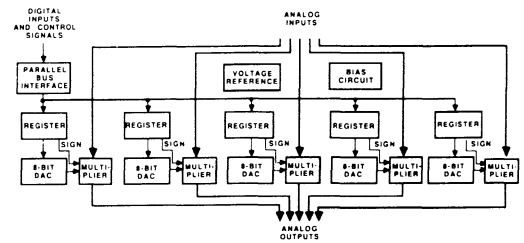
HIGH-SPEED MODEM CHIP SET



Transversal Filter Element

This circuit implements five taps of a finite-impulse response filter. Each tap comprises an 8-bit DAC and a multiplier, which handle signals up to 40MHz. A parallel interface sets the tap weights.

TRANSVERSAL FILTER ELEMENT



HIGH PERFORMANCE PROCESSES

Analog Devices' semicustom and custom circuits are fabricated using the same high performance processes as our standard ICs. These technologies include two mixed bipolar-CMOS processes, a high voltage CMOS

ANALOG DEVICES

Application Specific Integrated Circuits

process and high speed and low power bipolar processes. These processes can include thin-film resistors which may be laser trimmed for precise matching and stable performance over a wide temperature range.

The BiMOS II and Linear Compatible CMOS (LC^2MOS) processes combine bipolar and CMOS devices on one chip. Functional density is an order of magnitude greater than previous mixed-signal processes; over 20,000 devices can be placed on a single chip. Bipolar transistors provide low noise, low offset input stages and high power output stages. The CMOS devices offer high input impedance, and make dense logic and good switches for data converters, multiplexers and switched-capacitor filters. LC^2MOS also provides a JFET for very low input noise.

The bipolar-CMOS processes operate on supply voltages ranging from single +5 volts to split ±15V, with signal levels ranging from single-ended +3V to ±10V. These processes are ideally suited for applications in data acquisition, instrumentation, industrial automation and telecommunications.

The High-Voltage Switch (HVS) process provides quality analog switches that can operate with supply voltages up to ±22 volts. It can combine switches and multiplexers with CMOS logic.

The Flash bipolar process makes high speed linear signal processing, data conversion and ECL logic functions on one chip. Signal levels are ±4 volts with ±5V supplies or up to +10V with a +12V supply. Applications include disk-drive read/write circuitry and high speed telecommunications equipment.

The Complementary Bipolar (CB) process features high speed PNP and NPN devices for precision, low power linear applications. It also offers low noise buried Zener references and dual-gate JFETs. CB runs on +5V to ±15V supplies.

The table below summarizes the processes available for designing ASICs. Other processes in development will offer even higher speed, denser logic and higher integration of analog and digital functions.

ANALOG DEVICES HIGH-PERFORMANCE PROCESSES FOR ASICs

Process	Power	Signal	Features
BiMOS II	±12V	±8V	Wide Variety of Precision Linear and Digital Functions
LC^2MOS	+5V to ±15V	+3V to ±10V	Wide Variety of Precision Linear and Digital Functions
HVS	+5V to ±22V	+2V to ±18V	High Voltage Switches, Muxes and Logic Functions
Flash	±5V or +12V	±4V or +10V	High Speed Linear and Digital Functions
CB	+5V to ±15V	+2V to ±10V	High Speed, Low Power Linear Functions

CELL LIBRARIES

Cell libraries for the bipolar CMOS processes are described below. These libraries are growing with the development of new processes, macrocells and cells. Many new catalog parts will also be available as cells. Your local sales office can give you current information on the cell libraries and available Linear System Macros.

Operational amplifiers are available in bipolar, JFET and CMOS configurations. Representative bipolar op amp cells have performance characteristics similar to an AD OP-27 and a slew-enhanced AD741. The LC^2MOS process offers JFET op amps, including an AD544 equivalent.

Instrumentation amplifiers with performance comparable to the AD521 and AD524 are available. Comparators suitable for 12-bit-accurate applications are available. Linear comparators have response times down to 100 nanoseconds and strobed comparators have setup/access times down to 50 nanoseconds.

Digital-to-analog converters range in resolution from 8 to 14 bits, and include cells similar to the AD667 and AD1856. Analog-to-digital converters vary from 8 to 12 bits in resolution, and include cells equivalent to the AD7572 and AD674. One half-flash ADC cell converts to 8-bit accuracy in 500 nanoseconds, and one successive approximation cell converts to 12 bits in 5 microseconds.

Support cells include sample-and-hold amplifiers with performance comparable to the AD585, low-voltage bandgap references comparable to the AD584 and low noise buried Zener references.

RC active filters and programmable switched-capacitor filters are available with specifications in these ranges:

Topology: all classical filter types
Frequency Range: 200Hz to 20kHz (switched-cap) or 100Hz to1MHz (RC)
Number of Sections: up to 10th-order (switched-cap) or 4th-order (RC)
Signal/Noise and THD: >72dB, compatible with 12-bit data acquisition.

Logic cells include gates, counters, registers, PLA, RAM and ROM. Interface cells include 8-bit and 16-bit parallel I/O ports and UARTs.

DESIGN AND LAYOUT

Analog Devices engineers will design your integrated circuit, drawing on their years of experience and using powerful computer-aided design (CAD) tools. These comprehensive CAD tools help design, simulate and lay out the circuit and aid in generating test programs.

The following figure shows the standard design cycle which begins with schematic entry. After logic and initial electrical simulation, the designer uses the graphics editor to lay out the circuit. Parasitics and other data are extracted from the layout and circuit operation is simulated again. Finally, the system checks that the layout follows process design rules and matches the schematic.

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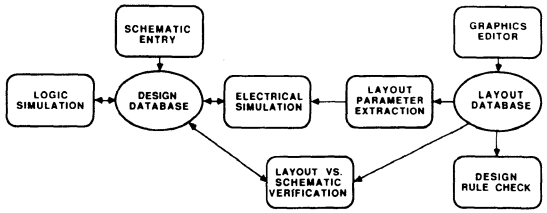
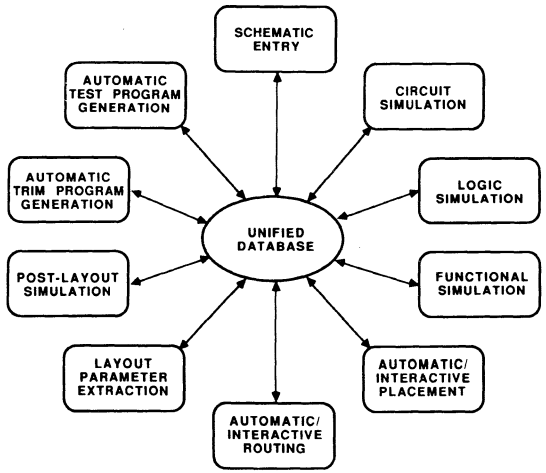
IC DESIGN WITH COMMERCIAL CAD SYSTEM



In addition to using these commercial CAD tools, Analog Devices has developed a proprietary compiler for mixed-signal IC design, called JANUS. By integrating all design functions into one environment with a common database, JANUS reduces design time by an order of magnitude.

IC DESIGN WITH JANUS PROPRIETARY CAD SYSTEM



To speed schematic entry, the designer selects devices, cells and macrocells from comprehensive menus. Device generators allow the designer to specify devices for maximum performance and minimum size. Analog, logic and functional simulators verify the performance of individual cells and the overall chip design. Placement and routing algorithms complete circuit layouts automatically, yet allow interaction with the designer to handle special cases. When placing devices and cells, JANUS considers thermal and electrical matching as well as die area. An expert system optimizes routing to minimize interconnect length and number of vias. Post-layout simulation comprehends the parasitics of the final routing and is more accurate than the initial simulation.

Future goals for JANUS include automatically generating programs for production trim and test of analog/digital ICs.

TEST AND TRIM

Analog Devices has over 20 years of experience in testing complex circuits and manufactures commercial test systems for precision linear ICs. In each fabrication facility, a computer network integrates Analog Devices, Teradyne and LTX test equipment. The design, wafer probe and test areas share data on the network for statistical analysis and device modelling.

All Analog Devices ASICs are tested at the wafer level, and most are laser-wafer trimmed to achieve high accuracy. Untrimmed thin-film resistors match within 1% to 0.1%, depending on area. Trimmed resistors can match to better than 0.01%. Wafers may be laser drift trimmed with a hot-chuck probe to minimize the effects of temperature on accuracy.

After packaging, all parts are tested to assure that they meet guaranteed specifications. Environmental handlers can verify parts at multiple temperatures. Burn-in is performed as specified by the customer.

PACKAGING

Analog Devices ICs are available in most modern package types, including high pin-count and surface mount varieties. ASICs may be assembled in any of Analog Devices' standard packages, listed below. This list is constantly expanded and other packages may be used if they are suitable for high performance applications.

Available Packages

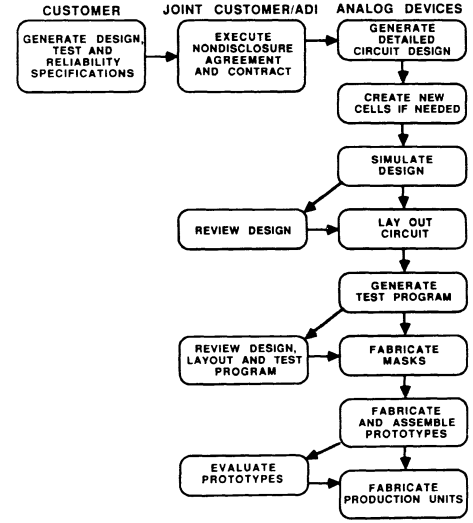
Pin-grid array (PGA): 68 to 144 pins
Leaded ceramic chip carrier (LDCC): 44 pins
Leadless ceramic chip carrier (LCC): 20 to 68 I/Os
Plastic quad flat pack (PQFP): 100 pins
Plastic leaded chip carrier (PLCC): 20 to 52 pins
Plastic dual in-line package (DIP): 14 to 64 pins
Side-brazed DIP: 14 to 64 pins
Frit-seal DIP (Cerdip): 14 to 28 pins
Small outline (SO): 14 and 16 pins

PROGRAM RESPONSIBILITIES AND INTERFACES

The following chart shows the major phases in developing an ASIC and responsibilities during each phase. The overall development time depends on the complexity of the circuit and on how custom the design is.

Your Analog Devices Sales Engineer is your first interface for ASIC development. Your local sales office can provide further information on Analog Devices' custom/semicustom capabilities.

PROGRAM RESPONSIBILITIES AND INTERFACES



ANALOG DEVICES

ANALOG DEVICES

Power Supplies

Modular AC/DC Power Supplies

GENERAL DESCRIPTION

Analog Devices offers a broad line of modular ac/dc power supplies that provide both OEMs and designers a reliable, easy to use, low cost solution to their power requirements. Models are available in PC mountable and chassis mountable designs with 5 volt to 15 volt (single, dual, triple) outputs and current ratings from 25mA to 5 amps. Since these modular supplies are fully encapsulated, no trimming or external component selection is necessary; simply mount the unit, connect power and output leads, and you're on the air! Most Analog Devices' power supplies are available from stock in both large and small quantities with substantial discounts being applied to large quantity orders.

AC/DC POWER SUPPLY FEATURES

- Current Limit Short Circuit Protection
- PC Mounted and Chassis Mounted Versions
- Single (+5V), Dual (±12V, ±15V), and Triple (±15V/+5V, ±15V/+1V to +15V) Output Supplies
- Current Outputs:
  25mA to 1000mA for Dual and Triple Output Supplies
  250mA to 5000mA for Single Output Supplies
- Wide Input Voltage Range
- Low Output Ripple and Noise
- Excellent Line & Load Regulation Characteristics
- High Temperature Stability
- Free-Air Convection Cooling; No External Heat Sink Required

SPECIFICATIONS – Typical @ +25°C and 115V ac 60Hz unless otherwise noted

		Model	Output Voltage Volts	Output Current mA	Line Reg max %	Load Reg max %	Output Voltage Error max	Ripple & Noise mV rms max	Dimensions Inches
PC Board Mounted	Dual Output	904	±15	±50	0.02	0.02	±200mV −0mV	0.5	3.5×2.5×0.875
		902	±15	±100	0.02	0.02	+300mV −0mV	0.5	3.5×2.5×1.25
		902-2	±15	±100	0.02	0.02	+300mV −0mV	0.5	3.5×2.5×0.875
		920	±15	±200	0.02	0.02	+300mV −0mV	0.5	3.5×2.5×1.25
		925	±15	±350	0.02	0.02	±1%	0.5	3.5×2.5×1.62
		921	±12	±240	0.02	0.02	+300mV −0mV	0.5	3.5×2.5×1.25
	Single Output	905	5	1000	0.02	0.05	±1%	1	3.5×2.5×1.25
		922	5	2000	0.02	0.05	±1%	1	3.5×2.5×1.62
		928	5	3000	0.05	0.10	±2%	5 (typ)	3.5×2.5×1.25
	Triple Output	923	±15	±100	0.02	0.02	±1%	0.5	3.5×2.5×1.25
			+5	500	0.02	0.05	±1%	0.5	
		927	±15	±150	0.02	0.02	±2%	0.5 (typ)	3.5×2.5×1.62
			+5	1000	0.02	0.10	±2%	1.0 (typ)	
		2B35J	±15	±65	0.08	0.1	(−0, +300mV)	0.5	3.5×2.5×1.25
			+1 to +15[1]	125	0.08	0.1		0.25	
		2B35K	±15	±65	0.01	0.02	(−0, +300mV)	0.5	3.5×2.5×1.25
			+1 to +15[1]	125	0.01	0.02		0.25	
Chassis Mounted	Dual Output	952	±15	±100	0.05	0.05	±2%	1	4.4×2.7×1.44
		970	±15	±200	0.05	0.05	±2%	1	4.4×2.7×1.44
		973	±15	±350	0.05	0.05	±2%	1	4.4×2.7×2.00
		975	±15	±500	0.05	0.05	±2%	1	4.4×2.7×2.00
	Single Output	955	5	1000	0.05	0.15	±2%	2	4.4×2.7×1.45
		976	5	3000	0.05	0.10	±2%	5 (typ)	4.75×2.7×1.45
		977	5	5000	0.05	0.10	±2%	5 (typ)	4.75×2.7×1.45
	Triple Output	972	±15	±150	0.02	0.02	±2%	0.5 (typ)	4.75×2.7×1.45
			+5	300	0.02	0.10	±2%	1.0 (typ)	
		974	±15	±150	0.02	0.02	±2%	0.5 (typ)	4.75×2.7×1.45
			+5	1000	0.02	0.10	±2%	1.0 (typ)	

NOTE
[1]Resistor programmable.

GENERAL SPECIFICATIONS

Power Requirements

Input Voltage Range:	105V ac to 125V ac
Frequency:	50Hz to 250Hz

Electrical Specifications

Temperature Coefficient:	0.02%/°C
Output Voltage Accuracy:	±2%, max See Specification Table
Breakdown Voltage:	500V rms, min
Isolation Resistance:	50MΩ
Short Circuit Protection:	All ac/dc power supplies employ current limiting. They can withstand substantial overload including direct short. Prolonged operation should be avoided since excessive temperature rises will occur.

Environmental Requirements

Operating Temperature Range:	−25°C to +71°C
Storage Temperature Range:	−25°C to +85°C

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Modular DC/DC Converters

GENERAL DESCRIPTION

Analog Devices' line of compact dc/dc converters offer system designers a means of supplying a reliable, easy to use, low cost solution to a variety of floating (analog and digital) power applications. These devices provide high accuracy, short circuit protected, regulated outputs with very low output noise and ripple characteristics.

Fourteen models are offered in five power levels of 1 watt, 1.8 watts, 4.5 watts, 6 watts and 12 watts. Input voltage versions include 5 volt, 12 volt, 24 volt and 28 volt with output ranges as follows: +5 volt, ±12 volts and ±15 volts at ±60mA to 1000mA output current capability.

Most models are high efficiency (typically over 60% at full load) and feature complete 6-sided continuous shielding for EMI/RFI protection. A π-type input filter is contained, in some models, which virtually eliminates the effects of reflected input ripple current. Most Analog Devices' dc/dc converters are available from stock in both large and small quantities with substantial discounts being applied to large quantity orders.

DC/DC POWER SUPPLY FEATURES

- Inaudible (>20kHz) converter switching frequency
- Continuous, Six-Sided EMI/RFI Shielding Except on 1 Watt and 1.8 Watt Models
- Output Short Circuit Protection (either output to common)
- Automatic Restart After Short Condition Removed
- Automatic Starting with Reverse Current Injected into Outputs
- Low Output Ripple and Noise
- High Temperature Stability
- Free Air Convection Cooling

No external heat sink or specification derating is required over the operating temperature range.

SPECIFICATIONS – Typical @ +25°C at nominal input voltage unless otherwise noted

Model	Output Voltage Volts	Output Current mA	Input Voltage Volts	Input[1] Voltage Range Volts	Input Current Full Load	Output Voltage Error max	Temperature Coefficient /°C max	Efficiency Full Load min	Dimensions Inches
943	5	1000	5	4.75/5.25	1.52A	±1%	±0.02%	62%	2.0×2.0×0.38
958	5	100	5	4.5/5.5	200mA	±5%	±0.01% (typ)	50%	1.25×0.8×0.4
941	±12	±150	5	4.75/5.25	1.17A	±1%	±0.01%	58%	2.0×2.0×0.38
960	±12	±40	5	4.5/5.5	384mA	±5%	±0.01% (typ)	50%	1.25×0.8×0.4
962	±15	±33	5	4.5/5.5	396mA	±5%	±0.01% (typ)	50%	1.25×0.8×0.4
964	±15	±33	12	10.8/13.2	165mA	±5%	±0.01% (typ)	50%	1.25×0.8×0.4
965	±15	±190	5	4.65/5.5	1.7A	±1%	±0.005% (typ)	62% (typ)	2.0×2.0×0.38
966	±15	±190	12	11.2/13.2	710mA	±1%	±0.005% (typ)	62% (typ)	2.0×2.0×0.38
967	±15	±190	24	22.3/26.4	350mA	±1%	±0.005% (typ)	62% (typ)	2.0×2.0×0.38
949	±15	±60[2]	5	4.65/5.5	0.6A	±2%	±0.03%	58%	2.0×1.0×0.375
940	±15	±150	5	4.75/5.25	1.35A	±1%	±0.01%	62%	2.0×2.0×0.38
953	±15	±150	12	11/13	0.6A	±0.5%	±0.01%	62%	2.0×2.0×0.38
945	±15	±150	28	23/31	250mA	±0.5%	±0.01%	61%	2.0×2.0×0.38
951	±15	±410	5	4.65/5.5	3.7A	±0.5%	±0.01%	62%	3.5×2.5×0.88

NOTES

[1]Models 940 and 941 will deliver up to 120mA output current (and model 943 will deliver up to 600mA) over an input voltage range of 4.65V dc and 5.5V dc.

[2]Single-ended or unbalanced operation is permissible such that total output current load does not exceed a total of 120mA.

GENERAL SPECIFICATIONS FOR 1W AND 1.8W MODELS

Line Regulation–full range: ±0.3% (±1% max, 949)
Load Regulation–no load to full load: ±0.4% (±0.5% max, 949)
Output Noise and Ripple: 20mV p-p (with 15μF tantalum capacitor across each output) (2mV rms max, 949)
Breakdown Voltage: 300V dc min (500V dc min, 949)
Input Filter Type: π
Operating Temperature Range: −25°C to +71°C
Storage Temperature Range: −40°C to +125°C (+100°C, 949)
Fusing: If input fusing is desired, we recommend the use of a slow blow type fuse that is rated at 150%–200% of the dc/dc converter's full load input current.

GENERAL SPECIFICATIONS FOR 4.5W, 6W, 12W MODELS

Line Regulation–full range: ±0.07% max (±0.02% max, 951, 960 series) (±0.1% max, 943)
Load Regulation–no load to full load: ±0.07% max (±0.02% max, 951, 960 series) (±0.1% max, 943)
Output Noise and Ripple: 1mV rms max
Breakdown Voltage: 500V dc min
Input Filter Type: π
Operating Temperature Range: −25°C to +71°C
Storage Temperature Range: −40°C to +125°C
Fusing: If input fusing is desired, we recommend the use of a slow blow type fuse that is rated at 150%–200% of the dc/dc converter's full load input current.

ANALOG DEVICES

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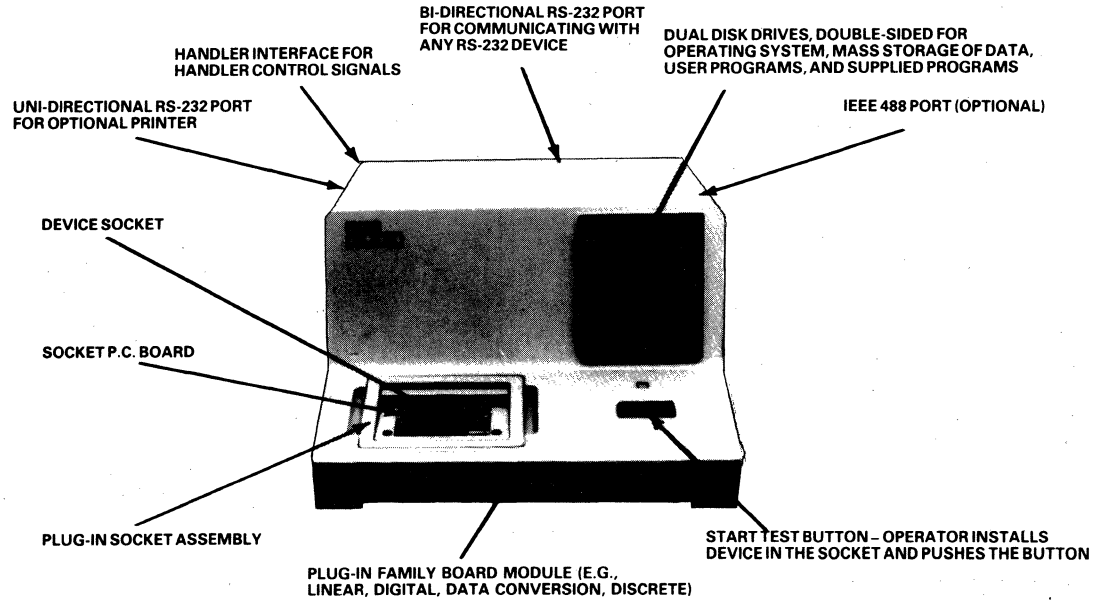
ANALOG DEVICES

LTS-2020 Component Test Systems



LTS-2020 CONSOLE SPECIFICATIONS

Voltage Measurement Range
± 10V

Current Measurement Range
10mA to + 150mA
– 150mA to + 10mA
– 1.0mA to + 1.0mA
– 10mA to + 10mA

Voltage Forcing Range
0 to + 20V
0 to – 20V
0 to + 10V
– 10V to + 10V

Operating Voltage Range
105V to 125V ac @ 50Hz to 60Hz
210V to 250V ac @ 50Hz to 60Hz

System Reference Stability
10V ± 25 ppm/1000hrs. Noncumulative

Current Range	Resolution	Accuracy
HI Z	10μV	± (0.0015% + 150μV)
Voltage Range	**Resolution**	**Accuracy**
0 to + 20V	2μA	± (2.5% + 100μA/V + 15μA)
0 to – 20V	2μA	± (2.5% + 100μA/V + 15μA)
0 to + 10V	0.2μA	± (0.5% + 10μA)
± 10V	0.1μA	± (0.5% + 10μA)
Current Range	**Resolution**	**Accuracy**
– 10mA to + 150mA	100mV	± 50mV
– 150mA to + 10mA	100mV	± 50mV
– 1.0mA to + 1.0mA	50mV	± 25mV
– 10mA to + 10mA	1mV	± 500μV

Console Dimensions
W 19in. × D 26in. (66cm.) × H 12in. (31cm.)
Wt. 75lbs. (39Kgs.)

Operating Temperature Range
0 to + 40°C, + 32°F to 104°F

THE LTS CONCEPT

The LTS-2020 is a versatile component test system which tests a multitude of components to the manufacturer's specifications (linear, digital, data conversion and discrete devices). The system offers such features as RS-232 ports for networking, IEEE for compatibility with handlers and probers, dual disk drives for mass storage of data, automatic self calibration and a full statistical analysis software package.

The LTS-2020 provides several data output formats – datalog, yield analysis and statistical analysis. The console provides the primary measurement and control functions to test a specific class of devices. The socket assembly is the mechanical and electronic interface for the family board and the DUT board. The DUT board plugs directly into the socket assembly and contains the circuitry and socket, specific to the actual device under test.

Analog Devices' component test systems are the first benchtop testers that are programmable in BASIC and fill-in-the-blanks CREATE. CREATE is menu-driven software which prompts the user for data sheet limits and conditions, then builds a completed test program for the specified device. Turnkey program libraries are available for each of the device families.

Far more than just comprehensive production testers, these test systems can handle complex engineering analysis and incoming inspection. They are the first systems that can provide all the capabilities of today's large centralized test systems at a price that is approximately one-third the cost. The LTS-2020 not only provides the flexibility of distributed or decentralized testing, it allows for cost effective multiple system purchases. They increase overall test reliability, since the threat of a single big failure is eliminated in a distributed testing environment.

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LINEAR DEVICE TEST CAPABILITY

The LTS-2101 Operational Amplifier Family Board tests today's very demanding high precision op amps, comparators and regulators. This board houses the test loop used in testing op amps and comparators and the pulse load circuitry used in developing the high currents needed for voltage regulator testing.

For testing devices under 100μV, the LTS-2101 offers a tight offset spec of ±(0.25% + 5μV). Use of low thermal Emf relays and a test loop gain of 10,045 ensures superior low level V_{OS} measurement performance for optimum repeatability of low level signals.

Testing of low current devices is achieved with the LTS-0614 Socket Assembly which is designed to test bias and offset currents with an accuracy of ±(5% + 25fA) for any FET amplifier, including quad devices. Program libraries containing prewritten test programs for many standard op amps, comparators and regulators are available on disk.

ANALOG–TO–DIGITAL TEST CAPABILITY

The LTS-2200 ADC Family Board provides the test circuitry required for testing monolithic, hybrid or modular ADCs. An on-board 16-bit microprocessor with 8K bytes of memory acts as a slave for the system console and executes preprogrammed test routines such as linearity, all codes existence, transition noise measurements and conversion time measurements at high speed. Absolute accuracy can be measured within 200μV. Linearity, differential nonlinearity, offset, gain and PSSR are tested to ±.05 DUT LSB +200μV. Turnkey test packages are available for many of the standard ADCs currently in use.

DIGITAL-TO-ANALOG TEST CAPABILITY

The LTS-2302 DAC Family Board utilizes advanced state of the art test techniques to provide comprehensive test capabilities for a wide variety of D/A converters. It will test both voltage and current output DACs, DACs with and without buffer registers and serial or parallel input DACs to 16-bit accuracy.

High repeatability on low level signals is achieved because of the grounding scheme on the LTS-2302. The incorporation of high level components in the V/I circuits ensures true accuracy. In addition, the methodology for measuring low bit currents allows appropriate testing of this parameter on CMOS DACs.

Output leakage current on the LTS-2302 is measured with the bit drivers to the DAC set to logic 0. Current is measured using the I to V converter. A 1mΩ resistor within the I to V circuitry ensures sensitivity, thereby measuring current down to ±1μA full scale.

DIGITAL DEVICE TEST CAPABILITY

The LTS-2510 Digital Device Family Board provides 24 pin driver/detectors and a precision, four quadrant V/I source for testing SSI/MSI TTL and CMOS digital devices. This board contains four programmable device supplies and switching circuitry necessary for performing accurate parametric measurements on all device pins.

Together with the LTS-0655 remote ac test fixture, dynamic parametric testing of 24-pin SSI/MSI TTL digital devices can be achieved. Accuracies are achieved down to ±4% + 1.5ns at a resolution of 500ps. Dynamic parameters tested are propagation delay, setup and hold times.

DISCRETE DEVICE TEST CAPABILITY

The LTS-2600 Transistor Family Board tests bipolar transistors, JFETs, diodes and optocouplers. An on-board 16-bit microprocessor with 4K bytes of memory acts as a slave for the LTS system and coordinates the timing and pulse width control of the stimulus and measurement signals. In addition, the microprocessor monitors the interlock circuitry to insure safe handling of high power test signals.

MOSFET software packages support the testing of N and P channel enhancement mode and N channel depletion mode devices. Tests which may be performed on MOSFET devices include Idss, Igss, Igssf, Igssr, Id (off), Id (on), B Vdss, B Vgss, B Vgssf, B Vgssr, Vds (on), Vgs (th), Vgsoff, Vsd, Rds (on) and Gsf.

ANALOG SWITCH TEST CAPABILITY

The LTS-2700 Analog Switch Family Board adds switch and multiplexer testing capability to the LTS-2020. This test capability, with CREATE software allows datalogged device testing at the incoming inspection and semiconductor manufacturing levels and includes software power for use in component evaluation applications.

The LTS-2700 tests on and off drain to source leakage currents with an accuracy of 250pA, while forcing differential voltages up to 50V (±25V from GND). Other tests performed are drain to source on resistance, greatest change in drain-source on resistance between channels, digital input current and supply current.

Twenty high integrity analog lines are provided – 4 to be used as drain connections and 16 for source connections. Also provided are 8 programmable digital drivers, 4 digital control bits, 6 variable power supplies and 1 fixed +5V supply. These combinations of sources provide testing of devices such as 4-channel switches, 16 to 1 multiplexers and other combinations of switches and multiplexers.

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ANALOG DEVICES

Product Families Not Included in the Databook

The information published in this *Short Form Designers' Guide* is intended to assist the user in choosing components for the design of *new* equipment, using the most cost-effective products available from Analog Devices. The popular product types listed below may have been designed into your circuits in the past, but they are no longer likely to be the most economic choice for your new designs. However, these products are still being used in current designs in large volume and are in full production at Analog Devices. We will continue to support current production needs and future designs indefinitely. Data sheets on these products are available upon request.

AD101
AD108/208/308
AD108A/208A/308A
AD111/211/311
AD293
AD294
AD351
AD370/371
AD503
AD506
AD510
AD515
AD518
AD528
AD530
AD531
AD533
AD545
AD567
AD611
AD651
AD801
AD2004
AD2006
AD2008
AD2009
AD2016
AD2020
AD2022
AD2023
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AD2036
AD2037
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AD2040
AD3554
AD3860
AD6012
AD7110
AD7118
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AD7525
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AD7531
AD7541
AD7546
AD7550
AD7552
AD7571
AD7574
AD ADC-816
ADC-8S
ADC-10Z
ADC-12QZ
ADC-14I/17I
ADC1100
ADC1102
ADC1105
ADC1111
ADC1133
ADC1143
ADC-QM
AD DAC-08
ADG201
ADSHC-85
API1620/1718
BDM 1615/16
BDM 1617
CAV-0920
CAV-1210
DAC-M
DAC-QS
DAC-QZ
DAC-10Z
DAC1009
DAC1106
DAC1108
DAC1132
DAC1420
DAC1422
DAC1423
DAS1128
DAS1150
DAS1151
DRC1765/66
DSC1705/06
DTM1716/17
HAS-0802
HAS-1002
HDD-1409
HDH-0802
HDH-1003
HDH-1205
HDL-3806
HDS-0810E
HDS-0820
HDS-1015E
HDS-1025
HDS-1240E
HDS-1250
IPA1751
IPA1764
IRDC1730
IRDC1731
IRDC1732
IRDC1733
MATV-0811
MATV-0816
MATV-0820
MCI1794
MDA-10Z
MOD-1005
MOD-1020
OSC1754
OSC1758
RDC1721
RTM Series
SAC1763
SBCD1752/53
SBCD1756/57
SCDX1623
SCM1677
SDC1604
SDC1700/RDC1700
SDC1702/RDC1702
SDC1704/RDC1704
SDC1711/RDC1711
SDC1721
SDC1725/RDC1725
SDC1726/RDC1726
SDC1768/RDC1768
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SHA-2A
SHA-4
SHA-5
SHA-1114
SHA-1134
SSCT1621
STM Series
TSL1612
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Substitution Guide for Product Families No Longer Available

The products listed in the left-hand column are no longer available from Analog Devices. In many cases, comparable functions and performance may be obtained with newer models, but – as a rule – they are not directly interchangeable. The closest recommended Analog Devices equivalent, physically and electrically, is listed in the right-hand column. If no equivalent is listed, or for further information, contact your local sales office.

Model	Closest Recommended Equivalent	Model	Closest Recommended Equivalent	Model	Closest Recommended Equivalent	Model	Closest Recommended Equivalent	Model	Closest Recommended Equivalent
AD501	AD711	AD7519	None	MDA-UD	None	THC-1500	None	282J	292A
AD502	AD711	AD7527	None	MDA-8H	MDA-10Z	THS-0025	HTC-0300	283J	292A
AD505	AD509	AD7544	None	MDA-10H	MDA-10Z	THS-0060	HTC-0300	301 (Module)	52
AD508	AD517	AD7555	None	MDA-11MF	AD7521	THS-0225	None	302	310 (Module)
AD511	AD711	AD7560	None	MDH-0870	None	TSDC1608-1611	TSL1612	350	None
AD512	AD711	AD7570	None	MDH-1001	None	2N3954	None	427	424
AD513	AD711	AD7583	None	MDH-1202	None	2N5900	None	602J10	AD524
AD514	AD711	ADC1103	None	MDMS-0801	AD9768	41	AD515	602J100	AD524
AD516	AD711	ADC1109	None	MDMS-1001	HDM-1210	47	48	602K100	AD524
AD520	AD524	ADC1121	AD7550	MDMS-1101	HDM-1210	101 (Module)	45	603	AD524
AD523	AD549	AD DAC100	None	MDS-0815	None	102	48	605	AD524
AD546	AD711	ADG200	None	MDS-0815E	None	106	118	901	904
AD555	AD7519	ADM501	ADM501/506	MDS-0830	HDS-0820	107	118	907	921
AD559	None	ADP501	ADP511	MDS-0850	HDS-0820	108	52	908	921
AD612	AD524	ADSHM-5	HTC-0300	MDS-1020	None	110	48	909	921
AD614	AD524	CAV-1020	MOD-1020	MDS-1020E	None	111	AD308	931	None
AD810-813	None	DAC-100F	None	MDS-1040	HDS-1025	114	119	932	None
AD814-816	None	DAC-10H	DAC-10Z	MDS-1080	HDS-1025	115	43	933	None
AD818	None	DAC1112	DAC12QS	MDS-1240	None	120	50	935	None
AD820-822	None	DAC1118	None	MDSL-0802	HDS-0820	142	48	942	None
AD830-833	None	DAC1122	AD7541	MDSL-0825	None	143	52	948	947
AD835-839	None	DAC1125	AD7533	MDSL-1002	HDS-1025	146	AD382	956	None
AD1408	None	HDL-3805	HDL-3806	MDSL-1035	None	149	50	971	921
AD1508	None	HTC-0500	HTC-0300	MDSL-1201	HDS-1250	153	AD517		
AD2003	AD2021	IDC1703	IRDC1730/1731	MDSL-1250	None	161	165		
AD2024	None	MAH-0801	HAS-0802	RTI-1200	RTI-711 Series	163	165		
AD2025	None	MAH-1001	HAS-1002	RTI-1201	RTI-711 Series	170	171		
AD2027	None	MAS-0801	HAS-0802	RTI-1202	RTI-711	180	AD OP-07		
AD2028	None	MAS-1001	HAS-1002	SERDEX	μMAC-5000	220	234		
AD5010/6020	AD9000	MAS-1202	HAS-1202	SHA-3	None	231	233		
AD7115	None	MDA-LB	None	SHA-6	SHA1144	274J	284J		
AD7513	None	MDA-LD	None	THC-0300	HTC-0300	279	286J		
AD7516	AD7510DI	MDA-UB	None	THC-0750	None	280	281		

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SELECTOR GUIDE

Model	Output Current ±A Pk Min	Output Voltage ±V Pk Min	V_S-Out Delta V	Supply Range ±V Min/Max	Internal Power Watts Max	V_{offset} Initial mV Max	V_{offset} vs Temp μV/°C Max	I Bias nA Max	I_q mA Max	PWR BW @ Nom V_{out} KHz[2] Typ	Slew Rate V/μs Typ	Unity GBW MHz Typ
PA03	30	68	7	15/75	500	3	30	.05	300	30	8	1
PA03A	*	*	*	*	*	1	10	.01	*	*	*	*
PA04A	20	184	8	15/100	250	5	30	.05	90	40	26	10
PA04	*	*	*	*	*	10	50	.1	*	*	*	*
PA12A	15	43	7	10/50	125	3	40	20	50	20	4	4
PA12M	10	39	6	10/45	*	6	65	30	*	*	*	*
PA12/PA12Q	*	*	*	*	*	*	*	*	*	*	*	*
PA61A[3]	10	39	6	10/45	97	3	40	20	10	16	2.6	1
PA61M	*	38	7	*	*	6	65	30	*	*	*	*
PA61/PA61Q	*	*	*	*	*	*	*	*	*	*	*	*
PA51A[3]	10	32	8	10/40	97	5	40	20	10	16	2.6	1
PA51M	*	*	*	*	*	10	65	40	*	*	*	*
PA51/PA51Q	*	28	*	10/36	*	*	*	*	*	*	*	*
PA07A	5	45	5	12/50	67	.5	10	.01	30	18	5	1.3
PA07/PA07Q	*	*	*	*	*	2	30	.05	*	*	*	*
PA07M	*	*	*	*	*	*	*	*	*	*	*	*
PA10A	5	44	6	10/50	67	3	40	20	30	23	5	6
PA10M	*	37	8	10/45	*	6	65	30	*	*	*	*
PA10/PA10Q	*	*	*	*	*	*	*	*	*	*	*	*
PA73/PA73Q[3]	5	22	8	10/30	67	10	65	40	5	23	2.6	1
PA73M	*	*	*	*	*	*	*	*	*	*	*	*
PA01	5	18	10	10/28	67	12	65	50	50	23	2.6	1
PA02A	5	15	4	7/19	48	3	25	.1	37	350	20	4.5
PA02M	*	*	*	*	*	10	50	.2	40	*	*	*
PA02/PA02Q	*	*	*	*	*	*	*	*	37	*	*	*
PA19	4A	35	5	14/40	78	3	30	.2	120	3500	900	75
PA19A	*	*	*	*	*	.5	10	.1	*	*	*	*
PA21A	3.0	17.0	3.0	2.5/20	36	4	10^4	250	90	13	1.2	.8
PA21	2.5	17.5	2.5	*	*	10	15^4	1000	*	*	*	*
PB50	2	89	11	30/100	35	2500	7000	—	25	60	100	15
PA09A	2	32	8	10/40	78	.5	10	.02	85	2500	400	75
PA09M	*	*	*	*	*	3	30	.1	*	*	*	*
PA09/PA09Q	*	*	*	*	*	*	*	*	*	*	*	*
PA12H	1	41	4	45		6		30	100			
WA01	.4A	12	4	7/16	5	10	50	2000	35	60000	4500	—
WA01A	*	*	*	*	*	5	25	1000	*	*	*	*
PA85	.2	215	10	15/225	34	2	30	.05	23	700	1000	20
PA85A	*	*	*	*	*	.5	10	.01	*	*	*	*
PA08A	.15	135	15	15/150	17.5	.5	10	.01	8.5	90	30	5
PA08V	*	160	*	15/175	*	2	30	.05	*	*	*	*
PA08/PA08Q	*	135	*	15/150	*	*	*	*	*	*	*	*
PA08M	*	*	*	*	*	*	*	*	*	*	*	*
PA88	.1	215	10	15/225	15	5	30	.05	1	10	30	1
PA88A	*	*	*	*	*	1	10	.01	*	*	*	*
PA83A	.075	140	10	15/150	17.5	1	10	.01	8.5	60	30	5
PA83M	*	*	*	*	*	3	25	.05	*	*	*	*
PA83/PA83Q	*	*	*	*	*	*	*	*	*	*	*	*
PA80J/PA80Q	.06	30	5	15/35	11.5	10	30	.05	10	100	15	5
PA84A	.04	143	7	15/150	17.5	1	10	.01	7.5	250	200	75
PA84M	*	*	*	*	*	3	25	.05	*	*	*	*
PA84/PA84Q	*	*	*	*	*	*	*	*	*	*	*	*
PA84S	*	*	*	*	*	*	*	*	*	*	*	*
PA81J	.03	70	5	32/75	11.5	3	25	.05	8.5	60	20	5
PA82J/PA82Q	.015	145	5	70/150	11.5	3	25	.05	8.5	30	20	5

NOTES:

1. Second source explanation.
   Direct = All major specifications are equal.
   Possible = Pin for pin but differences in specifications.
   The APEX part is usually superior in one or more parameters.
   Similar = External connections and specifications are similar.
2. Higher frequencies are possible at reduced output levels.
3. Class "C" outputs are optimized for low cost - not recommended above 1kHz.
4. Specification is typical value.

*Specification is the same as above.
**Applies to all grades of the model.

M = MIL-STD Screening
Q = High Rel Screening

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V_{os} Adj	Current Limit	Thermal Shutdown	Input Stage	Temp Range Max	Second Source
Yes	Thermal	Yes	FET	−25/85	No
*	*	*	*	*	*
No	Ext Adj	No	FET	−25/85	No
*	*	*	*	*	*
No	Ext Adj	No	Bipolar	−55/125	Direct
*	*	*	*	*	No
*	*	*	*	−25/85	Direct
No	Ext Adj	No	Bipolar	−25/85	No
*	*	*	*	−55/125	*
*	*	*	*	−25/85	*
No	Ext Adj	No	Bipolar	−55/125	Direct
*	*	*	*	*	*
*	*	*	*	−25/85	*
Yes	Ext Adj	Yes	FET	−25/85	Possible
*	*	*	*	*	*
*	*	*	*	−55/125	*
No	Ext Adj	No	Bipolar	−55/125	Possible
*	*	*	*	*	*
*	*	*	*	−25/85	*
No	Ext Adj	No	Bipolar	−25/85	Direct
*	*	*	*	−55/125	No
No	Ext Adj	No	Bipolar	−25/85	Possible
No	Ext Adj	No	FET	−55/125	Similar
*	*	*	*	*	*
*	*	*	*	−25/85	*
No	Ext Adj	Yes	FET	−25/85	Similar
*	*	*	*	*	*
No	3	Yes	Bipolar	−25/85	No
*	2.5	*	*	*	*
No	Ext Adj	No	Bipolar	−25/85	No
Yes	4.5	Yes	FET	−25/85	No
*	*	*	*	−55/125	*
*	*	*	*	−25/85	*
No	Ext Adj	No	Bipolar	−25/200	No
Yes	.7A	No	Bipolar	−25/85	Possible
*	*	*	*	*	*
No	Ext Adj	Yes	FET	−55/125	Similar
*	*	*	*	*	*
Yes	Ext Adj	Yes	FET	−25/85	No
*	*	*	*	*	*
*	*	*	*	*	*
*	*	*	*	−55/125	*
No	Ext Adj	Yes	FET	−25/85	No
*	*	*	*	*	*
Yes	.1A	Yes	FET	−25/85	Possible
*	*	*	*	−55/125	No
*	*	*	*	−25/85	Possible
Yes	.1A	Yes	FET	0/70	Direct
Yes	.05A	Yes	FET	−25/85	Possible
*	*	*	*	−55/125	No
*	*	*	*	−25/85	Possible
*	*	*	*	*	No
Yes	.05A	Yes	FET	0/70	Direct
Yes	.025A	Yes	FET	0/70	Direct

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- Output Current — 20A continuous
- Supply Voltage — 200V
- Internal Dissipation — 250W

PB50 — Power Booster
- Supply Voltage — 200V
- High Current — 2A
- High Slew Rate — 50V/μs (min)

PA21 — Low Cost Dual Amplifier
- Wide Supply Range — 5V to 40V
- Common Mode Range includes $-V_S$
- High Current — 3.0A (PA21A)

PA85/PA88 — Industry's Highest Voltage Amplifiers
- Supply Voltage — 450V
- High Current — 200mA (PA85)
- Low IQ — 2mA (PA88)

WA01 — Wideband Amplifier
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AT&T's DSP FAMILY: The Most Advanced Digital Signal Processors

Introduction

AT&T offers the most advanced family of single-chip digital signal processors. Designed by AT&T Bell Laboratories, the *WE*® DSP32 Digital Signal Processor and the *WE* DSP16 Digital Signal Processor families offer unprecedented speed, accuracy, and ease of use.

The DSP32 was the first 32-bit single-chip floating-point DSP produced and has been in volume production since 1984. Its 32-bit floating-point format ends the need for scaling and allows easy implementation for algorithms that may be impossible to code in 16-bit fixed point due to precision or dynamic range limitations. Programming is also greatly simplified by the DSP32's C-like syntax. Equations are coded in an easy-to-read form, which makes programs almost self-documenting. Also, the DSP32 is supported with a full Kernighan and Ritchie C compiler.

The *WE* DSP32C is AT&T's latest generation 32-bit floating-point DSP. Both source and object code are upward compatible with the DSP32. A large address space (16 Mbytes), blazing speed, and easy hardware system interfaces all characterize the DSP32C. Like the DSP32, the DSP32C has its own Kernighan and Ritchie C compiler.

The DSP16 is a 16-bit fixed-point digital signal processor; it is AT&T's fourth generation DSP. It is the DSP of choice when very high speed and low power are required. It features a 55 ns instruction cycle time (multiply and accumulate) and a powerful set of microprocessor-type instructions. Hardware features include a programmed instruction cache for low overhead looping, dedicated registers for virtual shift (modulo) addressing and advanced I/O ports. Both the 16-bit parallel port and the high-speed serial port allow easy glueless interfaces to many external devices such as memories, codecs, or other DSPs.

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The *WE* DSP16A is an extension of the DSP16 architecture. This high-performance fixed-point processor features a 33 ns instruction cycle time. On-chip memory includes twice the amount of on-chip ROM and four times the amount of on-chip RAM as the DSP16. The DSP16A is pin, source-code, and object-code compatible with the DSP16 device.

Hardware Development

Application system hardware and software development is supported by the *WE* DSP32, DSP32C, DSP16, and DSP16A Development Systems. These hardware development systems provide real-time in-circuit emulation and real-time algorithm development. A single host computer can support multiple development systems.

Development Software

To complement the family's hardware tools, support software tools are available to help create, test, and debug application programs. The *WE* DSP32 and DSP32C Support Software Library and the *WE* DSP16 and DSP16A Support Software Library run under the *MS-DOS**, *UNIX*® , or *VMS*** Operating System. These libraries provide an assembler, loader, and device simulator, as well as other utilities that aid and simplify program development.

High-level language support for the DSP32 and DSP32C processors is provided by the *WE* DSP32 and DSP32C C Language Compiler. Using this optimizing compiler and the libraries of functions supplied with the compiler allows efficient programs to be written quickly — and without an intimate knowledge of the device's architecture and instruction set. The compiler runs under the *MS-DOS* or *UNIX* Operating System.

Application Software

Complementing the development software, AT&T offers software application libraries containing source code for algorithms and transcendental math functions. The *WE* DSP32 and DSP32C Application Software Library and the *WE* DSP16 and DSP16A Application Software Library contain carefully optimized assembly language programs for the DSP32 and DSP16 families.

Some of the routines included are:

- sin, cos, tan, log, square root power
- N-by-N matrix routines
- Nth order FIR, IIR filters and Nth order real and complex adaptive FIR filters
- N-point FFT and window functions
- Image processing routines

These are just a few of the many attributes that give the AT&T DSP family excellent performance and assurance against obsolescence in the future.

The Floating-Point Solution

The DSP32 — the first single-chip 32-bit floating-point digital signal processor. The DSP32 combines state-of-the-art technology, advanced circuit design, and extensive simulation techniques to achieve the following user-significant features:

- 12.5 MFLOP throughput
- 32-bit data bus
- 56 Kbyte off-chip memory expansion
- 4 memory accesses per instruction
- No speed penalty for using off-chip memory
- 40 powerful instruction types
- 12.5 Mb/s serial I/O rate
- 4 Mbyte/s parallel I/O rate

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** Registered trademark of the Digital Equipment Corporation

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The DSP32 floating-point format consists of a 24-bit mantissa that encodes the fractional part of the number and an 8-bit exponent that encodes the magnitude of the number. The exponent provides greater than 1500 dB of dynamic range, making overflow or underflow unlikely. The 24-bit normalized mantissa yields a precision that is independent of the magnitude of the number. The format is very useful for high-precision calculations used in FFTs and adaptive filters; the floating-point format eliminates scaling and decimal tracking and greatly reduces quantization noise during intermediate calculations. Another state-of-the-art feature of the DSP32 is its instruction set. Instead of using mnemonics, the DSP32 uses a C-like instruction set. This instruction set improves documentation by making it easier for designers to move high-level code onto the DSP.

Utilizing input from DSP32 users and Bell Laboratories design experience with the DSP32, AT&T designed the DSP32C to be the world's most advanced digital signal processor. In addition to the DSP32's impressive list of features, the DSP32C offers:

- Upward compatibility with DSP32
- 25 MFLOP throughput
- 16 Mbyte address space
- 8 vectored interrupts
- 16 Mb/s serial I/O
- IEEE 754 format conversion (single cycle)

The Fixed-Point Solution

The *WE* DSP16A — the fastest currently available single-chip digital signal processor and the *WE* DSP16 digital signal processor are the right choice for applications that require very high speed and low power. These devices perform a multiply and accumulate operation in a single instruction cycle (33 ns for the DSP16A). The DSP16 is available in 55 ns and 75 ns versions.

The DSP16 features:

- 55 ns parallel multiplier
- Program controlled instruction cache
- Modulo addressing for efficient vector operations
- 10 Mb/s serial I/O rate
- 18.2 Mbyte/s parallel I/O rate
- 16-bit data bus
- Hardware/software interrupt capability

In addition to these features, the DSP16A includes:

- 33 ns parallel multiplier
- 30 Mbyte/s parallel I/O rate

The DSP16 family is ideally suited for high-speed applications, which include high-speed modems, process controllers, graphics, and most computationally intensive signal processing algorithms. A military qualified (MIL-STD 883) 75 ns version of the DSP16 is available.

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DIGITAL

WE® DSP32 Digital Signal Processor

Description

The *WE* DSP32 Digital Signal Processor is a high-speed, programmable, 32-bit digital signal processing device capable of supporting a wide range of applications. These applications include digital control, digital audio, graphics processing, image processing, speech recognition, high-speed modems, low bit-rate codecs, filtering, and multi-channel signaling systems. Support tools include a full Kernighan and Ritchie C compiler optimized for the DSP32's architecture. A pipelined architecture allows the DSP32 device to achieve high throughput. This architecture includes a 32-bit floating-point arithmetic unit that performs 12.5 million floating-point computations per second and a 16-bit integer arithmetic unit that executes 6.25 million instructions per second. The DSP32 device is implemented using NMOS technology and is available in a 40-pin DIP or a 100-pin pin-grid-array (PGA) package. The PGA package provides pins for an external 32-bit data bus and a 16-bit address bus for use with external memory expansion.

Architectural Summary

The DSP32 uses two execution units to achieve its high throughput. The control arithmetic unit (CAU) is used as a 16-bit microprocessor, or it may be used to generate and modify addresses for the data arithmetic unit (DAU). The CAU performs ALU and data move instructions as well as conditional and unconditional branch operations. When used to generate addresses for the DAU, it can generate and post-modify four addresses in a single instruction cycle.

The DAU employs a straightforward three-stage fetch/multiply/accumulate pipeline for 32-bit floating-point operands. Results are automatically normalized without additional instructions or pipeline stages. On-chip memory consists of two 512-word banks of RAM and one 512-word ROM bank. External memory is expandable to 56 Kbytes (directly addressable). Full-speed execution and accesses of instructions and data is presented for the entire external address space.

Serial and parallel ports which support DMA are provided to ease interfacing.

Features

- 25 MHz version (160 ns)
- 16 MHz version (250 ns)
- Twenty-one 16-bit general purpose registers
- Four 40-bit accumulators
- 32-bit floating-point arithmetic
- 32-bit instructions
- Full C compiler
- All instructions are single-cycle
- 16-bit integer microprocessor operations for logic and control
- User-selectable memory configurations
- Data addressable as 8-, 16-, or 32-bit words
- Mask-programmable ROM
- 2048 bytes of ROM organized as 512 × 32 bits
- 4096 bytes of RAM organized as two banks of 512 × 32 bits
- 56 Kbytes of direct memory addressing off-chip with pin-grid-array package
- No speed penalty for off-chip program or data memory
- Serial and parallel I/O ports with DMA
- Interfaces to a microprocessor without any additional peripherals
- Error control logic to detect and mask errors
- Available in 40-pin DIP or 100-pin pin-array package
- Supported by:
  - — DSP32 Software Library
  - — DSP32 Development System
  - — DSP32 C compiler
  - — DSP32 Application Library
  - — DSP32 Application Guide

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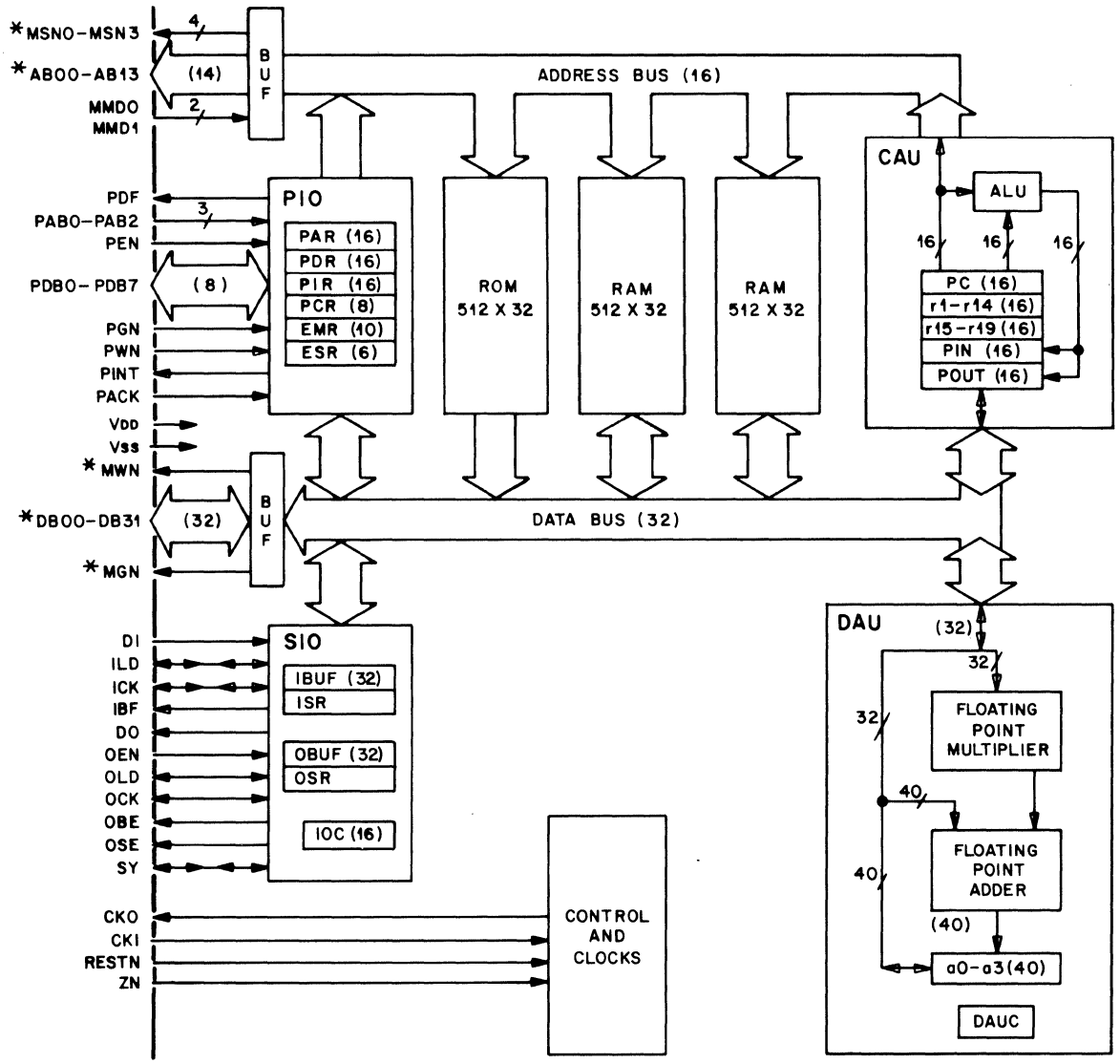
Figure 1. DSP32 Block Diagram



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LEGEND:

a0—a3	Accumulators 0—3	**FPM**	Floating-Point Multiplier	**PDR**	PIO Data Register
ALU	Arithmetic Logic Unit	**IBUF**	Input Buffer	**PIO**	Parallel I/O Unit
CAU	Control Arithmetic Unit	**IOC**	Input/Output Control Register	**PIR**	PIO Interrupt Register
DAU	Data Arithmetic Unit	**ISR**	Input Shift Register	**R1—r19**	Registers 1—19
DAUC	Data Arithmetic Unit Control Register	**OBUF**	Output Buffer	**PIN**	Parallel Input Register
		OSR	Output Shift Register	**POUT**	Parallel Output Register
EMR	Error Mask Register	**PAR**	PIO Address Register	**RAM**	Read/Write Memory
ESR	Error Source Register	**PC**	Program Counter	**ROM**	Read-Only Memory
FPA	Floating-Point Adder	**PCR**	PIO Control Register	**SIO**	Serial I/O Unit

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WE® DSP32C Digital Signal Processor

Description

The *WE* DSP32C Digital Signal Processor is the world's most advanced DSP. Targeted at high-performance applications, the DSP32C brings an unprecedented level of performance to the systems designer. Upward compatibility has been preserved with the DSP32, so current DSP32 users can easily upgrade to the DSP32C if greater performance is desired. The DSP32C features a 16 Mbyte address space, vectored interrupts, a full C compiler, enhanced instruction set, and powerful format conversions.

Architectural Summary

The DSP32C uses two execution units to achieve its high throughput. The control arithmetic unit (CAU) is used as a 16- or 24-bit microprocessor, or it may be used to generate and modify addresses for the data arithmetic unit (DAU). The CAU executes conditional and unconditional ALU and branch operations as well as data move instructions. When used to generate addresses for the DAU, it can generate and post-modify four addresses in a single instruction cycle.

The DAU employs a straightforward three-stage fetch/multiply/accumulate pipeline for 32-bit floating-point operands. Results are automatically normalized without additional instructions or pipeline stages.

On-chip memory consists of three banks of RAM each with 512 words. A ROM coded version is also available, which substitutes a 2048-word ROM for one 512-word RAM bank. External memory is expandable to 16 Mbytes (directly addressable). A flexible wait-state generator allows efficient use of slower memories and memory-mapped peripherals. Rather than imposing full instruction cycle penalty for each wait state, the DSP32C inserts one quarter of an instruction cycle for each wait state.

Both serial and parallel ports are provided to further ease interfacing. Input and output DMA to any location in the DSP32C address space is supported by both ports.

Features

- 50 MHz version (80 ns)
- 40 MHz version (100 ns)
- Object-code compatible with DSP32
- Twenty-two 24-bit general-purpose registers
- 32-bit floating-point arithmetic
- Full C compiler
- 24-bit and 16-bit integer microprocessor operations for logic and control
- Data addressable as 8-, 16-, or 32-bit words
- 2048 words of ROM and 2 banks (512 words each) of RAM, or 3 banks (512 words each) of RAM
- 16 Mbytes of directly addressable off-chip memory
- Wait states for slow memories
- Powerful single-cycle data format conversions:
  - — IEEE 754 floating point
  - — 24-bit and 16-bit integer
  - — 8-bit linear byte
  - — 8-bit μ-law and A-law
- Serial and parallel ports with DMA
- Interfaces to a microprocessor without glue logic
- Eight vectored interrupts
- 133-pin PGA package
- Supported by:
  - — DSP32C Software Library
  - — DSP32C Development System
  - — DSP32C C Compiler
  - — DSP32C Application Library

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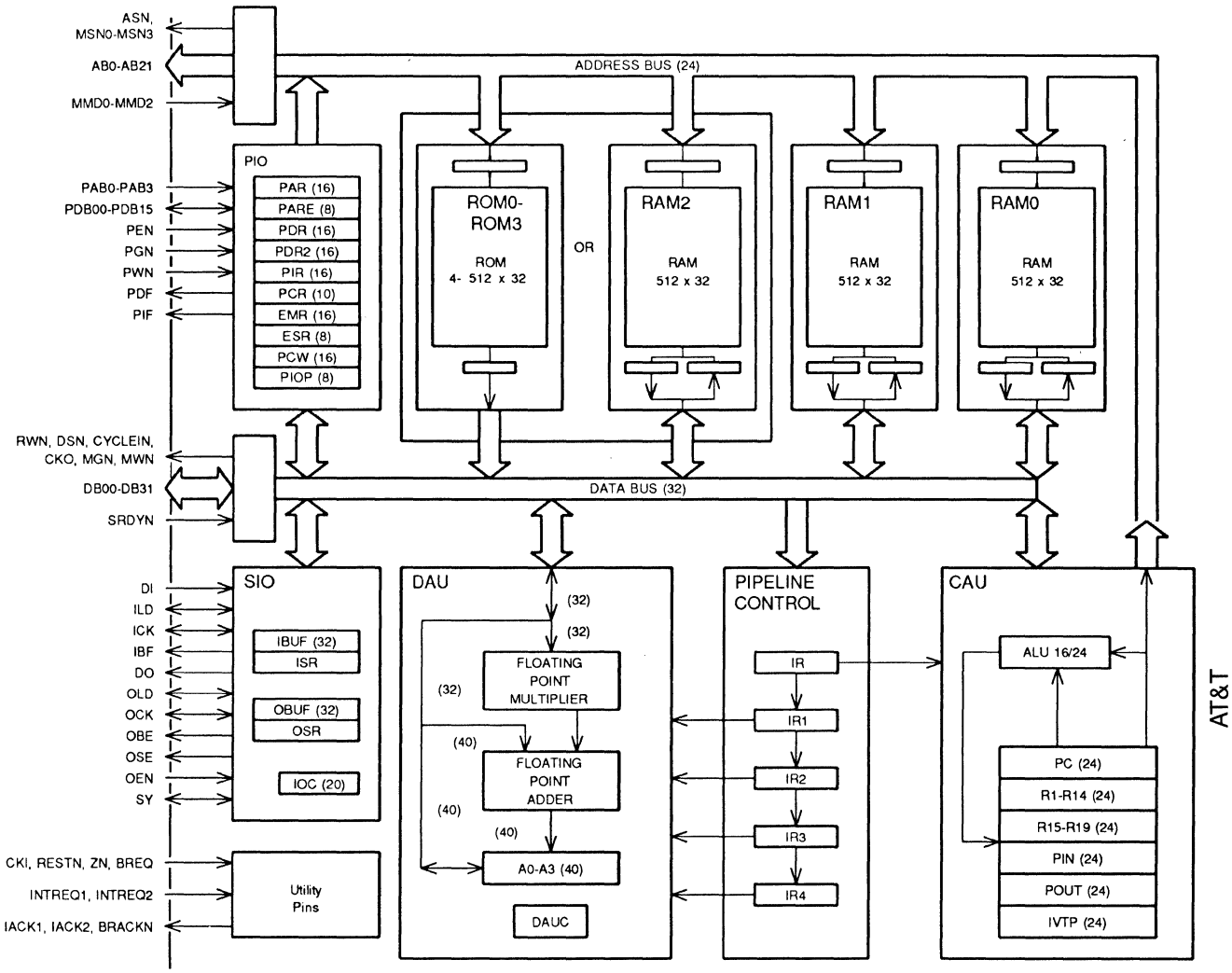
Figure 1. DSP32C Block Diagram



LEGEND:

A0—A3	Accumulators 0—3	**ISR**	Input Shift Register	**PDR2**	PIO Data Register 2
ALU	Arithmetic Logic Unit	**IVTP**	Interrupt Vector Table Pointer	**PIN**	Serial DMA Input Pointer
CAU	Control Arithmetic Unit	**OBUF**	Output Buffer	**PIO**	Parallel I/O Unit
DAU	Data Arithmetic Unit	**OSR**	Output Shift Register	**PIOP**	Parallel I/O Ports
DAUC	DAU Control Register	**PAR**	PIO Address Register	**PIR**	PIO Interrupt Register
EMR	Error Mask Register	**PARE**	PIO Address Register Extended	**POUT**	Serial DMA Output Pointer
ESR	Error Source Register	**PC**	Program Counter	**R1—R19**	Registers 1—19
IBUF	Input Buffer	**PCR**	PIO Control Register	**RAM**	Read/Write Memory
IOC	Input/Output Control Register	**PCW**	Processor Control Word	**ROM**	Read-Only Memory
IR	Instruction Register	**PDR**	PIO Data Register	**SIO**	Serial I/O Unit

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WE® DSP16 Digital Signal Processor

Description

The DSP16 Digital Signal Processor integrated circuit is a 16-bit, high-speed, programmable digital signal processor. The device is fabricated in low-power CMOS technology and is packaged in an 84-pin plastic leaded chip carrier. A military qualified version is available in a 13 x 13 pin PGA package. It is a general-purpose building block that can be programmed to perform a wide variety of signal processing functions. It achieves high throughput with its parallel pipelined architecture without programming latencies or restrictions. The processor has an arithmetic unit capable of multiplying two 16-bit words of data and accumulating the product in a single 55 ns cycle. The arithmetic data is supplied by two independent addressing units. The DSP16 device can function in a stand-alone manner, requiring only an external clock.

Architectural Summary

The DSP16 device contains a data arithmetic unit (DAU) that performs signal processing arithmetic; a ROM address arithmetic unit (XAAU); a RAM address arithmetic unit (YAAU); a 2048 by 16-bit ROM that contains program instructions and fixed data; a 512 by 16-bit RAM for variable data; an instruction cache (CACHE); a serial I/O unit (SIO); and a 16-bit parallel I/O unit (PIO).

The arithmetic unit contains a 16 × 16 bit parallel multiplier that generates a full 32-bit product in 55 ns. The product can be accumulated with one of two 36-bit accumulators. The data in these accumulators can be directly loaded from or stored to memory in two 16-bit words with automatic saturation on overflow. The ALU supports a full set of arithmetic and logical operations on either 16- or 32-bit data. A standard set of ALU conditions can be tested for conditional operations, branches, and subroutine calls. This allows the processor to perform as a powerful 16/32-bit microprocessor for logical and control applications.

Two addressing units support high-speed register-indirect memory addressing with post-modification of the register. Direct and immediate addressing is supported at a cost of only one additional instruction cycle and ROM location. Four address registers in the YAAU (r0—r3) can be used for either read or write addresses to the RAM without restrictions. Registers j and k provide user-defined post-increments for the addresses. Fixed increments of 0, +1, −1, and +2 are also available. The YAAU also supports a flexible modulo addressing mode for efficient filter implementations. Registers rb and re are used to define the beginning and end of the modulo. Four compound addressing modes are provided to make read/write operations more efficient. In the XAAU, one register (pt) is used for ROM table look-up. Register i holds a user-defined post-increment. A fixed post-increment of +1 is also available. Register pc is the program counter. Registers pr and pi hold the return address for subroutine calls and interrupts.

The on-chip memory includes 4096 bytes of ROM organized as 2048 × 16 and 1024 bytes of RAM organized as 516 × 16. The ROM can be replaced with up to 64 Kwords of external memory for prototyping or for applications that require frequent program modification.

An on-chip cache memory can be selectively used to store repetitive operations such as those found in a filter section. Up to 15 words in the cache can be repeated up to 127 times with no looping overhead. In addition, operations in the cache that require a ROM access (for example, fixed coefficients) will execute at twice the normal rate. The cache greatly reduces the need for writing repetitive code "inline" and therefore conserves ROM storage.

The DSP16 device has both serial and parallel I/O ports. The serial I/O unit is an asynchronous, full duplex, double-buffered channel operating at up to 10 Mb/s that easily interfaces with other DSP16 devices in a multiple DSP16 environment. AT&T codecs and time division multiplex (TDM) channels can be interfaced to the DSP16 device with few (if any) additional components. The parallel I/O unit is capable of interfacing to a 16-bit bus containing other DSP16 devices, microprocessors, or peripheral I/O devices. Data rates of up to 145.5 Mb/s are possible through this port.

Features

- 36.4 MHz version (55 ns)
- 26.6 MHz version (75 ns)
- MIL-STD 883 version (75 ns)
- Low-power CMOS technology
- Two 36-bit accumulators
- 16 × 16 multiply and 86-bit addition in 55 ns
- Instruction cache for high-speed, ROM efficient vector operations
- 2048-word ROM, 512-word RAM (on-chip)
- Off-chip ROM expansion to 64 Kword
- Serial and parallel I/O ports with multi-processor capability
- Five maskable interrupts
- Single +5 V power supply
- Supported by *WE* DSP16 Support Software Library and *WE* DSP16 Digital Signal Processor Development System

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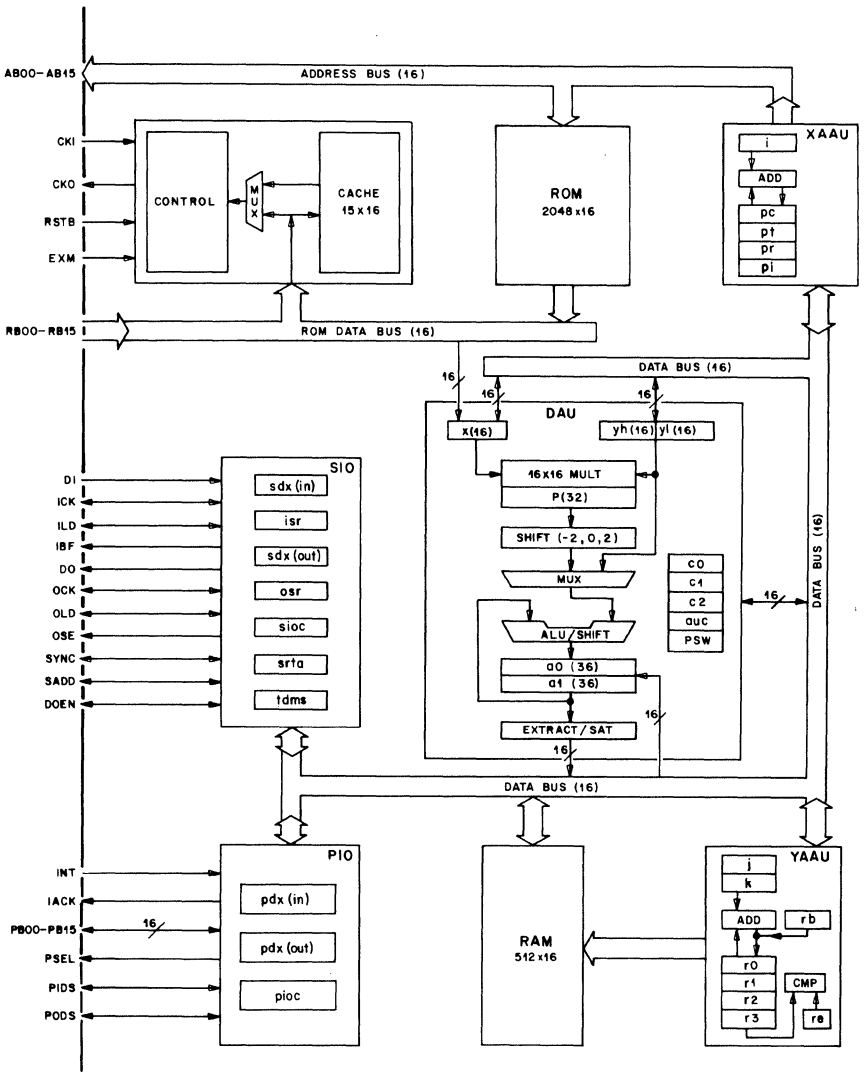
Figure 1. DSP16 Block Diagram



16 x 16 Mult	16-bit by 16-bit Multiplier
a0—a1	Accumulators 0—1
ADD	Adder
ALU/SHIFT	Arithmetic Logic Unit/Shifter
auc	Arithmetic Unit Control
c0—c2	Counters 0—2
CMP	Comparator
DAU	Data Arithmetic Unit
i	Increment Register
isr	Input Shift Register
j	Increment Register
k	Increment Register
MUX	Multiplexer
osr	Output Shift Register
p	Product Register
pc	Program Counter
pdx(in)	Parallel I/O Data Transmit Input Register
pdx(out)	Parallel I/O Data Transmit Output Register
pi	Program Interrupt Register
PIO	Parallel I/O Unit
pioc	Parallel I/O Control Register
pr	Program Return Register
psw	Processor Status Word
pt	ROM Table Pointer
r0—r3	RAM Pointer Registers 0—3
RAM	Read/Write Memory
rb	Modulo Addressing Register
re	Modulo Addressing Register
ROM	Read-Only Memory
sdx(in)	Serial Data Transmit Input Register
sdx(out)	Serial Data Transmit Output Register
SIO	Serial I/O Unit
sioc	Serial I/O Control Register
srta	Serial Receive/Transmit Address Register
tdms	Serial I/O Time Division Multiplex Signal Control Register
x	Multiplier Input Register
XAAU	ROM Address Arithmetic Unit
YAAU	RAM Address Arithmetic Unit
yh	y(high) DAU Register
yl	y(low) DAU Register

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WE® DSP16A Digital Signal Processor

Description

The DSP16A Digital Signal Processor integrated circuit is a 16-bit, high-speed, programmable digital signal processor. The device is fabricated in low-power CMOS technology and is packaged in an 84-pin plastic leaded chip carrier. A military qualified version is available in a 13 x 13 pin PGA package. It is a general-purpose building block that can be programmed to perform a wide variety of signal processing functions. It achieves high throughput with its parallel pipelined architecture without programming latencies or restrictions. The processor has an arithmetic unit capable of multiplying two 16-bit words of data and accumulating the product in a single 33 ns cycle. The arithmetic data is supplied by two independent addressing units. The DSP16 device can function in a stand-alone manner, requiring only an external clock.

Architectural Summary

The DSP16A device contains a data arithmetic unit (DAU) that performs signal processing arithmetic; a ROM address arithmetic unit (XAAU); a RAM address arithmetic unit (YAAU); a 4096 by 16-bit ROM that contains program instructions and fixed data; a 2048 by 16-bit RAM for variable data; an instruction cache (CACHE); a serial I/O unit (SIO); and a 16-bit parallel I/O unit (PIO).

The arithmetic unit contains a 16 × 16 bit parallel multiplier that generates a full 32-bit product in 33 ns. The product can be accumulated with one of two 36-bit accumulators. The data in these accumulators can be directly loaded from or stored to memory in two 16-bit words with automatic saturation on overflow. The ALU supports a full set of arithmetic and logical operations on either 16- or 32-bit data. A standard set of ALU conditions can be tested for conditional operations, branches, and subroutine calls. This allows the processor to perform as a powerful 16/32-bit microprocessor for logical and control applications.

Two addressing units support high-speed register-indirect memory addressing with post-modification of the register. Direct and immediate addressing is supported at a cost of only one additional instruction cycle and ROM location. Four address registers in the YAAU (r0—r3) can be used for either read or write addresses to the RAM without restrictions. Registers j and k provide user-defined post-increments for the addresses. Fixed increments of 0, +1, −1, and +2 are also available. The YAAU also supports a flexible modulo addressing mode for efficient filter implementations. Registers rb and re are used to define the beginning and end of the modulo. Four compound addressing modes are provided to make read/write operations more efficient. In the XAAU, one register (pt) is used for ROM table look-up. Register i holds a user-defined post-increment. A fixed post-increment of +1 is also available. Register pc is the program counter. Registers pr and pi hold the return address for subroutine calls and interrupts.

The on-chip memory includes 8192 bytes of ROM organized as 4096 × 16 and 4096 bytes of RAM organized as 2048 × 16. The ROM can be replaced with up to 64 Kwords of external memory for prototyping or for applications that require frequent program modification.

An on-chip cache memory can be selectively used to store repetitive operations such as those found in a filter section. Up to 15 words in the cache can be repeated up to 127 times with no looping overhead. In addition, operations in the cache that require a ROM access (for example, fixed coefficients) will execute at twice the normal rate. The cache greatly reduces the need for writing repetitive code "inline" and therefore conserves ROM storage.

The DSP16A device has both serial and parallel I/O ports. The serial I/O unit is an asynchronous, full duplex, double-buffered channel operating at up to 10 Mb/s that easily interfaces with other DSP16 devices in a multiple DSP16 environment. AT&T codecs and time division multiplex (TDM) channels can be interfaced to the DSP16 device with few (if any) additional components. The parallel I/O unit is capable of interfacing to a 16-bit bus containing other DSP16 devices, microprocessors, or peripheral I/O devices. Data rates of up to 240 Mb/s are possible through this port.

Features

- 30.3 MHz version (33 ns)
- Low-power CMOS technology
- Two 36-bit accumulators
- 16 × 16 multiply and 36-bit addition in 55 ns
- Instruction cache for high-speed, ROM efficient vector operations
- 2048-word ROM, 512-word RAM (on-chip)
- Off-chip ROM expansion to 64 Kword
- Serial and parallel I/O ports with multi-processor capability
- Five maskable interrupts
- Single +5 V power supply
- Supported by *WE* DSP16A Support Software Library and *WE* DSP16A Digital Signal Processor Development System

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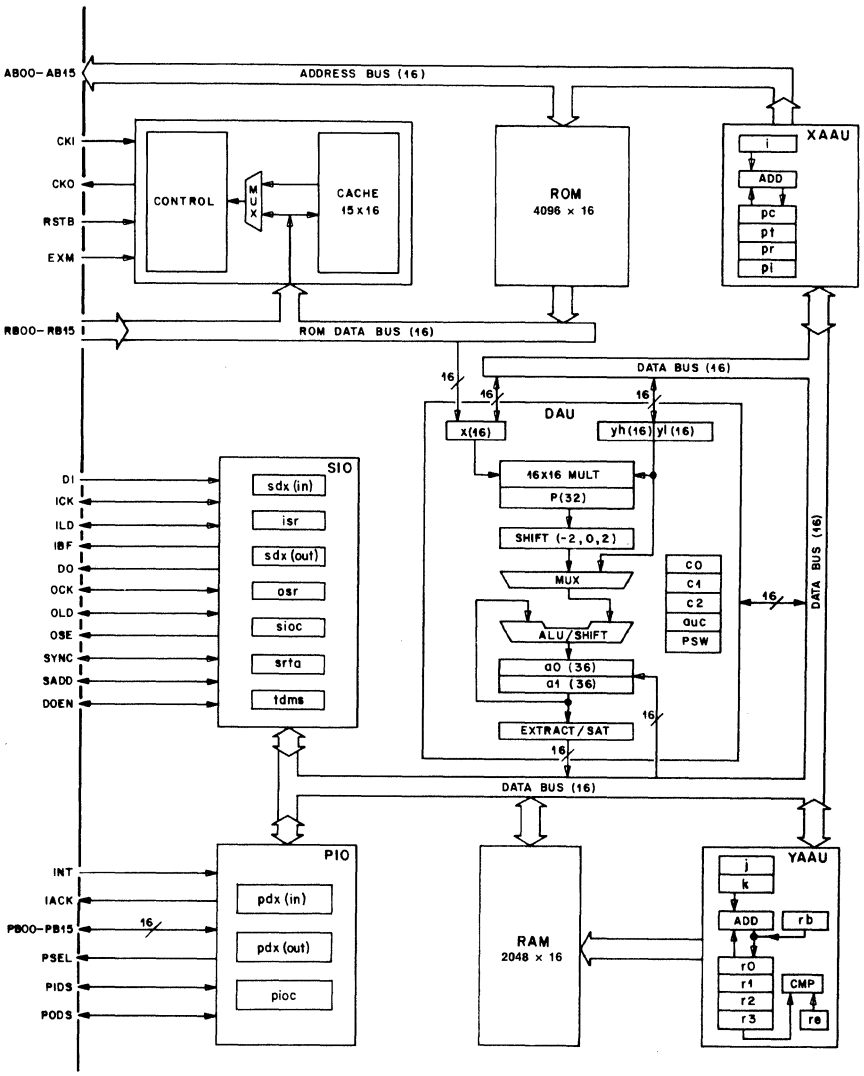
Figure 1. DSP16A Block Diagram



16 x 16 Mult 16-bit by 16-bit Multiplier
a0—a1 Accumulators 0—1
ADD Adder
ALU/SHIFT Arithmetic Logic Unit/Shifter
auc Arithmetic Unit Control
c0—c2 Counters 0—2
CMP Comparator
DAU Data Arithmetic Unit
i Increment Register
isr Input Shift Register
j Increment Register
k Increment Register
MUX Multiplexer
osr Output Shift Register
p Product Register
pc Program Counter
pdx(in) Parallel I/O Data Transmit Input Register
pdx(out) Parallel I/O Data Transmit Output Register
pi Program Interrupt Register
PIO Parallel I/O Unit
pioc Parallel I/O Control Register
pr Program Return Register
psw Processor Status Word
pt ROM Table Pointer
r0—r3 RAM Pointer Registers 0—3
RAM Read/Write Memory
rb Modulo Addressing Register
re Modulo Addressing Register
ROM Read-Only Memory
sdx(in) Serial Data Transmit Input Register
sdx(out) Serial Data Transmit Output Register
SIO Serial I/O Unit
sioc Serial I/O Control Register
srta Serial Receive/Transmit Address Register
tdms Serial I/O Time Division Multiplex Signal Control Register
x Multiplier Input Register
XAAU ROM Address Arithmetic Unit
YAAU RAM Address Arithmetic Unit
yh y(high) DAU Register
yl y(low) DAU Register

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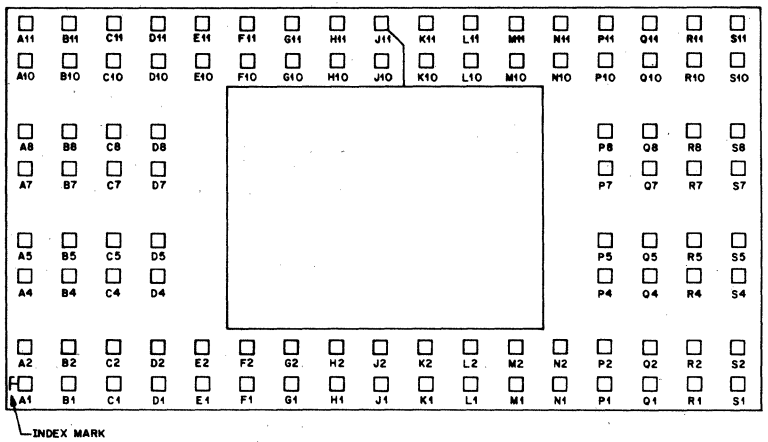
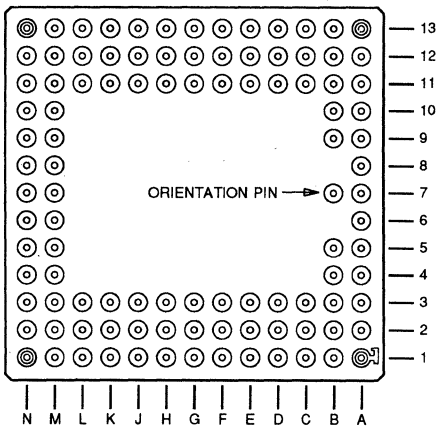
DSP32 Pin Assignments

100-Pin Rectangular PGA Diagram

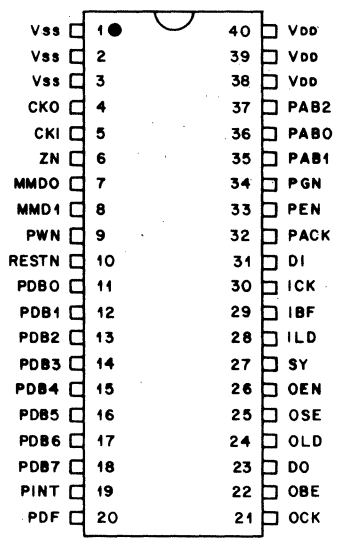


DSP32 and DSP32C Pin Assignments

13 x 13 Square PGA Package



40-Pin DIP



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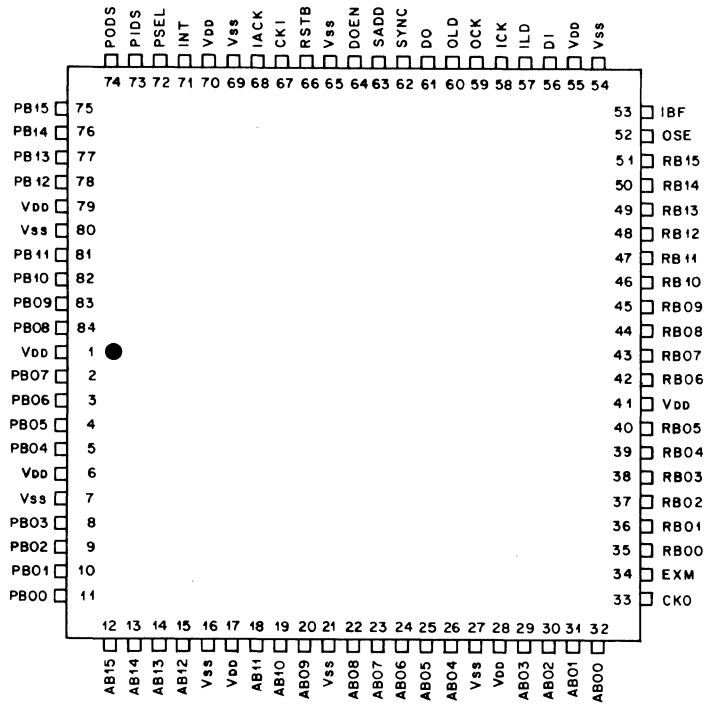
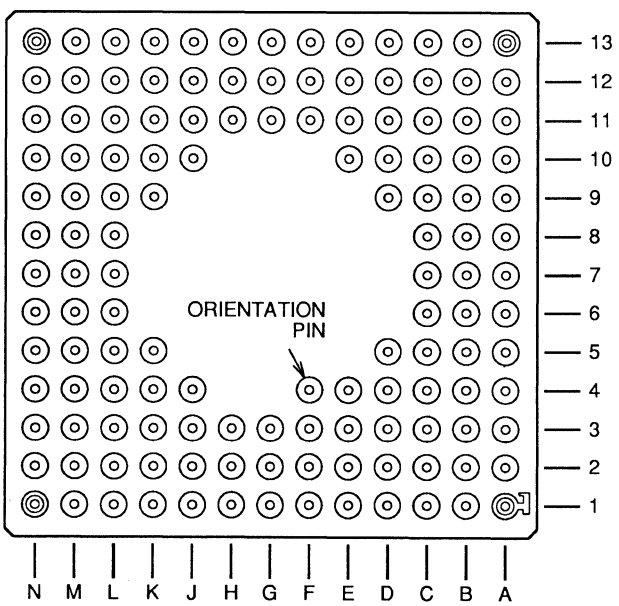
DSP16 and DSP16A Pin Assignments

84-Pin Chip Carrier Diagram



DSP16, DSP16A, and DSP16 Military Version Pin Assignments

13 x 13 Square PGA



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AT&T Digital Signal Processor Family of Devices

Device Type	Tool Type	Speed (ns)	Availability	
			Samples	Production
WE DSP16	M	075	—	Now
		055	—	Now
	R	075	—	Now
		055	—	Now
WE DSP16A	M	075	1Q89	2Q89
		055	1Q89	2Q89
		033	1Q89	2Q89
	R	075	2Q89	3Q89
		055	2Q89	3Q89
		033	2Q89	3Q89
WE DSP32	C	250	—	Now
		160	—	Now
	G	250	—	Now
		160	—	Now
	R	250	—	Now
		160	—	Now
WE DSP32C*	R	100	Now	2Q89
		080	Now	2Q89

Packages: M = Plastic Leaded Chip Carrier
C = Hermetic Ceramic DIP
G = Hermetic Ceramic Rectangular PGA
R = Hermetic Ceramic Square PGA

* These are the CMOS (DSP32C) devices.

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AT&T Digital Signal Processor Family Development Tools

Device Type	Tool Type	O.S./Host*	Availability
WE DSP16	SL	All	Now
	AL	All Except VMS	1Q89
		VMS	TBD
	DS	—	Now
WE DSP16/*WE* DSP16A (Combined Tools)	SL	All Except VMS	4Q88
		VMS	TBD
	AL	All	TBD
WE DSP16A	DS	—	4Q88
WE DSP32	DS	—	Now
WE DSP32/*WE* DSP32C (Combined Tools)	SL	All Except VMS	Now
		VMS	TBD
	CC	All Except VMS	Now
		VMS	TBD
	AL	All	1Q89
WE DSP32C	DS	—	4Q88

* O.S./Host: MS-DOS = *MS-DOS* (AT&T PC6300 and Compatible)
UN5VX = *UNIX* V (VAX 11/780 Series)
UN5B2 = *UNIX* V (3B2 Series)
VMS = *VMS* (VAX 11/780 Series)
UNB42 = *UNIX* Berkeley 4.2 (VAX 11/780 Series)
BKSUN = *UNIX* Berkeley 4.2 (Sun Series)

Media: F
T
F
T
T
C

Media: T = 1600 BPI Magnetic Tape
F = 5¼" DSDD Diskettes
C = 4" × 6" Data Cartridge

Operating Systems Supported:
— *MS-DOS*
— *UNIX* V
— *UNIX* Berkeley 4.2

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INTERFACE

Digital Encryption Processor — T7000A

Description

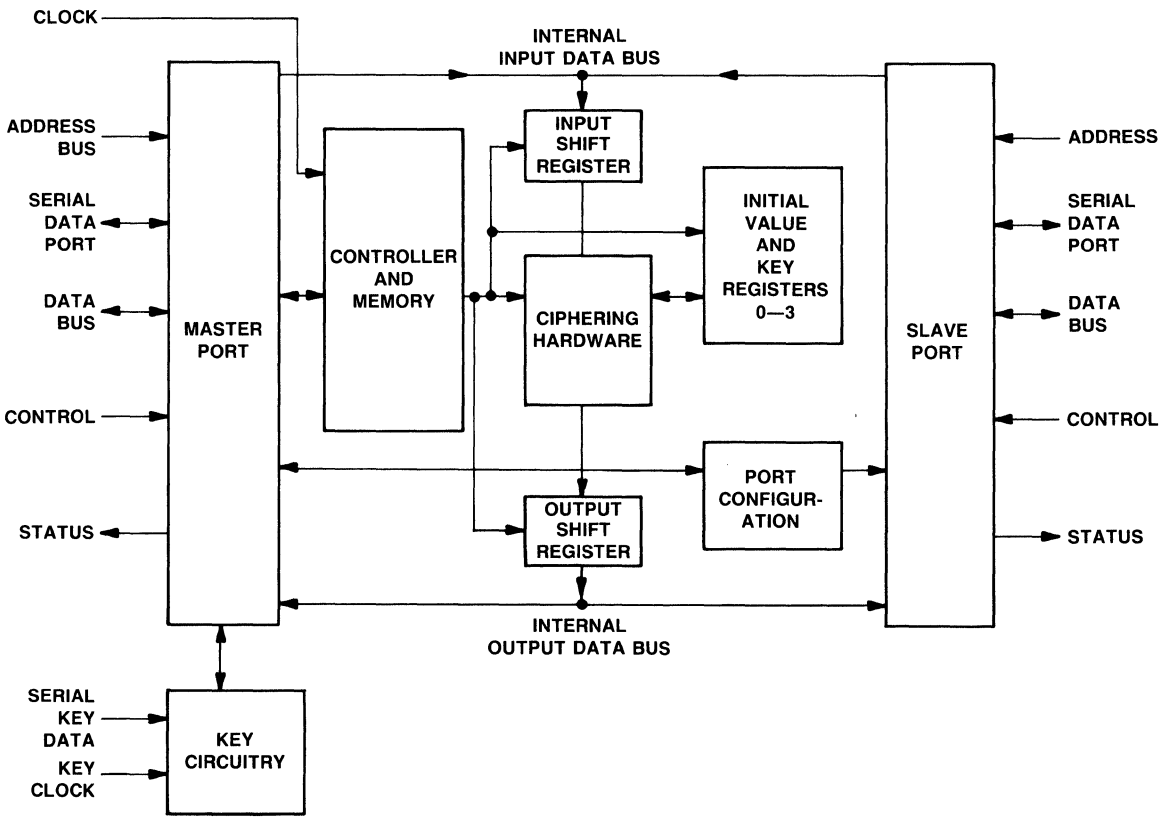
The Digital Encryption Processor (DEP) provides a low-cost, high security cryptographic system for encrypting and decrypting digital signals. It implements the four data encryption standard (DES) modes specified by the National Bureau of Standards (NBS), and is capable of performing multiple encryption operations or multiplexed key and initial value ciphering.

This programmable device provides a ciphering rate of 235,000 operations/second for any of the DES modes. It is manufactured using CMOS technology, requires a single +5 volt supply, and is packaged in a 40-pin plastic DIP.

Features

- Programmable DES ciphering modes
- Programmable multiple or multiplexed ciphering
- On-chip RAM and ROM program memory
- Separate parallel and/or serial plain-text and cipher-text ports
- Separate serial key input port
- Data throughput of 1.882 Mbytes/s using the entire DES output block
- Validated by the NBS

T7000A DEP Block Diagram



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Description

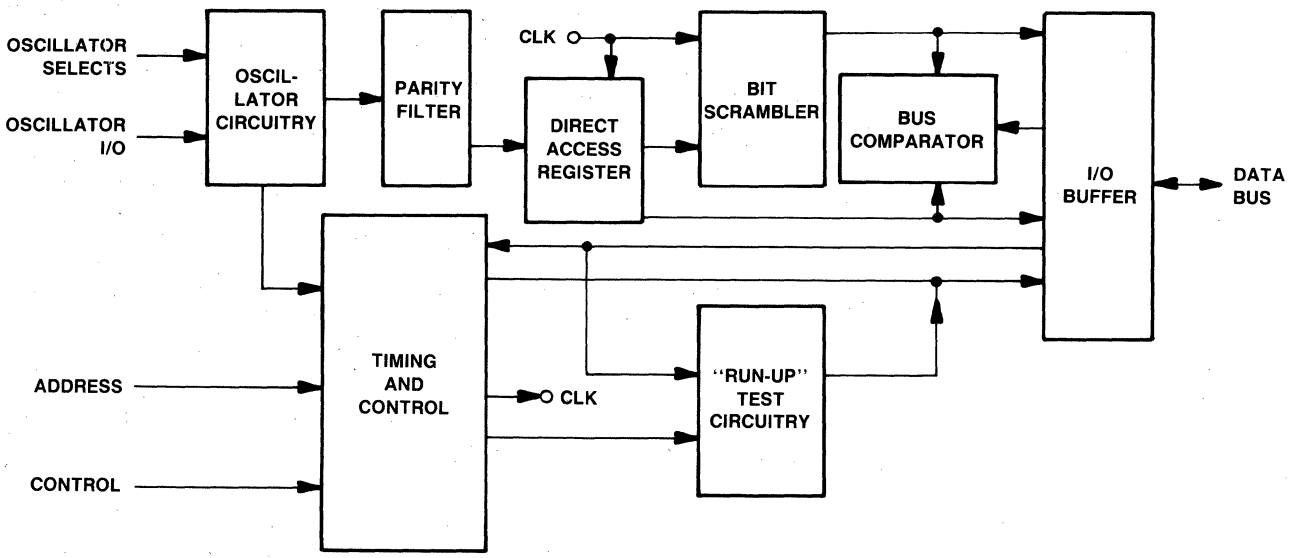
The Random Number Generator (RNG) produces random bits based on the phase jitter of a free-running oscillator. The output data stream of this device is truly random (not pseudorandom). In the data encryption unit, the RNG generates a random number that can be used as a session key.

This device is fabricated in CMOS technology, requires a single +5 volt supply, and is available in a 32-pin plastic DIP.

Features

- On-chip or external HF oscillator source option
- On-chip or external jitter oscillator source option
- Generation of a 536-bit random number available in 8-bit bytes
- Internal elementary randomness check with external access to generated statistics

T7001 RNG Block Diagram



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Description

The T7032 and T7033 Clock Recovery Circuits operate over a 1 MHz to 50 MHz frequency range. The T7032 device provides clock recovery, data retiming, and a polynomial-based descrambler. The T7033 device is similar but without the descrambler and associated output mux. These devices accept TTL-NRZ data from a receiver (optical or electrical), recover the clock, and retime the data to the recovered clock. The inputs and outputs are TTL-compatible and the circuits require a single +5 V supply. The clock recovery circuits are manufactured using CMOS technology and are available in a 300 mil, 20-pin plastic DIP.

Features

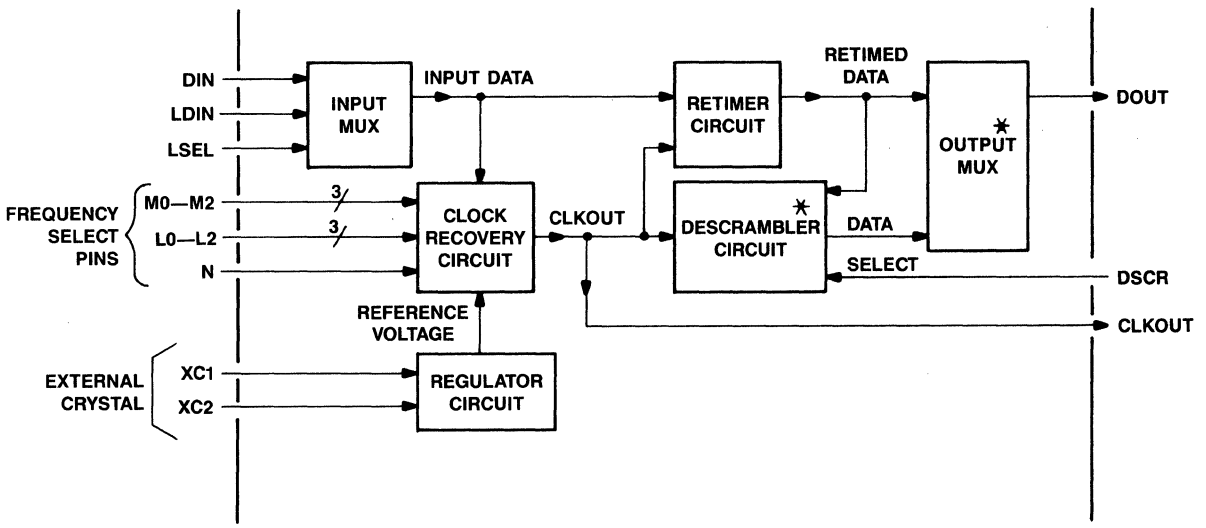
- Pin-programmable for 1 MHz to 50 MHz operation
- Fiber and wire applications
- Single +5 V supply
- Only one external component required: 3.58 MHz crystal

System Applications

The clock recovery circuits are used for a variety of applications:

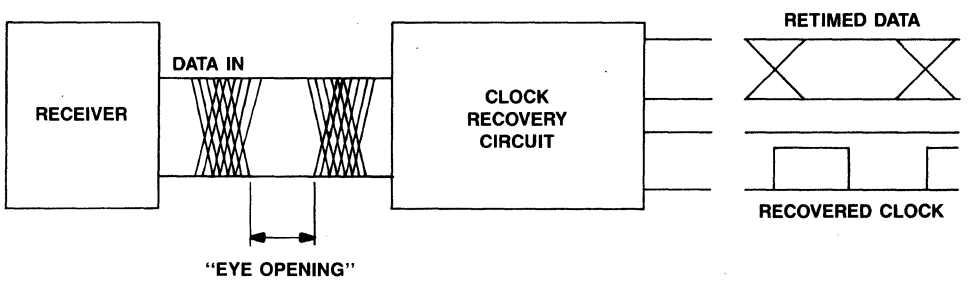
- Optical data links
- Multiplexers
- Digital PBXs
- Cluster concentrators
- Local area networks
- Front end processors
- Terminals and workstations
- Communications test equipment

Clock Recovery Circuit Block Diagram



* The T7033 device does not contain the descrambler or output mux.

Application Diagram



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INTERFACE
X.25 Protocol Controller — T7100A

Description

The T7100A X.25 Protocol Controller, also known as XPC-8, implements the data link control functions defined in the X.25 packet switching communication standard for an 8-bit data bus. The level-2 protocol controller is fabricated using NMOS silicon gate technology, is TTL-compatible, and may be interfaced with an 8-bit microprocessor. It is available in a 48-pin nonhermetic ceramic DIP.

Features

- DMA with standard interface including DMA request, DMA acknowledge, DMA read, and DMA write
- Programmable timers and window size
- Serial data rate of 250 kb/s
- Wait-state generator (on DMA side) for slow memory
- Two independent test modes to verify the XPC-8 and its link

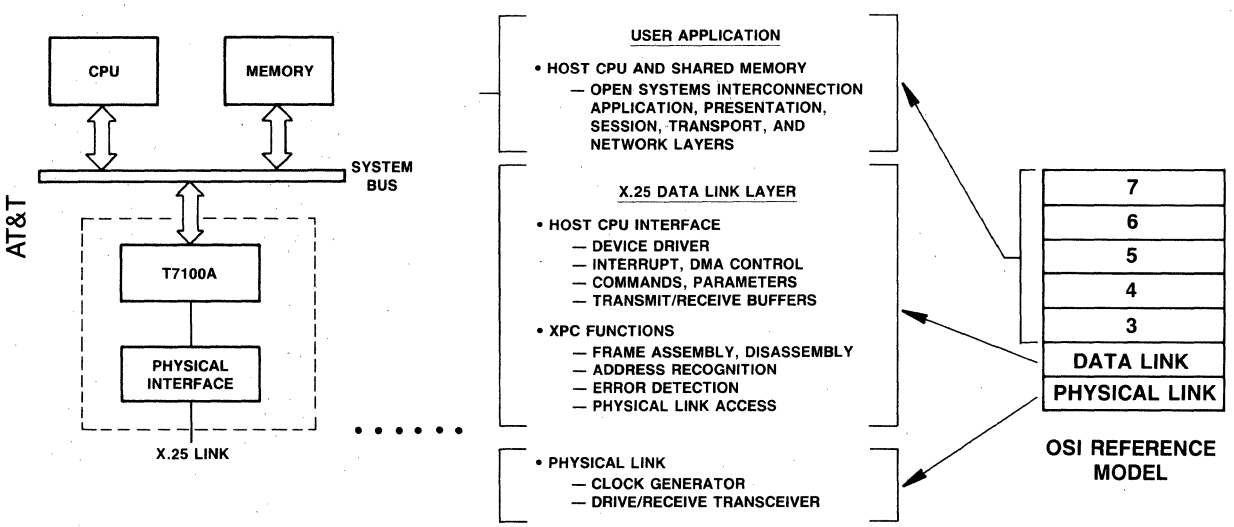
System Applications

The X.25 Protocol Controller provides a building block for data communications in a packet switching environment.

The XPC-8 transmits and receives frames using the X.25 packet switching network access protocol. (A frame is defined as a block of information transferred over an access link.) It implements level 2 link interface, so minimum intervention by the central processing unit (CPU) is needed when sending and receiving frames.

In this common bus application, the XPC-8 is used as a peripheral off the main system bus. The diagram also indicates the mapping between the seven X.25 levels and defines which functions are performed and where they are performed.

XPC-8 Typical Application Diagram (with Mapping)



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X.25/X.75 Protocol Controller — T7102A

Description

The T7102A XPC device satisfies the X.25 link layer (level 2) requirements for a balanced link access procedure (LAPB) for data interchange over a synchronous full-duplex serial data link. This device also implements X.75 level 2 protocol used in inter-network applications. It is bit-oriented with a maximum transmit and receive speed of 333 kb/s. A set of programmable registers control and record vital events during data transmission.

This single-chip LSI device, available in a 70-pin pin-grid-array package, is fabricated using NMOS silicon gate technology.

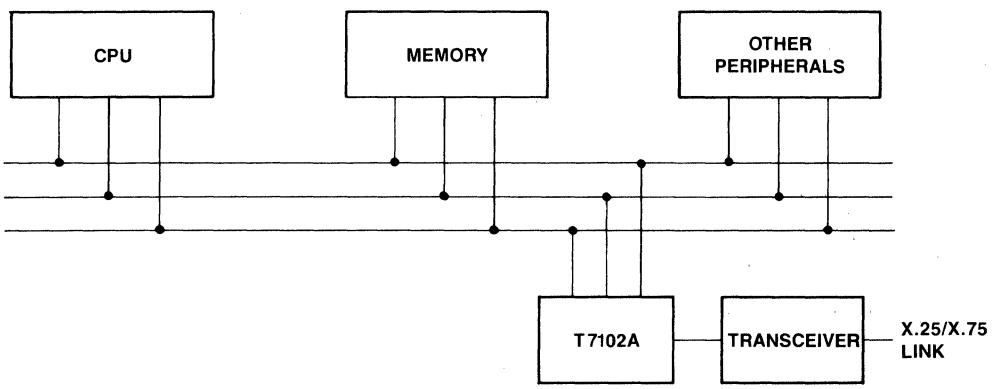
Features

- 24-bit address bus to address 16-Mbyte address space
- Dual-channel DMA with standard interface including DMA request, DMA acknowledge, DMA read, and DMA write
- Independently programmable timers, retransmission counter, window size (transmit and receive), and Modulo 8 or 128 frame sequence numbering
- Daisy chain DMA for priority-controlled CPU interface
- Event counters and registers
- Supports 8-bit or 16-bit data buses

System Applications

As with the other protocol controllers, the T7102A Protocol Controller is used for transmitting and receiving, and interpreting information between system elements. In addition, this device can read and write memory using either Intel or Motorola data byte ordering convention. Shown in the diagram below is an example of the XPC used in a common bus application.

XPC Common Bus Application Diagram



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INTERFACE

Synchronous Protocol Data Formatter with Serial Interface — T7110

Description

The T7110 Synchronous Protocol Data Formatter with Serial Interface (SPYDER-S) is a synchronous packet data communications controller. It is used to interface physical link level lines using bit-synchronous (HDLC/SDLC) protocols to 16-bit and 32-bit microprocessor systems. All inputs and outputs are TTL-compatible. The device is fabricated using CMOS technology, requires a single +5 volt power supply, and is packaged in a 68-pin plastic leaded chip carrier (PLCC).

Features

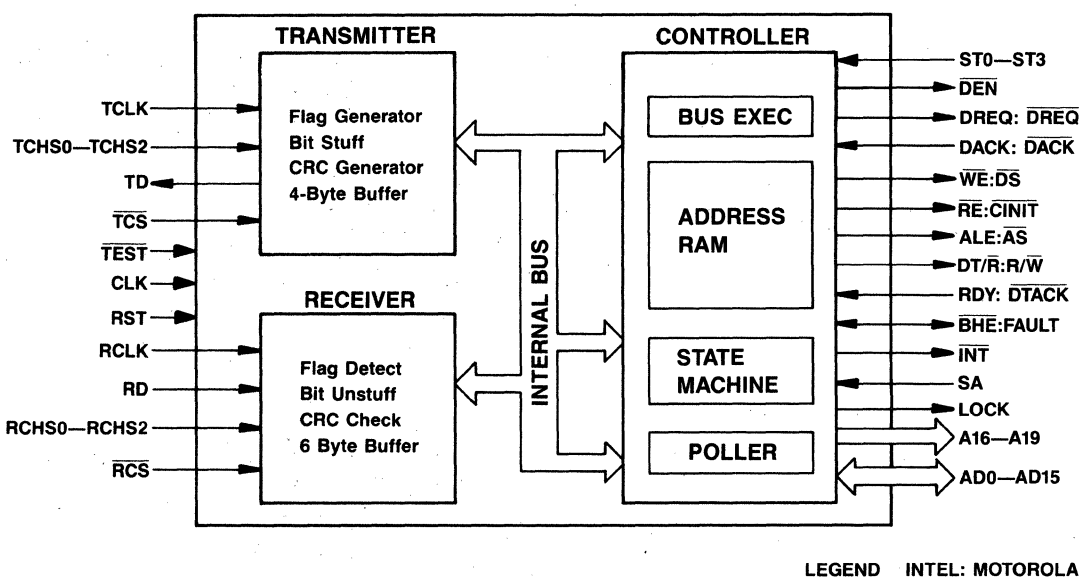
Host Interface

- Compatible with iAPX86, MC68000, or *WE*® 32100 Microprocessor systems
- On-chip 16-channel DMA memory address generator and buffer management with a 4 Mbyte/s maximum transfer rate
- Software register interface for maximum flexibility

Serial Interface

- 8-channel multiplexed serial input/output
- Automatic flag transmission and detection
- Zero bit insertion and deletion
- CRC generation and checking
- 2 Mb/s continuous serial data rate, 4 Mb/s instantaneous data rate

T7110 SPYDER-S Block Diagram



LEGEND INTEL: MOTOROLA

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(Preliminary) Synchronous Packet Data Formatter — T7111A

Description

The T7111A Synchronous Packet Data Formatter (ANT) integrated circuit is used to interface serial data link level lines, which use HDLC bit-synchronous protocol, to 8-bit microprocessor or microcontroller systems. All inputs and outputs of the T7111A ANT are TTL-compatible. It is implemented using CMOS technology and requires a single 5 V supply. The device is available in a 28-pin plastic DIP or small-outline J-lead (SOJ) package.

Features

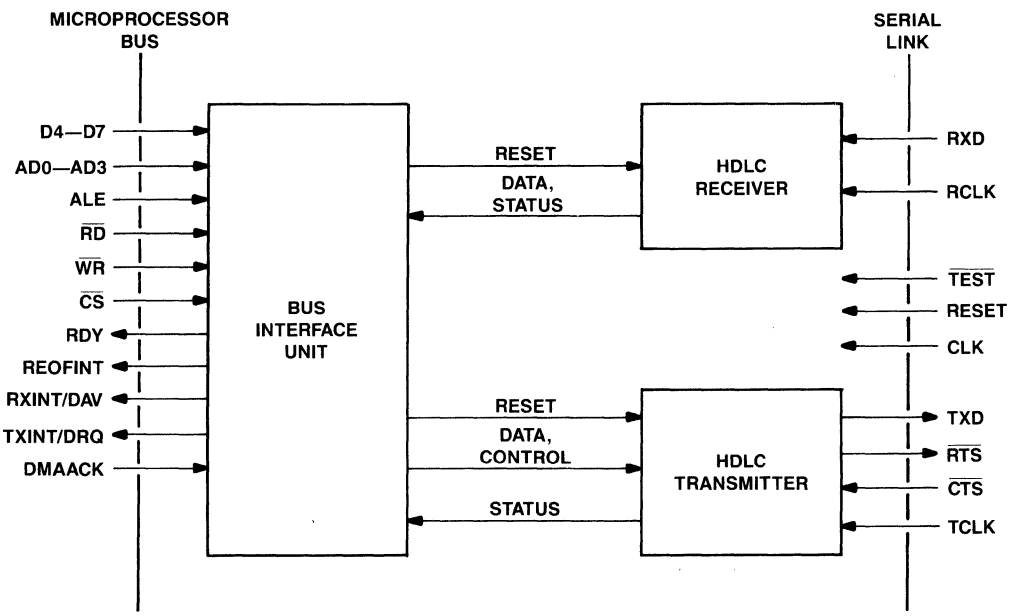
Host Interface

- Compatible with 8088 and 80188 microprocessor-based systems and 8051 microcontroller
- Compatible with 8237 and 8257 DMA controllers in extended write mode
- Simple register control interface
- Wait-state initiator (80188)
- Receiver end-of-frame interrupt
- Programmable receive and transmit queue interrupts with variable fill levels
- Programmable receive and transmit DMA requests with variable fill levels

Serial Link Interface

- Full-duplex serial receive and transmit data lines
- Separate receive and transmit clocks
- 4 Mb/s maximum data rate
- 7-byte receive queue
- 4-byte transmit queue
- Programmable request-to-send/clear-to-send handshaking
- Near- and far-end loop test modes
- Automatic flag transmission and detection
- Data metering via programmable interframe spacing
- Zero bit insertion and deletion for data transparency
- CRC-CCITT 16-bit polynomial generation and check with inhibit option
- Abort/idle detection and transmission
- Detection of transmitter underrun and receiver overrun
- Optional inversion of serial bit streams

T7111A Synchronous Packet Data Formatter Block Diagram



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INTERFACE

Asynchronous Receiver/Transmitter Interface — T7112

Description

The T7112 ARTI is an asynchronous, single-channel, full-duplex receiver/transmitter interface for terminals and modems. The ARTI is compatible with the bus protocol and timing specifications of both the 8051 microcontroller and the 8088 microprocessor. It may be used in a polled or interrupt driven system. The transmitter is quadruple buffered and the receiver has six buffers to reduce the interrupt overhead and the potential for overruns. The device is implemented in low-power, CMOS technology and is available in a 24-pin plastic DIP or a 28-pin plastic SOJ surface-mount package.

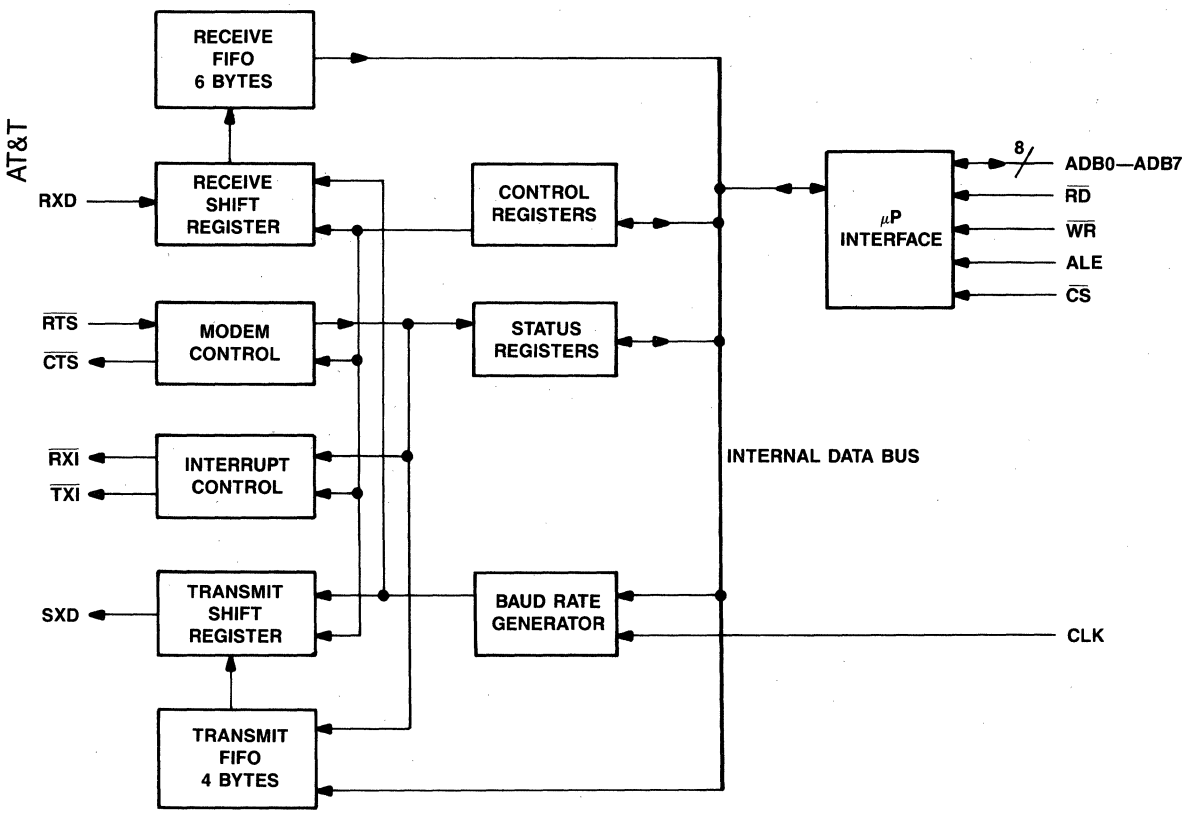
Features

- Programmable data format:
  - — Seven data bits plus parity
  - — Odd, even, no parity
  - — One or two stop bits
- Six receive and four transmit data buffers
- 8088 (8 MHz) and 8051 (16 MHz) microprocessor interface without wait states
- Clear-to-send/request-to-send selectable signals for DTE or DCE modes and flow control
- Programmable interrupt systems:
  - — Full level interrupt of receive FIFOs (first-in, first-out)
  - — Receive break detection and error interrupt
  - — Empty level of transmit FIFO and error interrupt
- Transmit/receive FIFO status bits indicate FIFO levels
- Flexible polling capabilities
- On-chip baud rate generator
- Speedmatching (autobaud capability)

System Application

As an asynchronous interface to customer terminals or modems, the ARTI provides standard UART functions with additional data buffering. In the illustrations below, the ARTI is used with EIA drivers and receivers to interface with data communications equipment (DCE) and with data terminal equipment (DTE).

T7112 ARTI Block Diagram



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(Advance) Synchronous Protocol Data Formatter — T7115

Description

The T7115 Synchronous Protocol Data Formatter (SPYDER-T) integrated circuit is a synchronous packet data communications controller device. All inputs and outputs of the T7115 SPYDER-T are TTL-compatible. The device is fabricated using CMOS technology, requires a single 5 V supply, and is available in a 68-pin plastic chip carrier.

Features

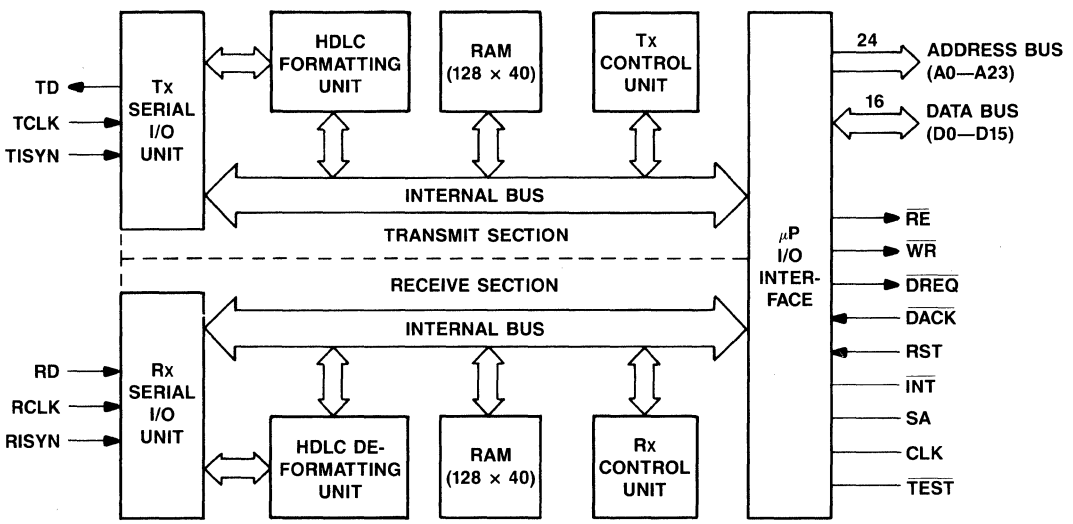
Serial Port Interface

- 32-channel (full-duplex) multiplexed serial input/output supports T1/DS1 24-channel and CEPT 32-channel modes
- Automatic flag transmission and detection
- Flag stuffing up to 2047 flags
- Flag adjustment for the synchronous rate adaption
- Full, partial, or no CRC generation and checking
- Zero bit insertion and deletion
- Abort/idle detection and transmission
- Short and long frame detection
- 2-Mb/s continuous serial data rate
- Dynamic channel allocation (or channel concatenation) supports DS0, H0, H11, and H12 channels
- Bit-rate control on each channel
- Channel inversion
- Transparent mode (no protocol) supports ECMA 102 and CCITT I.463 RA2 rate adaption standards
- Loopback mode
- DMA CRC for relay mode

Microprocessor Interface

- Compatible with 16-bit or 32-bit microprocessor systems
- On-chip 64-channel DMA memory address generator and buffer manager
- Nonmultiplexed 16-bit data and 24-bit address (16 Mbytes) buses
- Transmit and receive buffers accessible through memory-mapped look-up tables
- Interrupt queue (up to 4096 interrupts)

SPYDER-T Simplified Block Diagram



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(Preliminary) Multi-Port Repeater Unit Controller — T7200

Description

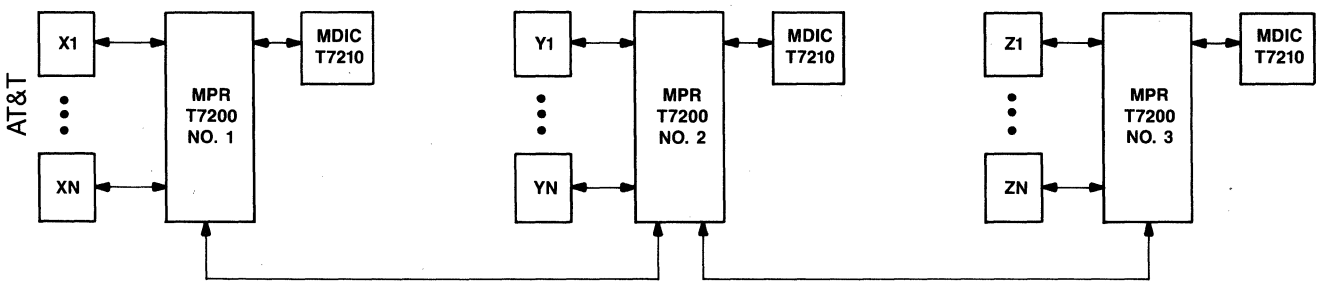
The T7200 Multi-Port Repeater Unit Controller (MPR) integrated circuit is a VLSI device that simplifies the design and implementation of a twisted-pair compatible multi-port repeater for use in 10BASE5 and 10BASE2 networks. Used with a single MDIC integrated circuit, the repeater unit provides the functions necessary for the repeater set. These functions include APG to minimize bit loss, lockup, and auto-partitioning jabber timing to isolate network failures. Additional functions of the T7200 MPR include minimum frame length enforcement (MFE) to eliminate packet fragments, Manchester encoding of transmitted data, automatic address generation to disable transmission to the active port, a facility for providing traffic, jam, lockup, and auto-partition status via LED indicators.

In addition to the basic functions, the repeater unit provides external retiming using a commercially available FIFO and selectable FIFO fill level for both the internal and external FIFOs. The T7200 MPR is fabricated using 1.25 μm CMOS technology and requires a single +5 V supply. The device is available in a 68-pin plastic leaded chip carrier (PLCC) and all the inputs and outputs are TTL compatible.

Features

- Functionally conforms to IEEE 802.3 CSMA/CD specifications
- 12-port repeater: 11 twisted-pair, 1 AUI
- Automatic preamble generation (APG) to minimize bit loss
- Manchester encoding of transmitted data
- Jabber function isolates network failures (auto partition)
- Jam signal generation
- Minimum frame length enforcement (MFE) for 96 bits
- External collision assert input: AUI port only
- Input protection (blinder) at end of transmission: 8 bit-times
- Supports internal or external FIFO (74ALS232A compatible) via pin select
- Pin selectable FIFO fill level
- Traffic status LED output control
- Jam status LED output control
- Per port Jabber status LED output control
- FIFO error status LED output control

Data Flow Through 10 Mb/s MPRs



Notes:
X1—XN, Y1—YN, and Z1—ZN are users on the local area network.
All MPRs are equal.

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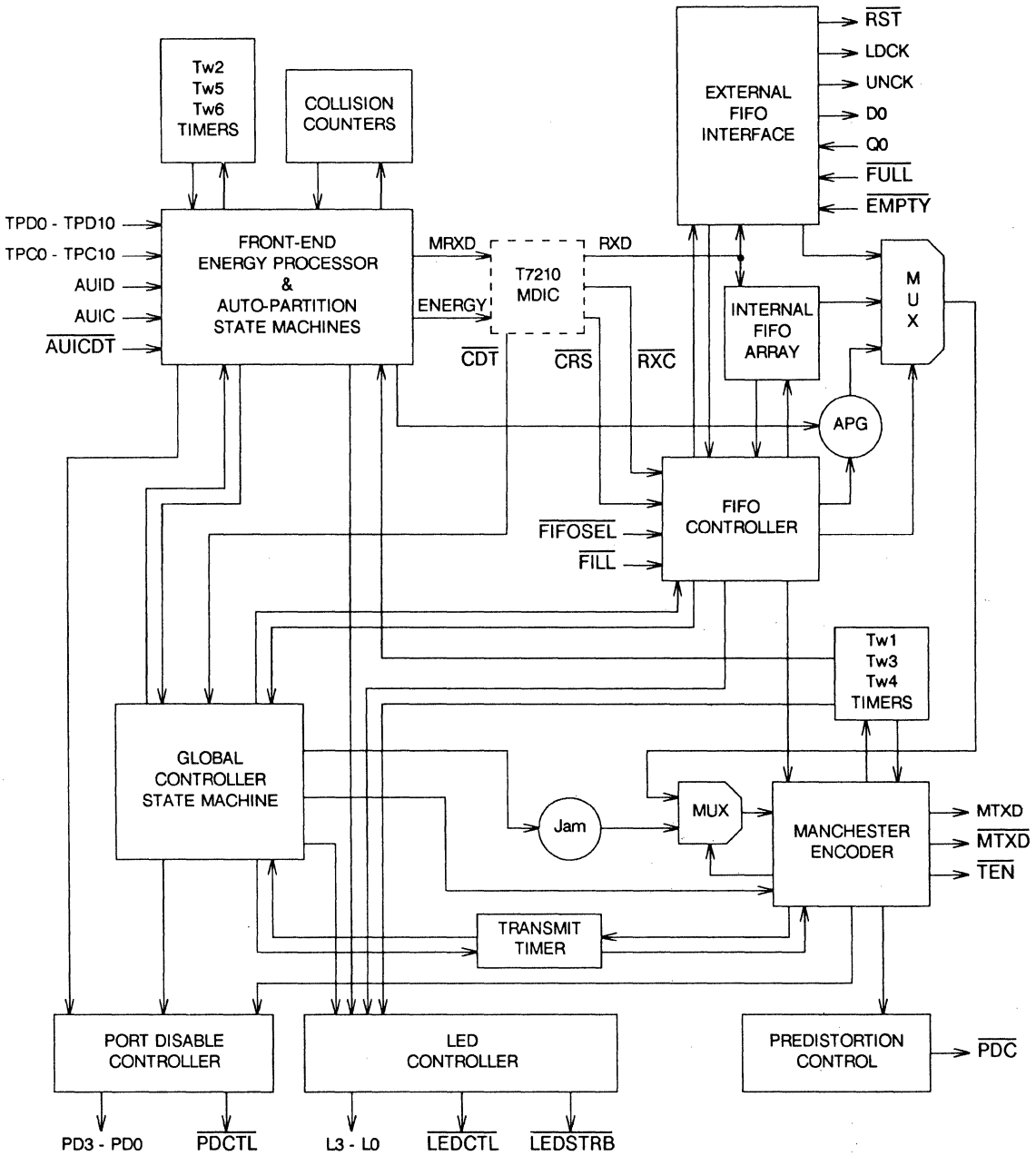
T7200 Multi-Port Repeater Block Diagram



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(Preliminary) Manchester Decoder and Interface Chip (MDIC) — T7210

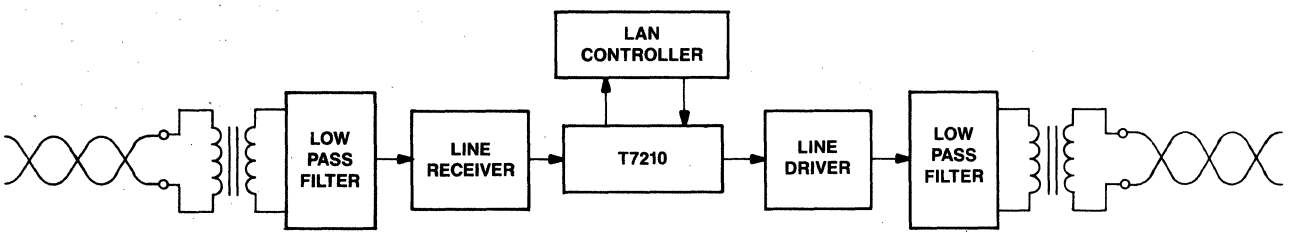
Description

The T7210 Manchester Decoder and Interface Chip (MDIC) is a general purpose VLSI device that provides 10 Mb/s Manchester decoding and interfacing functions. The device recovers and decodes 10 Mb/s serial Manchester data from a line receiver and produces NRZ data and clock signals for the controller chip. The T7210 MDIC detects Manchester code violations and reports these to the controller. The transmitter control section of the MDIC provides a predistortion signals to prevent line over-charge. The device provides essential functions for the high-speed StarLAN-10 stations, repeaters, and any LAN applications based to 10 Mb/s Manchester-coded data format. The T7210 MDIC is fabricated using 1.5 μm linear CMOS technology and is available in a 24-pin plastic DIP.

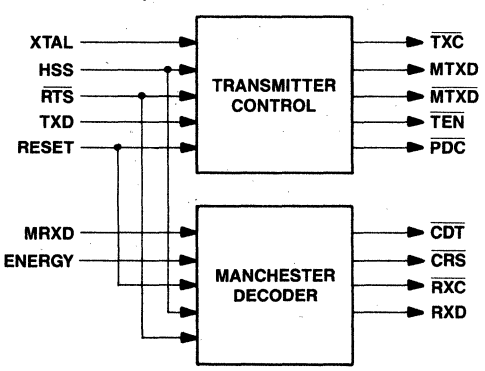
Features

- Conforms with IEEE 802.3 10BASE-T proposed standards
- Contains precision timing elements controlled by a delay-locked loop
- Detects end-of-packet delimiter (IDL)
- Detects Manchester code violations
- Recovers data and clock signals from incoming 10 Mb/s Manchester data
- Decodes the recovered Manchester data into NRZ form
- Interfaces to Intel 82586 LAN Controller
- Designed for 10BASE-T station or repeater

T7210 Application Diagram



T7210 MDIC Block Diagram



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INTERFACE

User Network Interface for Terminal Equipment — T7250A

Description

The T7250A User Network Interface for Terminal Equipment (UNITE) provides the line interface in terminal equipment used for basic access service offered by the Integrated Services Digital Network (ISDN). The device conforms to the CCITT Recommendation I.430 for point-to-multipoint configurations. Priority, contention resolution, multiframing, and activation/deactivation processes are fully supported. Impedance and voltage requirements for recommendation I.430 can be met with a simple line interface circuit. An HDLC formatter and a sophisticated queue manager are provided to simplify the D-channel interface.

The T7250A device is manufactured using CMOS technology and is available in either a 40-pin plastic DIP or 44-pin plastic leaded chip carrier. The 44-pin chip carrier provides two features that the 40-pin DIP package does not: a 16-kHz or an 8-kHz clock and a 6.144-MHz or 192-kHz system clock. The T7250A device uses a 5 V supply and has a nominal power consumption of 35 mW.

Features

- Supports CCITT Recommendation I.430 for ISDN Basic Access (2B+D) at the S/T reference point in terminal equipment
- Supports S- and Q-channel multiframing
- Built-in deeply buffered HDLC formatter for D channel
- Interchangeable B channels
- Optional B-channel inversion
- Power-up reset
- Programmable 0.127 second—2.032 second multifunction timer
- Local and remote loopback test modes
- All outputs are 3-statable
- Parallel microprocessor interface with separate address and data leads, programmable interrupt polarity, and maskable interrupts
- Programmable clock and synchronization signals allow for interfacing with codecs, HDLC controllers, and rate adapters
- Transmitter and receiver each interface to a 2.5:1 transformer
- TTL/CMOS-compatible I/O
- Crystal or clock input acceptable — no external circuitry required for crystal

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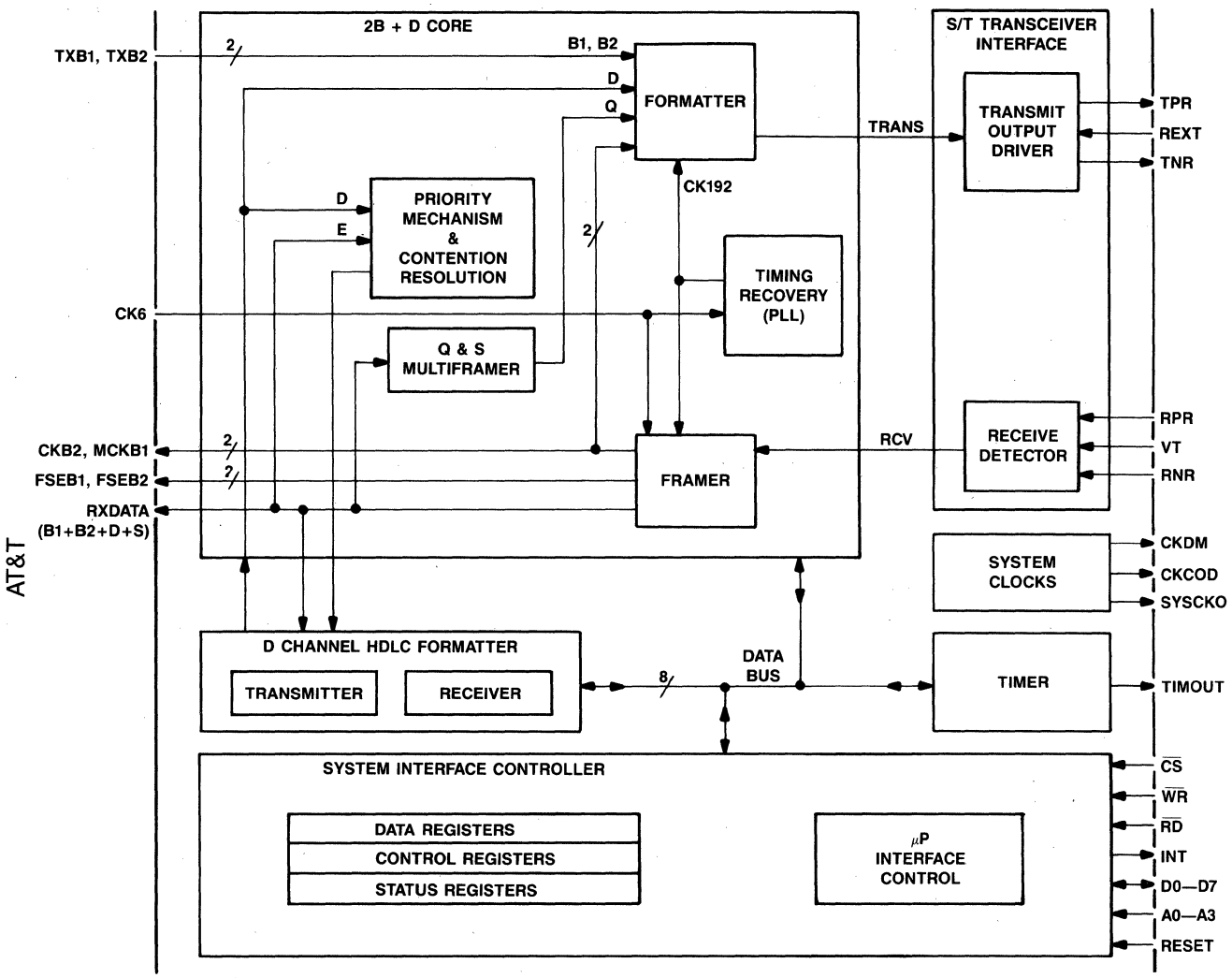
T7250A UNITE Block Diagram



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INTERFACE

(Preliminary) User Network Interface Termination for Switches — T7252A

Description

The T7252A User Network Interface Termination for Switches (UNITS) is a silicon integrated circuit that provides the user with level 1 network termination (NT) functions in the Integrated Services Digital Network (ISDN). The UNITS device provides full-duplex 2B+D communication at 192 kb/s over a 4-wire digital subscriber loop. Channels B1 and B2 are 64-kb/s voice or data channels, and the D channel is a 16-kb/s control or data channel. All point-to-point and point-to-multipoint (passive bus) configurations are supported as defined in the 1986 version of CCITT Recommendation I.430 and the November, 1986, Draft US Specification for the Basic Rate Interface Physical Layer. The T7252A UNITS communicates with a switching network over a user-configured time-division multiplexed (TDM) highway called the concentration highway. A generic microprocessor interface is also provided.

The T7252A UNITS is manufactured using low-power 1.25-micron CMOS technology and is available in either a 44-pin plastic leaded chip carrier or a 40-pin plastic DIP. The T7252A UNITS uses a 5 V power supply and has a maximum power consumption of less than 100 mW.

Features

- 4-wire 192-kb/s line interface for point-to-point and point-to-multipoint (passive bus) arrangements at the ISDN S/T reference point
- CCITT Recommendation I.430 basic access B1, B2, and D (2B+D) channels separated from and combined into 192-kb/s stream
- Two transmit/receive serial highways with assignable time slots for voice or data transfer
- Programmable offset and edge-selection bits for organization of serial highways
- Compatible with AMD and Intel dual PCM highways for configurations requiring 32 or 64 time slots
- Selectable speeds on serial highways: 256 kHz (4 time slots) to 4.096 MHz (64 time slots)
- Fully adaptive timing for the analog receiver in all link configurations, with automatic level switching between two sampling thresholds
- Parallel microprocessor interface with either multiplexed or demultiplexed address/data lines and maskable interrupts
- All digital input/outputs are TTL-compatible (except the two crystal inputs)
- Memory-mapped registers to control time-slot assignment, activation/deactivation, 14 local/remote loopback modes, and interrupts
- Capability of direct microprocessor control of the B1, B2, or D channel through the microprocessor interface
- On-chip digital divider for 192-kHz clock derivation from a user-supplied 6.144-MHz clock, crystal, or CMOS oscillator
- Supports multiframing for S- and Q-channel operation
- Power-down mode of operation with less than 25-mW power dissipation
- High-impedance outputs for board-level testing

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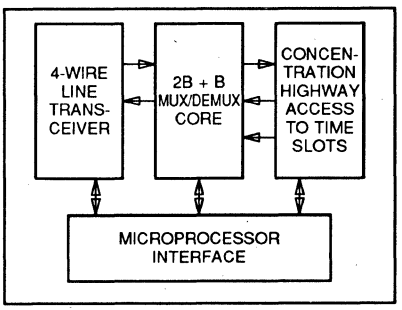
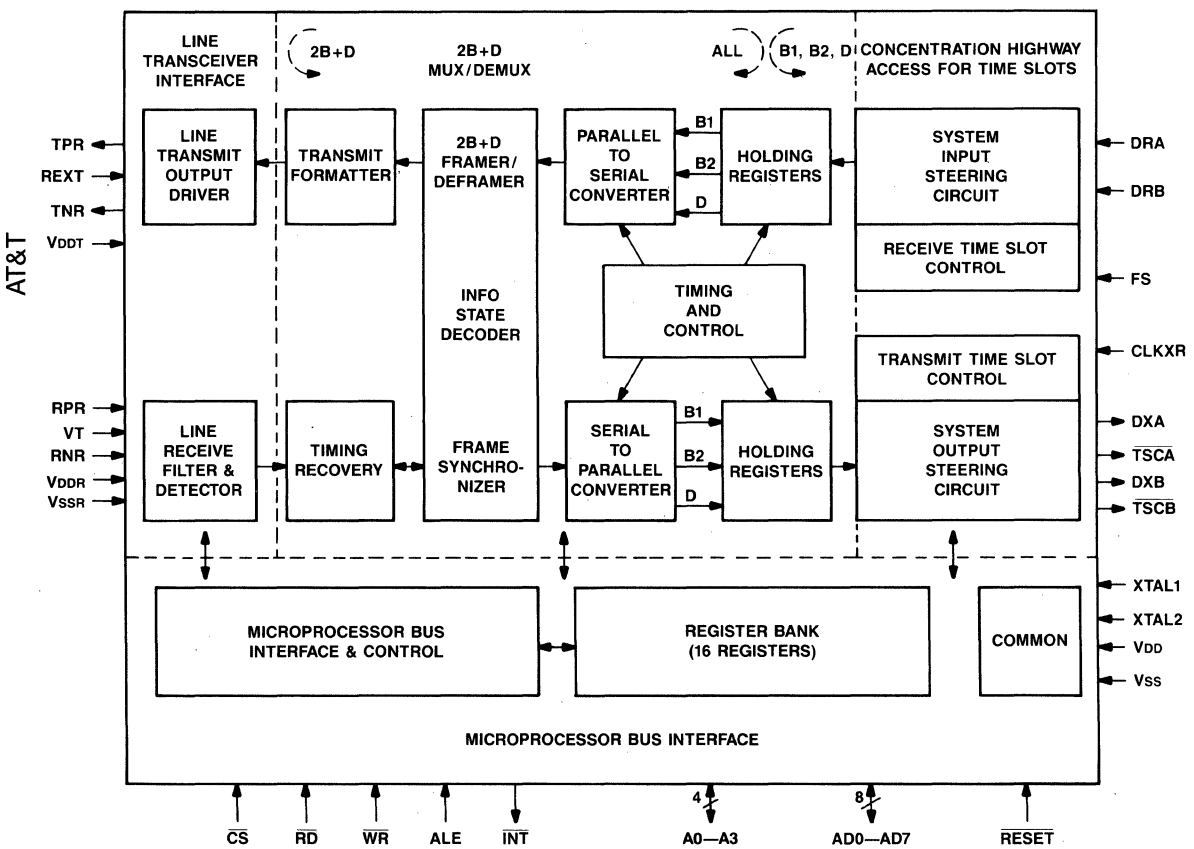
T7252A UNITS Block Diagrams





INTERFACE

ISDN U-Interface Basic Access Transceiver Chip Set — T7260 and T7261

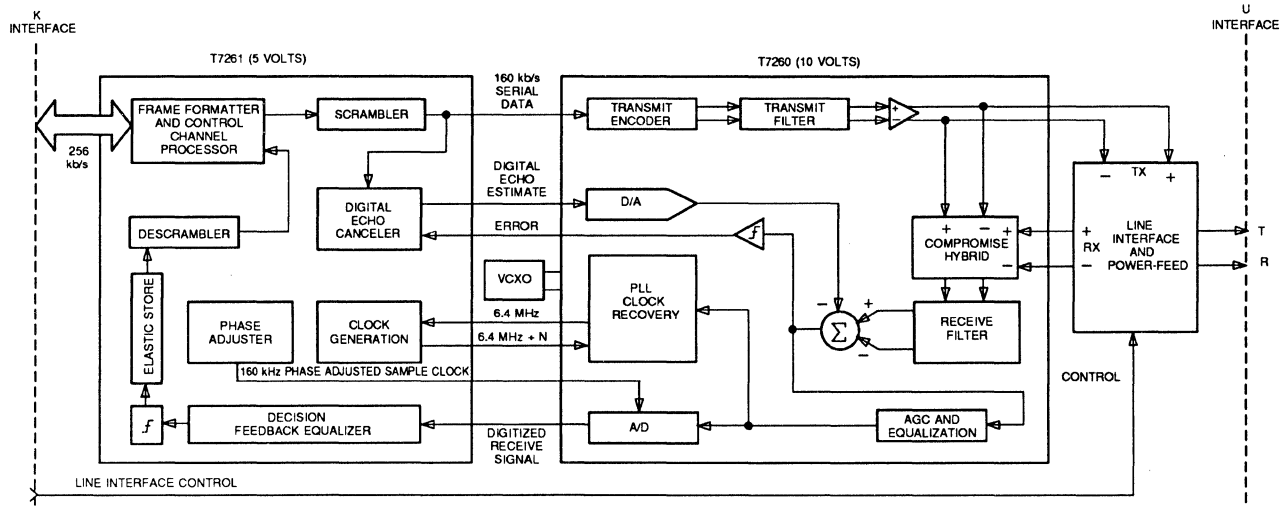
Description

The AT&T T7260 and T7261 ISDN U-Interface Basic Access Transceiver (U-BAT) Chip Set is a pair of silicon integrated circuits providing full-duplex 2B+D communication on a 2-wire digital subscriber loop. The T7260 and T7261 devices perform line transceiver functions at either the central office (CO) switch or at the network termination (NT) and operate at a data transfer rate of 144 kbits/s. Adaptive echo cancellation and equalization techniques provide a loss budget of 38 dB. The T7260 requires both a +5 V and −5 V supply; the T7261 requires only a +5 V supply. Both are manufactured in CMOS technology and are packaged in 44-pin plastic leaded chip carriers (PLCC).

Features

- U-interface for 2-wire operation
- Pin-selectable for central office (CO) switch and network termination (NT) applications
- 144 kbits/s full-duplex using echo cancellation (EC)
- Alternate mark inversion (AMI) line code
- Digital I/O via the AT&T K-interface
- On-chip balanced line driver
- Balanced continuous time filters
- Adaptive equalization and automatic gain control (AGC)
- LED driver to signal loss of framing
- Decision feedback equalizer (DFE) for increased tolerance to bridged taps
- EC and DFE reset pins for external power-up reset

T7260 and T7261 Basic Access ISDN U-Interface Block Diagram



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INTERFACE

(Advance) ISDN ANSI Standard U-Interface Basic Access Transceiver Chip Set — T7262 and T7263

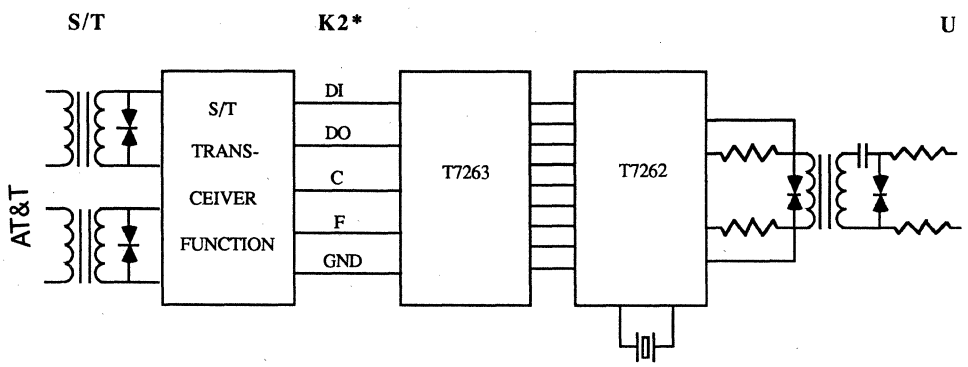
Description

The AT&T T7262 and T7263 ISDN ANSI Standard U-Interface Basic Access Transceiver (SUBAT) chip set is a pair of silicon integrated circuits providing full-duplex 2B+D communication on a 2-wire digital subscriber loop. The SUBAT performs line transceiver functions at either the LT or NT and operates at a data rate of 144 kbits/s. The design objective is to fully meet the range objective of the ANSI North American Standard. Both devices use CMOS technology and 44-pin leaded chip carriers for surface-mount applications.

Features

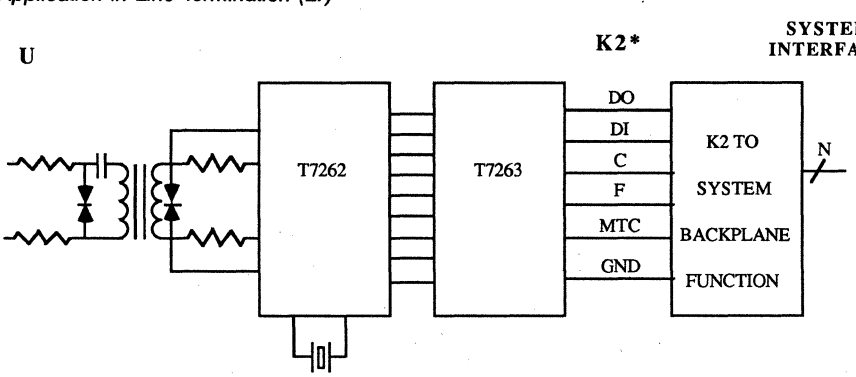
- Conforms to ANSI North American Standard:
  - 2B1Q line code
  - 13.5 dBm, 2.5 V pulses on 135 Ω line
  - Echo canceler and hybrid for full duplex operation
  - Two 64 kbits/s B channels and one 16 kbits/s D channel
  - Superframing with EOC, PS, CRC, FEBE, and NTM
  - Scrambled data stream
  - 9-symbol non-scrambled synchronization word frame heading
  - Includes activation/deactivation option
- Interfaces with the network or customer via the AT&T K2 Interface
- Mode pin selects NT or central office (LT) operation
- Single 5 V, ±5% supply
- Surface mount packages

Application in NT1



* The K2 interface is an AT&T proprietary 5-wire unbalanced interface (data upstream, data downstream, 512 kHz symbol clock, 8 kHz frame sync, and 8 kHz master timing clock, all referenced to ground). For NT operation, DU is data input of the T7263 and DD is data output. For LT operation, DU is data output of the T7263, DD is data input, and MTC is the 8 kHz system reference clock. DU and DD are serial streams at 512 kbits/s containing B1, B2, D plus framing, and five additional channels named S1 through S5.

Application in Line Termination (LT)



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INTERFACE

(Advance) Adaptive Differential Pulse Code Modulation Transcoder — T7280

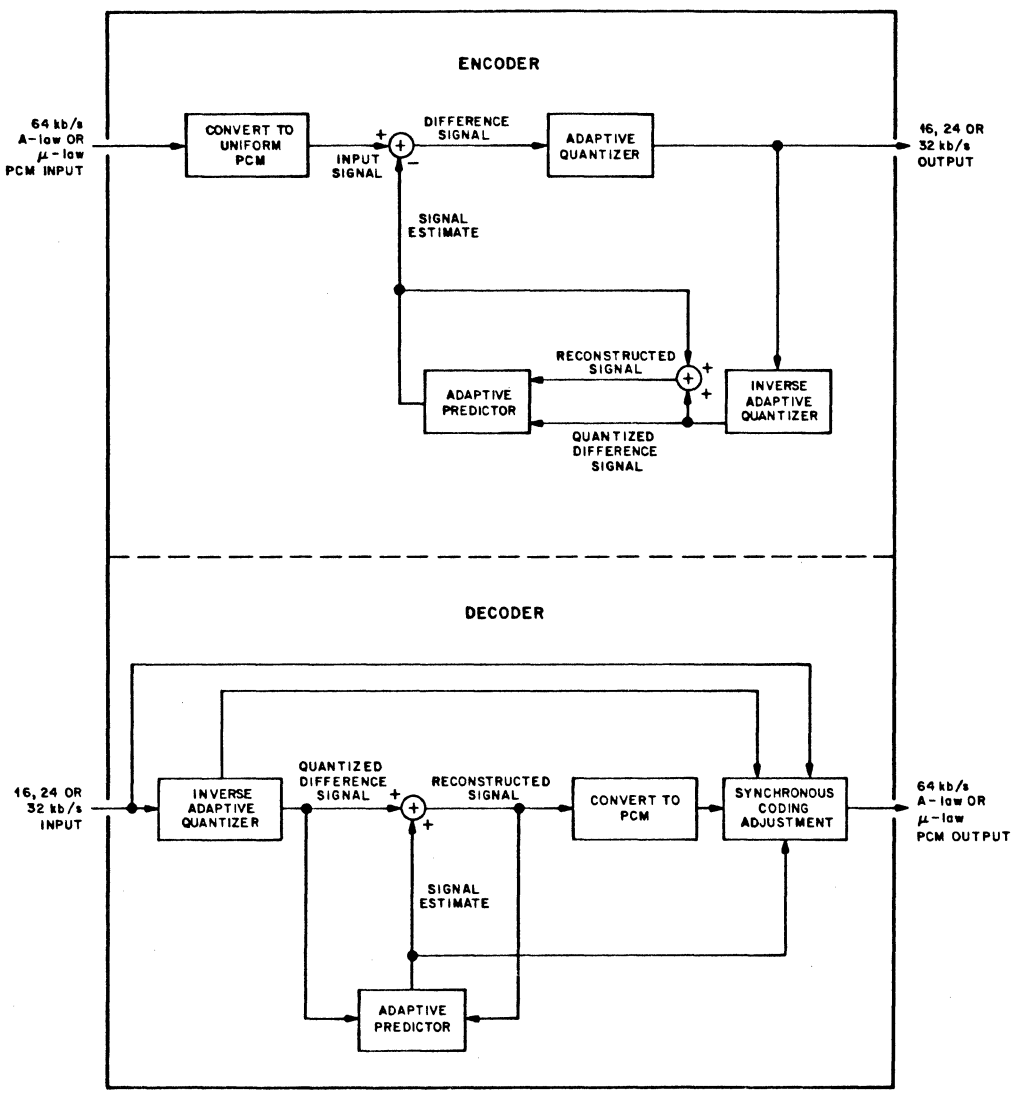
Description

The T7280 Adaptive Differential Pulse Code Modulation (ADPCM) Transcoder is a single-chip integrated circuit that digitally re-encodes 64 kb/s PCM (8-kHz sampling) to ADPCM at various bit rates. It provides 16 channels of encoding or decoding, any one of which can function as either an encoder or decoder independent of the other channels. The T7280 is manufactured using CMOS technology and is available in a 24-pin plastic DIP.

Features

- ADPCM coding and decoding, with bypass processing
- μ-law and A-law 64 kb/s PCM-compatible
- ANSI T1LB/81 and CCITT G.721 compatible at 32 kb/s
- Variable rate ADPCM, coding at 16 kb/s, 24 kb/s, and 32 kb/s
- 16-channel implementation (M encoders and N decoders, where M + N = 16)
- Independent feature control on a per-channel, 125 μs time-slot basis
- Reset of internal memory states under user control

T7280 ADPCM Transcoder Block Diagram



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Description

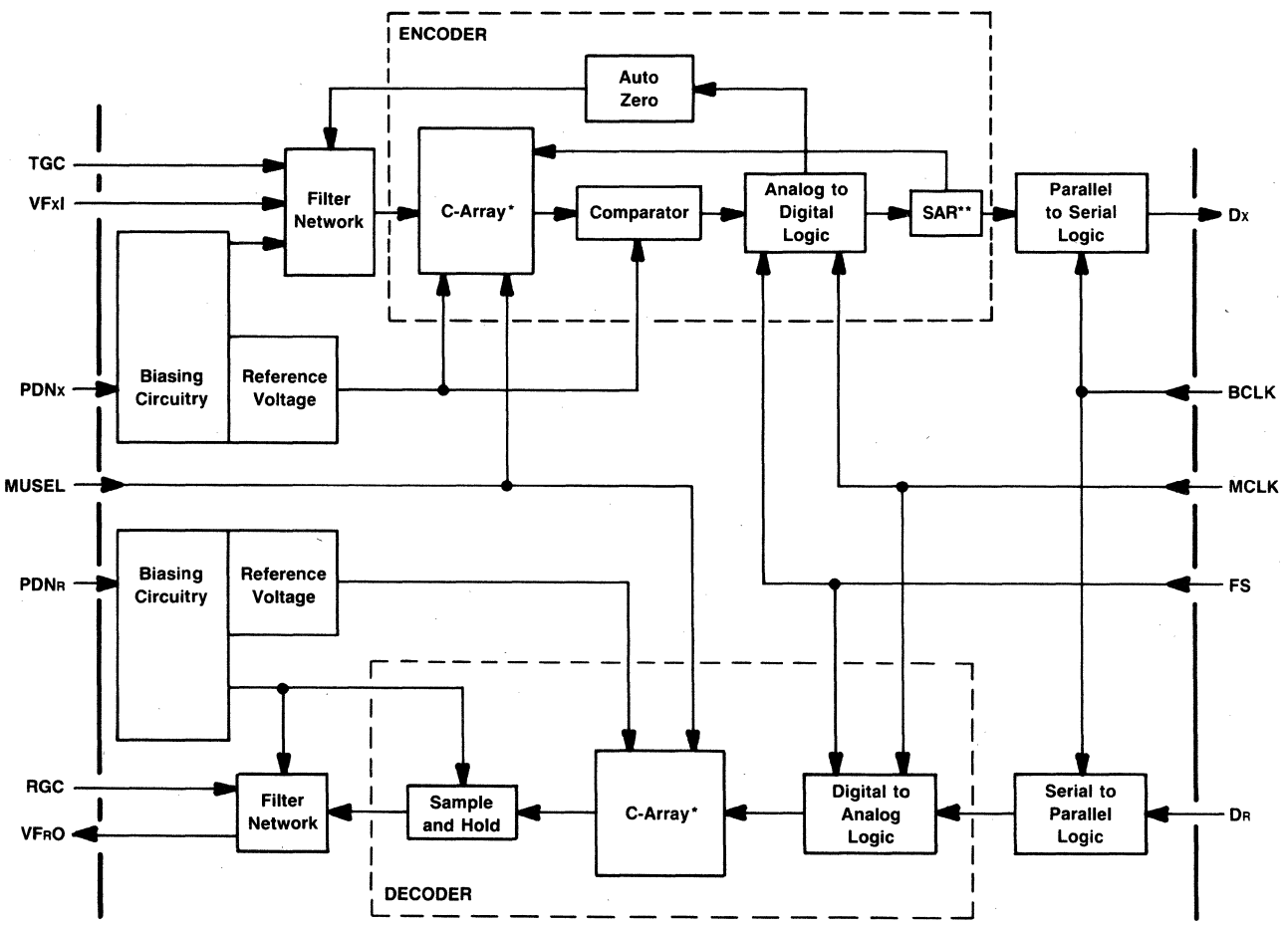
The T7500 PCM Codec with Filters integrated circuit performs the analog-to-digital and digital-to-analog translation functions in a circuit. It incorporates the transmit and receive filtering necessary to interface a voice telephone circuit to a time division multiplexed (TDM) system. The device is a full-duplex, 8-bit codec that operates from a ±5 volt power supply and provides A-law and/or μ-law conversion algorithms.

The T7500 Codec is synchronized off the positive-going edge and has separate power-down for the transmitter and receiver. The device is manufactured using CMOS technology and is available in an 18-pin plastic DIP or in a 20-pin plastic SOJ. Custom configurations and/or special packages may be available on request.

Features

- AT&T/CCITT compatible
- Pin selectable μ-law or A-law operation
- Pin selectable transmit and receive gain
- Variable data rate (128 kHz to 4.096 MHz)
- On-chip voltage reference
- Low power dissipation
- TTL-compatible inputs and outputs
- Low power dissipation:
  — 20 mW typical power-down
  — 80 mW typical operation

T7500 PCM Codec Block Diagram



* Capacitor Array

** Successive Approximation Register

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INTERFACE

PCM Codec with Filters — T7512

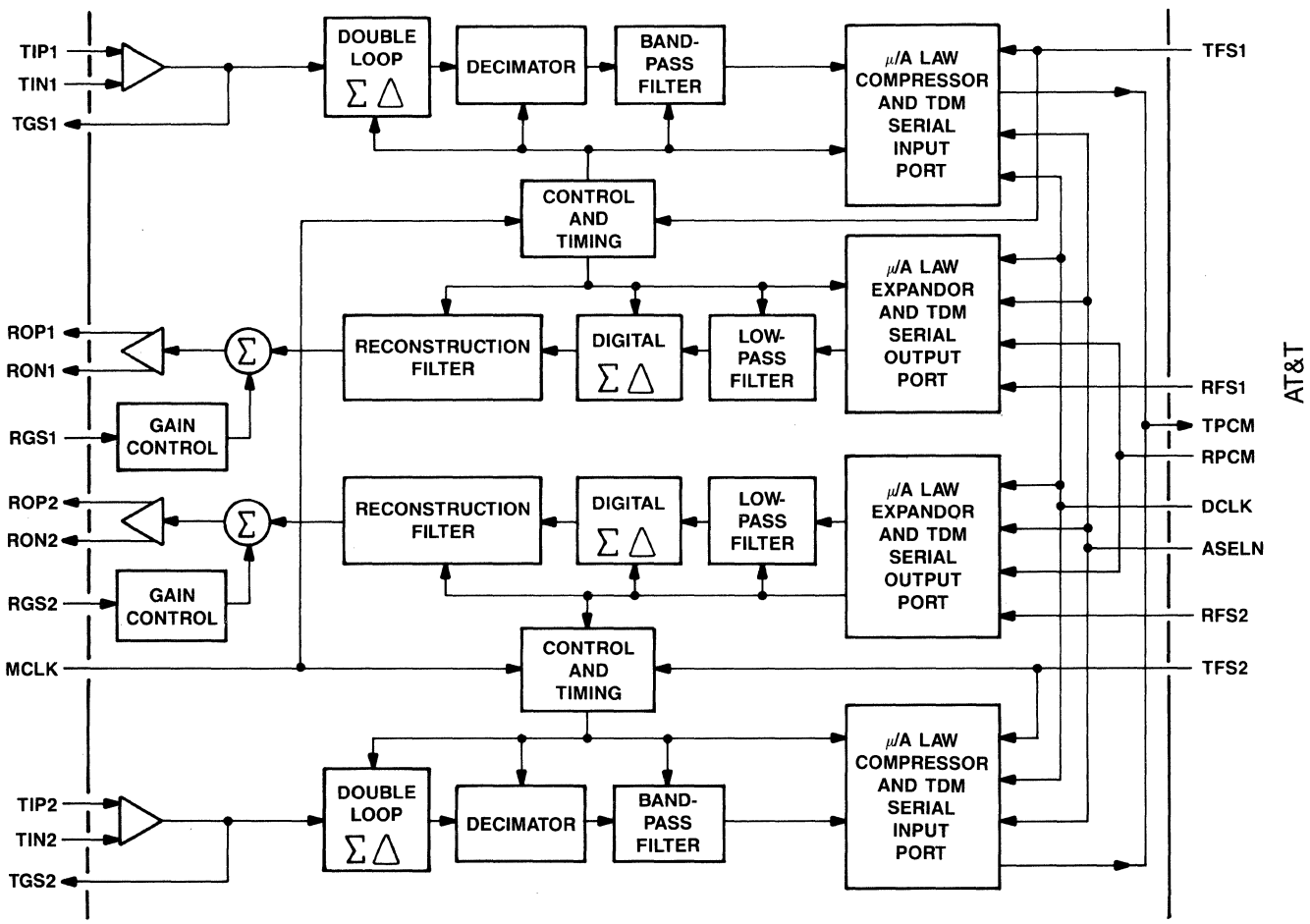
Description

The AT&T T7512 integrated circuit is a dual PCM sigma-delta codec with transmit/receive filters. It provides two channels of analog-to-digital and digital-to-analog conversion as well as the transmit and receive filtering necessary to interface two voice telephone circuits to a time division multiplexed system. The device is fabricated using a low-power CMOS technology and requires a single +5 volt supply. It is available in either a 28-pin plastic DIP package or 28-pin plastic SOJ package.

Features

- AT&T/CCITT-compatible
- Pin selectable μ-law or A-law operation
- Transmit and receive gain control with external resistors
- Two timing modes:
  - — Fixed data rate mode at 2.048 MHz
  - — Variable data rate mode — 128 kHz to 2.048 MHz
- On-chip voltage reference
- Differential output amplifier
- TTL-compatible inputs and outputs

T7512 PCM Codec Block Diagram



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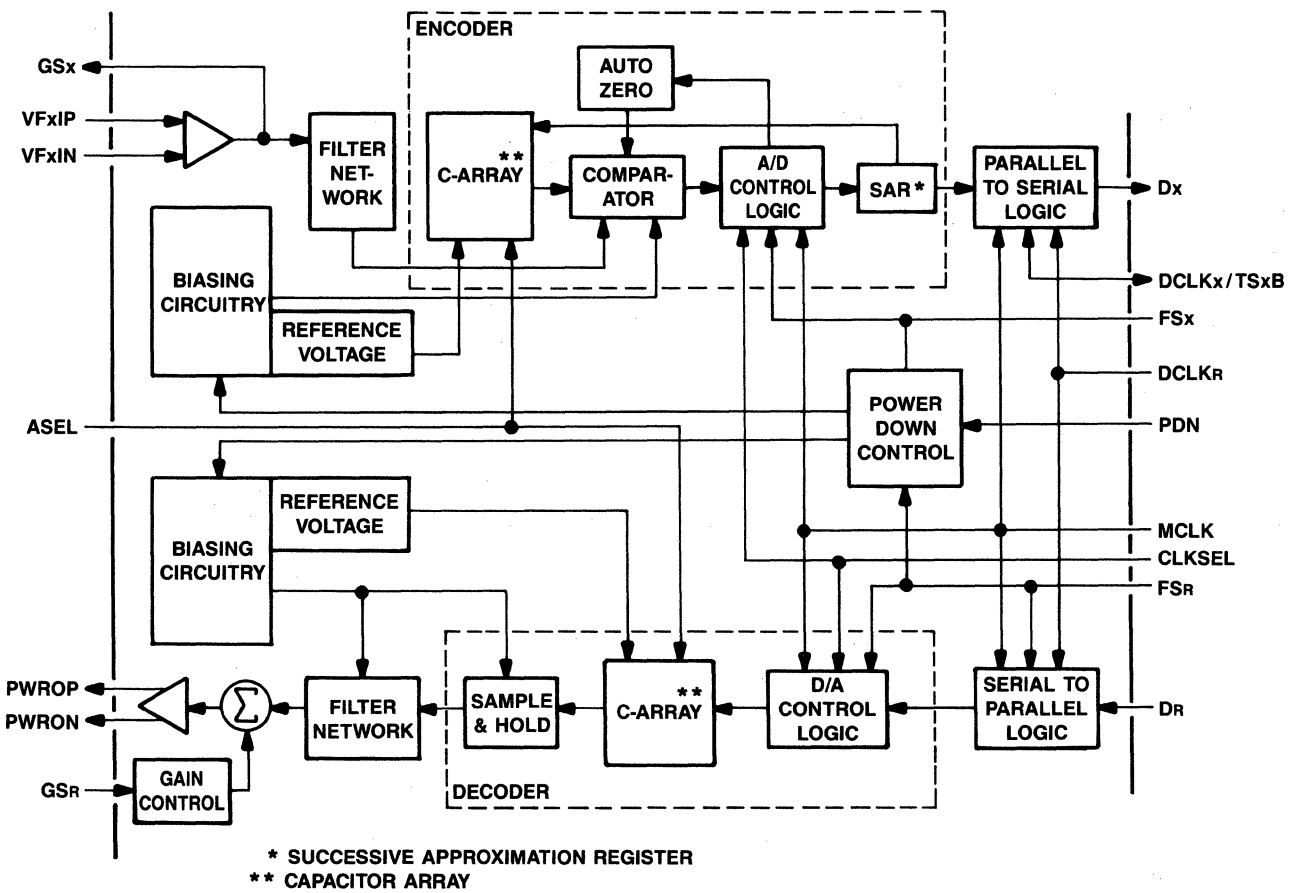
Description

The T7513A PCM Codec with Filters is a single-chip integrated circuit that provides analog-to-digital and digital-to-analog conversion; in addition, it provides the transmit and receive filtering necessary to interface a voice telephone circuit to a time-division multiplexed system. The T7513A is a direct replacement for the T7513, offering enhanced functionality and significantly reduced power consumption. The T7513A is available in a 20-pin plastic DIP or small outline J-lead (SOJ) package for surface mounting.

Features

- Direct replacement for the industry standard 2913 device
- Low-power, latchup-free CMOS technology:
  - — 65-mW typical operating power dissipation
  - — 5-mW typical power-down dissipation
- Differential architecture for high noise immunity and PSRR
- Pin-selectable master clock rates of 2.048, 1.544, or 1.536 MHz
- Two timing modes:
  - — fixed data rate: 2.048, 1.544, or 1.536 MHz
  - — variable data rate: 64 kHz to 2.048 MHz
- On-chip sample and hold, autozero, and precision voltage reference — no external components required
- Excellent noise performance
- Pin-selectable μ- or A-law operation

T7513A PCM Codec Block Diagram



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High-Precision PCM Codec with Filters — T7522

Description

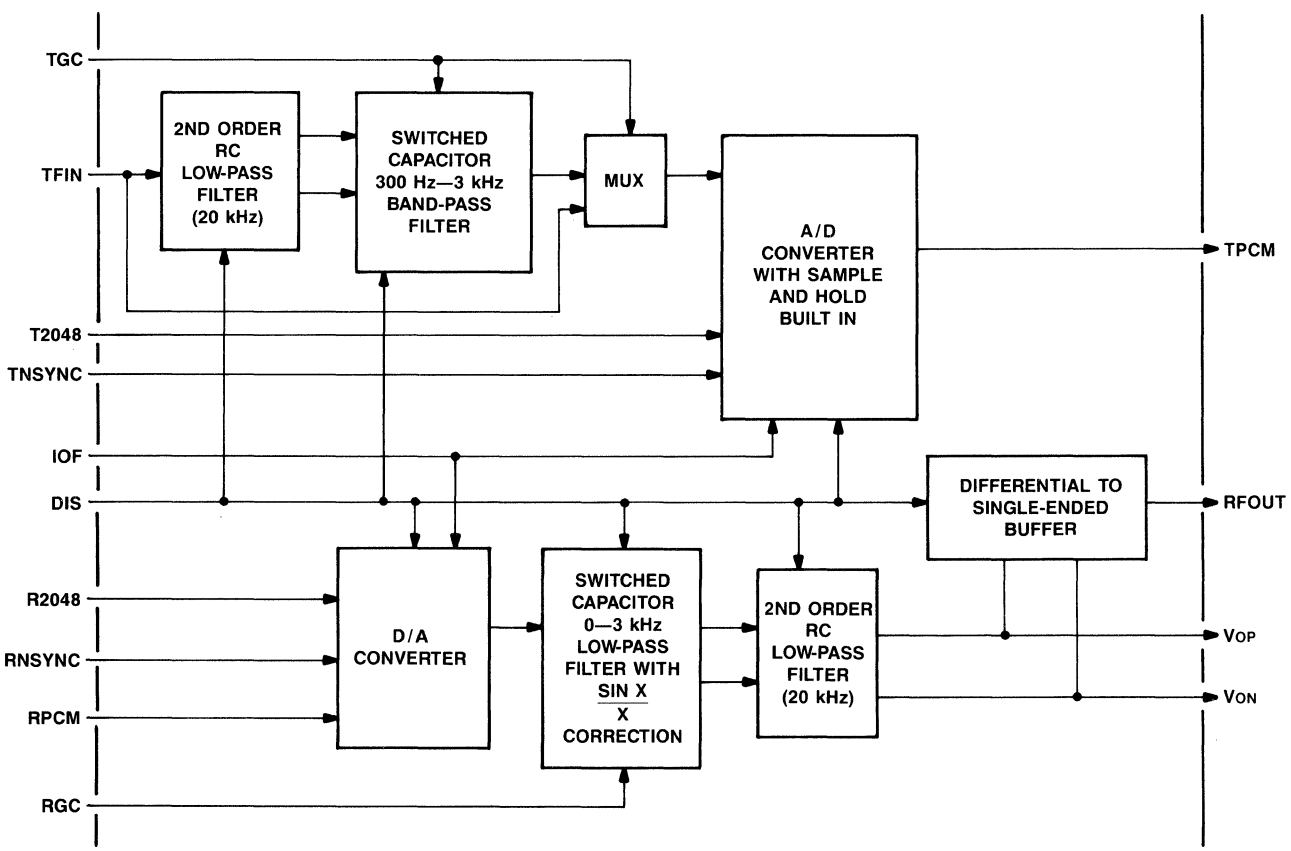
The T7522 High-Precision PCM Codec with Filters integrated circuit performs analog-to-digital and digital-to-analog conversion with 15-bit resolution and 10-bit linearity. The device provides anti-aliasing and reconstruction filters and a precision voltage reference. The device is designed for use in signal-processing applications that require PCM data with a higher resolution than PCM μ-law data. The T7522 Codec is a linear device with 16-bit PCM I/O data in 2's complement binary format. Typical applications include the use of this codec with echo cancelers, digital signal processors, and in data sets. This chip has programmable capabilities as LSB or MSB first I/O. The T7522 Codec is manufactured using CMOS technology and is available in a 24-pin hermetic, ceramic DIP.

The T7522 can directly replace the T7520 and T7521 in applications not requiring independent A/D and D/A power-down options, and is recommended for all new designs. Designs requiring the independent A/D and D/A power-down options should use the T7523.

Features

- Encoder and decoder with on-chip filters
- On-chip precision-trimmed reference voltages
- Charge redistribution and switched capacitor techniques
- ±5 V power supplies, with 120 mW nominal power
- Easy interface to a DSP device
- Sync deglitching circuitry on-chip
- 3-state TTL-output bus
- Data format: 16-bit PCM in 2's complement binary (LSB or MSB first)
- Gain selection — transmit: 0 or −3 dB
  receive: +3 or 0 dB
- Guaranteed monotonic to 15 bits
- Balanced filters for improved power supply rejection ratio (PSRR)
- A/D filter/without filter selection
- A/D has sample and hold built in

T7522 High-Precision PCM Codec Block Diagram



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Description

The DS1 Chip Set performs the various multiplexing and framing functions required by a digital multiplexed interface (DMI). This chip set consists of a T7229 Framer, 229FB Maintenance Buffer, 257AL Transmit Formatter, 257AU Receive Synchronizer, and the LC1046 (DS1) or LC1135B (CEPT) Digital Signaling Interface (DSI). For DMI applications the 229GB Framer is an excellent alternative. The two transformers provide impedance matching to the twisted pair cable. The received information is input to the LC1046/LC1135B DSI in alternate mark inversion (AMI) format. The DSI then converts this signal into a TTL-level signal that is output to the 229GB Framer. The DSI also uses an internal phase-locked loop (PLL) to extract the receive line clock (RCLK) from the signal. This clock is output to the framer and the 257AU Receive Synchronizer. The framer detects frame boundaries and monitors the received data stream for facility trouble conditions and alarms. The 257AU Receive Synchronizer then receives the data signal from the framer and converts this serial data stream into parallel time-division multiplexed (TDM) data while extracting signaling information. The parallel data and signaling information are output on a per time slot basis to a PBX switching network or a host computer. The data and signaling information to be transmitted from the PBX or host computer is input to the 257AL Transmit Formatter. The transmit formatter converts this parallel data and signaling information back into a serial data stream. The information is input to the framer for in-line processing and output to the LC1046/LC1135B DSI for conversion back to a digital AMI signal and output to the transformers. The 229FB Maintenance Buffer provides an interface between the controlling processor and the serial report and control streams of the framer, transmit formatter, and the receive synchronizer.

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229FB Maintenance Buffer

Description

The 229FB Maintenance Buffer integrated circuit provides the microprocessor interface for the serial report and control streams of the T7229 or 229GB Framer, 257AU Receive Synchronizer, and 257AL Transmit Formatter. The device also processes facility alarms received from the framer and provides additional latched inputs and outputs for microprocessor use. The maintenance buffer is manufactured using depletion-mode NMOS technology, requires a single +5 V supply, and is available in a 40-pin plastic DIP.

Features

- 8-bit interface bus
- Microprocessor access to control/report streams
- Ten general-purpose latched outputs
- Two error-source latched inputs
- Preprocessing counters for facility error conditions updated by the framer
- Built-in operational testing capability
- TTL-compatible

229GB Framer

Description

The 229GB Framer integrated circuit provides the line format and frame format interfaces for DS1 (1.544 Mb/s) digital carrier systems. It performs on-line and off-line frame-oriented functions in both the receive and transmit directions. In addition, the device provides an auxiliary signaling format known as DMI Bit-Oriented Signaling (BOS). The 229GB Framer is TTL-compatible and is packaged in a 40-pin ceramic DIP.

Features

- Bipolar and B8ZS line format capability
- Multiple TDM frame formats:
  - — Independent formats — D4, *SLC*® Carrier, ESF, and DDS T1DM
  - — Auxiliary signaling format — DMI BOS
- Off-line, defensive, and fast frame synchronization
- *SLC* Carrier, ESF, and DDS T1DM facility data-link insertion and extraction
- Remote frame/multiframe alarm activation and detection
- Transmission performance monitoring capability:
  - — Bipolar and B8ZS violations
  - — Frame-alignment signal (frame bit) errors
  - — Loss-of-frame/multiframe alignment
  - — CRC-6 errors (ESF mode)
  - — Change-of-frame alignment

T7229 Framer

Description

The T7229 Framer integrated circuit provides the line format and frame format interfaces for both DS1 (1.544 Mb/s) and CEPT (2.048 Mb/s) digital carrier systems. It performs on-line and off-line frame-oriented functions in both the receive and transmit directions. The T7229 Framer is TTL-compatible and is packaged in a 40-pin plastic DIP.

Features

- Bipolar, B8ZS, and HDB3 (CEPT) line format capability
- Multiple TDM frame formats:
  - — Independent formats — D4, *SLC* Carrier, ESF, and DDS T1DM
  - — CCITT 30-channel format with optional TS-16 signaling
- Off-line, defensive, and fast frame synchronization
- *SLC* Carrier, ESF, and DDS T1DM facility data-link insertion and extraction
- Remote frame/multiframe alarm activation and detection
- Transmission performance monitoring capability:
  - — Bipolar and B8ZS violations
  - — Frame-alignment signal (frame bit) errors
  - — Loss-of-frame/multiframe alignment
  - — CRC-6 errors (ESF mode)
  - — Change-of-frame alignment

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257AU Receive Synchronizer

Description

The 257AU Receive Synchronizer performs serial-to-parallel conversion, slip compensation, and signaling extraction on the serial data received from the framer. The receive synchronizer is a part of an LSI digital facility interface chip set that also includes the 257AL Transmit Formatter, the T7229 or 229GB Framer, and the 229FB Maintenance Buffer. The receive synchronizer is manufactured using NMOS technology and is available in a 32-pin plastic DIP.

Features

- Selectable DS1 (1.544 Mb/s) or CEPT (2.048 Mb/s) formats
- 4- or 16-state, RSM signal extraction
- Internal maintenance circuits
- Single +5 V supply
- TTL-compatible inputs and outputs

257AL Transmit Formatter

Description

The 257AL Transmit Formatter integrated circuit converts 14 bits of parallel data (8 traffic bits, 5 signaling bits, 1 parity bit), received from a time slot interchanger, into a serial stream. The device is manufactured using NMOS technology, requires a single +5 volt supply, and is available in a 32-pin plastic DIP.

Features

- Selectable DS1 (1.544 Mb/s) or CEPT (2.048 Mb/s) formats
- 2-, 4-, 16-state signaling or inhibit signaling insertion
- Variable F bit and parity bit delays
- TTL-compatible

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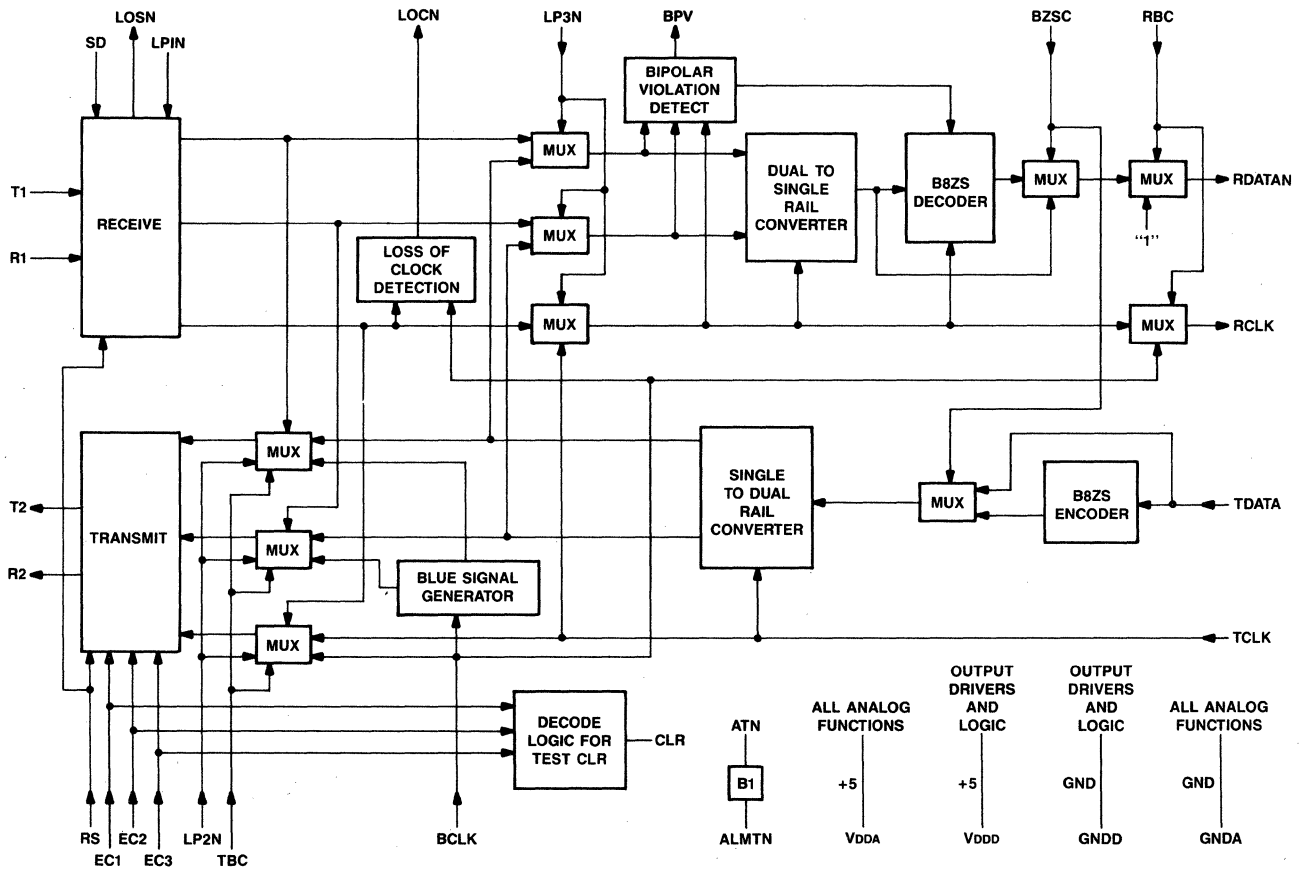
Description

The LC1046 Digital Signaling Interface (DSI) is an integrated circuit that provides a line interface between the DS1 or DS1C cross-connect and terminal equipment circuits for cable distances of up to 655 feet for 22-gauge plastic insulated cable. The device performs receive pulse regeneration, timing recovery, and transmit pulse shaping and equalization functions. The LC1046 DSI device is manufactured using 1.75 micron CMOS technology and is available in a 28-pin plastic DIP or 28-pin plastic small-outline J-leaded (SOJ) package for surface mounting.

Features

- Fully integrated DS1/DS1C line interface
- Compatible with Technical Advisory #34 (TA34) and PUB 43802 specifications
- On-chip transmit equalization
- Monolithic clock recovery
- Pin-selectable B8ZS encoder and decoder
- Loopback modes for fault isolation
- Multiple link-status and alarm features
- Minimal external circuitry required

LC1046 DSI Block Diagram



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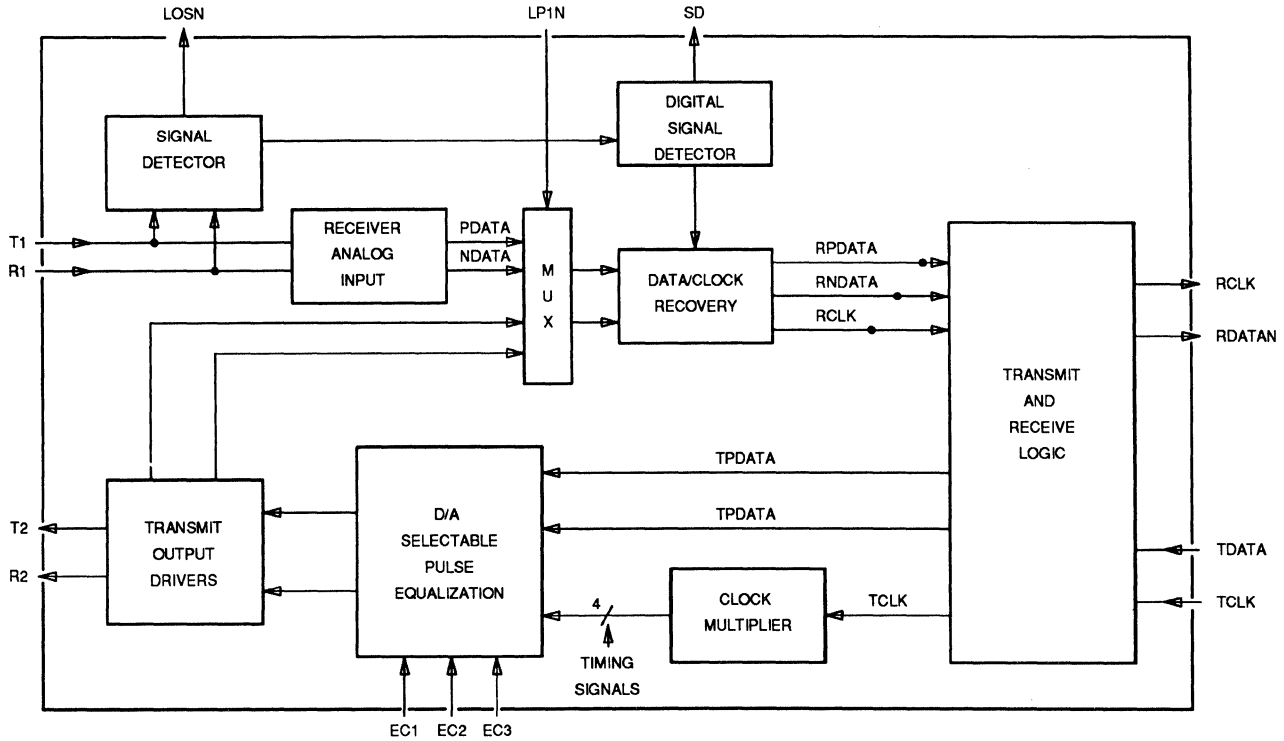
LC1046 DSI Analog Block Diagram



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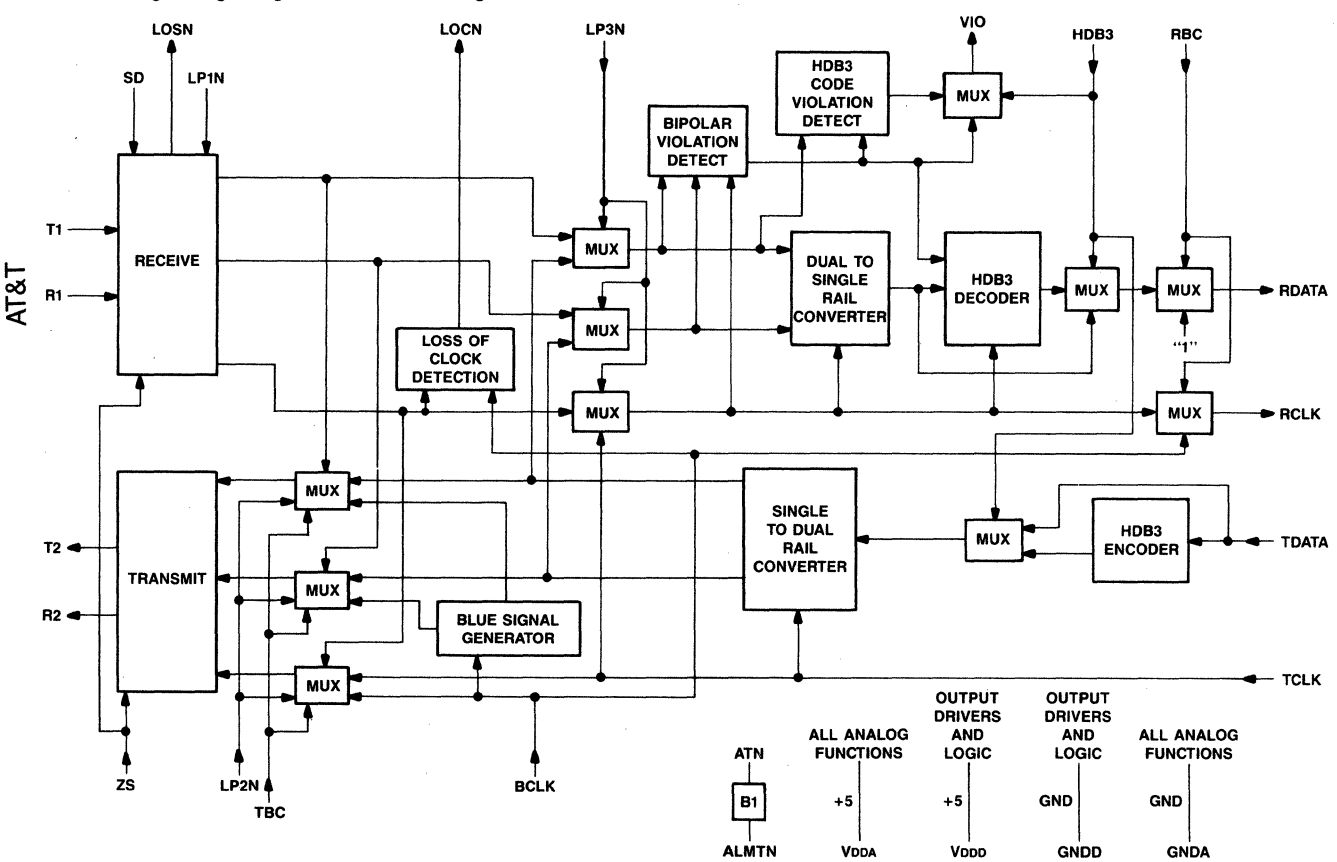
Description

The LC1135B Digital Signaling Interface (DSI) is an integrated circuit that provides a 2.048-Mb/s line interface to either twisted-pair or coaxial cable as specified in CCITT requirements G.703 and G.823. It performs receive pulse regeneration, timing recovery, and transmit pulse driving functions. The DSI device is manufactured using 1.75-micron CMOS technology and is available in a 28-pin plastic DIP or small-outline J-lead (SOJ) package for surface mounting. The digital and analog circuitry is shown below.

Features

- Fully integrated 2.048-Mb/s line interface
- Complies with CCITT specifications G.703 and G.823
- Pin-selectable 75 Ω or 120 Ω operation
- Monolithic clock recovery
- Minimal external circuitry required
- Low-power dissipation — 75 mW for 120 Ω twisted pair and 78 mW for 75 Ω coaxial, typical operating conditions
- Pin-selectable HDB3 encoder and decoder
- Loopback modes for fault isolation
- Multiple link-status and alarm features

LC1135B Digital Signaling Interface Block Diagram



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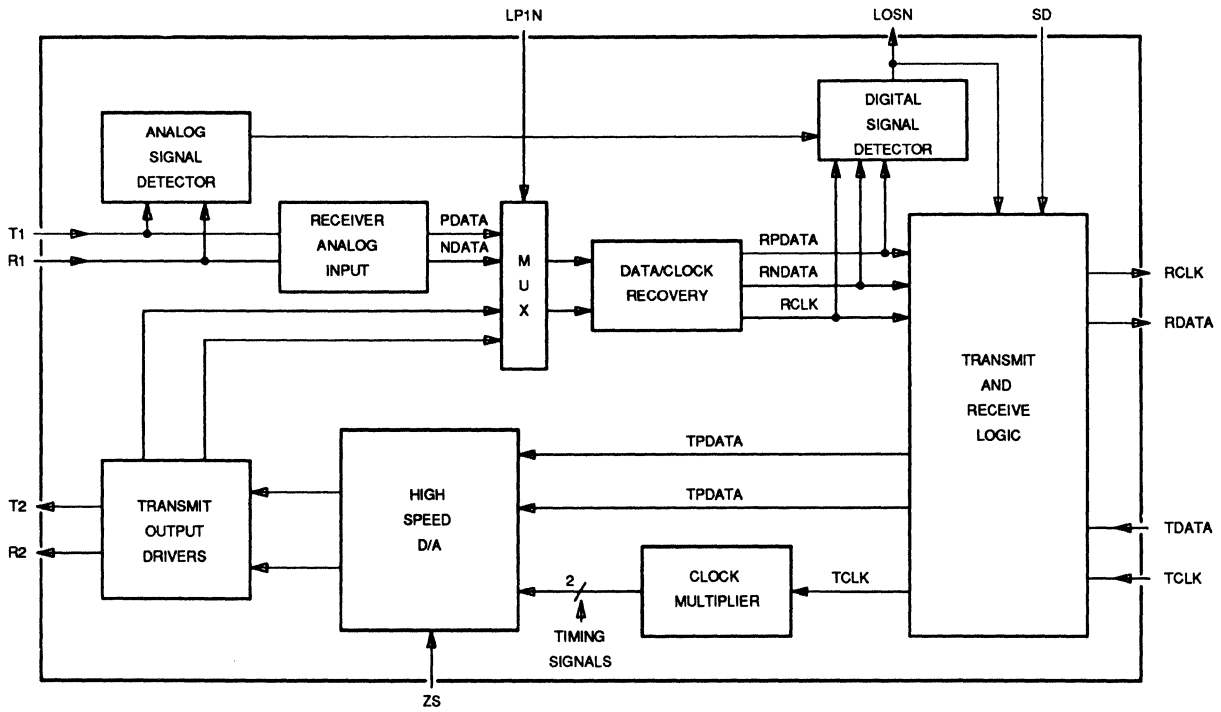
LC1135B Digital Signaling Interface Analog Block Diagram



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8 x 8 Bipolar Bilateral Crosspoint Array — 129EH-P

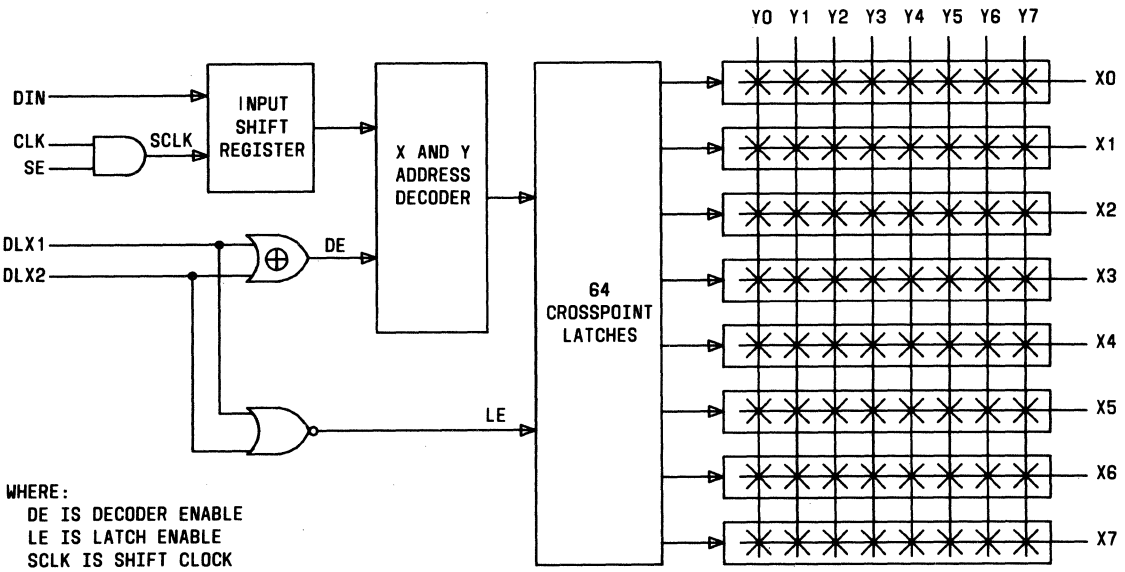
Description

The 129EH-P 8 x 8 Bipolar Bilateral Crosspoint (B^2X) Array integrated circuit is a high-density, high-performance, bipolar space division switch. It is organized as an 8 x 8 crosspoint array, with crosspoints consisting of 64 symmetrical, lateral P^+NP^+ transistors. Each crosspoint is a nearly ideal switch, capable of conducting current in both directions with an insertion impedance of less than 20 Ω. The on-board I^2L control and interface logic is TTL-compatible. The 129EH-P B^2X device is available in a 24-pin molded plastic DIP.

Features

- Crosstalk < −90 dB @ 3 kHz, 900 Ω
- Off isolation < −90 dB @ 3 kHz, 900 Ω
- Crosspoint-on resistance: 7 Ω ≤ R_{ON} ≤ 20 Ω
- Crosspoint signal bandwidth > 5 MHz
- Power dissipation < 100 mW, all crosspoints off
- TTL-compatible

129EH-P 8 x 8 Bipolar Bilateral Crosspoint Array Simplified Block Diagram



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8 × 8 Bipolar Bilateral Crosspoint Array — 129EH-P

Electrical Characteristics

T_A = 0 to 70°C, V_{CC} = 5.0 ±0.5 V, V_{EE} = −4 ±0.4 V, GND = 0 V

Parameter	Symbol	Min	Max	Unit
Input Voltages				
Low	V_{IL}	—	1.0	V
High	V_{IH}	1.8	—	V
Input Clamp Diode Voltage				
(I_I = −18 mA)	V_{IK}	−0.5	−1.35	V
Input Currents				
Low, V_{IN} = 0.0 V	I_{IL}	10	−30	μA
High, V_{IN} = 2.7 V	I_{IH1}	−1	2	μA
High, V_{IN} = 4.0 V	I_{IH2}	−1	10	μA
Power Supply Current				
V_{CC} = 5.5 V, V_{EE} = −4.4 V	I_{CC}	23	40	mA
For 8 Crosspoints On	I_{EE}	−23	−45	mA
Power Dissipation				
For 8 Crosspoints On	PD_{on}	200	420	mW
For All Crosspoints Off	PD_{off}	40	100	mW

Maximum Ratings

Rating	Value	Unit
Power Supply Voltage (V_{CC})	7.0	V
Input Voltage (V_{IH})	5.5	V
Operating Temp. Range (T_J)	0 to 70	°C
Storage Temp. Range (T_{stg})	−40 to +125	°C

Maximum ratings are the limiting conditions that can be applied under all variations of circuit and environmental conditions without the occurrence of permanent damage.

External leads can be bonded or soldered safely at temperatures up to 300°C.

Crosspoint Characteristics

Parameter	Symbol	Min	Max	Unit
Bandwidth	BW	—	5.0*	MHz
On Resistance	R_{ON}	7	20	Ω
Offset Voltage	V_{OF}	−30	30	mV
Offset Current	I_{OF}	−200	200	μA
Crosstalk (3 kHz, 900 Ω)	—	—	−90	dB
Off Isolation (3 kHz, 900 Ω)	—	—	−90	dB
Signal Bias Voltage (Off)	—	−3.0	3.0	V
Signal Bias Voltage (On)	—	−2.0	2.0	V
Signal Bias Current (On)	—	−4.5	4.5	mA

* This device has been tested to 5 MHz. Higher frequencies may be acceptable, depending on application.

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Quad Differential Line Receiver — 41LF

Description

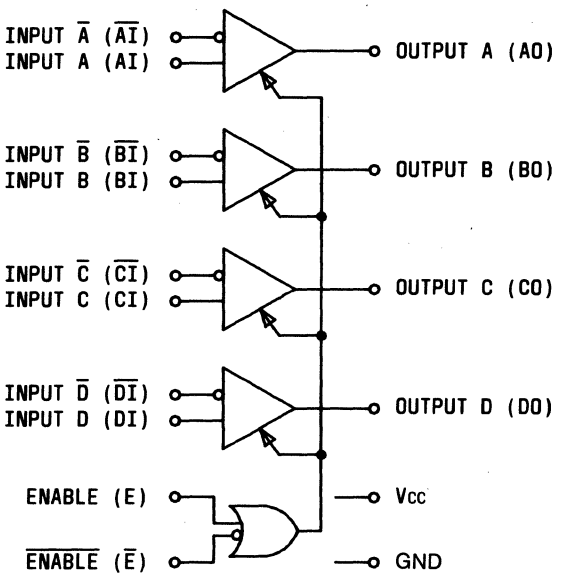
The 41LF Quad Differential Line Receiver integrated circuit is a quad differential input to TTL output line receiver. This OXIL technology device contains four receiver clusters and enable circuitry. The average propagation delay is 4 ns, and the common mode operating range is ±4 V. The 41LF line receiver is pin-equivalent to the general-trade AM26LS32 device, but has improved speed and decreased power consumption.

The quad differential line receiver is available in a 16-pin plastic DIP (41LF), a 16-pin SOJ (1041LF), and a 16-pin SOIC-GW (1141LF).

Features

- Pin-equivalent to general-trade AM26LS32, with increased speed and reduced power
- Single +5 V supply
- 0 to 85°C operating temperature
- Four line receivers per package
- Complementary inputs for each line receiver
- 250 mW maximum power dissipation
- 7 ns maximum propagation delay
- 0.20 V input sensitivity
- ±4 V common mode rejection

Logic Diagram



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Electrical Characteristics

T_A = 0 to 85°C, V_{CC} = 5.0 ±0.5 V

Parameter	Symbol	Min	Typ	Max	Unit
Output Voltage, V_{CC} = 4.5 V					
Low, I_{OL} = 8 mA	V_{OL}	—	—	0.5	V
High, I_{OH} = −400 μA	V_{OH}	2.5	—	—	V
Input Voltages (E, $\overline{E}$)					
Low, V_{CC} = 5.5 V	V_{IL}**	—	—	0.7	V
High, V_{CC} = 4.5 V	V_{IH}**	2.0	—	—	V
Clamp, V_{CC} = 4.5 V; I_{IN} = −18 mA	V_{IK}	—	—	−1.5	V
Differential Input Voltages* (AI, $\overline{AI}$, BI, $\overline{BI}$, CI, $\overline{CI}$, DI, $\overline{DI}$)					
V_O = V_{OL} or V_{OH}** −0.80 V < V_{IH} < 7.2 V, −1.2 V < V_{IL} < 6.8 V	V_{TH}**	0.20	0.1	—	V
Output Currents, V_{CC} = 5.5 V					
Off-State (High Z), V_O = 0.4 V	I_{OZL}	—	—	20.0	μA
Off-State (High Z), V_O = 2.4 V	I_{OZH}	—	—	20.0	μA
Short-Circuit	I_{SC}	−25.0	—	−100.0	mA
Input Currents (E, $\overline{E}$) V_{CC} = 5.5 V					
Low, V_{IN} = 0.4 V	I_{IL}	—	—	−360	μA
High, V_{IN} = 2.7 V	I_{IH}	—	—	20.0	μA
Reverse, V_{IN} = 5.5 V	I_{IH}	—	—	100	μA
Input Currents (AI, $\overline{AI}$, BI, $\overline{BI}$, CI, $\overline{CI}$, DI, $\overline{DI}$)					
Low, V_{IN} = −1.2 V	I_{IL}	—	—	−1.0	mA
High, V_{IN} = 7.2 V	I_{IH}	—	—	1.0	mA
Power Supply Current, V_{CC} = 5.5 V All outputs disabled	I_{CC}	—	35.0	45.0	mA

* Unused differential input pairs should be biased alternately to V_{CC} and GND. No protection resistor required.
** These input levels and difference voltage provide zero noise immunity and should only be tested in a static, noise-free environment.

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Maximum Ratings

Rating	Value	Unit
DC Power Supply Voltages (V_{CC})	7.0	V
Ambient Operating Temperature (T_A)	0 to 125	°C
Storage Temperature (T_{stg})	−40 to +125	°C

Maximum ratings are the limiting conditions that can be applied under all variations of circuit and environmental conditions without the occurrence of permanent damage.

External leads can be bonded or soldered safely at temperatures up to 300°C.

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Quad Differential Line Driver — 41LG

Description

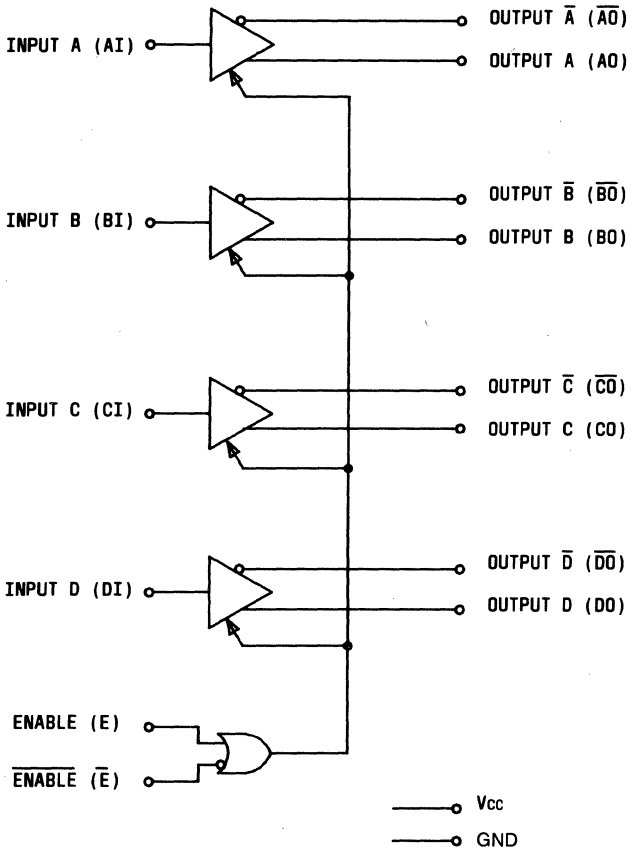
The 41LG Quad Differential Line Driver integrated circuit transmits digital data over balanced transmission lines. It translates input TTL logic levels to ECL-like output levels that directly drive the line. This OXIL technology device is pin-equivalent to the general-trade 26LS31 device; however, it has decreased power consumption and generates lower levels of electromagnetic interference (EMI). By having four drivers in one 41LG device, circuit board package count is reduced. All four line drivers in the device have common enable and disable functions. The 41LG line driver is compatible with many line receivers including the AT&T 41LF and 858B HIC (built-in terminations) devices, and the general-trade AM26LS32 device.

The quad differential line driver is available in a 16-pin plastic DIP (41LG), a 16-pin SOJ (1041LG), and a 16-pin SOIC-GW (1141LG).

Features

- Pin-equivalent to general-trade AM26LS31 device with increased speed, reduced power, and reduced EMI
- Single +5 V supply
- Four line drivers per package
- Complementary outputs from each line driver
- No line loading when Vcc = 0
- 40 mA drive capability
- High output drive for 50 Ω lines
- 100 mA minimum output short-circuit current
- 300 mW maximum power dissipation
- 6 ns maximum propagation delay
- 0.2 ns output skew, typical
- 0 to 85°C operating temperature

Logic Diagram



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Electrical Characteristics

T_A = 0 to 85°C, V_{CC} = 5.0 ±0.5 V

Parameter	Symbol	Min	Typ	Max	Unit
Output Voltages, V_{CC} = 4.5 V					
Low, I_{OL} = −40.0 mA	V_{OL}	—	—	V_{OH} − 0.8*	V
High, I_{OH} = −40.0 mA	V_{OH}	3.0	—	—	V
High Z, I_{OZ} = −1.0 mA, V_{CC} = 4.5 V	V_{OZ}	—	2.0	V_{OL} − 0.05	V
V_{CC} = 4.75 V			2.0	V_{OL} − 0.2	V
Input Voltages					
Low, V_{CC} = 5.5 V	V_{IL}**	—	—	0.8	V
High, V_{CC} = 4.5 V	V_{IH}**	2.0	—	—	V
Clamp, V_{CC} = 4.5 V; I_{IN} = −18.0 mA	V_{IK}	—	—	−1.5	V
Output Currents					
Short-Circuit	I_{SC}	−100.0	−20.0	−300.0	mA
Input Currents, V_{CC} = 5.5 V					
Low, V_{IN} = 0.4 V	I_{IL}	—	—	−400	μA
High, V_{IN} = 2.7 V	I_{IH}	—	—	20.0	μA
Reverse, V_{IN} = 5.5 V	I_{IH}	—	—	100	μA
Power Supply Current, V_{CC} = 5.5 V					
All outputs disabled	I_{CC}	—	60.0	75.0	mA
All outputs enabled	I_{CC}	—	35.0	55.0	mA

* V_{OL} must be a minimum of 0.8 V (800 mV) less than its complementary output.
** These input levels provide zero noise immunity and should only be tested in a static, noise-free environment.

Maximum Ratings

Rating	Value	Unit
Power Supply Voltage (V_{CC})	7.0	V
Ambient Operating Temp. Range (T_A)	0 to 125	°C
Storage Temp. Range (T_{stg})	−40 to +125	°C

Maximum ratings are the limiting conditions that can be applied under all variations of circuit and environmental conditions without the occurrence of permanent damage.

External leads can be bonded or soldered safely at temperatures up to 300°C.

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Dual Differential Line Driver & Receiver Pairs — 41LK, 41LL, and 41LM

Description

The 41LK, 41LL, and 41LM devices are dual differential line driver and line receiver pairs, consisting of two differential ECL-to-TTL converters and two TTL-to-differential ECL converters. These OXIL technology devices contain individual enabling circuitry for the driver and receiver pairs. The average propagation delay for the driver and receiver is 3.0 ns and 4.0 ns, respectively. By having two receivers and two drivers in one package, the serial data and control clock are transmitted and received using a single integrated circuit.

The 41LK device is intended for use where the minimization of electromagnetic interference is required. The 41LL device has internal 200 Ω discharge resistors on each driver output and is equivalent to the DS8923A. The 41LM device has resistor terminations for both the driver (200 Ω) and receiver (100 Ω) and is intended for use with 100 Ω impedance (Z) twisted pair or flat cable — since this device eliminates the need for external resistors.

The 41LK, 41LL, and 41LM dual line driver and line receiver pairs are available in a choice of packaging: 16-pin plastic DIP, 16-pin SOJ, or 16-pin SOIC-GW.

Features

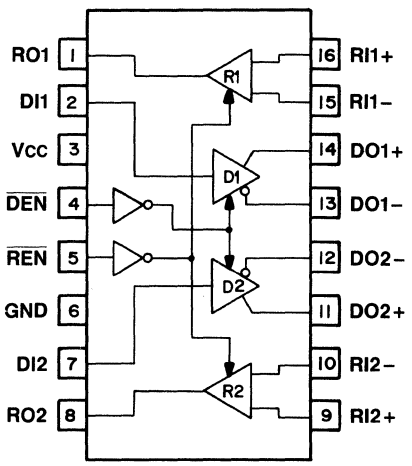
Driver

- Single +5 V supply
- Two line drivers per package
- Complementary outputs for each line driver
- No line loading when Vcc = 0 V
- 100 mA minimum output short-circuit current
- 6 ns maximum propagation delay
- 0.2 ns output skew, typical
- 0 to 85°C operating temperature

Receiver

- Two line receivers per package
- Complementary outputs for each line receiver
- 7 ns maximum propagation delay
- 0.20 V input sensitivity
- ±4 V common mode rejection
- 0 to 85°C operating temperature

Pin Function Diagram



Logic Table

DEN	REN	R01	R02	D01	D02
0	0	ACTIVE	ACTIVE	ACTIVE	ACTIVE
1	0	ACTIVE	ACTIVE	HI-Z	HI-Z
0	1	HI-Z	HI-Z	ACTIVE	ACTIVE
1	1	HI-Z	HI-Z	HI-Z	HI-Z

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Electrical Characteristics

T_A = 0 to 85°C, V_{CC} = 5.0 ±0.5 V

Driver

Parameter	Symbol	Min	Typ	Max	Unit
Output Voltages, V_{CC} = 4.5 V					
Low, I_{OL} = −40.0 mA	V_{OL}	—	—	V_{OH} − 0.8*	V
High, I_{OH} = −40.0 mA	V_{OH}	3.0	—	—	V
High Z, I_{OZ} = −1.0 mA, V_{CC} = 4.5 V	V_{OZ}	—	2.0	V_{OL} − .05	V
V_{CC} = 4.75 V	V_{OZ}	—	2.0	V_{OL} − 0.2	V
Input Voltages					
Low, V_{CC} = 5.5 V	V_{IL}	—	—	0.7	V
High, V_{CC} = 4.5 V	V_{IH}	2.0	—	—	V
Clamp, V_{CC} = 4.5 V; I_{IN} = −18.0 mA	V_{IK}	—	—	−1.5	V
Output Currents					
Short-Circuit	I_{SC}	−100.0	—	−300.0	mA
Input Currents, V_{CC} = 5.5 V					
Low, V_{IN} = 0.4 V	I_{IL}	—	—	−400	μA
High, V_{IN} = 2.7 V	I_{IH}	—	—	20.0	μA
Reverse, V_{IN} = 5.5 V	I_{IH}	—	—	100	μA
Power Supply Current, V_{CC} = 5.5 V					
41LK: All outputs disabled	I_{CC}	—	40.0	75.0	mA
All outputs enabled	I_{CC}	—	30.0	50.0	mA
41LL, 41LM: All outputs disabled	I_{CC}	—	60.0	90.0	mA
All outputs enabled	I_{CC}	—	90.0	135.0	mA

* V_{OL} must be a minimum of 0.8 V (800 mV) less than its complementary output.

One input of unused differential input pairs should be based to Vcc. No protection resistor required.

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Receiver

Parameter	Symbol	Min	Typ	Max	Unit
Output Voltage, V_{CC} = 4.5 V					
Low, I_{OL} = 8 mA	V_{OL}	—	—	0.5	V
High, I_{OH} = −40.0 μA	V_{OH}	2.5	—	—	V
Input Voltages (E, $\bar{E}$)					
Low, V_{CC} = 5.5 V	V_{IL}*	—	—	0.7	V
High, V_{CC} = 4.5 V	V_{IH}*	2.0	—	—	V
Clamp, V_{CC} = 4.5 V; I_{IN} = −18 mA	V_{IK}	—	—	−1.5	V
Differential Input Voltages					
V_O = V_{OL} or V_{OH}*	V_{TH}*	0.20	0.1	—	V
−0.80 V < V_{IH} < 7.2 V, −1.2 V < V_{IL} < 6.8 V					
Output Currents, V_{CC} = 5.5 V					
Off-State (High Z), V_O = 0.4 V	I_{OZL}	—	—	20.0	μA
Off-State (High Z), V_O = 2.4 V	I_{OZH}	—	—	20.0	μA
Short-Circuit	I_{SC}	−25.0	—	−100.0	mA
Input Currents (E, $\bar{E}$)					
V_{CC} = 5.5 V					
Low, V_{IN} = 0.4 V	I_{IL}	—	—	−400	μA
High, V_{IN} = 2.7 V	I_{IH}	—	—	20.0	μA
Reverse, V_{IN} = 5.5 V	I_{IH}	—	—	100	μA
Input Currents					
Low, V_{IN} = −1.2 V	I_{IL}	—	—	−1.0	mA
High, V_{IN} = 7.2 V: 41LK, 41LM (Only)	I_{IH}	—	—	1.0	mA

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* The input levels and difference voltage provide zero noise immunity and should only be tested in a static, noise-free environment.

One input of unused differential input pairs should be based to V_{CC}. No protection resistor required.

Maximum Ratings

Rating	Value	Unit
Power Supply Voltage (V_{CC})	7.0	V
Ambient Operating Temp. Range (T_A)	0 to 125	°C
Storage Temp. Range (T_{stg})	−40 to +125	°C

Maximum ratings are the limiting conditions that can be applied under all variations of circuit and environmental conditions without the occurrence of permanent damage.

External leads can be bonded or soldered safely at temperatures up to 300°C.

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ANALOG

Octal High-Voltage MOSFET Arrays

Monolithic N-Channel and P-Channel Enhancement-Modes — Advanced Information

Description

The AT&T MOSFET Arrays contain eight P-Channel DMOS drivers (AP0130NA) and eight N-Channel DMOS drivers (AN0130NA) configured with common-source, open drain, and ESD protection gates. The device interfaces with MOS logic inputs to outputs capable of withstanding 300 volts, sinking 15 and 30 mA respectively.

Typical Characteristics	AN0130NA N-Channel	AP0130NA P-Channel
BV_{DS}	350 V	380 V
$R_{DS(ON)}$	300 Ω	600 Ω

Features

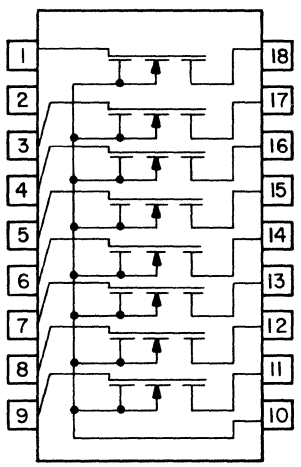
- On-chip ESD protection
- Operating voltage up to 300 V
- Processed with BCDMOS technology
- Freedom from secondary breakdown
- Interfaces directly to CMOS logic
- PIN compatible with industry standard driver arrays
- Low crosstalk between channels

Maximum Ratings

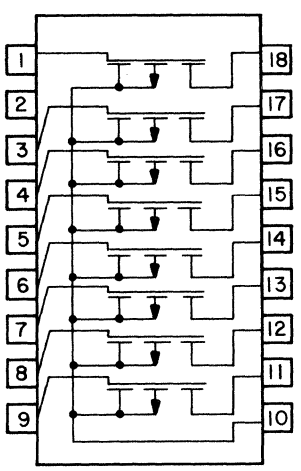
At 25°C unless otherwise specified

	AN0130NA N-Channel		AP0130NA P-Channel	
Rating	**Value**	**Unit**	**Value**	**Unit**
Ambient Operating Temperature Range	−40 to +85	°C	−40 to +85	°C
Drain Current, dc	30	mA	−15	mA
Drain Current, Pulsed (tP=200 μs; duty cycle=2%)	75	mA	−40	mA
Gate-to-Source Voltage	±20	V	±20	V
Drain-to-Source Voltage	300	BV_{DS}	300	BV_{DS}

AN0130NA Functional and Pin Configuration



AP0130NA Functional and Pin Configuration



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Description

The LB1006AB Telephone Ringing Detector provides ringing detection functions from the Tip-Ring pair of a telephone loop. This device provides a nominal output current (up to approximately 1 mA) for two types of output drivers. The output can be connected to either an opto-isolator device or to a logic interface with a microprocessor.

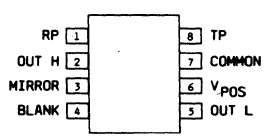
Applications

The LB1006AB Detector derives its power by rectifying the ac ringing signal from the Tip-Ring pair of a telephone loop. It operates over widely varying ringing waveforms (15 to 68 Hz at 40 to 150 Vrms). It uses this derived power to activate ringing-detector logic, and then transfers most of this power to an output current driver. There is essentially no loading under non-ringing conditions. This device has two outputs, OUT H and OUT L. The OUT H output is used to source output current when ringing is detected. The OUT L output becomes functional when the OUT H output is connected to the mirror input. The OUT L output will sink current when ringing is detected (see Simplified Output Diagram). This device does not have to depend upon power derived from the Tip-Ring inputs to become operational. Connecting an external voltage source to V+ will also allow the device to operate in what is described as "stand alone applications." Applications for the two types of outputs (source or sink current) are shown in the Application Diagrams.

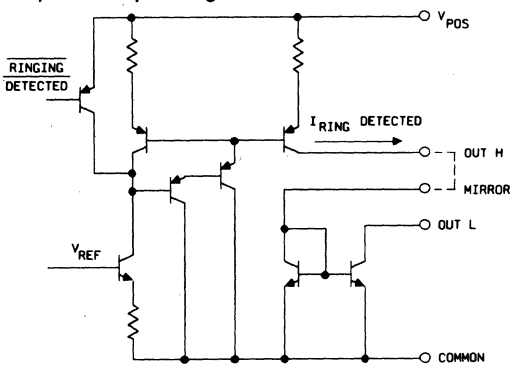
Features

- Provides an inexpensive means of ringing detection
- Operates on less than 1.0 mA from the telephone loop
- Internal polarity guard and 2000 V lightning surge protection
- Immune to rotary dial pulsing (bell tap)
- Meets both Type A and B ringing requirements (40 Vrms $<V_{IN}<$ 150 Vrms, 15 Hz $<f_{in}<$ 68 Hz) as specified by EIA RS-470 and FCC Part 68
- Ringer equivalency: 0.8 B when configured as shown in the Application Diagrams

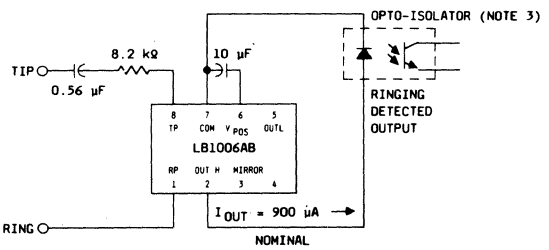
8-Pin Plastic DIP



Simplified Output Diagram

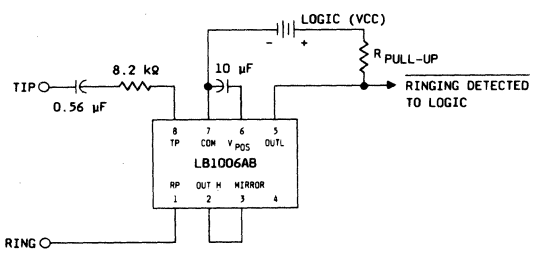


Typical Application for Opto-isolator Drive



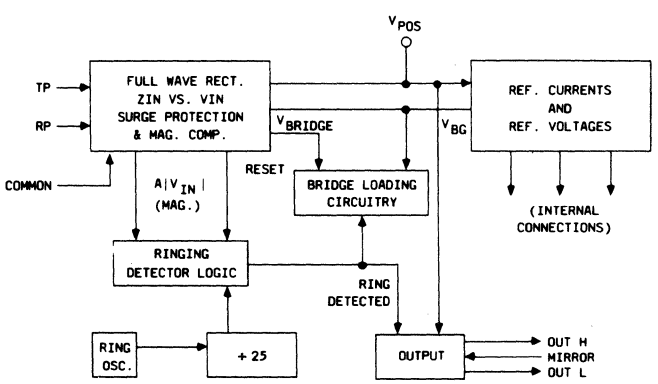
Note 3: AT&T 4U GI MCT210Q4898 or similar devices.

Typical Application for Interface Direct to Logic



CAUTION: Care must be taken when interfacing to a load which is referenced to earth ground. (See Applications text for further details.)

Functional Diagram



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Description

The LB1011AB integrated circuit is an electronic battery-feed circuit which supplies dc currents to a telephone line with minimal loading on the ac signals. The LB1011AB is integrated as two complementary chips to supply dc currents of both negative and positive polarities to either balanced or unbalanced lines. In the balanced line application, this device helps suppress undesirable common-mode signals.

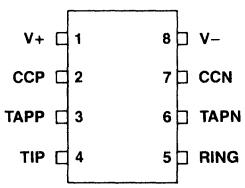
Features

- Basic battery-feed function at a low cost
- High ac-impedance characteristics for balanced-line, differential-mode, voice-band signals
- Full internal lightning surge protection
- dc voltage drops can be adjusted to accommodate different peak signal levels

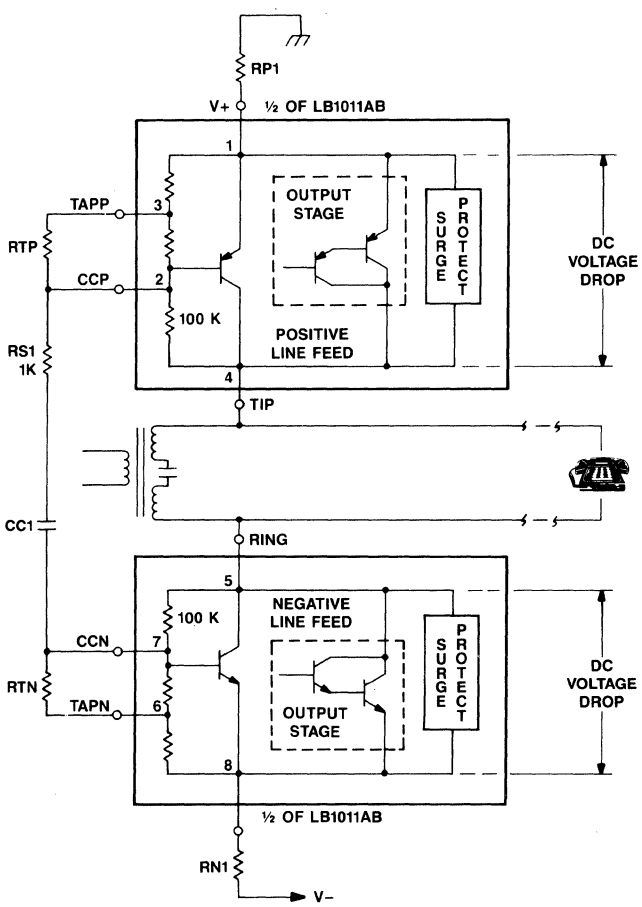
Maximum Ratings

Rating	Value	Unit
Ambient Operating Temperature Range	−20 to +70	°C
Storage Temperature Range	−40 to +125	°C
Pin Temperature (Soldering, 15 sec)	300	°C
Operating Voltages (dc Voltage Drop)	−4.00 to +4.85	V

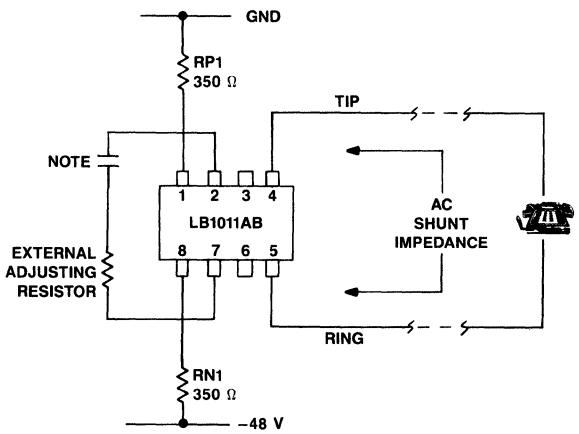
8-Pin Plastic DIP



Functional Diagram

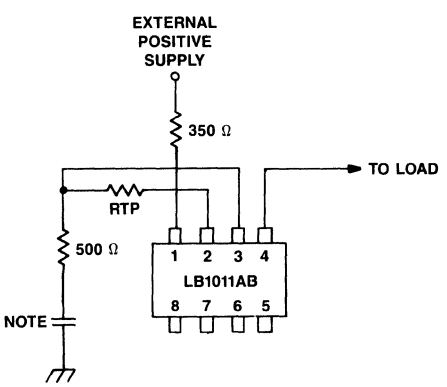


Battery Feed Application Diagram (Balanced Configuration)



Note: Capacitor value based on frequency requirements.

ac Blocking, dc Current Feed Applications



Note: Capacitor value based on frequency requirements.

AT&T

ANALOG
High-Voltage Solid State Relays

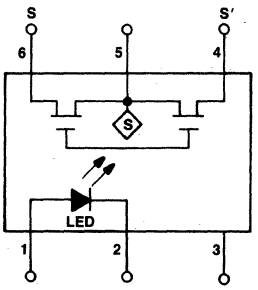
Description

AT&T's multi-purpose, solid-state relays are low-cost bi-directional linear switches that can replace mechanical relays for audio and dc applications. These relays can be controlled by TTL levels and feature 1500 Vrms of input/output isolation and internal current limiting. Maximum output ratings of 440 volts per pole with maximum current loads to 225 mA are available. Typical applications are telephone switchhook, high-voltage testers, industrial controls, and isolation switching.

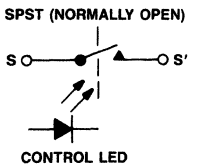
Features

- Low ON-Resistance
- Clean, bounce-free switching
- High solid-state reliability
- Low power consumption
- Noise-free operation
- High-surge capability
- dv/dt typically better than 500 V/μs
- No electromagnetic interference

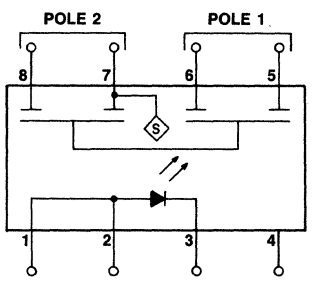
SPST Functional Diagram



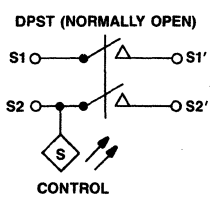
Equivalent Relay Diagram



DPST Functional Diagram



Equivalent Relay Diagram



Typical Electrical Characteristics T_A = 25°C

	SPST				DPST	
Parameter	**LH1056AT**	**LH1085AT**	**LH1191AT**	**LH1192AT**	**LH1061AB**	**LH1193AB**
Operating Voltage	350 V	350 V	280 V	440 V	200 V	280 V
Peak Load Current	100 mA	225 mA	100 mA	100 mA	200 mA	200 mA
Typical ON-Resistance @ 25 mA	30 Ω	30 Ω	25 Ω	50 Ω	12 Ω	25 Ω

For additional information, contact your AT&T Account Manager, or call:
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WE 32103 DRAM Controller

Description

The *WE* 32103 DRAM Controller provides the control and interface required between the *WE* 32100 CPU and commercially available dynamic RAM memories. It can be used with DRAMs as large as the AT&T 1-Mbit memory device, control 16 Mbytes of DRAM, and drive as many as 88 DRAM devices without external buffers. The *WE* 32103 DRAM Controller uses a pre-translation technique allowing it to work in parallel with a memory management unit (MMU). With an MMU in the system, the DRAM controller can respond to a CPU-initiated read in five clock cycles. While the MMU is translating a paged virtual address into a corresponding physical address, the DRAM controller initiates the actual memory access. This is possible because the low order bits of the virtual address do not change during virtual-to-physical address translation.

Data Sizes

The *WE* 32103 DRAM Controller supports byte, half-word, word, double-word, and quad-word accesses. The designer can interface any commercially available DRAMs using the controller's configuration registers to match the design properties of the selected DRAM.

Error Detection and Correction

High-performance fault-tolerant systems can be designed using commercially available error detection and correction units (EDCs) with the DRAM controller. The controller provides all of the signals needed to interface to an EDC unit. For high reliability applications, programmable support is provided for periodic error scrubbing and automatic check-bit initialization.

Other Features

A dual-ported memory can be configured using two DRAM controllers and ordinary DRAM devices. Additionally, the controller can be programmed to provide a wide variety of refresh schemes using an internal programmable refresh timer and an external refresh request input.

Military Specification Device

The 10 MHz and 14 MHz DRAM controllers are scheduled to be offered in military versions in 1989. The controllers will meet military standard 883C and possibly the Joint Army-Navy (JAN) qualification.

Features

- Low-power, 1.5-micron, CMOS technology
- 10-, 14-, and 18-MHz operations
- Overlaps memory accesses with MMU address translation
- Provides 5-cycle access for CPU, CPU/MMU, and CPU/MMU/DMAC systems
- Supports double- and quad-word memory access
- Full support for error detection and correction devices
- Drives up to 88 DRAM devices without external buffers
- Controls a variety of DRAM configurations including 1-Mbit DRAM devices
- Internal refresh timer and refresh address counter
- Programmable DRAM access times
- Programmable support for page and nibble mode DRAM
- Supports dual-ported memory configurations using two DRAM controllers

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WE 32104 DMA Controller

Description

The *WE* 32104 DMA Controller provides the ability to transfer large amounts of data quickly and efficiently between the main memory subsystem and I/O devices or between different memory locations. The DMA controller permits the full 32-bit system bus to be used without external logic and provides a separate 8-bit peripheral bus to decouple I/O devices from the system bus. This allows concurrent operation with the CPU as well as greater system throughput. Four independent prioritized DMA channels are provided. Request chaining allows multiple transfer requests to be serviced without CPU intervention.

The DMA controller has four independent channels that allow it to serve four unrelated requests simultaneously. Each channel has a set of registers that configures and controls its operations. In addition there is one mask register shared by four channels.

System Bus Interface — provides address, data, and control signals needed to interface the *WE* 32104 DMA Controller to the *WE* 32100 Microprocessor.

Data Buffers — each of the four channels has a 32-byte data buffer. The lowest address data buffer is used as the memory fill data register (MFDR). This register contains the data written to consecutive locations during memory fill operations.

Register File — contains eight control registers for each DMA channel and one global register. The control registers consist of source address, destination address, transfer count, base address, mode, device control, interrupt vector, and status and control registers. The global register is a mask register used to disable particular channel activity.

Address Arithmetic Unit (AAU) — calculates addresses of source and destination using information from the per channel registers and the data size and request generator.

Count Arithmetic Unit (CAU) — calculates number of bytes to be transferred using information from the per channel registers and the data size and request generator.

Packing Registers — used to pack bytes into larger operands when transferring from the peripheral bus to the system bus. Also, to unpack large system bus operands to bytes when transferring to the peripheral bus.

Peripheral Bus — used to communicate with 8-bit I/O devices.

Military Specification Device

The 10 MHz and 14 MHz DMA controllers are scheduled to be offered in military versions in 1989. The controllers will meet military standard 883C and possibly the Joint Army-Navy (JAN) qualification.

Features

- Low-power, 1.5-micron, CMOS technology
- 10-, 14-, and 18-MHz operation
- Full 32-bit address and data buses
- 8-bit peripheral bus for decoupling I/O devices from the system bus
- Double- and quad-word bus cycles available for high system throughput
- Internal data buffers to support burst data peripherals
- Four independent prioritized DMA channels
- Two programmable interrupt vectors per channel
- Memory-to-memory transfers at rates up to 14.4 Mbytes/s at 18 MHz
- Memory-to-peripheral transfers at rates up to 9.0 Mbytes/s at 18 MHz (with burst mode)

WE 32204 DMA Controller

Description

The *WE* 32204 DMA Controller is a memory-mapped peripheral device that performs memory-to-memory, memory-to-peripheral, peripheral-to-memory, and memory fill data transfers quickly and efficiently. The DMA controller contains specialized hardware that permits transfers at a much faster rate than possible under microprocessor control. When used with the *WE* 32200 Microprocessor, the *WE* 32204 DMA Controller permits the full 32-bit width of the system bus to be used without external interfacing logic. In addition, a peripheral bus is provided to decouple 8-bit input/output devices from the system bus.

The DMA controller has four independent channels, which allow it to serve four unrelated transfer requests simultaneously. Each channel has a set of registers that configures and controls its operation. In addition, there is one mask register that is shared between the four channels. When the DMA controller is in peripheral mode, registers within the DMA controller and registers within devices connected to the peripheral bus are accessed by the CPU. This procedure provides the CPU an access path to the peripheral bus. The seven functional elements of the DMA controller are:

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System Bus Interface — provides the address, data, and control signals needed to interface the DMA controller to the *WE* 32200 Microprocessor.

Data Buffers — each of the four channels has a 32-byte data buffer. The lowest address data buffer is used as the memory fill data register (MFDR). This register contains the data that is written to consecutive locations during memory fill operations.

Register File — contains eight control registers for each DMA channel and one global register. The control registers consist of source address, destination address, transfer count, base address, mode, device control, interrupt vector, and status and control registers. The global register is a mask register used to disable particular channel activity.

Address Arithmetic Unit (AAU) — calculates the addresses of source and destination using information from the per channel registers and the data size and request generator.

Count Arithmetic Unit (CAU) — calculates the number of bytes to be transferred using information from the per channel registers and the data size and request generator.

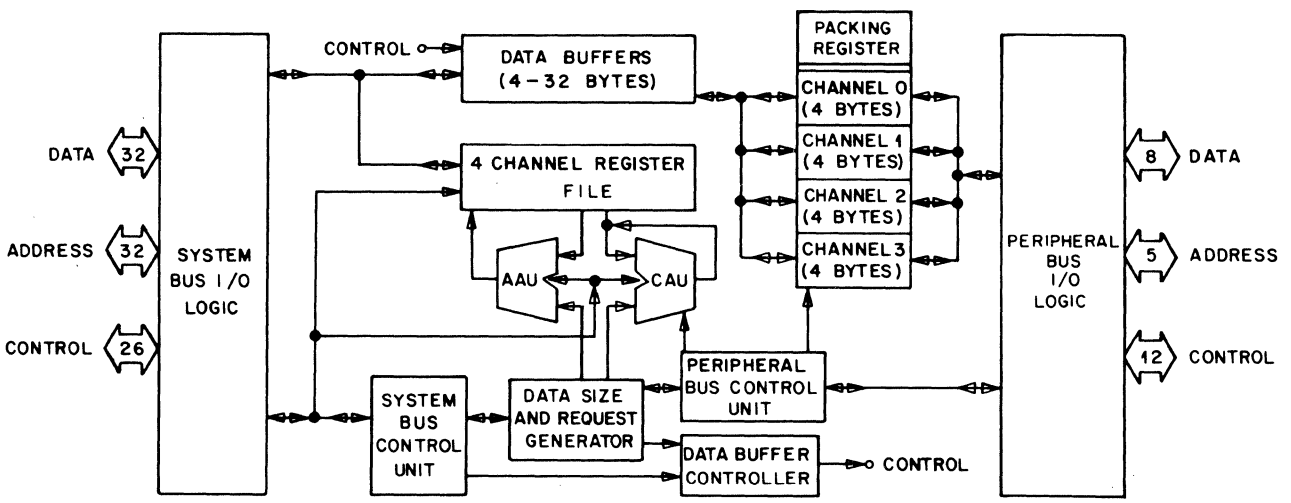
Packing Registers — used to pack bytes into larger operands when transferring from the peripheral bus to the system bus. Also, it is used to unpack large system operands to bytes when transferring to the peripheral bus.

Peripheral Bus — used to communicate with 8-bit I/O devices.

Features

- Low-power, CMOS technology
- 24-MHz frequency operation
- Full 32-bit address and data buses
- 8-bit peripheral bus for decoupling I/O devices from the system bus
- Double- and quad-word bus cycles available for high system throughput
- Internal data buffers to support burst data peripherals
- Four independent prioritized DMA channels
- Two programmable interrupt vectors per channel
- Memory-to-memory transfers at rates of up to 19.2 Mbytes/s at 24 MHz
- Memory-to-peripheral transfers at rates of up to 12.0 Mbytes/s at 24 MHz (with burst mode)
- Memory fill operations available for writing an arbitrary constant to a block of memory

WE *32104 and 32204 DMA Controller Block Diagram*



AAU – ADDRESS ARITHMETIC UNIT
CAU – COUNT ARITHMETIC UNIT

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LOW DRIFT

Low offset voltage drift vs temperature performance in both FET and bipolar input types is obtained by our sophisticated drift compensation techniques. First, the drift is measured and then special laser trim techniques are used to minimize the drift and the initial offset voltage at 25°C. Finally, "max drift" performance is retested for conformance with specifications.

LOW DRIFT (≤5μV/°C) **Boldface = NEW**

Description	Model	Offset Voltage, max: At 25°C, (±mV)	Offset Voltage, max: Temp Drift, (±μV/°C)	Bias Current (25°C), max (nA)	Open Loop Gain, min (dB)	Frequency Response: Unity Gain (MHz)	Frequency Response: Slew Rate (V/μs)	Rated Output, min: (±V)	Rated Output, min: (±mA)	Temp Range[1]	Pkg	Page
FET	**OPA627M**	**0.1**	**0.8**	**20**	**110**	**16**	**45**	**12**	**30**	**Ind**	**TO-99**	**2-174**
	OPA627P	**0.25**	**2**	**50**	**104**	**16**	**40**	**12**	**30**	**Ind**	**DIP**	**2-174**
	OPA111M	0.25	1	±0.001	120	2	2	11	5	Ind	TO-99	2-55
Wideband	OPA156M	2	5	0.05	94	6	14	10	5	Mil	TO-99	2-80
	OPA356M	2	5	0.05	94	6	14	10	5	Com	TO-99	2-80
	OPA602M	**0.25**	**2**	**±.001**	**92**	**6.5**	**28**	**10**	**15**	**Ind**	**TO-99**	**2-145**
	OPA602P	**0.5**	**5**	**±.002**	**88**	**6.5**	**24**	**10**	**15**	**Ind**	**DIP**	**2-145**
	OPA606M	0.5	5	±0.01	100	13	35	12	5	Com	TO-99	2-158
Dual FET	OPA2111M	0.5	2.8	±0.004	114	2	2	11	5	Ind	TO-99	2-195
	OPA2107P	**0.5**	**5**	**0.006**	**80**	**5**	**15**	**11**	**10**	**Ind**	**DIP**	**2-193**
Bipolar	OPA27J, Z	0.025	0.6	±40	120	8	1.9[3]	12	16.6	Mil	TO-99, DIP	2-27
	OPA37J, Z	0.025	0.6	±40	120	63[2]	11.9[3]	12	16.6	Mil	TO-99, DIP	2-27
	OPA27P	0.100	1.8	±80	117	8	1.9[3]	12	16.6	Com	DIP	2-27
	OPA37P	0.100	1.8	±80	117	63[2]	11.9[3]	12	16.6	Com	DIP	2-27
Low Power	OPA21Z	0.1	1	25	120	0.3	0.2	13	5	Ind	DIP	2-21

NOTES: (1) Com = 0°C to +70°C, Ind = −25°C to +85°C, Mil = −55°C to +125°C. (2) Gain-bandwidth product for OPA37. A_V = 5 min. (3) Typical.

LOW BIAS CURRENT

Our many years of experience in designing, manufacturing and testing FET amplifiers gives us unique abilities in providing low and ultra low bias current op amps. These amplifiers offer bias currents as low as 75fA (75 x 10^{-15}A) and voltage drift as low as 1μV/°C. With offset voltage laser-trimmed to as low as 250μV, the need for expensive trim pot adjustments is eliminated.

LOW BIAS CURRENT (≤50pA) **Boldface = NEW**

Description	Model	Offset Voltage, max: At 25°C, (±mV)	Offset Voltage, max: Temp Drift, (±μV/°C)	Bias Current (25°C), max (pA)	Open Loop Gain, min (dB)	Frequency Response: Unity Gain (MHz)	Frequency Response: Slew Rate (V/μs)	Rated Output, min: (±V)	Rated Output, min: (±mA)	Temp Range[1]	Pkg	Page
FET	OPA111M	0.25	1	±1	120	2	2	11	5	Ind	TO-99	2-55

(Continued on next page.)

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LOW BIAS CURRENT (≤50pA) (Continued) — **Boldface = NEW**

Description	Model	Offset Voltage, max: At 25°C, (±mV)	Offset Voltage, max: Temp Drift, (±µV/°C)	Bias Current (25°C), max (pA)	Open Loop Gain, min (dB)	Frequency Response: Unity Gain (MHz)	Frequency Response: Slew Rate (V/µs)	Rated Output, min (±V)	Rated Output, min (±mA)	Temp Range[1]	Pkg	Page
FET	**OPA627M**	**0.1**	**0.8**	**20**	**110**	**16**	**45**	**12**	**30**	**Ind**	**TO-99**	**2-174**
	OPA627P	**0.25**	**2**	**50**	**104**	**16**	**40**	**12**	**30**	**Ind**	**DIP**	**2-174**
Low Noise	OPA101M	0.25	5	–10	94	10	6.5	12	12	Ind	TO-99	2-43
	OPA102M	0.25	5	–10	94	40	14	12	12	Ind	TO-99	2-43
Ultra-Low Bias Current	OPA128M	0.5	5	±0.075	110	1	3	10	5	Com	TO-99	2-72
	AD515H	1	25	0.075	88	0.35	1	10	5	Com	TO-99	2-13
Dual FET	OPA2111M	0.5	2.8	±4	114	2	2	11	5	Ind	TO-99	2-195
	OPA2111P	2	15	±15	106	2	2	11	5	Com	DIP	2-195
	OPA2107P	**0.5**	**5**	**6**	**80**	**5**	**15**	**11**	**10**	**Ind**	**DIP**	**2-193**
Quad FET	OPA404G	0.75	3[2]	±4	92	6.4	35	12	5	Ind	DIP	2-94
	OPA404P	2.5	5[2]	±12	88	6.4	35	11.5	5	Com	DIP	2-94
Low Cost	OPA121M	2	10	±5	110	2	2	11	5	Com	TO-99	2-66
	OPA121P	3	10	±10	106	2	2	11	5	Com	DIP	2-66
	OPA602M	**0.25**	**2**	**1**	**92**	**6.5**	**28**	**10**	**15**	**Ind**	**TO-99**	**2-145**
	OPA602P	**0.5**	**5**	**2**	**88**	**6.5**	**24**	**10**	**15**	**Ind**	**TO-99**	**2-145**
Wideband	OPA606M	0.5	5	±10	100	13	35	12	5	Com	TO-99	2-145
	OPA606P	3	10[2]	±25	90	12	30	11	5	Com	DIP	2-145

NOTES: (1) Com = 0°C to +70°C, Ind = –25°C to +85°C, Mil = –55°C to +125°C. (2) Typical.

LOW NOISE

Now both FET and bipolar input op amps are offered with guaranteed low noise specifications. Until now the designer had to rely on "typical" specs for his demanding low noise designs. These fully characterized parts allow a truly complete error budget calculation.

LOW NOISE (Very Low e_N) — **Boldface = NEW**

Descrip.	Model	Noise Voltage at 10kHz, max (nV/√Hz)	Bias Current (25°C), max (pA)	Offset Voltage, max: at 25°C (±mV)	Offset Voltage, max: Temp Drift (±µV/°C)	Open Loop Gain, min (dB)	Frequency Response: Gain BW (MHz)	Frequency Response: Slew Rate, min (V/µs)	Rated Output, min (±V)	Rated Output, min (±mA)	Temp Range[1]	Pkg	Page
Bipolar	OPA27J, Z	3.8	±40nA	0.025	0.6	120	8	1.9[2]	12	16.6	Mil	TO-99, DIP	2-27
	OPA37J, Z	3.8	±40nA	0.025	0.6	120	63	11.9[2]	12	16.6	Mil	TO-99, DIP	2-27
Wide Bandwidth	OPA101M	8	–10	0.25	5	94	20	5	12	12	Ind	TO-99	2-43
	OPA102M	8	–10	0.25	5	94	40	10	12	12	Ind	TO-99	2-43
FET	OPA111M	8	±1	0.25	1	120	2	1	11	5	Ind	TO-99	2-55
	OPA602M	**12[2]**	**1**	**0.25**	**2**	**92**	**6.5**	**28**	**10**	**15**	**Ind**	**TO-99**	**2-145**

(Continued on next page.)

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LOW NOISE (Very Low e_N) (Continued) — **Boldface = NEW**

Descrip.	Model	Noise Voltage at 10kHz, max (nV/√Hz)	Bias Current (25°C), max (pA)	Offset Voltage, max at 25°C (±mV)	Offset Voltage, max Temp Drift (±µV/°C)	Open Loop Gain, min (dB)	Frequency Response Gain BW (MHz)	Frequency Response Slew Rate, min (V/µs)	Rated Output, min (±V)	Rated Output, min (±mA)	Temp Range[1]	Pkg	Page
FET	**OPA627M**	**5.4**	**20**	**0.1**	**0.8**	**110**	**16**	**45**	**12**	**30**	**Ind**	**TO-99**	**2-174**
	OPA627P	**6.2**	**50**	**0.25**	**2**	**104**	**16**	**40**	**12**	**30**	**Ind**	**DIP**	**2-174**
Low Cost	OPA27P	4.5	±80nA	0.100	1.8	117	8	1.9[2]	10	16.6	Com	DIP	2-27
	OPA37P	4.5	±80nA	0.100	1.8	117	63	11.9[2]	10	16.6	Com	DIP	2-27
Dual FET	OPA2111M	8	±4	0.5	2.8	114	2	1	11	5	Ind	TO-99	2-195
	OPA2111P	6[2]	±15	2	15	106	2	1	11	5	Com	DIP	2-195

NOTES: (1) Ind = –25°C to +85°C, Mil = –55°C to +125°C, Com = 0°C to +70°C. (2) Typical.

UNITY-GAIN BUFFER (POWER BOOSTER)

These versatile amplifiers boost the ouput current capability of another amplifier; buffer an impedance that might load a critical circuit; and may be used inside the feedback loop of another op amp to form a current-boosted, composite amplifier. Currents as high as ±200mA are available with speeds of 2000V/µs.

UNITY-GAIN BUFFER — **Boldface = NEW**

Description	Model	Rated Output, min (±V)	Rated Output, min (±mA)	Frequency Responses –3dB (MHz)	Frequency Responses Full Power (MHz)	Slew Rate (V/µs)	Gain (V/V)	Input Impedance (Ω)	Temp Range[1]	Pkg	Page
High Performance	3553AM	10	200	300	32	2000	≈1	10^{11}	Ind	TO-3	2-225
Low Cost	**OPA633H, P**	**11**	**80**	**275**	**65**	**2500**	**≈1**	**1.5 x 10^6**	**Ind**	**TO-8, DIP**	**2-176**

NOTE: (1) Ind = –25°C to +85°C.

WIDE BANDWIDTH

Design expertise in wideband circuits combines with our fully developed technology to create cost-effective wideband op amps. Burr-Brown high-speed amplifiers also offer outstanding DC performance specifications.

WIDE BANDWIDTH (≥5MHz)

Descrip.	Model	Frequency Response Gain BW (MHz)	Frequency Response Slew Rate min (V/µs)	Frequency Response t_S ±0.1% (ns)	Comp	Rated Output, min (±V)	Rated Output, min (±mA)	Offset Voltage, max At 25°C (±mV)	Offset Voltage, max Temp Drift (±µV/°C)	Open Loop Gain, min (dB)	Temp Range[1]	Pkg	Page
FET	OPA156M	6	10	1.5µs	int	10	5	2	5	94	Mil	TO-99	2-80
	OPA356M	6	10	1.5µs	int	10	5	2	5	94	Com	TO-99	2-80

(Continued on next page.)

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WIDE BANDWIDTH (≥5MHz) (Continued) **Boldface = NEW**

Descrip.	Model	Frequency Response: Gain BW (MHz)	Slew Rate min (V/µs)	t_S ±0.1% (ns)	Comp	Rated Output, min (±V)	Rated Output, min (±mA)	Offset Voltage, max: At 25°C (±mV)	Offset Voltage, max: Temp Drift (±µV/°C)	Open Loop Gain, min (dB)	Temp Range[1]	Pkg	Page
FET	**OPA602M**	**6.5**	**28**	**600**	**int**	**10**	**15**	**0.25**	**2**	**92**	**Ind**	**TO-99**	**2-145**
	OPA602P	**6.5**	**24**	**600**	**int**	**10**	**15**	**0.5**	**5**	**88**	**Ind**	**TO-99**	**2-145**
(Dual)	**OPA2107**	**5**	**15**	**1µs**	**int**	**11**	**10**	**0.5**	**5**	**80**	**Ind**	**DIP**	**2-193**
	OPA605C	200, A=1000	300[3]	300	ext	10	30	0.5	5	96[3]	Ind	DIP	2-152
	OPA606M	13	25	1µs	int	12	5	0.5	5[2]	100	Com	TO-99	2-158
	OPA606P	12	20	1µs	int	11	5	3	10[2]	90	Com	TO-99	2-158
	OPA627M	**16**	**45**	**400**	**int**	**12**	**30**	**0.1**	**0.8**	**110**	**Ind**	**TO-99**	**2-174**
	OPA627P	**16**	**40**	**400**	**int**	**12**	**30**	**0.25**	**2**	**104**	**Ind**	**DIP**	**2-174**
	3554M	1700, A=1000	1000	120	ext	10	100	1	15	100	Ind	TO-3	2-229
	3551	50, A=10	250	400	ext	10	10	1	50[2]	88	Com	TO-99	2-221
	3550	20, A=1	100	400	int	10	10	1	50[2]	88	Com	TO-99	2-217
Bipolar	3508	100, A=100	20	—	ext	10	10	5	30[2]	98	Com	TO-99	2-215
	3507	20, A=10	80	200	ext	10	10	10	30[2]	83	Com	TO-99	2-213
Quad FET	OPA404G	6.4	28	600	int	11.5	5	0.75	3[2]	92	Ind	DIP	2-94
	OPA404P	6.4	24	600	int	11.5	5	2.5	5[2]	88	Com	DIP	2-94
Low Noise Bipolar	OPA27	8,A=1	1.9[2]	—	int[3]	12	16.6	0.025	0.6	120	Mil	TO-99, DIP	2-27
	OPA37	63,A=5	11.9[2]	—	int[3]	12	16.6	0.025	0.6	120	Mil	TO-99, DIP	2-27
Low Noise FET	OPA101M	20, A=100	5	2.5µs	int	12	12	0.25	5	94	Ind	TO-99	2-43
	OPA102M	40, A=100	10	1.5µs	int	12	12	0.25	5	94	Ind	TO-99	2-43
Fast Settling	**OPA600M**	**5000, A=1000**	**500**	**80**	**ext**	**9**	**180**	**4**	**40**	**86**	**Ind**	**DIP**	**2-137**
Very Fast Settling Precision	**OPA620**	**170**	**200[2]**	**10**	**int**	**2.7**	**150[2]**	**0.5**	**5[2]**	**55**	**Com, Mil**	**DIP**	**2-166**
	OPA621	**250, A=10**	**1000[2]**	**10**	**ext**	**2.7**	**150[2]**	**0.5**	**5[2]**	**55**	**Com, Mil**	**DIP**	**2-170**
Very Fast Settling	**OPA675G**	**3000, A=16**	**200**	**15**	**ext**	**2.1**	**30**	**1**	**5**	**65**	**Com, Mil**	**DIP**	**2-186**
Switched Input	**OPA676G**	**3000, A=16**	**200**	**15**	**ext**	**2.1**	**30**	**1**	**5**	**65**	**Com, Mil**	**DIP**	**2-186**
Low Cost	OPA27P	8,A=1	1.9[2]	—	int	12	16.6	0.100	1.8	117	Com	DIP	2-27
	OPA37P	63, A=5	11.9[2]	—	int[3]	12	16.6	0.100	1.8	117	Com	DIP	2-27
Wide Temp Range	OPA11HT	12,A=1	4	1.5µs	ext	10	15	5[2]	5	98	–55/+200°C	TO-99	2-17
	OPA27HT	6,A=1	1.9	—	int	12	16.6[2]	0.050	0.25[2]	120	–55/+200°C	TO-99	2-39

NOTES: (1) Com = 0°C to +70°C, Ind = –25°C to +85°C, Mil = –55°C to +125°C. (2) Typical. (3) G = 5 min. for OPA37.

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HIGH VOLTAGE, HIGH CURRENT — **Boldface = NEW**

Description	Model	Rated Output, min (±V)	Rated Output, min (±mA)	Offset Voltage, max At 25°C (±mV)	Offset Voltage, max Temp Drift (±µV/°C)	Bias Current (25°C), max (pA)	Frequency Response Unity Gain (MHz)	Frequency Response Slew Rate (V/µs)	Open Loop Gain (dB)	Temp Range[1]	Pkg	Page
High Power	OPA501M	26	10A	5	40	20nA	1	1.35	98	Ind	TO-3	2-109
	OPA511M	22	5A	10	65	40	1	1	91	Ind	TO-3	2-117
	OPA512BM	35	10A	6	65	30	4	2.5	110	Ind	TO-3	2-122
	OPA512SM	35	15A	3	40	20	4	2.5	110	Mil	TO-3	2-122
	OPA541M	**35**	**5A**	**1**	**30**	**50**	**1.6**	**8**	**90**	**Ind**	**TO-3**	**2-127**
(Dual)	**OPA2541M**	**35**	**5A**	**1**	**30**	**50**	**1.6**	**8**	**90**	**Ind**	**TO-3**	**2-205**
	OPA550	**35**	**2A**	**1**	**30**	**50**	**3**	**15**	**90**	**Ind**	**TO-220**	**2-135**
	3573M	20	2A[4]	10	65	40nA	1	2.6	94	Ind	TO-3	2-243
	3572M	30	2A[4]	2	40	100	0.5	3	94	Ind	TO-3	2-237
	3571M	30	1A[3]	2	40	100	0.5	3	94	Ind	TO-3	2-237
Wideband	3554M	10	100	1	15	50	1700[2]	1200	100	Ind	TO-3	2-229
High Voltage	3584M	145	15	3	25	20	20[2]	150	126	Com	TO-3	2-255
	3583M	140	75	3	25	20	5	30	118	Ind	TO-3	2-251
	3582	145	15	3	25	20	5	20	118	Com	TO-3	2-247
	3581	70	30	3	25	20	5	20	112	Com	TO-3	2-247
	3580	30	60	10	30	50	5	15	106	Com	TO-3	2-247
	OPA445BM	35	15	3	10	50	2	10	100	Ind	TO-99	2-104
Buffer	3553M	10	200	50	300[5]	200	300	2000	NA	Ind	TO-3	2-225
	OPA633	**11**	**80**	**15**	**33[5]**	**35µA**	**275[5]**	**2500**	**NA**	**Ind**	**TO-8, DIP**	**2-176**

NOTES: (1) Com = 0°C to +70°C, Ind = –25°C to +85°C, Mil = –55°C to +125°C. (2) Gain-bandwidth product. (3) 2A peak. (4) 5A peak. (5) Typical.

SPECIAL PURPOSE

These op amps offer specialized performance or function, including devices with wide temperature range, low quiescent current, and switched inputs.

SPECIAL PURPOSE — **Boldface = NEW**

Description	Model	Offset Voltage, max At 25°C, (±mV)	Offset Voltage, max Temp Drift, (±µV/°C)	Bias Current (25°C), max (nA)	Open Loop Gain, min (dB)	Frequency Response Unity Gain (MHz)	Frequency Response Slew Rate (V/µs)	Rated Output, min (±V)	Rated Output, min (±mA)	Temp Range[1]	Pkg	Page
Low Power	OPA21Z	0.1	1	25	120	0.3	0.2	13.7	1.4	Ind	DIP	2-21
Switchable Input	OPA201G	0.1	1	25	120	0.5	0.1	13.5	5	Com	DIP	2-86
Very Fast Settling	**OPA675G**	**1**	**5**	**35µA**	**65**	**185[3]**	**350**	**2.1**	**30**	**Com, Mil**	**DIP**	**2-186**
	OPA676G	**1**	**5**	**35µA**	**65**	**185[3]**	**350**	**2.1**	**30**	**Com, Mil**	**DIP**	**2-186**
Wide Temp Range	OPA11HT	5	5[2]	±25	94	12	7	10	15	–55°C to +175°C	TO-99	2-17
	OPA27HT	0.05	0.25[2]	1µA	120	6	1.9	12	16[2]	–55°C to +200°C	TO-99	2-39

NOTES: (1) Com = 0°C to +70°C, Ind = –25°C to +85°C Mil = –55°C to +125°C. (2) Typical. (3) –3dB BW at Gain of +10V/V.

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INSTRUMENTATION AMPLIFIERS

Boldface = NEW

Description	Model	Gain Range	Gain Accuracy, G=100 25°C, max(%)	Gain Drift, G=100 (ppm/°C)	Non-Linearity G=100 max(%)	Input Parameters CMR[6] min(dB)	Input Parameters Offset Voltage vs Temp max (µV/°C)	Dynamic Response, G=100 ±3dB BW (kHz)	Temp Range[1]	Pkg	Page
Very High Accuracy	INA104P	1-1000[2]	0.15	22	±0.003	96	±(0.25±10/G)	25	Com	DIP	3-34
	INA104M	1-1000[2]	0.15	22[3]	±0.003	96	±(0.25±10/G)	25	Ind	DIP	3-34
	INA101G	1-1000[2]	0.03	22[3]	±0.003	96	±(0.25±10/G)	25	Ind	DIP	3-11
	INA101P	1-1000[2]	0.3	22[3]	±0.007	90	±(2±20/G) typ	25	Com	DIP	3-11
Low Quiescent Power	INA102G	1,10,100, 1000	0.15	15	±0.02	90	±(2±5/G)	3	Ind	DIP	3-23
Fast Settling FET Input	INA110G	1,10,100, 200,500	0.1	20	±0.01	96	±(2±50/G)	470	Ind	DIP	3-65
	INA110P	1,10,100, 200, 500	0.2	6 typ	±0.02	87	±(2±20/G) typ	470	Com	DIP	3-65
Buffer, Unity-Gain Difference	3627M	1V/V,fixed	0.01[3]	5	±0.001[3]	100	20	800[3]	Ind	TO-99	3-158
	INA105M	1V/V,fixed	0.01[3]	5	±0.001[3]	86[5]	10	1000[3]	Ind	TO-99	3-45
	INA105P	1V/V,fixed	0.025[3]	5	±0.001[3]	72[5]	5 typ	1000[3]	Com	DIP	3-45
Gain of 10 Difference	**INA106M**	**10V/V,fixed**	**0.01[4]**	**10**	**±0.001[4]**	**100[5]**	**2**	**500[4]**	**Ind**	**TO-99**	**3-57**
	INA106P	**10V/V,fixed**	**0.025[4]**	**4 typ**	**±0.001[4]**	**86[5]**	**0.2 typ**	**500[4]**	**Com**	**DIP**	**3-57**
High Common Mode Voltage Difference (200VDC CMV)	**INA117G**	**1V/V,fixed**	**0.02[3]**	**10[3]**	**±0.001[3]**	**86[5]**	**20**	**200[3]**	**Ind**	**DIP**	**3-77**
	INA117P	**1V/V,fixed**	**0.05[3]**	**10[3]**	**±0.001[3]**	**74[5]**	**40**	**200[3]**	**Com**	**DIP**	**3-77**
4-20mA Loop Receiver	**RCV420BG**	**.3125V/mA**	**0.025**	**25**	**±0.001**	**86**	**25[7]**	**150**	**Ind**	**DIP**	**3-110**
	RCV420KP	**.3125V/mA**	**0.05**	**50**	**±0.001**	**74**	**50[7]**	**150**	**Com**	**DIP**	**3-110**

NOTES: (1) Com = 0°C to +70°C, Ind = –25°C to +85°C. (2) Set with external resistor. (3) Unity-gain. (4) Gain = 10. (5) No source imbalance. (6) DC to 60Hz, Gain = 10, 1kΩ unbalanced. (7) RTO.

PROGRAMMABLE GAIN AMPLIFIERS

Description	Model	Gain Range	Gain Accuracy, G=100 25°C, max(%)	Gain Drift, G=100 (ppm/°C)	Non-Linearity G=100 max(%)	Input Parameters CMR[6] min(dB)	Input Parameters Offset Voltage vs Temp max (µV/°C)	Dynamic Response, G=100 ±3dB BW (kHz)	Temp Range[1]	Pkg	Page
Noninverting Multiplexed Input	PGA100G	Gain set with 4-bit word 1, 2, 4, 8...128	0.02	10	±0.005	NA	6 typ	5MHz	Ind	DIP	3-85
	PGA102G	Gain set with 2-bit word 1, 10 100	0.01	20	±0.01		3,G=100	250	Ind	DIP	3-93
	PGA102P		0.02	50	±0.01		3,G=100	250	Com	DIP	3-93
Instrumentation Amplifier Input	PGA200G	Gain set with 2-bit word 1, 10, 100, 1000	0.02	10	±0.003	96	0.4,G=100	30	Ind	DIP	3-103
Differential Input	3606M	Gain set with 3-bit word 1, 2, 4, 8...1024	0.02	10	±0.004	90,G=1	±(1+20/G)	40	Ind	DIP	3-150

NOTES: (1) Com = 0°C to +70°C, Ind = –25°C to +85°C. (2) Set with external resistor. (3) Unity-gain. (4) Gain = 10 (5) No source imbalance. (6) DC to 60Hz, Gain = 10, 1kΩ unbalanced.

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PRECISION TRANSMITTERS

Description	Model	Span: Untrimmed Error, max (%)	Span: Non-linearity, max (%)	Span: Temp Drift[1] (ppm/°C)	Input Parameters: Offset Voltage max	Input Parameters: Offset Voltage vs Temp max (µV/°C)	Input Parameters: CMR, DC, min (dB)	Output Parameters: Current Range (mA)	Output Parameters: Offset Current Error, max (µA)	Output Parameters: FS Output Current Error, max (µA)	Temp Range[2]	Pkg	Page
Two-Wire	XTR100P	–3	0.01	±100	±25µV	±0.5	90	4-20	±4	±20	Ind	DIP	3-114
	XTR101G	–5	0.01	±100	±30µV	±0.75	90	4-20	±6	±30	Ind	DIP	3-126
	XTR101P	–5	0.01	±100	±100µV	±1.5	90	4-20	±19	±60	Ind[3]	DIP	3-126
Three-Wire and Current Source	XTR110G	0.2	0.005	30	—	—	—	4-20, 0-20, 5-25[4]	±16	±32	Ind	DIP	3-139
	XTR110P	0.6	0.025	50	—	—	—	4-20, 0-20, 5-25[4]	±64	±96	Com	DIP	3-139

NOTES: (1) With zero TC span resistor. (2) Com = 0°C to +70°C, Ind = –25°C to +85°C. (3) –40°C to +85°C. (4) Many more ranges with appropriate circuit.

TRANSFORMER-COUPLED AMPLIFIERS

Descrip	Model	Isolation Voltage (V): Cont Peak	Isolation Voltage (V): Pulse/ Test, Peak	Isolation Mode Rejection, typ: DC (dB)	Isolation Mode Rejection, typ: 60Hz (dB)	Leakage Current at Test Voltage (µA)	Iso Impedance (Ω)	Iso Impedance (pF)	Gain Nonlinearity max (%)	Gain Nonlinearity typ (%)	Voltage Drift max (±µV/°C)	Bias Current max	±3dB Freq (kHz)	Ext Iso Power Req	Temp[1]	Pg
High Isolation Voltage	3656G	±3500	±8000	160	125	0.5	10^{12}	6	±0.05	±0.03	5+ (1000/G_1)	100nA	30	No	Ind	4-108

NOTES: All packages are DIPs. (1) Ind = –25°C to +85°C.

OPTICALLY COUPLED AMPLIFIERS

Descrip	Model	Isolation Voltage (V): Cont Peak	Isolation Voltage (V): Pulse/ Test, Peak	Isolation Mode Rejection, typ: DC (dB)	Isolation Mode Rejection, typ: 60Hz (dB)	Leakage Current at Test Voltage (µA)	Iso Impedance (Ω)	Iso Impedance (pF)	Gain Nonlinearity max (%)	Gain Nonlinearity typ (%)	Voltage Drift max (±µV/°C)	Bias Current max	±3dB Freq (kHz)	Ext Iso Power Req	Temp[1]	Pg
Balanced Current Input	3650G	±2000	±5000	140	120	0.25[2]	10^{12}	1.8	±0.05	±0.02	5	10nA	15	Yes[3]	Ind	4-100
Balanced FET Input	3652G	±2000	±5000	140	120	0.25[2]	10^{12}	1.8	±0.1	±0.05	25	50nA	15	Yes	Ind	4-100
Low Drift Wide BW	ISO100P	750	2500	146[3]	108[3]	0.3	10^{12}	2.5	0.07	0.02	4[3]	10nA	60	Yes	Ind	4-8

NOTES: All packages are DIPs. (1) Ind = –25°C to +85°C. (2) At 240V/60Hz. (3) R_{IN} = 10k, Gain = 100.

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CAPACITOR COUPLED, HERMETICALLY SEALED AMPLIFIERS

Boldface = NEW

Descrip	Model	Isolation Voltage (V) Cont Peak	Isolation Voltage (V) Pulse/ Test, Peak	Isolation Mode Rejection, typ DC (dB)	Isolation Mode Rejection, typ 60Hz (dB)	Leakage Current at Test Voltage (μA)	Iso Impedance (Ω)	Iso Impedance (pF)	Gain Nonlinearity max (%)	Gain Nonlinearity typ (%)	Voltage Drift (±μV/°C) max	Bias Current max	±3dB Freq (kHz)	Ext Isol Power Req	Temp[1]	Pg
1500VAC Isolation	**ISO102B**	±2121	±4000	160	120	1.0	10^{14}	6	±0.025	±0.02	±250	100μA	70	Yes	Ind	4-20
	ISO120B	±2121	±3535[2]	160	115	0.5	10^{14}	2	±0.01	±0.005	±150	50μA	60	Yes	Ind	4-44
	ISO122	±2121	±3394		140	0.5	10^{14}	2	±0.01	±0.005	±200	50μA	50	Yes	Com	4-57
3500VAC Isolation	**ISO106B**	±4950	±8000	160	130	1.0	10^{14}	6	±0.012	±0.007	±250	100μA	70	Yes	Ind	4-20
	ISO121B	±4950	±5600[2]	160	115	0.5	10^{14}	2	±0.01	±0.005	±150	50μA	60	Yes	Ind	4-44

NOTES: All packages are DIPs. (1) Ind = –25°C to +85°C. Com = 0°C to +70°C. (2) Partial discharge voltage.

ISOLATION POWER SUPPLIES[1]

Boldface = NEW

Descrip	Model	Isolation Voltage (V) Cont Peak	Isolation Voltage (V) Pulse/ Test Peak	Input Voltage (VDC) min	Input Voltage (VDC) max	Leakage Current 240VAC 60Hz (μA)	Isolation Impedance (Ω)	Isolation Impedance (pF)	Current, Balanced Loads On All Outputs (mA) Rated	Current, Balanced Loads On All Outputs (mA) Max[1]	Sensitivity To Input Change (V/V)	Temp[2]	Pkg	Pg
Single ±15V Output	700	1500	4200	10	18	1	10^{10}	5	±3-30	±60	1.08	Ind	Mod	4-86
	700U	2000	5000	10	18	1	10^{10}	3	±3-30	±60	1.08	Ind	Mod	4-86
	PWS725	**2121**	**4000**	**7**	**18**	**1.2**	10^{12}	**9**	±15	±40	**1.15**	**Ind**	**DIP**	**4-65**
	PWS726	**4950**	**8000**	**7**	**18**	**1.2**	10^{12}	**9**	±15	±40	**1.15**	**Ind**	**DIP**	**4-65**
Dual ±15V Output	722	4950	8000	5	16	1	10^{10}	6	±3-40	±50	1.13	Ind	Mod	4-92
	PWS727	**2121**	**3394**	**10**	**18**	**1.5**	10^{14}	**8**	±15	±30	**1.15**	**Com**	**Mod**	**4-70**
	PWS728	**2121**	**3394**	**4.5**	**5.5**	**1.5**	10^{14}	**8**	±15	±30	**3.2**	**Com**	**Mod**	**4-73**
Quad ±15V Output	710	1000	3100	10	18	1	10^{10}	8	±9.5	±60	1.08	Ind	Mod	4-88
Quad ±8V Output	724	1000	3000	5	16	1	10^{10}	6	±3-16	±60	0.63	Ind	Mod	4-96
Multiple Output (1-8)	**PWS740**	**2121**	**4000**	**7**	**20**	**1.5**	10^{12}	**3**	**30[3]**	**60[3]**	**1.20**	Ind	**Sys[4]**	**4-76**
	PWS750	**2121**	**3394**	**4.5[5]**	**18[6]**	**1.5**	10^{14}	**8**	±15	**30**	**(7)**	**Com**	**Comp**	**4-83**

NOTES: (1) See complete Product Data Sheet for full specifications, especially regarding output current capabilities. (2) Ind = –25°C to +85°C. Com = 0°C to +70°C. (3) Per channel. (4) 1 TO-3 driver per 8 channels, plus 2 DIPs per channel. (5) 5V operation. (6) 15V operation. (7) 5V operation: 3.2; 15V operation: 1.15.

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CAPACITOR-COUPLED, WITH POWER — **Boldface = NEW**

Descrip	Model	Isolation Voltage (V) Cont Peak	Isolation Voltage (V) Pulse/ Test, Peak	Isolation Mode Rejection, typ DC (dB)	Isolation Mode Rejection, typ 60Hz (dB)	Leakage Current at Test Voltage (μA)	Iso Impedance (Ω)	Iso Impedance (pF)	Gain Nonlinearity max (%)	Gain Nonlinearity typ (%)	Voltage Drift (±μV/°C) max	Bias Current max	±3dB Freq (kHz)	Temp[1]	Pg
1500VAC Input Power	**ISO103**	**2121**	**3394**	**160**	**100**	**1.0**	**10^{12}**	**9**		**0.01**	**100[2]**	**50μA**	**30**	**Ind**	**4-34**
1500VAC Output Power	**ISO113**	**2121**	**3394**	**160**	**100**	**1.0**	**10^{12}**	**9**		**0.01**	**100[2]**	**50μA**	**30**	**Ind**	**4-41**
2500VAC Input Power	**ISO107**	**3535**	**5656**	**160**	**100**	**1.0**	**10^{12}**	**9**		**0.01**	**100[2]**	**50μA**	**30**	**Ind**	**4-34**

NOTES: All packages are DIPs. (1) Ind = –25°C to +85°C.

CAPACITATIVELY COUPLED VOLTAGE-TO-FREQUENCY CONVERTER — **Boldface = NEW**

Descrip	Model	Isolation Voltage (V) Cont Peak	Isolation Voltage (V) Pulse/ Test Peak	Leakage Current at Test Voltage (μA)	Isolation Impedance (Ω)	Isolation Impedance (pF)	Non-linearity at 1MHZ (typ)	Bias Current (max) (μA)	Operating Frequ (max) (kHz)	External Isolation Power Req	Temp[1]	Pg
1500V Isolation	**ISO108**	**2121**	**3394[2]**	**0.3 typ**	**10^{12}**	**3**	**0.01**	**250**	**4**	**Yes**	**Ind**	**4-38**

NOTES: Package is DIP. (1) Ind = –25°C to +85°C. (2) Partial discharge voltage.

Burr-Brown

MULTIPLIERS/DIVIDERS

You can select accuracy from 0.25% max and up from this complete line of integrated circuit multipliers. Most provide full four-quadrant multiplication. All are laser-trimmed for accuracy—no trim pots are needed to meet specified performance. These compact models bring the cost of high performance down to acceptable levels.

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MULTIPLIERS/DIVIDERS — **Boldface = NEW**

Model	Transfer Function	Error at +25°C max (%)	Temp Coeff (%/°C)	Feed-through (mV)	Offset Voltage (mV)	1% BW (kHz)	Temp Range[1]	Pkg	Page
MPY100	$[(X-X_2)(Y-Y_2)/10]+Z_2$	±0.5	0.008	30	7	70	Ind	TO-100	5-26
MPY534	$[(X-X_2)(Y-Y_2)/10]+Z_2$	±0.25	0.008	0.05%	2	3MHz	Com	TO-100	5-34
MPY634M	$[(X-X_2)(Y-Y_2)/10]+Z_2$	±0.5	0.015	0.15%	2	10MHz	Ind	TO-100	5-41
MPY634P	$[(X-X_2)(Y-Y_2)/10]+Z_2$	±2.0	0.03	0.3%	25	10MHz	Ind	DIP	5-41
AD632	**$[(X-X_2)(Y-Y_2)/10]+Z_2$**	**±0.5**	**0.01**	**0.15**	**15**	**50**	**Ind**	**TO-100**	**5-6.**

NOTE: (1) Com = 0°C to +70°C, Ind = –25°C to +85°C.

SPECIAL FUNCTIONS

This group of models offers many different functions that are the quick, easy way to solve a wide variety of analog computational problems. Most are in integrated circuit packages and are laser-trimmed for excellent accuracy.

SPECIAL FUNCTIONS

Function	Model	Description	Comments	Temp Range[1]	Pkg	Page
Multifunction Converter	4302	$Y(Z/X)^m$ This function may be used to multiply, divide, raise to powers, take roots and form sine and cosine functions.	Plastic Package.	Ind	DIP	5-109
	LOG100	$K \text{ Log } (I_1/I_2)$	Optimized for log ratio of current inputs. Specified over six decades of input (1nA to 1mA), 55mV total error, 0.25% log conformity.	Com	DIP	5-18
Logarithmic Amplifier	4127G 4127P	$K \text{ Log } (I_1/I_{REF})$	A more versatile part that contains an internal reference and a current inverter. 1% and 0.5% accuracy.	Com Com	DIP DIP	5-102 5-102
$\sqrt{\frac{1}{T}\int_0^T E_{IN}^2(t)\,dt}$	4341	True rms-to-DC conversion based on a log-antilog occupational approach.	Some external trimming required. Lower cost in plastic package. Pin compatible with 4340.	Ind	DIP	5-115
Peak Detector	4085	This is an analog memory circuit that holds and provides readout of a DC voltage equal to peak value of a complex input waveform.	Digital mode control provides reset capability and allows selection of peaks within a desired time interval. Maybe used to make peak-to-peak detector.	Com, Ind	DIP	5-94

NOTE: (1) Com = 0°C to +70°C, Ind = –25°C to +85°C.

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DIVIDERS

Using a special log/antilog committed divider design overcomes the major problem encountered when trying to use a multiplier in a divider circuit. Outstanding accuracy is maintained even at very low denominator voltages.

DIVIDERS

Model	Transfer Function	Input Range	Accuracy D = 250mV max (%)	Temp Coeff (%/°C)	0.5% BW (kHz)	Rated Output, min	Temp Range[1]	Pkg	Page
DIV100P	10 x N/D	250mV to 10V	0.25	0.2	15	±10V, ±5mA	Ind	DIP	5-10

NOTE: (1) Ind = –25°C to +85°C.

FREQUENCY PRODUCTS

This group of products consists of precision oscillators and active filters for both signal generation and attenuation. Both fixed frequency and user-selected frequency units are available.

FREQUENCY PRODUCTS

Function	Model	Description	Comments	Temp Range[1]	Pkg	Page
Oscillator	4423	Very-low cost in plastic package Provides resistor programmable quadrature outputs (sine and cosine wave outputs simultaneously available).	Frequency range: 0.002Hz to 20kHz. Frequency stability: 0.01%/°C. Quadrature phase error: ±0.1%.	Com	DIP	5-119
Universal Active Filter	UAF41 UAF21	These filters provide a complex pole pair. Based on state variable approach, low-pass, high-pass, and bandpass outputs are available.	Add only resistors to determine pole location (frequency and Q). Easily cascaded for complex filter responses.	Ind Ind	DIP DIP	5-82 5-74

NOTE: Com = 0°C to +70°C, Ind = –25°C to +85°C.

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VOLTAGE REFERENCE

These products are precision voltage references that provide a +10V output. The output can be adjusted with minimal effect on drift or stability.

VOLTAGE REFERENCE

Model	Output (V)	Min Output (mA)	Max Drift (ppm/°C)	Power Supply (V)	Power Supply (mA)	Temp Range[1]	Pkg	Page
REF10M	±10.00 ±0.005	10	1	+13.5/35	4.5	Com	TO-99	5-49
REF101M	±10.00 ±0.005	10	1	+13.5/35	4.5	Com	TO-99	5-55

NOTE: (1) Com = 0°C to +70°C.

CURRENT REFERENCE **Boldface = NEW**

Model	Output I (μA)	Compliance	Max Drift (ppm/°C)	Comments	Temp Range[1]	Pkg	Page
REF200M, P	**Dual 100±0.5**	**2.5V to 40V**	**25**	**Includes 0.5% accurate current mirror**	**Ind**	**DIP, TO-99**	**5-63**

NOTE: (1) Ind = –25°C to +85°C.

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DIGITAL-TO-ANALOG CONVERTERS SELECTION GUIDES

The Selection Guides show parameters for the high grade. Refer to the Product Data Sheet for a full selection of grades. Models shown in **boldface** are new products introduced since publication of the previous *Burr-Brown IC Data Book.*

INSTRUMENTATION DIGITAL-TO-ANALOG CONVERTERS — **Boldface = NEW**

Description	Model	Resolution (Bits)	Linearity Error (%FSR)	Settling Time (µs)	Output Range (V)	Temp Range[1]	Pkg[2]	Q, BI[3] Screen	Page
Very High Resolution	**DAC729**	**18**	**±0.00075**	**5**	**5,10,20 U/B[4]**	**Com**	**HCD**	**Q, BI**	**6.1-80**
High Resolution	DAC700	16	±0.0015	1	–2mA U	Com, Ind, Mil	HCD	Q, BI	6.1-43
	DAC701	16	±0.0015	8	10 U	Com, Ind, Mil	HCD	Q, BI	6.1-43
	DAC702	16	±0.0015	1	±1mA B	Com, Ind, Mil	HCD,PDIP	Q, BI	6.1-43
	DAC703	16	±0.0015	8	±10 B	Com, Ind, Mil	HCD,PDIP, SOIC	Q, BI	6.1-43
High Resolution	DAC70BH	16	±0.003	1	±1mA, 0 to –2mA U/B	Ind	HCD	Q, BI	6.1-5
	DAC71	16	±0.003	8	±1mA, –2mA, 10, 20 U/B	Com	HCD	Q, BI	6.1-13
	DAC72BH	16	±0.003	1	±1mA, –2mA, 10, 20 U/B	Ind	HCD	Q, BI	6.1-5
Bus Interface, High Resolution	DAC705	16	±0.003	8	±5V	Com, Ind, Mil	HCD	Q, BI	6.1-53
	DAC706	16	±0.003	1	±1mA	Com, Ind, Mil	HCD	Q, BI	6.1-53
	DAC707	16	±0.003	8	±10 B	Com, Ind, Mil	HCD, PDIP	Q, BI	6.1-53
	DAC708	16	±0.003	1	±1mA, U/B 0 to –2mA	Com, Ind, Mil	HCD	Q, BI	6.1-53
	DAC709	16	±0.003	8	±5,±10,10 U/B	Com, Ind, Mil	HCD	Q, BI	6.1-53
Dual, Bus Interface, High Resolution	**DAC725**	**16**	**±0.003**	**8**	**±5,±10,10 B**	**Com, Ind**	**HCD, PDIP**	**Q, BI**	**6.1-72**
Low Cost, High Resolution	DAC710	16	±0.003	8 typ	±1mA	Com	HCD		6.1-65
	DAC711	16	±0.003	8 typ	±10	Com	HCD		6.1-65
	DAC1600	16	±0.003	8 typ	±10 B	Com	PDIP		6.1-108
Low Cost, Bus Interface	DAC811	12	±0.006	4	±5,±10,10 U/B	Com, Ind, Mil	HCD, PDIP, SOIC	Q, BI	6.1-90
	DAC1201	12	±0.018	4 typ	±5,±10,10 U/B	Com	PDIP		6.1-103
CMOS, Industry Std	**DAC7541A**	**12**	**±0.012**	**1**	**Multiplying**	**Com, Ind, Mil**	**HCD, PDIP, SOIC**	**Q, BI**	**6.1-112**
	DAC7545	**12**	**±0.012**	**2**	**Multiplying**	**Com, Ind, Mil**	**HCD, PDIP, SOIC**	**Q, BI**	**6.1-120**

NOTES: (1) Temperature Range: Com = 0°C to +70°C, Ind = –25°C to +85°C, Mil = –55°C to +125°C. (2) HCD = Hermetic Ceramic DIP, PDIP = Plastic DIP, SOIC = Surface Mount Package. (3) Q indicates that optional reliability screening is available for the model. BI indicates that an optional 160 hour burn-in is available for the model. (4) U/B indicates the output voltage polarity range for the model: U = unipolar, B = bipolar.

(Continued on next page.)

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INSTRUMENTATION DIGITAL-TO-ANALOG CONVERTERS (Continued)

Description	Model	Resolution (Bits)	Linearity Error (%FSR)	Settling Time (µs)	Output Range (V)	Temp Range[1]	Pkg[2]	Q, BI[3] Screen	Page
Bus Interface	**DAC8012**	**12**	**±0.012**	**1**	**Multiplying**	**Com, Ind, Mil**	**HCD, PDIP, SOIC**	**Q, BI**	**6.1-127**
Lowest Cost Industry Std	DAC1200	12	±0.018	0.3, 3 typ	±1mA,–2mA, 10,20 U/B		PDIP		6.1-99
Low Cost Industry Std	DAC80	12	±0.012	0.3, 3 typ	±1mA,–2mA, 10,20 U/B	Com,Ind	HCD, PDIP	Q, BI	6.1-27
	DAC85H	12	±0.012	0.3, 3 typ	±1mA,–2mA, 10,20 U/B	Com,Ind	HCD	Q, BI	6.1-35
Military Temp Industry Std	DAC87H	12	±0.012	0.3, 3 typ	±1mA,–2mA, 10,20 U/B	Mil	HCD	Q, BI	6.1-35

NOTES: (1) Temperature Range: Com = 0°C to +70°C, Ind = –25°C to +85°C, Mil = –55°C to +125°C. (2) HCD = Hermetic Ceramic DIP, PDIP = Plastic DIP, SOIC = Surface Mount Package. (3) Q indicates that optional reliability screening is available for the model. BI indicates that an optional 160 hour burn-in is available for the model. (4) U/B indicates the output voltage polarity range for the model: U = unipolar, B = bipolar.

AUDIO, COMMUNICATIONS, DSP DIGITAL-TO-ANALOG CONVERTERS **Boldface = NEW**

Model	Resolution (Bits)	Linearity Error (%FSR)	Settling Time (µs)	Output Range (V)	Temp Range[1]	Pkg[2]	Q, BI[3] Screen	Page
DAC63	12	±0.012	50ns	±5, 10mA	Ind	24-p HDIP	NA	6.2-135
DAC65	**12**	**±0.012**	**40ns**	**±1.2, ±6.35mA**	**Ind**	**24-p HDIP**	**Q**	**6.2-143**
DAC812	12	±0.012	50ns	±5, 10mA	Ind	24-p HDIP	NA	6.2-146

Model	Resolution (Bits)	Max THD+N (V_{OUT} = ±FS)	Output Range (V)	Input Format	Supply Range (V)	Pkg	Power Dissipation (mW)	Page
PCM53	16	–88dB (JG)	±10 (–V) –88dB (JP) –92dB (KP)	Parallel ±1mA (–I)	±15, +5	24-p DIP	600	6.2-152
PCM54	16	–82dB (HP)	±3,±1mA –88dB (JP) –92dB (KP)	Parallel	±5 to ±12	28-p DIP	300	6.2-164
PCM55	16	–82dB (HP)	±3,±1mA –88dB (JP)	Parallel	±5 to ±12	24-p SOIC	125	6.2-164

NOTES: (1) Temperature Range: Com = 0°C to +70°C, Ind = –25°C to +85°C, Mil = –55°C to +125°C. (2) HCD = Hermetic Ceramic DIP, PDIP = Plastic DIP, SOIC = Surface Mount Package. (3) Q indicates that optional reliability screening is available for the model. BI indicates that an optional 160 hour burn-in is available for the model. (4) U/B indicates the output voltage polarity range for the model: U = unipolar, B = bipolar.

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AUDIO, COMMUNICATIONS, DSP DIGITAL-TO-ANALOG CONVERTERS (Continued) — **Boldface = NEW**

Model	Resolution (Bits)	Max THD+N (V_{OUT} = ±FS)	Output Range (V)	Input Format	Supply Range (V)	Pkg	Power Dissipation (mW)	Page
PCM56	16	–82dB (P) –88dB (P-J) –92dB (P-K)	±3, ±1mA	Serial Latched	±5 to ±12	16-p DIP	260	6.2-172
PCM60	16	–82dB (P) –88dB (P-J) –92dB (P-K)	2.8Vp-p 2-Channel	Serial Latched	+5	24-p SOIC	50	6.2-186
PCM58	18	–92dB (P) –94dB (P-J) –96dB (P-K)	±1mA	Serial Latched	+5, –12	28-p DIP	400	6.2-180
PCM64	18	–96dB	±1mA	Parallel	+5, –15	42-p "Shrink" DIP	400	6.2-194

NOTES: (1) Temperature Range: Com = 0°C to +70°C, Ind = –25°C to +85°C, Mil = –55°C to +125°C. (2) HCD = Hermetic Ceramic DIP, PDIP = Plastic DIP, SOIC = Surface Mount Package. (3) Q indicates that optional reliability screening is available for the model. BI indicates that an optional 160 hour burn-in is available for the model. (4) U/B indicates the output voltage polarity range for the model: U = unipolar, B = bipolar.

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ABOUT BURR-BROWN

Burr-Brown Corporation is a leading designer and manufacturer of precision microcircuits and microelectronic-based systems for use in data acquisition, signal conditioning, measurement, and control.

We make our products for customers who pursue business success much as we do—through worldwide competition based on high performance, high quality, and high value. Our customers include OEMs, sophisticated end-users, systems integrators, and VARs who demand an extra measure of performance for their products and operations.

COMPANY FACTS

- Founded in 1956.
- Corporate headquarters, Tucson, Arizona, U.S.A.
- 1500 employees.
- Manufacturing and technical facilities: Tucson; Livingston, Scotland; Atsugi, Japan.
- Sales and distribution subsidiaries in Austria, Belgium, England, France, Germany, Italy, Japan, the Netherlands, Sweden, and Switzerland; 19 international sales representative organizations worldwide.
- Over 300 sales and service staff worldwide.
- 800+ high-performance products.

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ANALOG MULTIPLEXERS SELECTION GUIDE

The Selection Guide shows parameters for all grades. Refer to the Product Data Sheet for additional information. Models shown in **boldface** are new products introduced since publication of the previous *Burr-Brown IC Data Book.*

ANALOG MULTIPLEXERS — **Boldface = NEW**

Description	Model	Channels	Input Range (V)	On Resistance max (Ω)	Settling Time (to 0.01%)	Temp Range[1]	Pkg[2]	Page
Protected Inputs	**HI3-0506A-5**	**16-channel single ended**	**±15**	**1.8k**	**3.5µs**	**Com**	**28-p PDIP**	**7-3**
	HI1-0506A-5	**16-channel single ended**	**±15**	**1.8k**	**3.5µs**	**Com**	**28-p CDIP**	**7-3**
	HI1-0506A-2	**16-channel single ended**	**±15**	**1.5k**	**3.5µs**	**Mil**	**28-p CDIP**	**7-3**
	HI3-0507A-5	**8-channel differential**	**±15**	**1.8k**	**3.5µs**	**Com**	**28-p PDIP**	**7-3**
	HI1-0507A-5	**8-channel differential**	**±15**	**1.8k**	**3.5µs**	**Com**	**28-p CDIP**	**7-3**
	HI1-0507A-2	**8-channel differential**	**±15**	**1.5k**	**3.5µs**	**Mil**	**28-p CDIP**	**7-3**
	HI3-0508A-5	**8-channel single ended**	**±15**	**1.8k**	**3.5µs**	**Com**	**16-p PDIP**	**7-13**
	HI1-0508A-5	**8-channel single ended**	**±15**	**1.8k**	**3.5µs**	**Com**	**16-p CDIP**	**7-13**
	HI1-0508A-2	**8-channel single ended**	**±15**	**1.5k**	**3.5µs**	**Mil**	**16-p CDIP**	**7-13**
	HI3-0509A-5	**4-channel differential**	**±15**	**1.8k**	**3.5µs**	**Com**	**16-p PDIP**	**7-13**
	HI1-0509A-5	**4-channel differential**	**±15**	**1.8k**	**3.5µs**	**Com**	**16-p CDIP**	**7-13**
	HI1-0509A-2	**4-channel differential**	**±15**	**1.5k**	**3.5µs**	**Mil**	**16-p CDIP**	**7-13**
High Speed	MPC800KG	16 single or 8 differential	±15	750	800ns	Com	CDIP	7-23
	MPC800SG	16 single or 8 differential	±15	750	800ns	Mil	CDIP	7-23
	MPC801KG	8 single or 4 differential	±15	750	800ns	Com	CDIP	7-30
	MPC801SG	8 single or 4 differential	±15	750	800ns	Mil	CDIP	7-30

NOTES: (1) Temperature Range: Com = 0°C to +70°C, Mil = –55°C to +125°C. (2) CDIP = Ceramic DIP, PDIP = Plastic DIP.

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SAMPLE / HOLD AMPLIFIERS
SELECTION GUIDES

The Selection Guides show parameters for the high grade. Refer to the Product Data Sheet for a full selection of grades. Models shown in **boldface** are new products introduced since publication of the previous *Burr-Brown IC Data Book.*

SAMPLE/HOLD AMPLIFIERS — **Boldface = NEW**

Description	Model	Gain Error (%)	Offset Error (mV)	Charge Offset (mV)	Acq Time (µs max)	Droop Rate (µV/ms)	Temp Range[1]	Pkg[2]	Q, BI[3] Screen	Page
Fast, High Accuracy	SHC76	±0.02	±3	±6 typ	3	1	Ind, Com, Mil	HMD	—	8-3
Fast, Industry Std	SHC85	±0.01	±2	±2 max	4.5	125	Com, Mil	HMD	Q	8-7
Low Cost, Fast Industry Std	SHC5320	NA	±0.5	±1 typ	1.5	0.5	Com, Mil	HCD	BI	8-32
Lowest Cost Industry Std	**SHC298**	**±0.01**	**±7**	**±25 max**	**10**	**100**	**Com, Ind**	**PDIP, MC, SOIC**	**BI**	**8-11**

HIGH-SPEED SAMPLE/HOLD AMPLIFIERS — **Boldface = NEW**

Description	Model	Gain Error (%)	Offset Error (mV)	Ampl BW –3dB, (MHz)	Acq Time (µs max)	Droop Rate (µV/µs)	Temp Range[1]	Input Range (Vp-p)	Pkg[2]	Q[3] Screen	Page
High Speed with Buffer	SHC803	±0.1	±3	16	0.35	±5	Ind	20	HDIP	Q	8-26
High Speed	SHC804	±0.1	±3	16	0.35	±5	Ind	20	HDIP	Q	8-26
Ultra-High Speed	SHC600	±0.1	±5	70	0.05	±180	Ind	2.5	CDIP	Q	8-18
	SHC601	**±2**	**±50**	**100**	**0.022**	**±100**	**Ind**	**2.5**	**CDIP**	**Q**	**8-22**
Very High Accuracy, Fast	**SHC702**	**±0.1**	**±3**	**3**	**0.8**	**±2**	**Ind**	**20**	**24-p DIP**	—	**9.2-118**

NOTES: (1) Temperature Range: Com = 0°C to +70°C, Ind = –25°C to +85°C, Mil = –55°C to +125°C. (2) MC = Metal Can, PDIP = Plastic DIP, HCD = Hermetic Ceramic DIP, CD = Ceramic DIP, HMD = Hermetic Metal DIP, SOIC = Surface Mount Package. (3) Q indicates optional reliability screening is available for this model. BI indicates that an optional 160 hour burn-in is available for the model.

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ANALOG-TO-DIGITAL CONVERTERS SELECTION GUIDES

The Selection Guide shows parameters for the high grade. Refer to the Product Data Sheet for a full selection of grades. Models shown in **boldface** are new products introduced since publication of the previous *Burr-Brown IC Data Book.*

INSTRUMENTATION ANALOG-TO-DIGITAL CONVERTERS — **Boldface = NEW**

Description	Model	Resolution (Bits)	Linearity Error (%FSR)	Input Range (V)	Conv Time (µs)	NMC Resolution	Temp Range[1]	Pkg[2]	Q, BI[3] Screen	Page
Serial Output	ADC804	12	±0.012	5,10,20 U/B[4]	17	12	Mil,Ind,Com	HCD	Q, BI	9.1-78
Low Cost Data-Bus Interface	ADC574A	12	±0.012	10, 20 U/B	25	12	Mil,Ind,Com	HCD, PDIP	Q, BI	9.1-52
	ADC674	12	±0.012	10, 20 U/B	15	12	Mil,Ind,Com	HCD, PDIP	Q, BI	9.1-62
	ADC774	**12**	**±0.012**	**10, 20 U/B**	**8**	**12**	**Mil,Ind,Com**	**HCD, PDIP**	**Q, BI**	**9.1-75**
Sampling Data-Bus Interface	**ADS807**	**12**	**±0.012**	**10, 20 U/B**	**10**	**12**	**Mil,Ind,Com**	**HCD**	**Q, BI**	**9.1-86**
	ADS808	**12**	**±0.012**	**10, 20 U/B**	**10**	**12**	**Mil,Ind,Com**	**HCD**	**Q, BI**	**9.1-86**
Low Cost	ADC80AG	12	±0.012	5, 10, 20 U/B	25	12	Ind	HCD	Q, BI	9.1-20
	ADC80MAH	**12**	**±0.012**	**5, 10, 20 U/B**	**25**	**12**	**Ind**	**HCD**	**Q, BI**	**9.1-36**
Medium Speed, Low Cost	**ADC84KG**	**12**	**±0.012**	**5, 10, 20 U/B**	**10**	**12**	**Ind**	**HCD**	**Q, BI**	**9.1-44**
	ADC85H	**12**	**±0.012**	**5, 10, 20 U/B**	**10**	**12**	**Com**	**HCD**	**Q, BI**	**9.1-44**
Medium Speed, Low Cost, Mil Temp	**ADC87H**	**12**	**±0.012**	**5, 10, 20 U/B**	**10**	**12**	**Mil**	**HCD**	**Q, BI**	**9.1-44**
High-Resolution Data-Bus Interface	**ADC700**	**16**	**±0.003**	**5, 10, 20 U/B**	**17**	**14**	**Mil, Ind, Com**	**HCD**	**BI**	**9.1-72**
High Resolution	ADC71	16	±0.003	5, 10, 20 U/B	50	14	Ind, Com	CD	Q, BI	9.1-4
	ADC72	16	±0.003	5, 10, 20 U/B	50	14	Ind, Com	MC	Q, BI	9.1-4
	ADC76	16	±0.003	5, 10, 20 U/B	17	14	Ind, Com	CD, MC	Q, BI	9.1-12

NOTES: (1) Temperature Range: Com = 0°C to +70°C, Ind = –25°C to +85°C, Mil = –55°C to +125°C. (2) HCD = Hermetic Ceramic DIP, PDIP = Plastic DIP, CD = Ceramic DIP, MC = Metal Can. (3) Q indicates optional reliability screening is available for this model. BI indicates that an optional 160 hour burn-in is available for this model. (4) U/B indicates the input voltage range for the model: U = unipolar, B = bipolar.

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AUDIO, COMMUNICATIONS, DSP ANALOG-TO-DIGITAL CONVERTERS — **Boldface = NEW**

Description	Model	Resolution (Bits)	Linearity Error (%FSR)	Input Range (V)	Conv Time (µs)	THD+N (Typ dB)	Temp Range[1]	Pkg[2]	Q[3] Screen	Page
Ultra-High Speed	**ADC600**	**12**	**±0.012**	**±1.25**	**0.1**	**68**	**Com, Ind**	**Module**		**9.2-89**
	ADC603	**12**	**±0.012**	**±1.25**	**0.1**	**68**	**Com, Mil**	**Special HDIP**		**9.2-110**
High Speed	ADC803	12	±0.012	10V/20V	1.5	NA	Ind, Mil	HMD	Q	9.2-124
	ADC601	**12**	**±0.012**	**10V/20V**	**1.0**	**70**	**Ind, Mil**	**HCD**		**9.2-107**
Very High Accuracy, High Speed	**ADC701**	**16**	**±0.0035**	**10V/20V**	**1.5**	**94**	**Com**	**40-p DIP**	—	**9.2-118**

	Model	Resolution (Bits)	Typical Linearity	Input Range (V)	Conv Time (µs)	Max THD+N (V_{IN} = ±FS)	Output Format	Pkg	Page
High Performance	PCM75	16	15-Bit 14-Bit	±2.5, ±5 ±10V	17	–84dB (JG) –88dB (KG)	Parallel or Serial	32-p DIP	9.2-136
Low Cost	**PCM78**	**16**	**14-Bit**	**±1.25**	**4**	**68**	**Serial**	**28-p DIP**	**9.2-145**

NOTES: (1) Temperature Range: Com = 0°C to +70°C, Ind = –25°C to +85°C, Mil = –55°C to +125°C. (2) HCD = Hermetic Ceramic DIP, HMD = Hermetic Metal DIP. (3) Q indicates optional reliability screening is available for this model.

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We have a large and competent field sales force, backed up by an experienced staff of technical applications specialists. They are eager to assist you in selecting the right product for your application. This free service is available from our Tucson-based headquarters and all sales offices.

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You can place orders via telephone, FAX, mail, TWX, or TELEX with any authorized Burr-Brown field sales office, sales representative, or our headquarters in Tucson. A complete list of sales offices is on the inside back cover of this book. When placing an order, please provide complete information, including model number with all option designations, product description or name, quantity desired, and ship-to and bill-to addresses. This will help us serve you most efficiently.

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VOLTAGE-TO-FREQUENCY CONVERTERS SELECTION GUIDE

The Selection Guide shows parameters for the high grade. Refer to the Product Data Sheet for a full selection of grades. Models shown in **boldface** are new products introduced since publication of the previous *Burr-Brown IC Data Book.*

VOLTAGE-TO-FREQUENCY CONVERTERS — **Boldface = NEW**

Description	Model	Frequency Range (kHz)	V_{IN} Range (V)	Linearity, max (% of FSR)	Tempco, max (ppm of FSR/°C)	Temp Range[1]	Pkg	Page
Low-Cost Monolithic	VFC32P VFC32M	User-selected 500kHz, max	User-selected	±0.01 at 10kHz ±0.05 at 100kHz	75 typ ±100	Com Ind	DIP TO-100	10-3 10-3
Low-Cost Complete	VFC42 VFC52	0 to 10 0 to 100	0 to +10 0 to +10	±0.01 ±0.05	±100 ±150	Ind Ind	DIP DIP	10-12 10-12
Precision Monolithic	VFC62 VFC320	User-selected, 1MHz max	User-selected	±0.002 at 10kHz ±0.002 at 10kHz	±20 ±20	Ind Ind	DIP, TO-100 for Both	10-18 10-54
Synochronized Monolithic	VFC100G	Clock Programmed, 2MHz max	0 to +10	0.1 at 1MHz	±50	Ind	DIP	10-26
	VFC101N	**Clock Programmed, 2MHz max**	**0 to +10, 0 to +5, 0 to +8, –5 to +5**	**±0.02 at 100kHz**	**±40**	**Ind**	**PLCC**	**10-41**
High-Performance	**VFC110**	**User-selected 4MHz max**	**0 to +10**	**±0.05 at 1MHz**	**±50**	**Ind**	**DIP**	**10-52**

NOTES: (1) Com = 0°C to +70°C, Ind = –25°C to +85°C.

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DATA ACQUISITION COMPONENTS SELECTION GUIDE

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DATA ACQUISITION COMPONENTS — **Boldface = NEW**

Model	Channels	Resolution (Bits)	Linearity Error (%FSR)	Input Range (V)[1]	Throughput Rate (kHz)	Temp Range[2]	Pkg[3]	Page
SDM862	**16 single ended**	**12**	**±0.012**	**10, 20 U/B**	**33**	**Com, Ind, Mil**	**LCC, PGA**	**11-3**
SDM863	**8 differential**	**12**	**±0.012**	**10, 20 U/B**	**33**	**Com, Ind, Mil**	**LCC, PGA**	**11-3**
SDM872	**16 single ended**	**12**	**±0.012**	**10, 20 U/B**	**50**	**Com, Ind, Mil**	**LCC, PGA**	**11-3**
SDM873	**8 differential**	**12**	**±0.012**	**10, 20 U/B**	**50**	**Com, Ind, Mil**	**LCC, PGA**	**11-3**

NOTES: (1) U/B indicates the input voltage range for the model: U = unipolar, B = bipolar. (2) Temperature Range: Com = 0°C to +70°C, Ind = –25°C to +85°C, Mil = –55°C to +125°C. (3) LCC = Hermetic 0.95" (typ) square Leadless Chip Carrier, PGA = Hermetic 1.1" (typ) square Pin Grid Array.

UNDERSTANDING COMPONENT MODEL NUMBERS

Most Burr-Brown component products in this book have model numbers in the following form:

ADC 80 M A H -12 /QM

- **/QM** — Quality Designator (optional)
- **-12** — Additional Performance Information (optional)
- **H** — Package Designator
- **A** — Performance Grade/Temp Range Designator
- **M** — Additional Performance Information (Second Generation, Improved Performance, etc.), 1 or 2 Letters (optional)
- **80** — Model Sequence Designator, 2 to 4 digits
- **ADC** — Product Type Prefix

Exceptions: Second-source products are marked as similarly to the original vendor's part number as possible.

Some products designed for digital audio and signal processing applications have model numbers as follows:

PCM 58 P -J

- **-J** — Performance Grade/Temp Range Designator
- **P** — Package Designator
- **58** — Model Sequence Designator, 2 to 4 digits
- **PCM** — Product Type Prefix

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INTRODUCTION & SELECTION GUIDES

Burr-Brown offers a wide selection of power conversion products. Hundreds of standard and unique DC/DC converters, including DIP sizes, high wattage, and wide-range modular packages are available. All carry Burr-Brown's guarantee of high quality and reliability.

The *Burr-Brown Power Sources Handbook* contains detailed Product Data Sheets for all of Burr-Brown's power conversion products. In addition, it includes supplementary data such as extensive Selection Guides, discussion of the advanced reliability programs available, a Glossary of power conversion terminology, and Application Notes for more effective use of these products. You'll also find information on how to get modified and custom products.

On the inside of the front cover is an index of all products in the handbook, listed in alphanumeric order. The inside back cover contains a directory of Burr-Brown sales offices and representatives.

ABOUT THE SELECTION GUIDES

Use the following Selection Guides to compare the many products in this book. Then refer to the Product Data Sheet for full specifications. Models shown in **boldface** are new products.

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HIGH-ISOLATION DC/DC CONVERTERS — **Boldface = NEW**

Model	Test Voltage (AC, V_{PEAK} 60Hz, 60s)	Rated Power (Watts)	Features	Page
PWR1726	**8000**	**1.5**	**High Isolation**	**66**
PWR70	5000	3	Small Size	29
PWS726	4950	450mW	High Isolation	82
PWR74	4000	3	Multichannel	35
PWR71	3000	3	Multichannel	31
PWR72	3000	3	Wide Input Range	33
PWR1XX Series	3000	450mW	General Purpose	37
PWR2XX Series	3000	1.5	General Purpose	39
PWR3XX Series	3000	2	Multichannel	41
PWR4XX Series	3000	3	Small Size	43
PWR6XX Series	3000	2	Regulated	47
PWR7XX Series	3000	5	Regulated	50
PWR1017	3000	3	Multichannel	55
PWS725	2121	450mW	High Isolation	82
PWS740	2121	0.9/Channel	Distributed Power	87

DIP-PACKAGED DC/DC CONVERTERS — **Boldface = NEW**

Model	Regulation	Internal Filtering	Features	Page
PWR11XX Series	**No**	**Yes**	**Filtered**	**59**
PWR13XX "Med-Pac" Series	**No**	**No**	**High Isolation**	**61**
PWR59XX Series	**Yes**	**Yes**	**Filtered**	**78**

MULTICHANNEL DC/DC CONVERTERS — **Boldface = NEW**

Model	Number of Channels	Number of Outputs Per Channel	Rated Power (Watts)	Features	Page
PWR1017	4	2	3	8 Outputs	55
PWR71	4	2	3	Small Size	31
PWR5XX Series	4	1 or 2	4	Small Size	45
PWR8XX Series	2	3 Total	5	5 ±12 or 5 ±15 V_{OUT}	53
PWR74	2	2	3	High Isolation	35
PWR3XX Series	2	1 or 2	2	Small Size	41
PWR53XX Series	**1 or 2**	**1 or 2**	**15**	**Wide Input Range**	**72**
PWS740	8	2	0.9/Channel	Distributed Power	87

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LOW-NOISE DC/DC CONVERTERS — **Boldface = NEW**

Model	Noise Out (mVp-p) Typ	Noise Out (mVp-p) Max	Rated Power (Watts)	Features	Page
PWR1546A		**1.0**	**5**	**Ultra-Low Noise**	**63**
PWR59XX Series	**20**		**2**	**DIP Package**	**78**
PWR6XX Series	30		3	Regulated	47
PWR7XX Series	30		5	Regulated	50
PWR74	40	100	3	High Isolation	35
PWR1726	**50**		**1.5**	**High Isolation**	**66**
PWR11XX Series	**50**		**3**	**DIP Package**	**59**
PWR1XX Series	50		2	General Purpose	37
PWR3XX Series	50		2	Multichannel	41
PWR53XX Series		**75**	**15**	**Wide Input Range**	**72**
PWR2XX Series	75		1.5	General Purpose	39
PWR70		80	3	High Isolation	29
PWR71		100	3	Multichannel	31
PWR4XX Series		100	3	Small Size	43
PWR1017		100	3	Multichannel	55

WIDE-INPUT-RANGE DC/DC CONVERTERS — **Boldface = NEW**

Model	Input Range (VDC)	Rated Power (Watts)	Features	Page
PWR53XX Series	**9-18**	**15**	**Single, Dual, & Triple Outputs**	**72**
	18-36	**15**	**Single, Dual, & Triple Outputs**	
	36-72	**15**	**Single, Dual, & Triple Outputs**	
PWR72	5-22	3	Dual Outputs	33
PWS740	7-20	0.9/Channel	Distributed Power	87

REGULATED DC/DC CONVERTERS — **Boldface = NEW**

Model	Regulation Line (%)	Regulation Load (%)	Rated Power (Watts)	Features	Page
PWR1546A	**±0.02**	**0.02**	**5**	**Low Noise**	**63**
PWR6XX Series	±0.02	0.04	3	General Purpose	47
PWR7XX Series	±0.02	0.04	5	General Purpose	50
PWR510X	±0.02	0.04	9	General Purpose	69
PWR59XX Series	**±0.3**	**0.4**	**2**	**DIP Package**	**78**
PWR53XX Series	**±0.2**	**1.0**	**15**	**Wide Input Range**	**72**

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UNREGULATED DC/DC CONVERTERS — **Boldface = NEW**

Model	Rated Power (Watts)	Package Size (Inches)	Features	Page
PWR1XX Series	450mW	1.0 x 1.0 x 0.4	General Purpose	37
PWS725	450mW	1.6 x 0.9 x 0.31	High Isolation	82
PWS726	450mW	1.6 x 0.9 x 0.31	High Isolation	82
PWR2XX Series	1.5	1.0 x 1.0 x 0.4	General Purpose	39
PWR1726	**1.5**	**1.2 x 1.6 x 0.4**	**High Isolation**	**66**
PWR11XX Series	**2**	**24-pin DIP**	**Filtered**	**59**
PWR3XX Series	2	1.0 x 1.0 x 0.4	Multichannel	41
PWR70	3	1.0 x 1.0 x 0.4	High Isolation	29
PWR71	3	2.0 x 2.0 x 0.4	Multichannel	31
PWR72	3	1.0 x 1.0 x 0.4	Wide Input Range	33
PWR74	3	1.0 x 1.0 x 0.4	Multichannel	35
PWR4XX Series	3	1.0 x 1.0 x 0.4	General Purpose	43
PWR1017	3	2.0 x 2.0 x 0.4	Multichannel	55
PWR5XX Series	4	1.2 x 1.6 x 0.4	Multichannel	45
PWR8XX Series	5	1.2 x 1.6 x 0.4	Multichannel	53
PWS740	0.9/Channel	Components	Distributed Power	87

DC/DC CONVERTERS BY WATTAGE — **Boldface = NEW**

Model	Rated Power (Watts)	Package Size (Inches)	Features	Page
PWR53XX Series	**15**	**2.5 x 3.5 x 0.7**	**Triple Output**	**72**
PWR510X	9	2.0 x 2.0 x 0.4	Regulated	69
PWR7XX Series	5	2.0 x 2.0 x 0.4	Regulated	50
PWR1546A	**5**	**2.0 x 2.0 x 0.4**	**Ultra-Low Noise**	**63**
PWR8XX Series	5	1.2 x 1.6 x 0.4	Multichannel	53

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CMD

G8880

Microcircuits

CMOS Integrated DTMF Transceiver

Features

- Advanced CMOS technology for low power consumption and increased noise immunity
- Complete DTMF Transmitter/Receiver within a single chip
- Standard 6500/6800 series microprocessor port
- Central office quality and performance
- Adjustable Guard Time
- Automatic Tone Burst mode
- Call Progress mode
- Single +5 volt power supply
- 20-pin DIP or 28-pin PLCC package

Applications

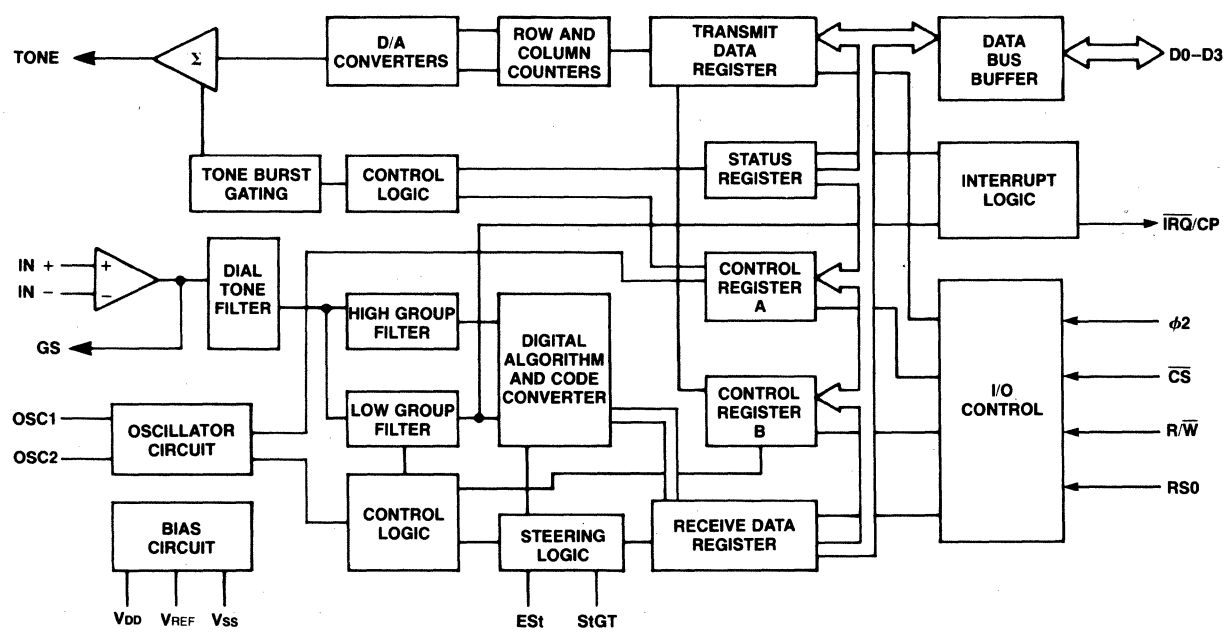
- Paging systems
- Repeater systems/mobile radio
- Interconnect dialers
- PABX systems
- Computer systems

General Description

The CMD G8880 is a fully integrated DTMF Transceiver, featuring Adjustable Guard Time, Automatic Tone Burst mode, Call Progress mode and a fully compatible 6500/6800 microprocessor interface. The G8880 is manufactured using state-of-the-art Advanced CMOS technology for low power consumption and precise data handling. The G8880 is based on the industry standard G8870 DTMF Receiver, while the transmitter utilizes a switched-capacitor D/A converter for low distortion, highly accurate DTMF signalling. Internal counters provide an Automatic Tone Burst mode which allows tone bursts to be transmitted with precise timing. A Call Progress filter can be selected by an external microprocessor for analyzing Call Progress tones.

California Micro Devices

Block Diagram



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CMD G8870

Microcircuits

CMOS DTMF Integrated Receiver

Features

- CMOS technology for low power consumption—35 mW max.
- Full DTMF receiver
- Provides DTMF high and low group filtering
- Adjustable acquisition and release times
- Dial tone suppression
- Integrated bandsplit filter and digital decoder functions
- On-chip differential amplifier, clock oscillator, and latched three-state bus.
- Uses inexpensive 3.58 MHz crystal
- Central office quality and performance
- Single +5 volt power supply
- 18-pin DIP or 20-pin PLCC package

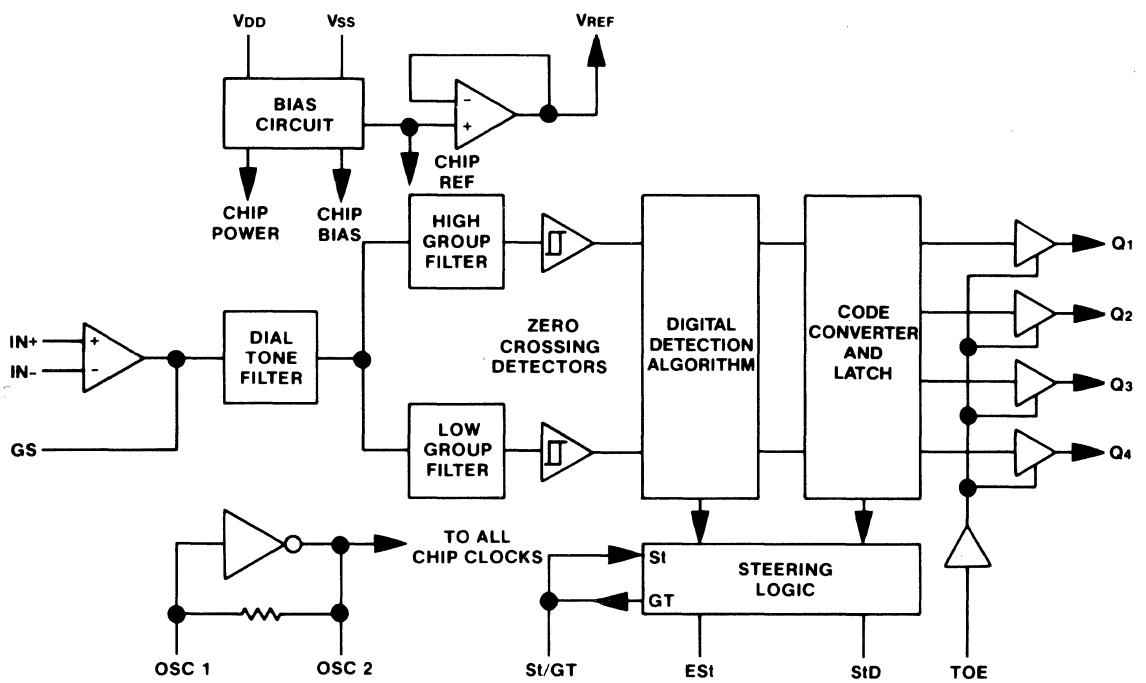
Applications

- PABX
- Central office
- Key systems
- Mobile radio
- Remote control
- Remote data entry

General Description

The CMD G8870 provides full DTMF receiver capability by integrating both the bandsplit filter and digital decoder functions into a single 18-pin DIP or 20-pin PLCC package. The G8870 is manufactured using state-of-the-art CMOS process technology for low power consumption (35 mW max.) and precise data handling. The filter section uses a switched capacitor technique for both high and low group filters and dial tone rejection. The G8870 decoder uses digital counting techniques for the detection and decoding of all 16 DTMF tone pairs into a 4-bit code. The G8870 minimizes external component count by providing an on-chip differential input amplifier, clock generator, and a latched three-state interface bus. The on-chip clock generator requires only a low cost TV crystal as an external component.

Block Diagram



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CMD

G65SC150

Microcircuits

CMOS Communications Terminal Unit (Telecommunication Microcomputer)

Features

- Generates signals compatible with switched telephone networks or packet switched data networks
- Provides Dial Pulse (DP), Dual Tone Multi-Frequency (DTMF), and 0-600 baud modem signaling capabilities
- Low power mode (300 μA) enables telephone line-powered operation
- External microprocessor address and data bus facilitates memory and I/O expansion
- On-chip memory: 2K bytes ROM
  64 bytes RAM
- Standard DTMF and modem frequencies can be generated which are accurate to ±1.0% with a 3.58 MHz crystal
- Two sine wave generators
- 6800 and 6500 bus compatibility
- Utilizes G65SC00 microprocessor as CPU
- 27 TTL compatible I/O lines
- Bus expandable to address 65K bytes of external memory
- Single +5 volt power supply
- Available in 68-pin chip carriers

General Description

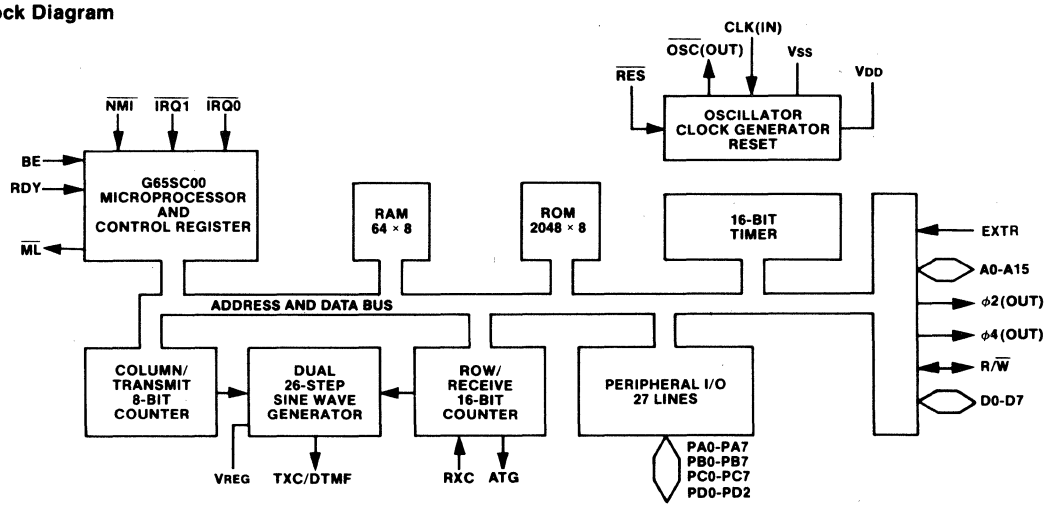
The CMD G65SC150 Communications Terminal Unit (CTU) is a single chip telecommunications microcomputer manufactured using state-of-the-art silicon gate CMOS process technology, which is optimized for telephone line signaling and data transmission applications. A functional block diagram is shown which illustrates the major system functions that are included on the integrated circuit.

The CTU uses the CMD G65SC00 8-bit microprocessor which executes the complete G65SC00 series instruction set. With 2K bytes of ROM and 64 bytes of RAM, the CTU operates as a single-chip microcomputer.

The internal bus interconnects all microcomputer functions. The address and databus buffers permit expansion of ROM, RAM and memory mapped I/O using the full 65K addressing space of the microprocessor. A peripheral mode is available for use with multiprocessor systems. A test and prototyping mode switches internal ROM addresses to external access. An on-chip oscillator may be driven by an external clock source.

The telecommunications interface circuitry consists of a timer, row/receive counter, column/transmit counter and dual sine wave generators. In addition, 27 general purpose I/O lines can be used for keyboard, telephone Dial Pulse (DP) signaling, phone line control, and other peripheral devices.

Block Diagram



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CMD

G65SC802
G65SC816

Microcircuits

CMOS 8/16-Bit Microprocessor Family

Features

- Advanced CMOS design for low power consumption and increased noise immunity
- Emulation mode for total software compatibility with 6502 designs
- Full 16-bit ALU, Accumulator, Stack Pointer, and Index Registers
- Direct Register for "zero page" addressing
- 24 addressing modes (including 13 original 6502 modes)
- Wait for Interrupt (WAI) and Stop the Clock (STP) instructions for reduced power consumption and decreased interrupt latency
- 91 instructions with 255 opcodes
- Co-Processor (COP) instruction and associated vector
- Powerful Block Move instructions

Features (G65SC802 Only)

- 8-Bit Mode with both software and hardware (pin-to-pin) compatibility with 6502 designs (64 KByte memory space)
- Program selectable 16-bit operation
- Choice of external or on-board clock generation

Features (G65SC816 Only)

- Full 16-bit operation with 24 address lines for 16 MByte memory
- Program selectable 8-Bit Mode for 6502 coding compatibility.
- Valid Program Address (VPA) and Valid Data Address (VDA) outputs for dual cache and DMA cycle steal implementation
- Vector Pull ($\overline{VP}$) output indicates when interrupt vectors are being fetched. May be used for vectoring/prioritizing interrupts
- Abort interrupt and associated vector for interrupting any instruction without modifying internal registers
- Memory Lock ($\overline{ML}$) for multiprocessor system implementation

General Description

The G65SC802 and G65SC816 are ADV-CMOS (ADVanced CMOS) 16-bit microprocessors featuring total software compatibility with 8-bit NMOS and CMOS 6500 series microprocessors. The G65SC802 is pin-to-pin compatible with 8-bit 6502 devices currently available, while also providing full 16-bit internal operation. The G65SC816 provides 24 address lines for 16 MByte addressing, while providing both 8-bit and 16-bit operation.

Each microprocessor contains an Emulation (E) mode for emulating 8-bit NMOS and CMOS 6500-Series microprocessors. A software switch determines whether the processor is in the 8-bit emulation mode or in the Native 16-bit mode. This allows existing 8-bit system designs to use the many powerful features of the G65SC802 and G65SC816.

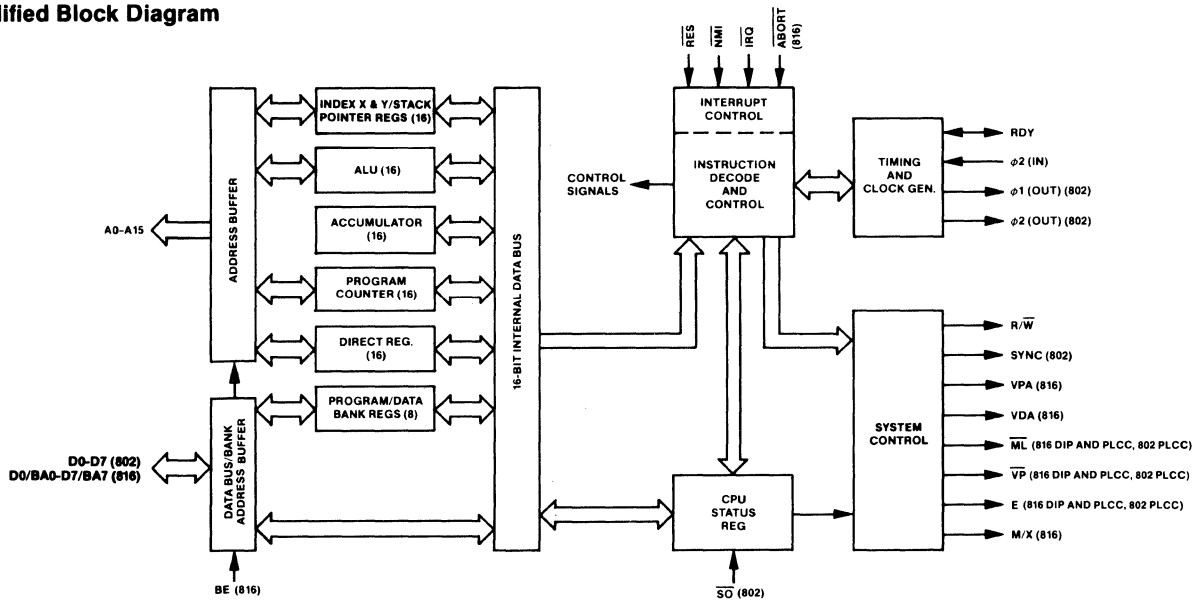
The G65SC802 and G65SC816 provide the system engineer with many powerful features and options. A 16-bit Direct Page Register is provided to augment the Direct Page addressing mode, and there are separate Program Bank Registers for 24-bit memory addressing. Other valuable features include:

- An Abort input which can interrupt the current instruction without modifying internal registers.
- Valid Data Address (VDA) and Valid Program Address (VPA) outputs which facilitate dual cache memory by indicating whether a data or program segment is being accessed.
- Vector modification by simply monitoring the Vector Pull ($\overline{VP}$) output.
- Block Move instructions.

CMD Microcircuits' G65SC802 and G65SC816 microprocessors offer the design engineer a new freedom of design and application, and the many advantages of state-of-the-art ADV-CMOS technology.

California Micro Devices

Simplified Block Diagram



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CMD

Microcircuits

C3052
C3053
C3054
C3057

CMOS Monolithic Serial Interface PCM Codec/Filter Family

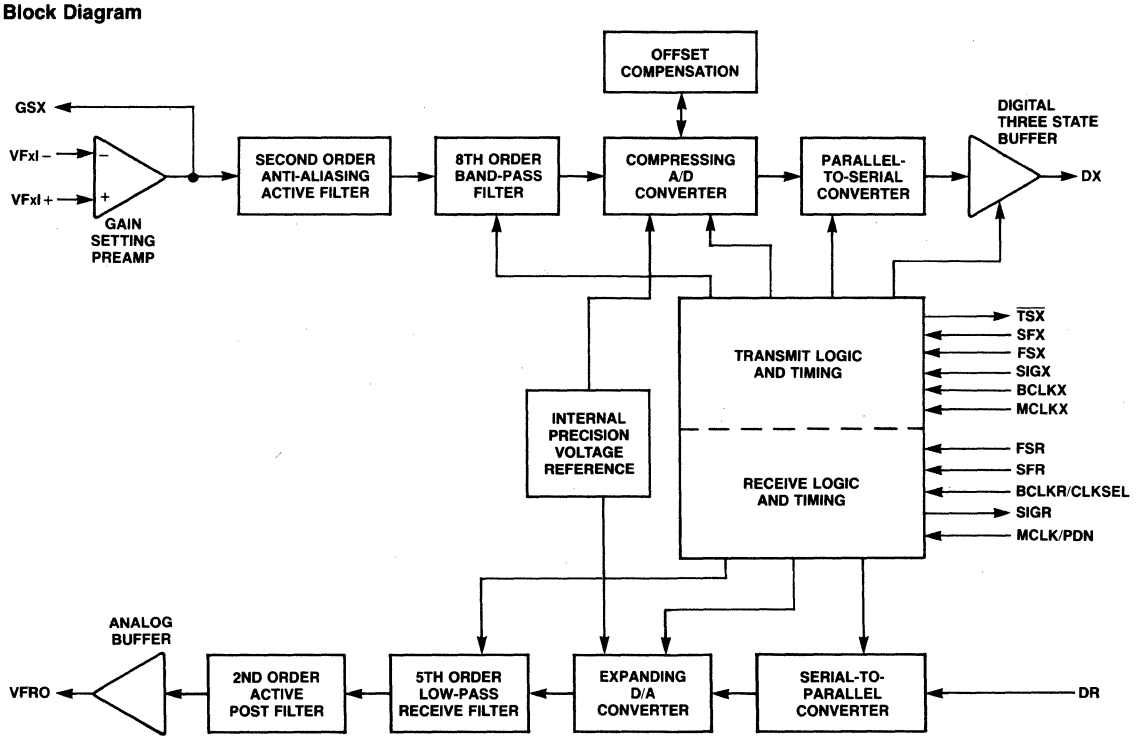
General Description

CMD's family of CMOS monolithic μ-law and A-law CODEC/filter circuits provide precision A/D and D/A signal conversion as well as the transmit and receive filtering required for companded PCM systems. Within each device, the encode section features an input gain adjust amplifier, an active RC anti-aliasing filter, offset compensation circuitry, and a switched-capacitor band-pass filter for rejecting frequencies outside a 200 to 3400 Hz band. Filtered signals are sampled and encoded into the compressed μ-law or A-law format and shifted out through the serial interface. The decode section features an expanding decoder for reconstructing the μ-law or A-law encoded signal, a low-pass filter with Sin x/x correction followed by an active RC smoothing filter, and a output power amplifier capable of driving low impedance loads. All devices within the CMD CODEC/filter family meet or exceed AT&T D3/D4 and CCITT specifications, and are manufactured using CMD's state-of-the-art CMOS process technology for increased noise immunity, higher reliability and reduced power consumption.

Features

- Four complete CODEC/filtering systems:
  - C3052 — μ-law with signaling (18 pin version)
  - C3053 — μ-law with signaling (20 pin version)
  - C3054 — μ-law without signaling (16 pin version)
  - C3057 — A-law (16 pin version)
- Pin compatible with industry standard (3052,53,54,57)
- Low power CMOS design; 60 mW operating (typ), 3 mW standby (typ)
- Low-pass and high-pass transmit filtering
- Receive low-pass filtering with Sin x/x correction
- Resistor programmable gain setting preamp for transmit section
- Synchronous or asynchronous transmit and receive operation
- Serial I/O interface
- 1.536 MHz, 1.544 MHz, or 2.048 MHz master clock timing; variable bit clock timing from 64 KHz to 2.048 MHz
- Short and long frame sync timing
- Active RC anti-aliasing and post filters
- Precision internal voltage reference and offset compensation circuits
- Automatic power-down by removing frame sync's and/or single pin power-down
- TTL or CMOS compatible interface
- ± 5V power input

Block Diagram



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G65SC51

Microcircuits

CMOS Asynchronous Communications Interface Adapter

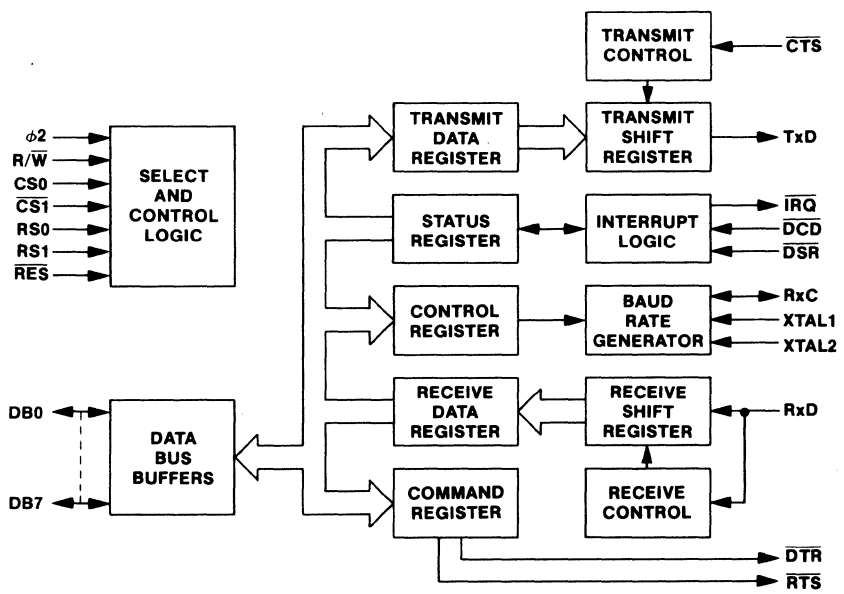
Features

- CMOS process technology for low power consumption
- 15 programmable baud rates (50 to 19,200 baud)
- External 16X clock input for nonstandard baud rates to 125,000 baud
- Programmable interrupt and status registers
- Full-duplex or half-duplex operating modes
- Selectable 5, 6, 7, 8 or 9 bit transmission rates
- Programmable word length, parity generation and detection, and number of stop bits
- Programmable parity options—odd, even, none, mark or space
- Includes data set and modem control signals
- False start bit detection
- Serial echo mode
- Four operating frequencies—1, 2, 3 and 4 MHz
- Available in 28-pin DIP or PLCC package

General Description

The CMD G65SC51 is an Asynchronous Communications Interface Adapter which offers many versatile features for interfacing 6500/6800 microprocessors to serial communication data sets and modems. The G65SC51's most significant feature is its internal baud rate generator, allowing programmable baud rate selection from 50 to 19,200 baud. This full range of baud rates is derived from a single standard 1.8432 MHz external crystal. For non-standard baud rates up to 125,000 baud, an external 16X clock input is provided. In addition to its powerful communications control features, the G65SC51 offers the advantages of CMD's leading edge CMOS technology, i.e., increased noise immunity, higher reliability, and greatly reduced power consumption.

Block Diagram



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CMD

G65SCXX Series
G65SC1XX Series

Microcircuits

CMOS G65SCXXX 8-Bit Microprocessor Family

Features

- CMOS family that is compatible with NMOS 6500 series microprocessors
- Uses single +5 volt power supply
- Low power consumption (4mA @ 1 MHz) allows battery-powered operation
- Enhanced instruction set: 27 additional op codes encompassing eight new instructions enhance software performance compared to existing NMOS 6500 microprocessor instruction set
  —64 microprocessor instructions
  —178 operational codes
  —15 addressing modes
- Choice of 4K, 8K or 65K-byte addressable memory
- 1, 2, 3 or 4 MHz operation
- Choice of external or on-board clock generator operation
- On-board clock generator/oscillator can be driven by an external single-phase clock input, an RC network, or a crystal circuit
- Advanced memory access timing (ϕ4) on selected versions
- Early address valid allows use with slower memories
- Early write data for dynamic memories
- 8-bit parallel processing
- Decimal and binary arithmetic
- Pipeline architecture
- Programmable stack pointer
- Variable length stack
- Interrupt capability
- Non-maskable interrupt
- 8-bit bidirectional data bus
- "Ready" input (for single cycle execution)
- Direct memory access capability
- Bus compatible with M6800
- Available on selected versions, a memory lock output and bus enable input signals simplify multiprocessor designs

General Description

The G65SCXXX is a totally software-compatible microprocessor family manufactured using the state-of-the-art silicon gate CMOS process. The family consists of two series of devices: one series, designated G65SCXX is pin-to-pin compatible with NMOS versions of the 6500 currently on the market; the other series, designated G65SC1XX includes several enhancements not available with other designs. The family provides the designer with a wide selection of addressable memory ranges, on-board or external clocks, and input interrupt options. All of the microprocessors are software compatible within the group and all are bus compatible with MC6800 products.

As shown in Table I, the family includes 18 microprocessors of which three have on-chip oscillators while the others require an external clock generator. The G65SC02, G65SC102 or G65SC112 clock generator circuit may be driven by an external crystal (Figure 2a), an RC network (Figure 2b) or by an external clock source. The versions of the microprocessor which require an external clock source are generally intended for multiprocessor applications where maximum timing control is necessary. The three family members with on-chip oscillators are intended for high performance, low cost operations where single phase inputs, crystals, or RC inputs provide the time base.

Ten of the microprocessors in the G65SCXX Series are pin-to-pin compatible with the NMOS 6500 microprocessors offered by several other manufacturers. However, the use of the leading-edge CMOS process technology ensures several software or programming enhancements not available to users of the NMOS 6500. The enhancements include two additional addressing modes, an expanded microprocessor instruction set (from 56 to 64 instructions), and expanded operational codes (from 151 to 178). In addition, a series of operational enhancements are provided which materially improve the effective use of the microprocessor. These enhancements are explained in Table V of the section of this data sheet devoted to system software and programming. This series of microprocessors provides the user an architecture and instruction set with which he is basically familiar (6502), the several operational enhancements notwithstanding, plus all of the advantages of leading edge CMOS technology; i.e., increased noise immunity, higher reliability, and greatly reduced power consumption.

TABLE I. G65SCXXX FAMILY MICROPROCESSOR CAPABILITIES

ITEM NO.	PART NUMBER	DIP PINS	ADDRESSABLE MEMORY (BYTES)	ON-BOARD CLOCK OSCILLATOR (SEE NOTE)	EXTERNAL CLOCK GENERATOR REQUIRED	ADVANCED MEMORY ACCESS (ϕ4)	$\overline{IRQ}$	$\overline{NMI}$	$\overline{SO}$	DBE	BE	SYNC	RDY	$\overline{ML}$	$\overline{RES}$
1	G65SC02	40	65K	•			•	•	•			•	•		•
2	G65SC03	28	4K		•		•	•							•
3	G65SC04	28	8K		•		•								•
4	G65SC05	28	4K		•		•						•		•
5	G65SC06	28	4K		•		•								•
6	G65SC07	28	8K		•								•		•
7	G65SC12	40	65K		•		•	•	•	•		•			•
8	G65SC13	28	4K		•		•	•							•
9	G65SC14	28	8K		•		•								•
10	G65SC15	28	4K		•		•						•		•
11	G65SC102	40	65K	•		•	•	•	•		•	•	•	•	•
12	G65SC103	28	4K		•	•	•	•							•
13	G65SC104	28	8K		•	•	•								•
14	G65SC105	28	4K		•	•	•						•		•
15	G65SC106	28	4K		•	•	•								•
16	G65SC107	28	8K		•	•							•		•
17	G65SC112	40	65K	•			•	•	•		•	•	•	•	•
18	G65SC115	28	4K		•		•						•	•	•

NOTE: These devices can operate in any of the following clock generation modes: 1. External crystal 2. External RC network 3. ϕ0(IN) from external clock source

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CMD

Microcircuits

C690
C691
C692
C693

CMOS Microprocessor Supervisory Circuits

Features

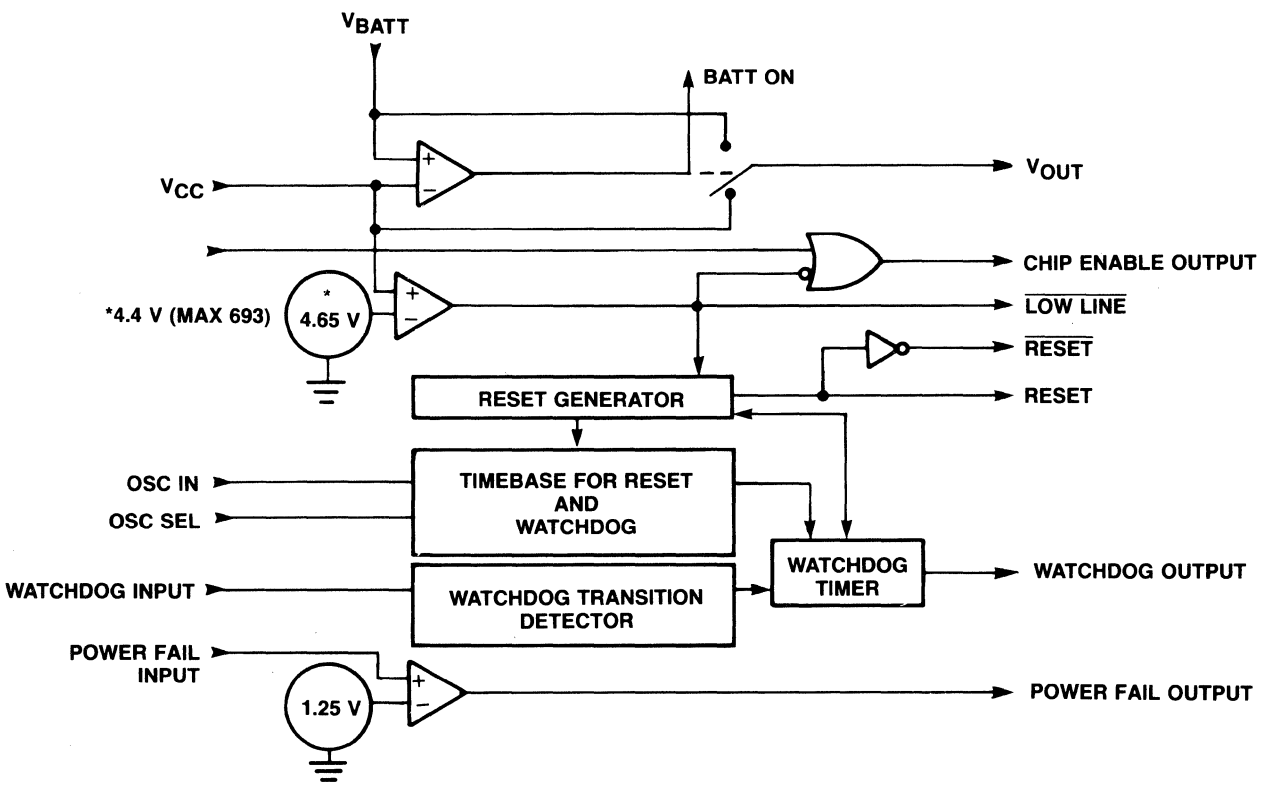
- Precision Voltage Monitor —
  5% Power Supply for C690 & C691
  10% Power Supply for C692 & C693
- Power On or Out of Tolerance Reset
- Watchdog Timer — 100 ms, 1.6 sec or adjustable
- Battery Backup Switching for Memory retention
- On Chip logic for Chip Enable
- Separate Voltage Monitor for power fail or low battery warning
- Low Power CMOS
- 8 Pin (C690 & C692) and 16 Pin (C691 & C693) versions

General Description

CMD Microcircuits' family of supervisory circuits feature precision circuitry for simplified supervision of microprocessor systems: power supply monitoring, software execution checking, and battery switching functions. The circuitry include microprocessor resets, battery backup switchover, RAM write protect, a watchdog timer, and power fail sense. The combination of CMD Microcircuits' Advanced CMOS and reduced system component count produces a more accurate and reliable system than is possible with discrete components.

The C690 and C692 are 8 pin devices with the following functions:
1) Battery Backup switching for low power RAM and Microprocessors.
2) A Reset signal that is active following power-up, power-down, or low power conditions.
3) A Watchdog timer to produce a Reset pulse if the Watchdog input has not been toggled prior to timeout.
4) A Power Fail detector, set for 1.25 V, to warn of low power, including low battery or drop-out of non 5 V supplies.

The C691 and C693 are 16 pin devices and add the following functions to those above:
1) Write protection output for RAM or EEPROM.
2) Adjustable periods for Reset and the Watchdog timer.
3) Additional outputs for the watchdog timer, battery backup switchover, and low V_{CC}.



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NEW 65CE02 MICROPROCESSOR

PRELIMINARY

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Features

- **CMOS technology**
- **0–10 Mhz operating speeds**
- **Code compatible with existing 6502/65C02**
- **Instruction set streamlined**
  - —Instructions require fewer cycles
  - —'Dead' cycles removed
  - —Execution times independent of page boundary crossings
- **Executes existing 6502/65C02 code in up to 25% fewer cycles**
- **Stack pointer increased to 16 bits with two modes of operation**
  - —Full 16 bit pointer
  - —Page programmable 8 bit pointer
- **Base page register**
  - —Allows relocation of 'zero' page to any page in memory
- **Additional index register**
  - —Functions similar to the Y index register
- **Enhanced instruction set**
  - —24 new instructions
  - —3 new addressing modes
  - —All 65C02 additions
  - —Z index register commands
  - —New register manipulation commands
  - —Word relative branching (16 bit offset)
  - —Branch to subroutine (word rel)
  - —Indirect and indirect indexed subroutine calls
  - —2's complement
  - —Arithmetic shift right
  - —Increment and decrement word
  - —Arithmetic shift left word
  - —Rotate left word
  - —Subroutine parameter passing via the stack supported
  - —Expandable for customized applications

Description

The Commodore 65CE02 is an enhanced version of the standard 6502, manufactured in CMOS technology for high speed and low power consumption. The 65CE02 is pin for pin compatible with the existing 6502/65C02.

Since the 65CE02 is a true static device, the clock may be stopped in either state, without loss of data and with almost no power dissipation. The instruction set has been expanded to 256 opcodes and streamlined to give up to a 25% improvement in code execution time over a standard 6502/65C02. All branching instructions have been expanded to include a word relative addressing mode which allows conditional branching anywhere within the 64K memory space. A new word relative branch to subroutine has also been added. This new addressing mode aids the programmer in creating re-locatable code modules, resulting in increased software flexibility. Also included is an addressing mode which facilitates parameter passing to subroutines via the stack. Parameters and/or pointers to data arrays can be passed to a subroutine via the stack, and a special return instruction will 'fix' the stack pointer when the subroutine is finished.

The 65CE02 provides the system designer with a high performance, low power microprocessor, while retaining its downward compatibility with the existing family of microprocessor support devices.

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SPECIAL APPLICATIONS

5720 PC MOUSE CONTROLLER CHIP

NEW

The 5720 is a low power CMOS circuit providing complete Mouse interface control for PC applications.

Features

- 100% *Microsoft*®* software compatible
- Address decoding for:
  - —Serial port—COM1, COM2, disable
  - —Parallel port—LPT1, LPT2, LPT3, disable
  - —Floppy disc controller IC
- Delayed read/write signal generation
- Control for expansion bus data buffers
- Interrupt multiplexing for serial port, parallel port and floppy disc controller
- Single wait state generator
- External device select (disableable)
- Floppy drive controller DRQ delay
- Available in 68 pin PLCC package

6500/1 ONE CHIP MICROCOMPUTER

The 6500/1 is a complete high-performance 8-bit microcomputer on a single chip, and is totally upward/downward software compatible with all members of the 6500 family.

Features

- 6502 CPU
- 2048 x 8 mask programmable ROM
- 64 x 8 static RAM
- 16 bit programmable counterlatch with four operating modes:
  - — Interval timer — Event Counter
  - — Pulse Generator — Pulse Width Measurement
- Separate power pin for RAM
- 32 bi-directional TTL compatible I/O lines (4 ports)
- Counter I/O line with asynchronous input mode
- Five Interrupts:
  - — Reset — Two external edge sensitive
  - — Non-maskable — Counter overflow
- 1 to 3 MHz internal clock frequency
- 1 of 3 frequency references
  - — Crystal — Clock — RC

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6551 ASYNCHRONOUS COMMUNICATION INTERFACE ADAPTER

The 6551 is an Asychronous Communication Adapter (ACIA) intended to provide for interfacing the 6500/6800 microprocessor families to serial communication data sets and modems.

Features

- On-chip baud rate generator: 15 programmable baud rates derived from a standard 1.8432 MHz external crystal (50 to 19,200 baud).
- Programmable interrupt and status register to simplify software design.
- Single +5 volt power supply.
- Serial echo mode.
- False start bit detection.
- 8-bit bi-directional data bus for direct communication with the microprocessor.
- External 16x clock input for non-standard baud rates (up to 125 Kbaud).
- Programmable: word lengths, number of stop bits, and parity bit generation and detection.
- Data set and modem control signals provided.
- Parity: odd, even, none, mark, space .
- Full-duplex or half-duplex operation.
- 5, 6, 7, 8 and 9 bit transmission.
- 1, 2, and 3 MHz operation

*Microsoft is a registered trademark of Microsoft Corporation.

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SPECIAL APPLICATIONS

6582 SOUND INTERFACE DEVICE (SID)

The 6582 Sound Interface Device (SID) is a sound generator chip compatible with the 6500/8500 microprocessor families.

Features

- 3 Tone Oscillators
  Range: 0-4 kHz
- 4 Waveforms per Oscillator
  Triangle, Sawtooth,
  Variable Pulse, Noise
- 3 Amplitude Modulators
  Range: 48 dB
- Random Number/Modulation Generator
- 3 Envelope Generators
  Exponential response
  Attack Rate: 2mS-8S
  Decay Rate: 6mS-24S
  Sustain Level: 0-peak volume
  Release Rate: 6mS-24S
- Oscillator Synchronization
- Ring Modulation
- Programmable Filter
  Cutoff range: 30 Hz-12 kHz
  12 dB/octave Rolloff
  Low pass, Band pass,
  High pass, Notch outputs
  Variable Resonance
- Master Volume Control
- 2 A/D POT Interfaces
- External Audio Input

STATIC READ ONLY MEMORY

Description

Commodore offers a variety of high performance ROMs with a wide range of access times providing compatibility with most microprocessor systems. The ROMs are TTL compatible, having a single +5 volt power supply and totally static operation.

The 2400 series "Power Down" ROMs offer significantly reduced power consumption while in stand-by mode. Each device has programmable chip select and/or output enable for output bus control and is designed to replace equivalent EPROMs.

Available ROMS

Device	Organization Words x Bits	Address Access Time (ns)	CE Access Time (ns)	CS/OE Access Time (ns)	Operating Current (Max)	Standby Current (Max)	Process Technology
2332/3	4096x8	200	N/A	75	100 mA	N/A	HMOS
2364	8192x8	200	N/A	100	100 mA	N/A	HMOS
23128	16384x8	250	N/A	100	100 mA	N/A	HMOS
24128	16384x8	250	250	100	100 mA	12 mA	HMOS
24256	32768x8	250	250	100	100 mA	12 mA	HMOS
24512	65536x8	250	250	100	100 mA	12 mA	HMOS
24C128	16384x8	200	200	100	10 mA	50 µA	CMOS
24C256	32768x8	250	250	100	10 mA	50 µA	CMOS

Packaging

Available in standard plastic 24/28 pin dual-in-line packages.

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MICROPROCESSORS

Description

The 6500/8500 Series family includes a range of software compatible microprocessors which provide a selection of addressable memory range, interrupt input options and on-chip clock oscillators and drivers. All of the microprocessors within the group are bus compatible with the M6800 product offering.

The family includes ten microprocessors with on-board clock oscillators and seven microprocessors driven by external clocks. The on-chip clock versions are aimed at high performance, low cost applications where single phase crystal or RC inputs provide the time base. The external clock versions are geared for multiprocessor system applications where maximum timing control is mandatory.

Available Microprocessors

Device	*Clocks	Pins	IRQ	NMI	RDY	Port	Address	AEC	Sync	Speed (MHz)
6502	O	40	X	X	X	—	64K	—	X	1,2,3,4
65CE02	O	40	X	X	X	—	64K	—	X	0-10
6503	O	28	X	X	—	—	4K	—	—	1,2,3,4
6504	O	28	X	—	—	—	8K	—	—	1,2,3,4
6505	O	28	X	—	X	—	4K	—	—	1,2,3,4
6506	O	28	X	—	—	—	4K	—	—	1,2,3,4
6507	O	28	—	—	X	—	8K	—	—	1,2,3,4
6508	E	40	X	—	—	8	64K	X	—	1,2,3
6509	E	40	X	X	X	**	1 MEG	X	X	1,2,3
6510	O,E	40	X	X	X	6,8	64K	X	—	1,2,3,4
6512	E	40	X	X	X	—	64K	—	X	1,2,3,4
6513	E	28	X	X	—	—	4K	—	—	1,2,3,4
6514	E	28	X	—	—	—	8K	—	—	1,2,3,4
6515	E	28	X	—	X	—	4K	—	—	1,2,3,4
8501	O	40	X	—	X	7	64K	X	—	1,2,3
8502	O	40	X	X	X	7	64K	X	—	1,2,3,4
8503	O	40	X	—	—	8	64K	X	—	1,2,3,4

*O — On chip clocks, E — External Clocks
**Four extended address pins expand memory capacity to one megabyte.

Features of the 6500/8500 Family

- Single +5 volt supply
- 56 Instructions
- Decimal and binary arithmetic
- True indexing capability
- 8 bit Bi-directional Data Bus
- Variable length stack
- Programmable stack pointer
- N channel, silicon gate, depletion load technology
- Thirteen addressing modes
- Tri-state address bus, data, bus, and R/W controlled by AEC input.
- Eight bit parallel processing
- Direct memory access capability
- "Ready" input (for single cycle execution)

Packaging

Available in standard plastic dual-in-line packages.

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PERIPHERAL INTERFACE DEVICES

Description

Commodore offers a wide assortment of peripheral interface devices compatible with the 6500/8500 microprocessor family. These devices were specifically designed to simplify the implementation of Input/Output control in microprocessor systems. All of the devices are TTL compatible, have a single +5 volt supply, and are based on N-channel depletion load technology. Each device features from 8 to 24 individually programmable I/O lines. Additional functions on selected devices include handshaking capability, control/interrupt input lines, interrupt output, serial I/O, timers, counters, RAM, and ROM.

Available Peripheral Devices

Device	Pins	8-bit Ports	IRQ	Hand-shaking (Port)	Control/ Interrupt Input Lines	Darling-ton Drive	Serial I/O	Timers	Timer/ Counters	RAM	ROM	Speed MHz
6522	40	2	X	Read A Write A, B	4/4	Port B, CB1, CB2	X	One 16 bit	One 16 bit	—	—	1, 2
6525	40	3**	X	Read A Write B	2/5	—	—	—	—	—	—	***
6526*	40	2	X	Read B Write B	2/1	—	X	—	Two 16 bit	—	—	1, 2, 3
6529	20	1	—	—	—	—	—	—	—	—	—	***
6530	40	2	X	—	—	Port A, B	—	One 8 bit	—	64x8	1024x8	1, 2
6532	40	2	X	—	—	Port B	—	One 8 bit	—	128x8	—	1, 2
6520	40	2	X	Read B Write B	2/1	—	X	—	Two 16 bit	—	—	1, 2

* Note: Supports Time of Day Clock function.
** Note: 2 ports if using control/interrupt lines.
*** Note: These devices are not clocked. Speed is determined by access time.

Packaging

Available in standard plastic dual-in-line packages.

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VIDEO DISPLAY DEVICES

Description

Commodore's family of Video Controllers offers attractive integration of all video logic necessary for color video graphics and text applications, such as low cost CRT terminals, industrial monitors, control system displays and home video games. Complete logic to implement all format timing, memory interface, attribute control, row buffering and high-speed shifting of pixel data are resident in each device.

The family of VIC II and TED devices provide fixed format display with 5 separate character/bit-map modes of operation. A Raster Compare Interrupt allows the easy mixing of these modes for display of high-res graphics with text. A transparent scheme of using PhO time for fetching video data from memory allows for optimal CPU thruput. The VICs also contain a special type of display image, Movable Image Block (MIB), that once defined, can be moved to any screen position without the inherent character cell constraints.

The programmable 8563/68 features digital RGBI output for very sharp 640V x 400H color video. Direct video memory interface to 64K of DRAM requires no external logic.

Available Video Devices

Part No.	Display Format	Display Modes	Video Output	Features	Memory Interface	Pins	Supply
VIC							
6560 (NTSC) 6561 (PALB)	programmable up to 24col/ 25rows 192H x 200V	2 character modes: Hi-Res Multi-color	16 color composite	on chip sound system, 2 8-bit A/D converters, interlace/non-interlace, light pen input	access 16K, transparent DMA	40	+5
VIC II							
6567 (NTSC) 6569 (PALB) 6572 (PALN) 6573 (PALM)	40col/25row text 320H x 200V bit-map	3 character modes: Standard Multicolor, Extended color. 2 bit-map modes: Hi-Res Multi-color.	16 color composite	8 MIB's (sprites), horz and vert scrolling, light pen input, Raster Compare Interrupt	access 16K, interface to multiplexed DRAM, transparent DMA, provides system RAS and CAS	40	+5, +12 ——
8562 (NTSC) 8565 (PALB)							+5
VIC IIE							
8564 (NTSC) 8566 (PALB) 8569 (PALN)	same as above	same as above	same as above	above, plus ... Keyboard Control Register, 2 MHz clock, true external DMA and arbitration control	same as above	48	+5
TED							
8360 (NTSC/ PALB) 8365 (PALN) 8366 (PALM)	same as above	same as above	121 color composite	2 voice sound, 8-bit keyport control, Clk doubling, horz & vert scroll, Raster Compare and 3 timer generated interrupts, hardware cursor, blink and reverse video attributes	access 64K, transparent DMA, provides system RAS, CAS and MUX	48	+5
DVDC							
8563	programmable text up to 80 col/25row bitmap 640H x 400V	3 char. modes: Std., semi-graph, and pixel double width 1 Hi-Res bit-map mode	digital RGBI 16 color or 16 gray-shades	interlace/noninterlace, horz and vert scroll, lightpen input, 80col dbl line buffer, hardware cursor, underline, blink and reverse video, supports 2 character sets of 256 each	access 64K, programmable to interface to either 4164 or 4416 DRAM	48	+5
8568				above, plus ... Update Ready Interrupt, composite video, and composite sync			
CRTC							
6545-1	programmable controller	—	—	programmable cursor lightpen input	access 16K, straight binary or row/column	40	+5

Packaging

Available in standard plastic Dual-In-Line packages.

Commodore Semiconductor

CMOS Fast Static RAMs

CYPRESS SEMICONDUCTOR

Features

- **CMOS for optimum speed/power**
- **High speed**
- **Low power**
- **TTL compatible inputs and outputs**
- **5 volt power supply ±10% tolerance both commercial and military**
- **Very broad product line**

Functional Description

Cypress Static RAMs offer high speed performance with CMOS power savings. A 0.8 micron channel length and lightly doped source and drain regions result in the fastest access times available. TTL conversion circuits provide full TTL compatibility. Latch-up is eliminated by utilizing guard rings and a substrate bias generator. Proprietary input circuitry guarantees electrostatic discharge protection of greater than 2000V.

Cypress RAMs are available in both plastic and ceramic DIP packages at commercial and military temperature ranges.

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Military	−55°C to +125°C	

Maximum Ratings

(Above which the useful life may be impaired)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential .... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State..... −0.5V to +7.0V

DC Input Voltage ..... −3.0V to +7.0V

Output Current, into Outputs (Low) .....20 mA

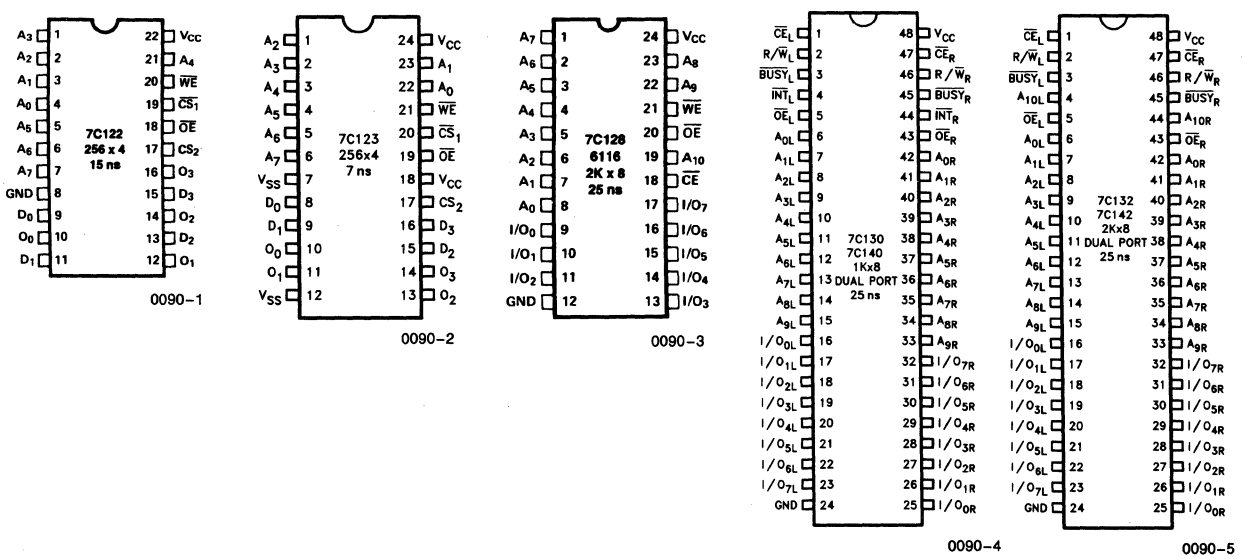
Electrical Characteristics over the operating range

Parameters	Description	Test Conditions	Min.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	2.4		V
V_{OL}	Output LOW Voltage[1]	V_{CC} = Min.		0.4	V
V_{IH}	Input HIGH Voltage		2.2	V_{CC}	V
V_{IL}	Input LOW Voltage		−3.0	0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}	−10	+10	μA

Note:

1. CY7C189/90 has a V_{OL} of 0.45V max.

Pin Configurations



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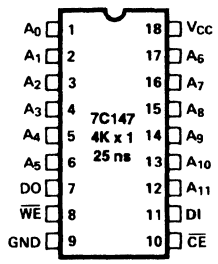
Pin Configurations (Continued)



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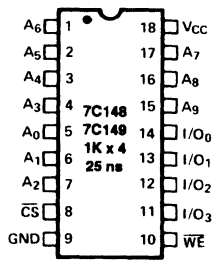

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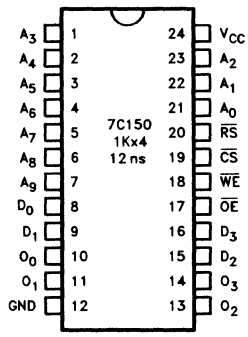
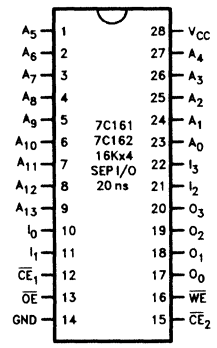
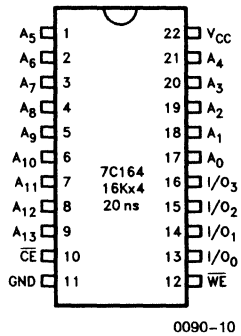


0090-8



0090-9



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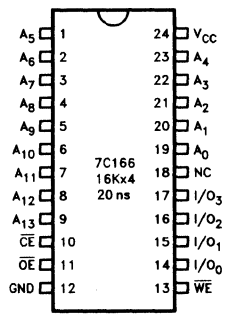

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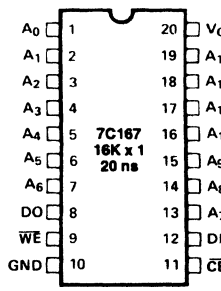

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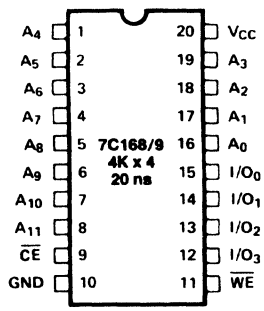

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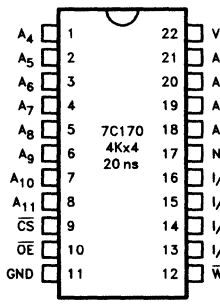

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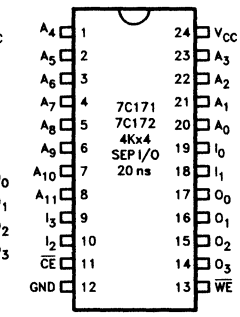

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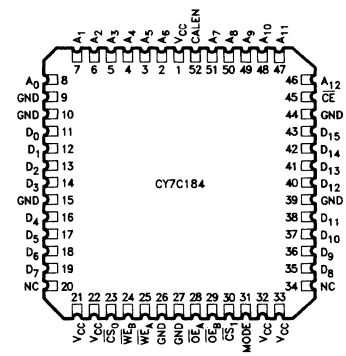

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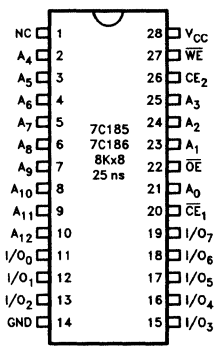

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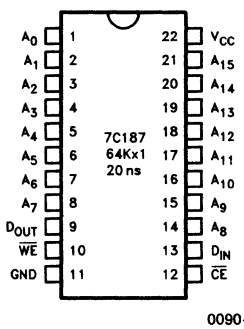

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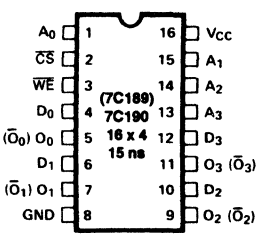
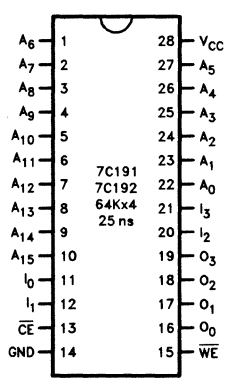


0090-18



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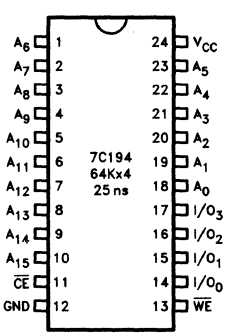

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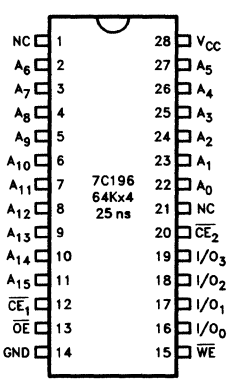

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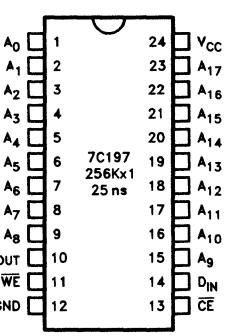

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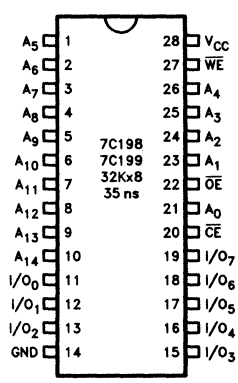

0090-24

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Selector Guide

Sorted by decreasing word depth.

								Read Cycle								Write Cycle						
			PINs	Commercial Power Supply Current	Military Power Supply Current	Commercial Power Down Current	Military Power Down Current	Address Access Time	Chip Select to Data Valid (Max.)	Chip Select Inactive to Output High Z (Max.)	Chip Select Active to Power Up (Min.)	Chip Select Inactive to Power Down (Max.)	Output Enable Active to Data Valid (Max.)	Output Enable Inactive to Output High Z (Max.)	Data Hold from Address Change (Min.)	Address Setup to Write Start (Min.)	Address Hold from Write End (Min.)	Data Setup to Write Start (Min.)	Data Hold from Write End (Min.)	Write Enable Pulse Width (Min.)	Write Enable Active to Output High Z (Max.)	Write Enable Inactive to Low Z (Min.)
Part No.	Speed (ns)	Organization		I_{CC}	I_{CC}	I_{SB}	I_{SB}	t_{AA}	t_{ACS}	t_{HZCS}	t_{PU}	t_{PD}	t_{DOE}	t_{HZOE}	t_{OHA}	t_{SA}	t_{HA}	t_{SD}	t_{HD}	t_{PWE}	t_{HZWE}	t_{LZWE}
				mA	mA	mA	mA	ns	ns	ns	ns	ns	ns	ns	ns	ns	ns	ns	ns	ns	ns	ns
CY7C197	25	262144x1	24	70	NA	20	NA	25	25	15	0	20	NA	NA	3	0	2	15	0	20	15	0
	35			70	80	20	20	35	35	20	0	25	NA	NA	3	0	2	20	0	25	20	0
	45			60	80	20	20	45	45	20	0	30	NA	NA	3	0	2	25	0	25	20	0
CY7C191 CY7C192	25	65536x4	28	80	NA	20	NA	25	25	10	0	25	NA	NA	3	0	2	10	0	20	10	3
	35			80	90	20	20	35	35	15	0	35	NA	NA	3	0	2	15	0	25	10	3
	45			70	90	20	20	45	45	15	0	45	NA	NA	3	0	2	20	0	35	15	3
CY7C194	25	65536x4	24	80	NA	20	NA	25	25	10	0	25	NA	NA	3	0	2	10	0	20	10	3
	35			80	90	20	20	35	35	15	0	35	NA	NA	3	0	2	15	0	25	10	3
	45			70	90	20	20	45	45	15	0	45	NA	NA	3	0	2	20	0	35	15	3
CY7C196	25	65536x4	28	80	NA	20	NA	25	25	10	0	25	15	15	3	0	2	10	0	20	10	3
	35			80	90	20	20	35	35	15	0	35	25	15	3	0	2	15	0	25	10	3
	45			70	90	20	20	45	45	15	0	45	30	15	3	0	2	20	0	35	15	3
CY7C198/9	35	32768x8	28	110	NA	20	NA	35	35	15	0	20	20	20	3	0	2	15	0	20	15	3
	45			110	120	20	20	45	45	20	0	25	20	25	3	0	2	20	0	25	20	3
	55			100	120	20	20	55	55	20	0	25	25	30	3	0	2	25	0	30	25	3
CY7C184	25	8192x16	52	220	265	NA	NA	25	12	15	NA	NA	9	9	3	0	2	10	0	20	15	3
	35			220	265	NA	NA	35	15	25	NA	NA	14	14	3	0	2	10	0	25	15	3
	45			220	265	NA	NA	45	20	30	NA	NA	16	14	3	0	2	10	0	30	20	3
CY7C187	20	65,536x1	22	80	NA	40	NA	20	20	8	0	20	NA	NA	3	0	0	10	0	15	10	0
	25			70	70	20	40	25	25	15	0	25	NA	NA	5	0	0	20	0	20	15	0
	35			70	70	20	20	35	35	20	0	25	NA	NA	5	0	0	25	0	25	20	0
	45			50	70	20	20	45	45	20	0	30	NA	NA	5	0	0	25	0	25	20	0
CY7C161	20	16,384x4 Separate I/O XWR	28	80	NA	40	NA	20	20	10	0	20	13	8	3	0	0	10	0	16	NA	NA
	25			70	80	20	40	25	25	15	0	25	15	15	3	0	0	13	0	20	NA	NA
	35			70	70	20	20	35	35	15	0	25	25	15	3	0	0	15	0	25	NA	NA
	45			50	70	20	20	45	45	15	0	30	30	15	3	0	0	20	0	35	NA	NA
CY7C162	20	16,384x4 Separate I/O	28	80	NA	40	NA	20	20	10	0	20	13	8	3	0	0	10	0	16	7	3
	25			70	80	20	40	25	25	15	0	25	15	15	3	0	0	13	0	20	7	3
	35			70	70	20	20	35	35	15	0	25	25	15	3	0	0	15	0	25	10	3
	45			50	70	20	20	45	45	15	0	30	30	15	3	0	0	20	0	35	15	3
CY7C164	20	16,384x4	22	80	NA	40	NA	20	20	10	0	20	NA	NA	3	0	0	11	0	15	7	3
	25			70	80	20	40	25	25	15	0	25	NA	NA	3	0	0	13	0	20	7	3
	35			70	70	20	20	35	35	15	0	25	NA	NA	3	0	0	15	0	25	10	3
	45			50	70	20	20	45	45	15	0	30	NA	NA	3	0	0	20	0	35	15	3
CY7C166	20	16,384x4 Output Enable	24	80	NA	40	NA	20	20	10	0	20	12	8	3	0	0	11	0	15	7	3
	25			70	80	20	40	25	25	15	0	25	15	15	3	0	0	13	0	20	7	3
	35			70	70	20	20	35	35	15	0	25	25	15	3	0	0	15	0	25	10	3
	45			50	70	20	20	45	45	15	0	30	30	15	3	0	0	20	0	35	15	3

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Selector Guide

Sorted by decreasing word depth. (Continued)

								Read Cycle								Write Cycle						
			PINs	Commercial Power Supply Current	Military Power Supply Current	Commercial Power Down Current	Military Power Down Current	Address Access Time	Chip Select to Data Valid (Max.)	Chip Select Inactive to Output High Z (Max.)	Chip Select Active to Power Up (Min.)	Chip Select Inactive to Power Down (Max.)	Output Enable Active to Data Valid (Max.)	Output Enable Inactive to Output High Z (Max.)	Data Hold from Address Change (Min.)	Address Setup to Write Start (Min.)	Address Hold from Write End (Min.)	Data Setup to Write Start (Min.)	Data Hold from Write End (Min.)	Write Enable Pulse Width (Min.)	Write Enable Active to Output High Z (Max.)	Write Enable Inactive to Low Z (Min.)
Part No.	**Speed (ns)**	**Organization**		I_{CC}	I_{CC}	I_{SB}	I_{SB}	t_{AA}	t_{ACS}	t_{HZCS}	t_{PU}	t_{PD}	t_{DOE}	t_{HZOE}	t_{OHA}	t_{SA}	t_{HA}	t_{SD}	t_{HD}	t_{PWE}	t_{HZWE}	t_{LZWE}
				mA	mA	mA	mA	ns	ns	ns	ns	ns	ns	ns	ns	ns	ns	ns	ns	ns	ns	ns
CY7C167	15*	16,384x1	20	80	NA	20	NA	15	15	12	0	15	NA	NA	3	0	2	10	0	13	12	0
	20			80	NA	40	NA	20	20	5	0	20	NA	NA	3	0	0	10	0	15	10	0
	25L			45	60	15	20	25	25	15	0	20	NA	NA	3	0	0	15	0	15	15	0
	35L			45	60	15	20	35	35	20	0	25	NA	NA	3	0	0	15	0	20	20	0
	45			50	50	15	20	45	45	25	0	30	NA	NA	3	0	0	15	0	20	20	0
CY7C185 CY7C186	20	8192x8 300/600 mil Pkg	28	100	NA	40	NA	20	20	10	0	20	13	10	3	0	0		0	16	8	3
	25			100	125	20	40	25	25	15	0	20	15	15	3	0	0		0	20	15	3
	35			100	125	20	20	35	35	15	0	20	20	20	3	0	0	15	0	20	15	3
	45			100	100	20	20	45	45	20	0	25	20	25	3	0	0	20	0	25	20	3
	55			80	100	20	20	55	55	20	0	25	25	30	3	0	0	25	0	30	25	3
CY7C168	15*	4096x4 Power Down	20	120	NA	20	NA	15	15	12	0	15	NA	NA	3	0	2	7	0	13	6	3
	20			90	NA	40	NA	20	20	10	0	20	NA	NA	3	0	0	10	0	15	8	3
	25L			70	90	15	20	25	25	15	0	25	NA	NA	3	0	0	10	0	20	10	6
	35L			70	90	15	20	35	35	20	0	25	NA	NA	3	0	0	15	0	30	15	6
	45			70	70	15	20	45	45	25	0	30	NA	NA	3	0	0	15	3	35	20	6
CY7C169	15*	4096x4 Fast CE	20	120	NA	NA	NA	15	12	12	NA	NA	NA	NA	3	0	2	7	0	13	6	3
	20			90	NA	40	NA	20	15	10	0	20	NA	NA	3	0	0	10	0	15	8	3
	25L			70	90	NA	NA	25	15	15	NA	NA	NA	NA	3	0	0	10	0	20	10	6
	35L			70	90	NA	NA	35	25	20	NA	NA	NA	NA	3	0	0	15	0	30	15	6
	40			70	70	NA	NA	40	25	20	NA	NA	NA	NA	3	0	0	15	3	35	20	6
CY7C170	20	4096x4 Output Enable	22	90	NA	NA	NA	20	15	10	NA	NA	12	8	3	0	0	10	0	15	8	3
	25			90	NA	NA	NA	25	15	15	NA	NA	15	15	3	0	0	10	0	20	10	6
	35			90	120	NA	NA	35	25	20	NA	NA	15	15	3	0	0	15	0	30	15	6
	45			90	120	NA	NA	45	30	25	NA	NA	20	15	3	0	0	15	3	35	20	6
CY7C171	20	4096x4 Separate I/O XWR	24	90	NA	40	NA	20	20	10	0	20	NA	NA	3	0	0	10	0	16	7	0
	25L			70	90	15	20	25	25	15	0	25	NA	NA	3	0	0	10	0	20	NA	NA
	35L			70	90	15	20	35	35	20	0	25	NA	NA	3	0	0	15	0	25	NA	NA
	45			70	70	15	20	45	45	20	0	30	NA	NA	3	0	0	15	3	30	NA	NA
CY7C172	20	4096x4 Separate I/O	24	90	NA	40	NA	20	20	10	0	20	NA	NA	3	0	0	10	0	16	7	0
	25L			70	90	15	20	25	25	15	0	25	NA	NA	3	0	0	10	0	20	10	0
	35L			70	90	15	20	35	35	20	0	25	NA	NA	3	0	0	15	0	25	50	0
	45			70	70	15	20	45	45	20	0	30	NA	NA	3	0	0	15	3	30	20	0
CY7C147	25	4096x1	18	90	NA	15	NA	25	25	20	0	20	NA	NA	5	0	0	15	0	15	15	0
	35			80	110	10	10	35	35	30	0	20	NA	NA	5	0	0	20	10	20	20	0
	45			80	110	10	10	45	45	30	0	20	NA	NA	5	0	0	25	10	25	25	0
CY7C132* CY7C142	25*	2048x8 Dual Port	48	170	NA	65	NA	25	30	15	0	25	15	15	0	0	2	15	0	20	15	0
	35			120	NA	30	NA	35	35	15	0	20	15	15	5	0	2	15	0	20	15	0
	45			120	150	30	40	45	45	20	0	25	20	20	5	0	2	20	0	20	20	0
	55			120	150	30	40	55	55	25	0	30	25	25	5	0	2	25	0	25	25	0

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Selector Guide

Sorted by decreasing word depth. (Continued)

				Read Cycle											Write Cycle						
			PINs	Commercial Power Supply Current	Military Power Supply Current	Commercial Power Down Current	Military Power Down Current	Address Access Time	Chip Select to Data Valid (Max.)	Chip Select Inactive to Output High Z (Max.)	Chip Select Active to Power Up (Min.)	Chip Select Inactive to Power Down (Max.)	Output Enable Active to Data Valid (Max.)	Output Enable Inactive to Output High Z (Max.)	Data Hold from Address Change (Min.)	Address Setup to Write Start (Min.)	Address Hold from Write End (Min.)	Data Setup to Write Start (Min.)	Data Hold from Write End (Min.)	Write Enable Pulse Width (Min.)	Write Enable Active to Output High Z (Max.)	Write Enable Inactive to Low Z (Min.)
Part No.	**Speed (ns)**	**Organization**		I_{CC}	I_{CC}	I_{SB}	I_{SB}	t_{AA}	t_{ACS}	t_{HZCS}	t_{PU}	t_{PD}	t_{DOE}	t_{HZOE}	t_{OHA}	t_{SA}	t_{HA}	t_{SD}	t_{HD}	t_{PWE}	t_{HZWE}	t_{LZWE}
				mA	mA	mA	mA	ns	ns	ns	ns	ns	ns	ns	ns	ns	ns	ns	ns	ns	ns	ns
CY7C128/ CY6116	25	2048x8 300/600 mil Pkg	24	120	NA	20	NA	25	25	15	0	20	15	15	3	0	0	10	0	20	10	0
	35			120	150	20	20	35	35	15	0	20	15	15	5	0	0	15	0	20	15	0
	45			120	130	20	20	45	45	20	0	25	20	15	5	0	0	20	0	20	15	0
	55			90	100	20	20	55	55	20	0	25	25	20	5	0	0	25	0	25	20	0
CY7C130* CY7C140	25*	1024x8 Dual Port	48	170	NA	65	NA	25	30	15	0	25	15	15	0	0	2	15	0	20	15	0
	35			120	NA	30	NA	35	35	15	0	20	15	15	5	0	2	15	0	20	15	0
	45			120	150	30	40	45	45	20	0	25	20	20	5	0	2	20	0	20	20	0
	55			120	150	30	40	55	55	25	0	30	25	25	5	0	2	25	0	25	25	0
CY7C148	25	1024x4 Power Down	18	90	NA	15	NA	25	25	15	0	20	NA	NA	0	0	5	12	0	20	8	0
	35			80	110	10	10	35	35	20	0	30	NA	NA	0	0	5	20	0	30	10	0
	45			80	110	10	10	45	45	20	0	30	NA	NA	5	0	5	20	0	35	15	0
CY7C149	25	1024x4 Fast CS	18	90	NA	NA	NA	25	15	15	NA	NA	NA	NA	0	0	5	12	0	20	8	0
	35			80	110	NA	NA	35	15	20	NA	NA	NA	NA	0	0	5	20	0	30	10	0
	45			80	110	NA	NA	45	20	20	NA	NA	NA	NA	5	0	5	20	0	35	15	0
CY7C150	12*	1024x4 Separate I/O	24	90	NA	NA	NA	12	10	8	NA	NA	8	8	2	2	2	9	9	9	8	0
	15			90	NA	NA	NA	15	12	11	NA	NA	10	9	2	2	2	11	2	11	12	0
	25			90	100	NA	NA	25	15	20	NA	NA	15	20	2	5	5	15	5	15	20	0
	35			90	100	NA	NA	35	20	25	NA	NA	20	25	2	5	5	20	5	20	25	0
CY7C123*	7	256x4 Separate I/O	24	120	NA	NA	NA	7	7	5	NA	NA	7	5	NA	0	3	5	2	5	5	2
	9			120	NA	NA	NA	9	8	6	NA	NA	8	6	NA	1	1.5	6	1	6.5	6	2
	10			NA	150	NA	NA	10	8	6	NA	NA	8	6	NA	1	2	7	1	7	6	2
	12			120	NA	NA	NA	12	8	10	NA	NA	8	10	NA	0	3	9	2	9	10	2
	15			120	150	NA	NA	15	10	12	NA	NA	10	12	NA	2	4	11	2	11	12	2
CY7C122	15	256x4 Separate I/O	22	90	NA	NA	NA	15	8	12	NA	NA	8	12	NA	0	4	NA	2	11	12	NA
	25			60	90	NA	NA	25	15	25	NA	NA	15	20	NA	5	5	NA	5	15	20	NA
	35			60	90	NA	NA	35	25	25	NA	NA	25	30	NA	10	5	NA	5	25	30	NA
CY7C189	15	64x4 Separate I/O Inverting Outputs	16	90	NA	NA	NA	15	12	12	NA	NA	NA	NA	5	0	0	15	0	11	15	12
	25			55	70	NA	NA	25	15	15	NA	NA	NA	NA	5	0	0	20	0	15	20	20
CY27LS03	65			NA	38	NA	NA	65	65	35	NA	NA	NA	NA	NA	0	0	55	0	55	35	NA
CY7C190	15	64x4 Separate I/O	16	90	NA	NA	NA	15	12	12	NA	NA	NA	NA	5	0	0	15	0	11	15	12
	25			55	70	NA	NA	25	15	15	NA	NA	NA	NA	5	0	0	20	0	15	20	20

*Preliminary

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CMOS High Speed PROMs

CYPRESS SEMICONDUCTOR

Features

- **CMOS for optimum speed/power**
- **High speed (25 ns 7C291, 7C292)**
- **Low power (1/2 Bipolar)**
- **Reprogrammable (7C245, 7C251, 7C254, 7C261, 7C263, 7C264, 7C268, 7C269, 7C271, 7C291, 7C291A, 7C292A and 7C293A)**
- **10% power supply**
- **TTL compatible**
- **100% tested**

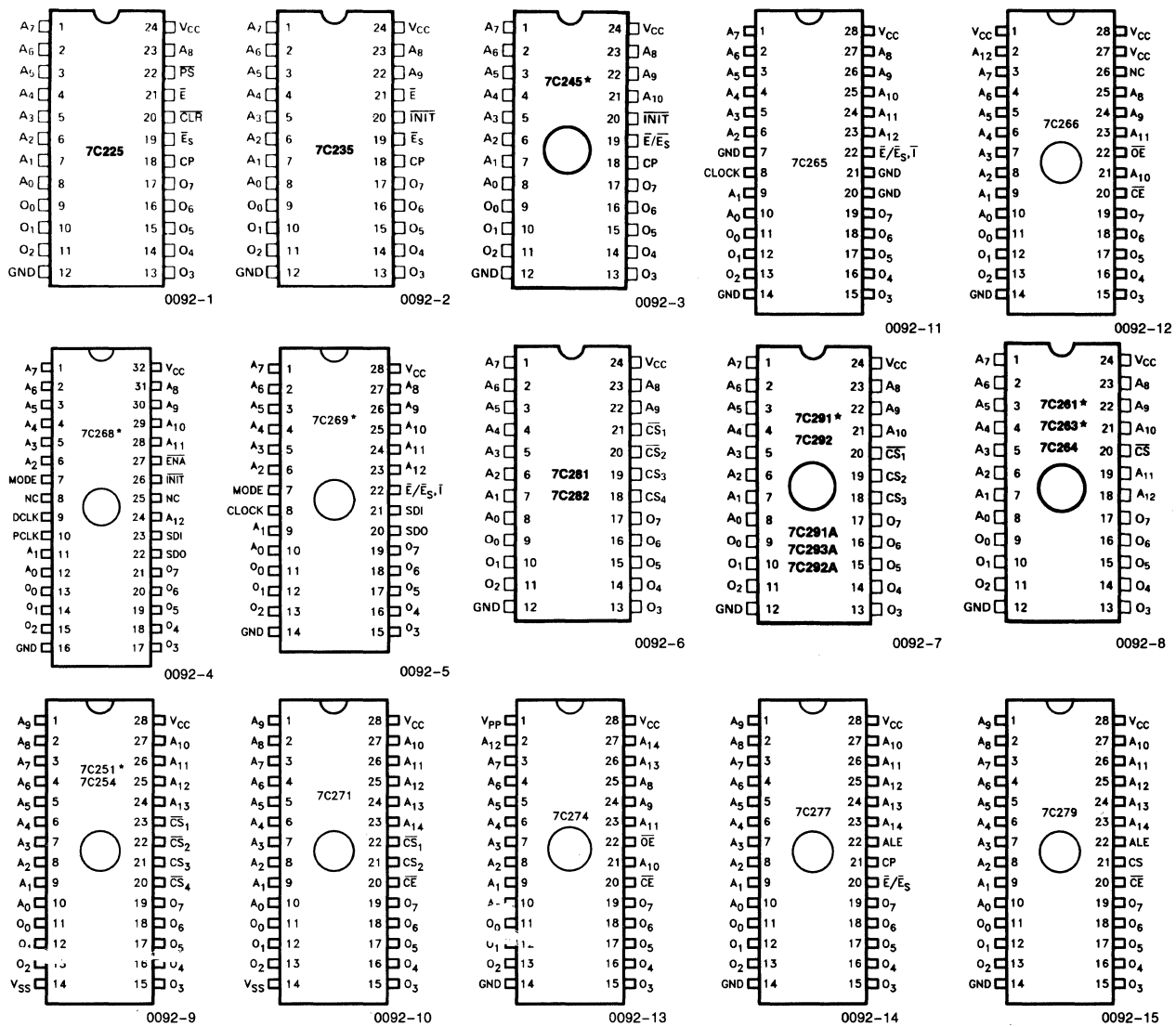
Product Characteristics

Cypress has blended 1.2 micron and floating gate technologies to produce a line of the fastest, lowest power PROMs in the world. Floating gate technology allows reprogrammability by the user and 100% testing at the factory. The 7C245, 7C245A, 7C251, 7C254, 7C261, 7C263, 7C264, 7C268, 7C269, 7C271, 7C291, 7C291A, 7C292A and 7C293A feature optional windows for reprogrammability by the user.

Cypress PROMs are offered in registered, registered diagnostic, and non-registered versions in a variety of packages including 300 mil DIP, LCC and PLCC.

CMOS PROMs offer advantages in reliability such as 2000 volt ESD protection on all pins, 10% power supplies, low power dissipation and latchup protection.

Pin Configurations



*Window Optional

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Electrical Characteristics Over the Operating Range

Parameters	Description	Test Conditions	Min.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min.		0.4	V
V_{IH}	Input HIGH Voltage		2.0		V
V_{IL}	Input LOW Voltage			0.8	V
I_{IX}	Input Leakage Current	$GND \le V_I \le V_{CC}$	−10	+10	μA

Selector Guide

Sorted by decreasing word depth.

								Registered						Non-Registered		
			PINs	Commercial Power Supply Current	Military Power Supply Current	Commercial Power Down Current*	Military Power Down Current*	Address Setup To Clock HIGH (Min.)	Address Hold From Clock HIGH (Min.)	Clock HIGH To Valid Output (Max.)	Clock Pulse Width (Min.)	Active Output From Clock HIGH (Max.)	Inactive Output From Clock HIGH (Max.)	Address To Output Valid (Max.)	Chip Select Inactive To High Z (Max.)	Chip Select Active To Output Valid (Max.)
Part No.	Speed (ns)	Organization		I_{CC}	I_{CC}	I_{SB}	I_{SB}	t_{SA}	t_{HA}	t_{CO}	t_{PWC}	t_{DOE}	t_{HZC}	t_{AA}	t_{HZCS}	t_{ACS}
				mA	mA	mA	mA	ns	ns	ns	ns	ns	ns	ns	ns	ns
CY7C268† CY7C269	40	8192x8 Registered Diagnostic	32/28	100	NA	—	—	40	0	20	15	20	20	—	—	—
	50			80	120	—	—	50	0	25	20	25	25	—	—	—
	60			80	100	—	—	60	0	25	20	25	25	—	—	—
CY7C265	40	8192x8 Registered	28	100	NA	—	—	40	0	20	15	20	20	—	—	—
	50			80	120	—	—	50	0	25	20	25	25	—	—	—
	60			80	100	—	—	60	0	25	20	25	25	—	—	—
CY7C245	18	2048x8 Registered	24	120	NA	—	—	18	0	12	12	15	15	—	—	—
	25			90	NA	—	—	25	0	12	15	15	15	—	—	—
	35			90	120	—	—	35	0	20	20	30	30	—	—	—
	45			120	120	—	—	45	0	25	20	30	30	—	—	—
CY7C245L	35	2048x8 Registered Low Power	24	60	NA	—	—	35	0	20	20	30	30	—	—	—
	45			60	NA	—	—	45	0	25	20	30	30	—	—	—
CY7C235	25	1024x8 Registered	24	90	NA	—	—	25	0	12	12	20	20	—	—	—
	30			90	120	—	—	30	0	15	15	20	20	—	—	—
	40			90	120	—	—	40	0	25	20	25	25	—	—	—
CY7C225	25	512x8 Registered	24	90	NA	—	—	25	0	12	10	20	20	—	—	—
	30			90	120	—	—	30	0	15	15	20	20	—	—	—
	35			NA	120	—	—	35	0	20	20	25	25	—	—	—
	40			90	120	—	—	40	0	25	20	30	25	—	—	—
CY7C271* CY7C274	45	32,768x8 Power Down	28	120	NA	30	NA	—	—	—	—	—	—	45	30	30
	55			120	130	30	40	—	—	—	—	—	—	55	30	30
	65			120	130	30	35	—	—	—	—	—	—	65	35	35
	75			NA	130	NA	35	—	—	—	—	—	—	75	45	45
CY7C277	40	32768x8 Registered	28	120	NA	30	NA	40	0	20	20	20	20	—	—	—
	50			120	130	30	40	50	0	25	20	30	30	—	—	—
CY7C279	45	32768x8 w/ALE	28	—	—	—	—	—	—	—	—	—	—	45	30	30
	55			—	—	—	—	—	—	—	—	—	—	55	30	30
CY7C251* CY7C254†	45	16,384x8 Power Down*	28	100	NA	20*	NA*	—	—	—	—	—	—	45	45*/25	45*/25
	55			100	120	20*	30*	—	—	—	—	—	—	55	55*/30	55*/30
	65			100	120	20*	30*	—	—	—	—	—	—	65	65*/35	65*/35
CY7C261* CY7C263 CY7C264†	30*	8192x8 Power Down	24	100	NA	30*	30*	—	—	—	—	—	—	30	25*/20	35*/20
	35			100	120	30*	30*	—	—	—	—	—	—	35	30*/25	40*/25
	40			—	—	30*	—	—	—	—	—	—	—	40	35*/25	45*/25
	45			100	120	30*	30*	—	—	—	—	—	—	45	45*/30	45*/30
	55			100	120	30*	30*	—	—	—	—	—	—	55	55*/35	55*/35
CY7C266	55	8192x8	28	80	90	15	15	—	—	—	—	—	—	55	20	20
CY7C291 CY7C292† CY7C293*	20	2048x8 Registered Power Down*	24	120	NA	20*	NA*	—	—	—	—	—	—	20	22*/15	22*/15
	25			130	NA	—	—	—	—	—	—	—	—	25	20	20
	30			NA	120	NA*	30*	—	—	—	—	—	—	30	32*/20	32*/20
	35			90	120	20*	30*	—	—	—	—	—	—	35	35*/25	35*/25
	50			90	120	20*	30*	—	—	—	—	—	—	50	45*/25	45*/25
CY7C291L CY7C292L†	35	2048x8 Low Power	24	60	NA	—	—	—	—	—	—	—	—	35	25	25
	50			60	NA	—	—	—	—	—	—	—	—	50	25	25
CY7C281 CY7C282†	30	1024x8	24	100	NA	—	—	—	—	—	—	—	—	30	20	20
	45			90	120	—	—	—	—	—	—	—	—	45	25	25

*Power Down †600 mil

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CMOS Cascadeable FIFOs

CYPRESS SEMICONDUCTOR

Features

- **CMOS for optimum speed/power**
- **Dual port RAM cell**
- **High speed: 15, 25, 35 MHz**
- **Fast, 50 ns bubblethrough**
- **Cascadeable**
- **Low power**
- **TTL compatible**
- **10% power supply**
- **300 mil packages**

Functional Description

Cypress First-in First-out memories, FIFOs, combine 1.2 micron CMOS technology with a unique dual port architecture to provide the fastest and lowest power FIFOs available. Unlike traditional FIFOs these devices are designed using dual port memory, read and write pointers, and control logic. The conventional concept of bubble-through is absent. Instead, the delay for input data to appear at the output is the time required to move a pointer and propogate an Output Ready (OR) signal.

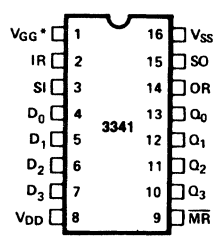
Other features of Cypress FIFOs include: cascadeability, power-on reset, independent asynchronous inputs and outputs, output enable (7C403, 7C404, 7C408), and latchup is prevented by careful layout, guard rings and a substrate bias generator.

Selection Guide

Part No.	Description	Temp. Range	Speed (MHz)	I_{CC} (mA)
CY3341	64 x 4 FIFO Serial Memory	COMM/MIL	1.2, 2	45/65
CY7C401	Cascadeable 64 x 4 FIFO	Commercial	5, 10, 15	75
		Military	10, 15	90
CY7C402	Cascadeable 64 x 5 FIFO	Commercial	5, 10, 15	75
		Military	10, 15	90
CY7C403	Cascadeable 64 x 4 FIFO with Output Enable	COMM/MIL	10, 15, 25	75/90
CY7C404	Cascadeable 64 x 5 FIFO with Output Enable	COMM/MIL	10, 15, 25	75/90
CY7C408	Cascadeable 64 x 8 FIFO with Output Enable	COMM/MIL	15, 25, 35†	100/125
CY7C409	Cascadeable 64 x 9 FIFO	COMM/MIL	15, 25, 35†	100/125

*I_{SB} = 8/15 mA Commercial/Military
†35 MHz COMM only

Pin Configurations



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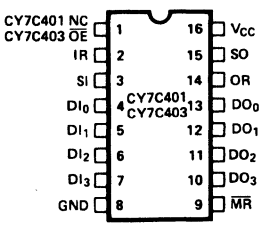
*Internally not connected



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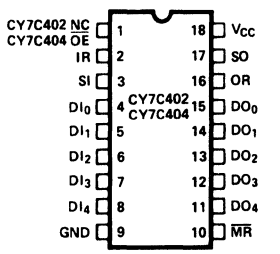

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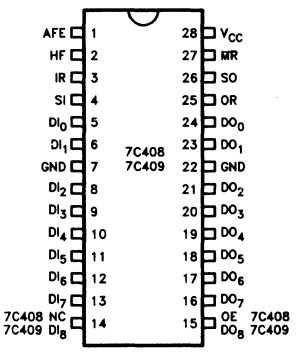

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Switching Characteristics Over the Operating Range[1]

Parameters	Description	Test Conditions	3341		3341-2		7C401-5 7C402-5		7C401/2/3/4-10		7C401/2/3/4-15		7C403-25[6] 7C404-25[6]		7C408-15 7C409-15		7C408-25 7C409-25		7C408-35 7C409-35		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
f_O	Operating Frequency	Note 2		1.2		2		5		10		15		25		15		25		35	MHz
t_{PHSI}	SI HIGH Time		80		80		20		20		20		11		23		11		9		ns
t_{PLSI}	SI LOW Time		80		80		45		30		25		24		25		24		17		ns
t_{SSI}	Data Setup to SI	Note 3	0		0		0		0		0		0		0		0		0		ns
t_{HSI}	Data Hold from SI	Note 3	200		100		60		40		30		20		30		20		10		ns
t_{DLIR}	Delay, SI HIGH to IR LOW	Note 6	20	350	20	160		75		40		35		21/22		35		21		15	ns
t_{DHIR}	Delay, SI LOW to IR HIGH	Note 6	20	450	20	200		75		45		40		28/30		40		23		16	ns
t_{PHSO}	SO HIGH Time		80		80		20		20		20		11		23		11		9		ns
t_{PLSO}	SO LOW Time		80		80		45		25		25		24		25		24		17		ns
$t_{OR} + t_{DLOR}$	Delay, SO HIGH to OR LOW	Note 6	20	370	20	160		75		40		35		19/21		35		21		15	ns
$t_{OR} - t_{DHOR}$	Delay, SO LOW to OR HIGH	Note 6	20	450	20	200		80		55		40		34/37		40		23		16	ns
t_{SOR}	Data Setup to OR HIGH		0		0		0		0		0		0		0		0		0		ns
t_{HSO}	Data Hold from SO LOW		75		20		5		5		5		5		0		0		0		ns
t_{BT}	Bubblethrough Time	Note 6		1000		500		200	10	95	10	65	10	50/60	10	65	10	60	10	50	ns
t_{SIR}	Data Setup to IR	Note 4					5		5		5		5		5		5		5		ns
t_{HIR}	Data Hold from IR	Note 4					30		30		30		20		30		20		20		ns
t_{PIR}	Input Ready Pulse HIGH						20		20		20		15		23		15		10		ns
t_{POR}	Output Ready Pulse HIGH						20		20		20		15		23		15		10		ns
t_{DHHF}	SI LOW to HF HIGH			—		—		—		—		—		—		65		55		45	ns
t_{DLHF}	SO LOW to HF LOW			—		—		—		—		—		—		65		55		45	ns
t_{DLAFE}	SO or SI LOW to AFE LOW			—		—		—		—		—		—		65		55		45	ns
t_{DHAFE}	SO or SI LOW to AFE HIGH			—		—		—		—		—		—		65		55		45	ns
t_{PMR}	$\overline{MR}$ Pulse Width		400		200		40		30		25		25		55		45		35		ns
t_{DSI}	$\overline{MR}$ HIGH to SI HIGH		30		30		40		35		25		10		25		10		10		ns
t_{DOR}	$\overline{MR}$ LOW to OR LOW			400		200		85		40		35		35		55		45		35	ns
t_{DIR}	$\overline{MR}$ LOW to IR HIGH			400		200		85		40		35		35		55		45		35	ns
t_{LZMR}	$\overline{MR}$ LOW to Output LOW	Note 5						50		40		35		25		55		45		35	ns
t_{DAE}	$\overline{MR}$ LOW to $\overline{AE}$ LOW			—		—		—		35		30		20		55		45		35	ns
t_{DAF}	$\overline{MR}$ LOW to $\overline{AF}$ HIGH			—		—		—		30		25		15		55		45		35	ns

Notes:

1. Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V and output loading of the specified I_{OL}/I_{OH} and 30 pF load capacitance, as in *Figure 1.*
2. $1/f_O > t_{PHSI} + t_{DHIR}$, $1/f_O > t_{PHSO} + t_{DHOR}$.
3. t_{SSI} and t_{HSI} apply when memory is not full.
4. t_{SIR} and t_{HIR} apply when memory is full, SI is HIGH and minimum bubblethrough (t_{BT}) conditions exist.
5. All data outputs will be at LOW level after reset goes HIGH until data is entered into the FIFO.
6. Commercial/Military.

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Cypress Semiconductor

Features

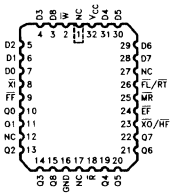
- 512 x 9, 1024 x 9, 2048 x 9 FIFO buffer memory
- Dual port RAM cell
- Asynchronous read/write
- High speed 25 MHz read/write independent of depth/width
- Half full flag in standalone
- Empty and full flags
- Retransmit in standalone
- Expandable in width and depth
- Parallel Cascade minimizes bubblethrough
- 5V ±10% supply
- 300 mil DIP packaging
- TTL compatible
- Three-state outputs
- CY7C421 pin compatible and functional equivalent to IDT7201

Functional Description

The (CY7C420, CY7C421,) (CY7C424, CY7C425,) and (CY7C428, CY7C429) are, respectively, 512, 1024 and 2048 words by 9-bit wide first-in first-out (FIFO) memories offered in 300 mil wide and 600 mil wide packages, respectively. Each FIFO memory is organized such that the data is read in the same sequential order that it was written. Full and Empty flags are provided to prevent over-run and under-run. Three additional pins are also provided to facilitate unlimited expansion in width, depth, or both. The depth expansion technique steers the control signals from one device to another in parallel, thus eliminating the serial addition of propagation delays so that throughput is not reduced. Data is steered in a similar manner.

Pin Configurations

PLCC/LCC
Top View



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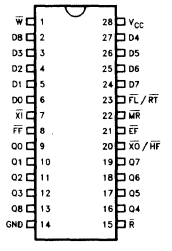
DIP
Top View



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Selection Guide

		7C420-30, 7C421-30 7C424-30, 7C425-30 7C428-30, 7C429-30
Frequency (MHz)		25
Access Time (ns)		30
Maximum Operating Current (mA)	Commercial	100
	Military	120

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C
Ambient Temperature with Power Applied ..... −55°C to +125°C
Supply Voltage to Ground Potential ..... −0.5V to +7.0V
DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V
DC Input Voltage ..... −3.0V to +7.0V
Power Dissipation 1.0W
Output Current, into Outputs (Low) 20mA

Electrical Characteristics Over Operating Range

Parameters	Description	Test Conditions		CY7C420-30, CY7C421-30 CY7C424-30, CY7C425-30 CY7C428-30, CY7C429-30	
				Min.	Max.
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −2 mA		2.4	
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4
V_{IH}	Input HIGH Voltage		Commercial	2.0	V_{CC}
			Military	2.2	V_{CC}
V_{IL}	Input LOW Voltage			−3.0	0.8
I_{IX}	Input Leakage Current	$GND \le V_I \le V_{CC}$		−10	+10
I_{CC}	Operating Current	V_{CC} = Max., I_{OUT} = 0 mA	Commercial		100
			Military		120
I_{SB_1}	Standby Current	$\overline{R} = \overline{W} = \overline{MR} = \overline{FL/RT} = V_{IH}$	Commercial		15
			Military		20
I_{SB_2}	Power Down Current	All Inputs V_{CC} − 0.2V	Commercial		5
			Military		9
I_{OS}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = GND			−90

Capacitance

Parameters	Description	Test Conditions
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz
C_{OUT}	Output Capacitance	V_{CC} = 4.5V

Switching Characteristics

Parameter	Description	7C420-30, 7C421-30 7C424-30, 7C425-30 7C428-30, 7C429-30		7C420-40, 7C421-40 7C424-40, 7C425-40 7C428-40, 7C429-40		7C420-65, 7C421-65 7C424-65, 7C425-65 7C428-65, 7C429-65		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	40		50		80		ns
t_A	Access Time		30		40		65	ns
t_{RR}	Read Recovery Time	10		10		15		ns
t_{PR}	Read Pulse Width	30		40		65		ns
t_{LZR}	Read LOW to Low Z	3		3		3		ns
t_{DVR}	Read HIGH to Data Valid	3		3		3		ns
t_{HZR}	Read HIGH to High Z		20		25		30	ns
t_{WC}	Write Cycle Time	40		50		80		ns
t_{PW}	Write Pulse Width	30		40		65		ns
t_{HWZ}	Write HIGH to Low Z	10		10		10		ns
t_{WR}	Write Recovery Time	10		10		15		ns
t_{SD}	Data Set-Up Time	18		20		30		ns
t_{HD}	Data Hold Time	0		0		10		ns
t_{MRSC}	$\overline{MR}$ Cycle Time	40		50		80		ns
t_{PMR}	$\overline{MR}$ Pulse Width	30		40		65		ns
t_{RMR}	$\overline{MR}$ Recovery Time	10		10		15		ns
t_{RPW}	Read HIGH to $\overline{MR}$ HIGH	30		40		65		ns
t_{WPW}	Write HIGH to $\overline{MR}$ HIGH	30		40		65		ns
t_{RTC}	Retransmit Cycle Time	40		50		80		ns
t_{PRT}	Retransmit Pulse Width	30		40		65		ns
t_{RTR}	Retransmit Recovery Time	10		10		15		ns
t_{EFL}	$\overline{MR}$ to $\overline{EF}$ LOW		40		50		80	ns
t_{HFH}	$\overline{MR}$ to $\overline{HF}$ HIGH		40		50		80	ns
t_{FFH}	$\overline{MR}$ to $\overline{FF}$ HIGH		40		50		80	ns
t_{REF}	Read LOW to $\overline{EF}$ LOW		30		35		60	ns
t_{RFF}	Read HIGH to $\overline{FF}$ HIGH		30		35		60	ns
t_{WEF}	Write HIGH to $\overline{EF}$ HIGH		30		35		60	ns
t_{WFF}	Write LOW to $\overline{FF}$ LOW		30		35		60	ns
t_{WHF}	Write LOW to $\overline{HF}$ LOW		40		50		80	ns
t_{RHF}	Read HIGH to $\overline{HF}$ HIGH		40		50		80	ns
t_{RAE}	Effective Read from Write HIGH		30		35		60	ns
t_{RPE}	Effective Read Pulse Width after $\overline{EF}$ HIGH	30		40		65		ns
t_{WAF}	Effective Write from Read HIGH		30		35		60	ns
t_{WPF}	Effective Write Pulse Width after $\overline{FF}$ HIGH	30		40		65		ns
t_{XOL}	Expansion Out LOW Delay from Clock		25		35		55	ns
t_{XOH}	Expansion Out HIGH Delay from Clock		25		35		60	ns

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CYPRESS SEMICONDUCTOR

Features

- **High speed**
- **Low power**
- **10% power supply**
- **Available in DIP, LCC, PLCC, PGA**

Product Characteristics

Cypress offers the low power alternative for Bit-Slice and DSP applications. 1.2 micron CMOS technology provides products that are faster or as fast as their bipolar equivalents at one-half to one-tenth the power.

These products are available in a variety of packages including DIP, LCC, PLCC, SOIC, and Pin Grid Array. Reliability advantages include ESD protection on all pins, latch-up protection via a substrate bias generator and layout techniques, and low power dissipation.

These products are the:

CY7C510	16 x 16 Multiplier-Accumulator
CY7C516	16 x 16 Multiplier
CY7C517	16 x 16 Multiplier
CY7C901	4-Bit Slice ALU
CY7C909	Microprogram Sequencer
CY7C910	Microprogram Controller
CY7C911	Microprogram Sequencer
CY7C9101	16-Bit Slice ALU

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Military	−55°C to +125°C	

Maximum Ratings

(Above which the useful life may be impaired)

Storage Temperature ..... −65°C to +150°C

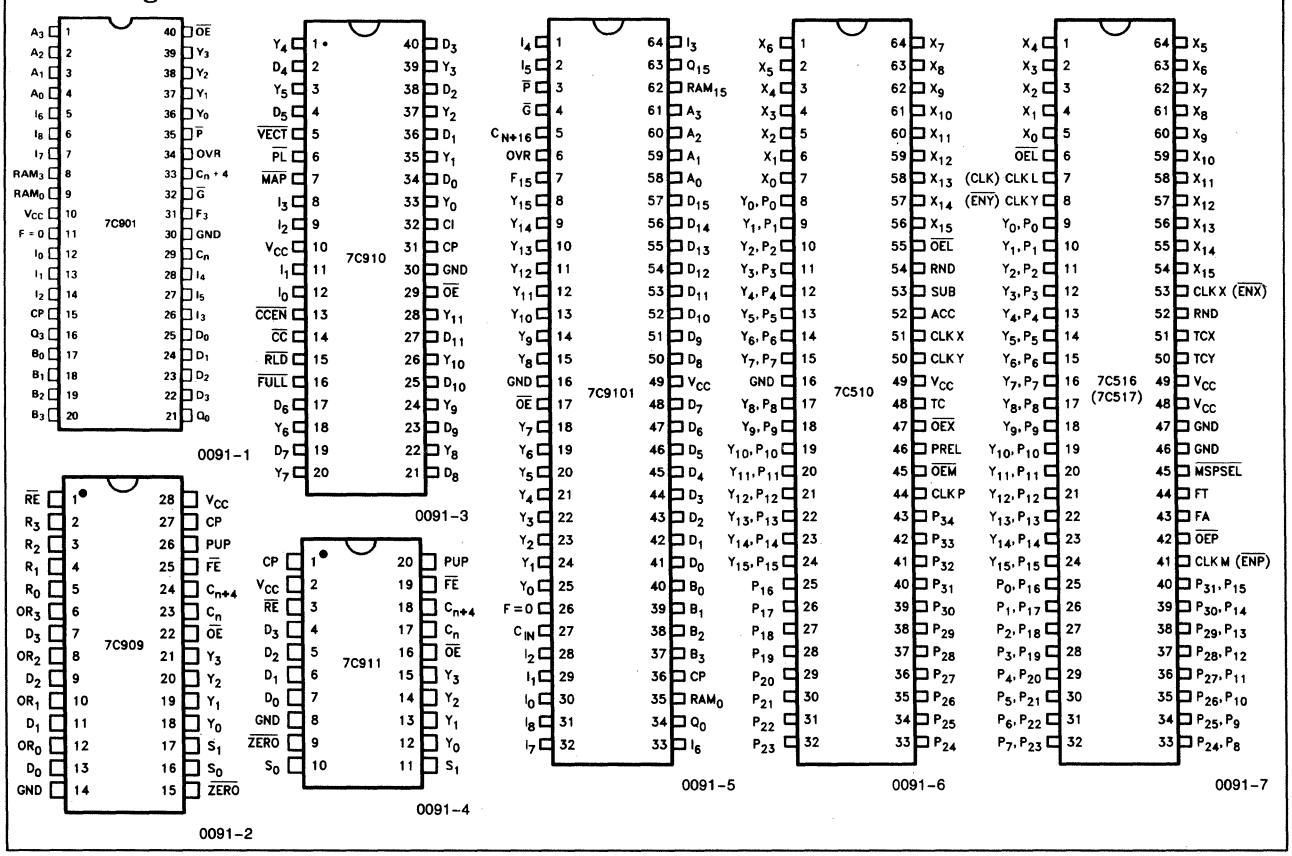
Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential .... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State..... −0.5V to +7.0V

DC Input Voltage ..... −3.0V to +7.0V

Pin Configurations



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Electrical Characteristics Over the Operating Range

Product	Parameters	Description	Test Conditions		Min.	Max.	Units
ALL	V_{OH}	Output HIGH Voltage	V_{CC} = Min.		2.4		V
	V_{OL}	Output LOW Voltage	V_{CC} = Min.			0.4	V
	V_{IH}	Input HIGH Voltage			2.0	V_{CC}	V
	V_{IL}	Input LOW Voltage				0.8	V
	I_{IX}	Input Leakage Current	$GND \le V_I \le V_{CC}$		−10	+10	μA
7C510 7C516 7C517	I_{CC}	Supply Current	$V_{IH} \ge 3.85V$, $V_{IL} \le 0.4V$	Commercial		20	mA
				Military		25	
	I_{CC}	Supply Current	V_{CC} = Max., f_O = 10 MHz	Commercial		100	mA
				Military		110	
7C901	I_{CC}	Supply Current	$V_{IH} \ge V_{CC} - 1.2V$, $V_{IL} \le 0.4V$, f_O = 10 MHz	Commercial		26.5	mA
				Military		31	
	I_{CC}	Supply Current	V_{CC} = Max.	Commercial		70	mA
				Military		90	
7C909 7C911	I_{CC}	Supply Current	$V_{IH} \ge 3.0V$, $V_{IL} \le 0.4V$, V_{CC} = Max.	Commercial		35	mA
				Military		35	
	I_{CC}	Supply Current	V_{CC} = Max., I_{OUT} = 0 mA	Commercial		55	mA
				Military		55	
7C910	I_{CC}	Supply Current	$V_{IH} \ge 3.85V$, $V_{IL} \le 0.4V$	Commercial		35	mA
				Military		50	
	I_{CC}	Supply Current	V_{CC} = Max.	Commercial		70	mA
				Military		90	
7C9101	I_{CC}	Supply Current (Quiescent)	$V_{IH} \ge 3.85V$, $V_{IL} \le 0.4V$, $\overline{OE}$ = High	Commercial		25	mA
				Military		30	
	I_{CC}	Supply Current	V_{CC} = Max., f_O = 10 MHz, $\overline{OE}$ = High	Commercial		60	mA
				Military		85	

Note:
1. All supply current specifications are at V_{CC} = Max.

Selector Guide

Product	Description	Temp. Range	Speed Grades	Units
7C510	Multiply-Accumulate Time	Commercial	45, 55, 65, 75	ns
		Military	55, 65, 75	
7C516	Clocked Multiply Time	Commercial	38, 45, 55, 65, 75	ns
		Military	42, 55, 65, 75	
7C517	Clocked Multiply Time	Commercial	38, 45, 55, 65, 75	ns
		Military	42, 55, 65, 75	
7C901	Read-Modify-Write Cycle Time	Commercial	23, 31	ns
		Military	27, 32	
7C909	Clock to Output Cycle Time	Commercial	30, 40	ns
		Military	30, 40	
7C910	Clock Period I = 14	Commercial	40, 50, 93	ns
		Military	46, 51, 99	
7C911	Clock to Output Cycle Time	Commercial	30, 40	ns
		Military	30, 40	
7C9101	Read-Modify-Write Cycle Time	Commercial	30, 40	ns
		Military	35, 45	

Cypress Semiconductor

Features

- Fast
  - 35 ns worst case propagation delay, I to Y
- Low power CMOS
  - I_{CC} (max. at 10 MHz) = 145 mA (commercial)
  - I_{CC} (max. static) = 30 mA (commercial)
- V_{CC} margin
  - 5V ±10%
  - All parameters guaranteed over commercial and military operating temperature range
- Instruction set and architecture optimized for high speed controller applications
- CY7C9117 separate I/O
  - One and two operand arithmetic and logical operations
  - Bit manipulation, field insertion/extraction instructions
  - Eleven types of instructions
- Immediate instruction capability
- 16-bit barrel shifter capability
- 32-word x 16-bit register file
- 8-bit status register
  - Four ALU status bits
  - Link bit and three user definable status bits
- ESD protection
  - Capable of withstanding greater than 2001V static discharge voltage
- Pin compatible and functionally equivalent to 29116, 29116A, 29C116, 29117, 29117A, 29C117

Functional Description

When used with the CY7C517 multiplier, the CY7C9115, CY7C9116 and CY7C9117 also support microprogrammed processor applications.

The CY7C9115, CY7C9116 and CY7C9117 are shown in the block diagram, consists of a 32-word by 16-bit single-port RAM register file, a 16-bit arithmetic unit and logic unit, an instruction latch and decoder, a data latch, an accumulator register, a 16-bit barrel shifter, a priority encoder, a status register, a condition code generator and multiplexer, and three-state output buffers.

The instruction set of the CY7C9115, CY7C9116 and CY7C9117 can be divided into eleven instruction types: single-operand, two-operand, single-bit shifts, rotate and merge, rotate and compare, rotate by n-bits, bit oriented instructions, prioritize, Cyclic Redundancy Check (CRC), status, and NO-OP. Instruction execution occurs in a single clock cycle except for Immediate Instructions, which require two clock cycles to execute.

The CY7C9116 and CY7C9117 are pin compatible, functional equivalent of the industry standard 29116, 29116A, 29C116, 29117, 29117A, 29C117 with improved performance.

Fabricated in an advanced 1.2 micron, two-level metal CMOS process, the CY7C9115, CY7C9116 and CY7C9117 eliminates latchup, has ESD protection greater than 2001V, and achieves superior performance with low power dissipation.

Description of Architecture

The CY7C9115, CY7C9116 and CY7C9117 are 16-bit microprogrammed arithmetic and logic units comprised of the following sections (see block diagram):

- 32 Word x 16-Bit Register File
- Data Latch
- Instruction Latch and Decoder
- Accumulator
- Logic Unit with a 16-Bit Barrel Shift Capability
- Arithmetic Unit
- Priority Encoder
- Condition Code Generator and Multiplexer
- Status Register
- Output Buffers

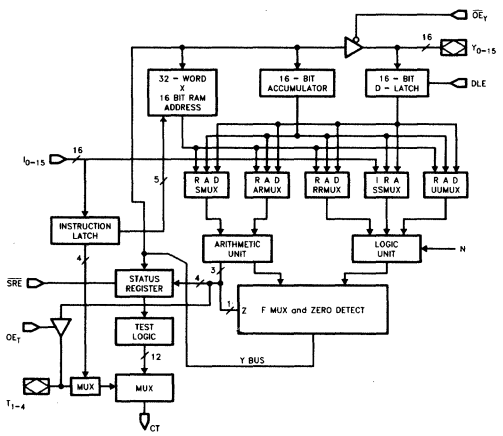


Figure 1. CY7C9115/9116 Block Diagram

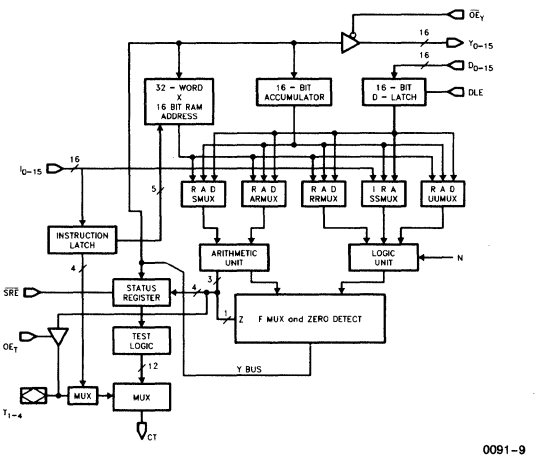
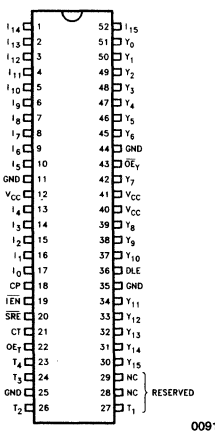


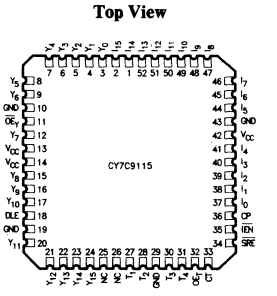
Figure 2. CY7C9117 Block Diagram

Pin Configurations CY7C9116



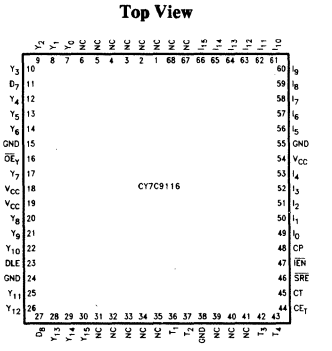
DIP

Top View



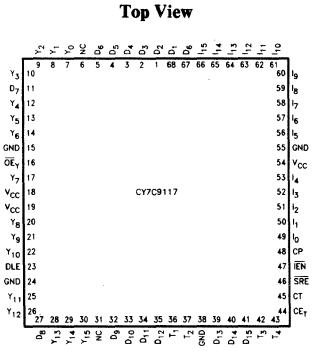
LCC
PLCC

Top View



PLCC

Top View



LCC/PLCC
NC = No Connect

Selection Guide

		7C9115-35 7C9116-35 7C9117-35	7C9115-4X 7C9116-53 7C9117-53	7C9115-65 7C9116-65 7C9117-65	7C9115-79 7C9116-79 7C9117-79
Worst Case I-Y Propagation Delay (ns)	Commercial	35	45	65	
	Military		40	65	79
Maximum Operating Current @ 12.5 MHz (mA)	Commercial	145	145	145	
	Military		165	165	165*

*10 MHz operation

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High Performance 32-Bit RISC Processor

CYPRESS SEMICONDUCTOR

CY7C601

Features

- **Reduced instruction set computer (RISC) architecture**
  - **— Simple format instructions**
  - **— Most instructions execute in single cycle**
- **Very high performance**
  - **— 30 ns instruction cycle with 4 stage pipeline**
  - **— 25 million instructions per second (MIPS)**
  - **— 20 equivalent VAX MIPS**
- **Large windowed register file**
  - **— 136 general purpose 32-bit registers**
  - **— 8 overlapping windows of 24 registers each**
- **All pipeline interlocks implemented in hardware**
- **Large virtual address space**
  - **— 32-bit virtual address bus**
  - **— 8-bit address space identifier**
- **Multitasking support**
  - **— User/supervisor modes**
  - **— Privileged instructions**
- **Parallel processing support**
- **Artificial intelligence support**
- **High performance coprocessor interface**
  - **— Concurrent execution of floating point instructions**
- **0.8 micron 2-layer metal CMOS technology**
- **207 pin grid array package**
- **Power less than two watts**

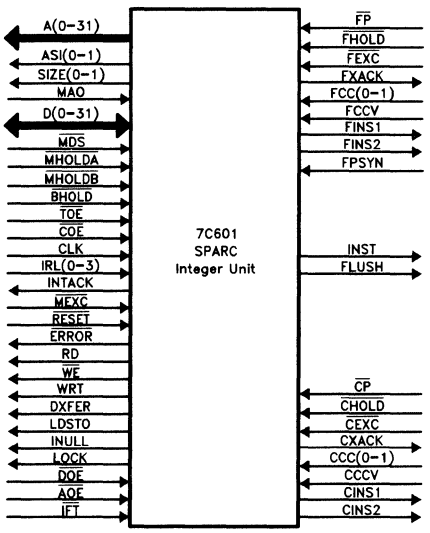
Overview

The CY7C601 Integer Unit is a high speed CMOS implementation of the new SPARC 32-bit RISC architecture microprocessor. This architecture makes possible the implementation of a microprocessor which can execute instructions for high level language programs at rates approaching one instruction per processor clock. The CY7C601 supports a tightly-coupled floating point coprocessor and a second implementation-definable coprocessor. The CY7C601 SPARC processor provides the following features:

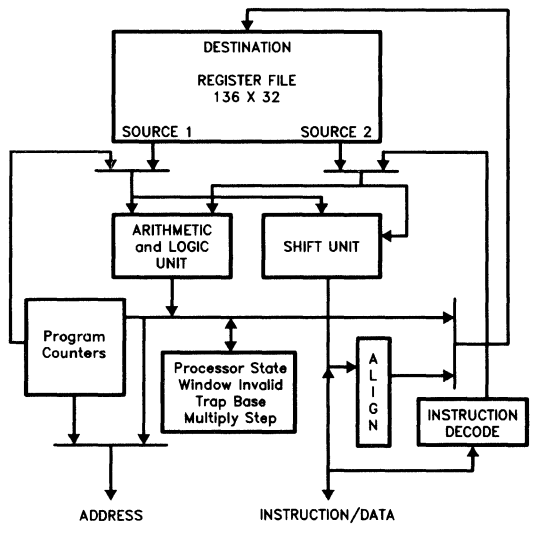
Simple Instructions—Most instructions require only a single arithmetic operation.

Simple Instruction Format—All instructions are 32 bits wide and are aligned on 32-bit boundaries in memory. There are only three basic instruction formats which feature uniform placement of opcode and address fields.

Block Diagrams



0144-1



0144-2

Selection Guide

		7C601-25	7C601-33
Clock Frequency (MHz)		25	33
Maximum Operating Current (mA)	Commercial	TBD	600
	Military	TBD	TBD

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Overview (Continued)

Register-Intensive Architecture—Most instructions operate on either two registers or one register and a constant, and place the result in a third register. Only load and store instructions access off chip memory.

A Large "Windowed" Register File—The processor has on chip a large number of 32-bit registers configured as 8 overlapping sets of 24 registers each. This scheme allows compilers to cache local values across subroutine calls, and provides a register-based parameter passing mechanism.

Delayed Control Transfer—The processor always fetches the next instruction after a control transfer, and either executes it or annuls it depending on the state of a bit in the control transfer instruction. This feature allows compilers to rearrange code to place a useful instruction after a delayed control transfer and thereby take better advantage of the processor's pipeline.

One Cycle Execution—The processor is capable of fetching instructions at a rate of one per processor cycle. This allows most instructions other than load/store and floating point instructions, to execute in one cycle.

Concurrent Floating Point—Floating point instructions can execute concurrently with each other and with non-floating point instructions.

Fast Interrupt Response—Interrupt inputs are sampled every cycle and can be acknowledged in one to three cycles. The first instruction of an interrupt service routine can be executed within 6 to 8 cycles of receiving the interrupt request.

The 7C600 Family

The SPARC processor family consists of a CY7C601 Integer Unit (IU) to perform all non-floating point operations and a CY7C608 Floating Point Controller (FPC) which interfaces to the CY7C609 FPU to perform floating point arithmetic concurrent with the IU. Support is also provided for a second generic coprocessor interface. The IU communicates with external memory via a 32-bit address bus and a 32-bit data/instruction bus. In typical data processing applications, the IU, FPC and FPU are combined with a high performance CY7C604 Cache Control/Memory Management Unit (CMU) and CY7C157 16K X 16 Cache RAMs. In many dedicated controller applications the IU can function by itself with high speed local memory.

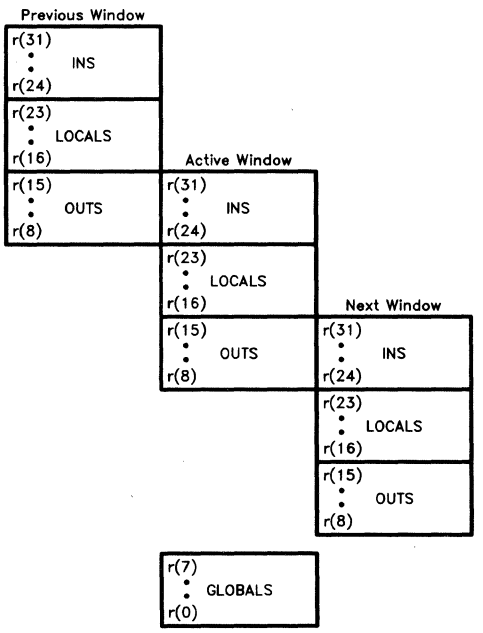
Coprocessor Interface

The IU is the basic processing engine which executes all of the instruction set except for floating point operations. The FPC and IU operate concurrently. The FPC recognizes floating point instructions and places them in a queue while the IU continues to execute non-floating point instructions. If the FPC encounters an instruction which will not fit in its queue, the FPC holds the IU until the instruction can be stored. The FPC contains its own set of registers on which it operates. The contents of these registers are transferred to and from external memory under control of the IU via floating point load/store instructions. Processor interlock hardware hides floating point concurrency from the compiler or assembly language programmer. A program containing floating point computations generates the same results as if instructions were executed sequentially.

Registers

The CY7C601 Integer Unit contains a large 136 X 32 register file which is divided into 8 windows, each with twenty-four 32-bit working registers, and each having access to the same eight 32-bit global registers. A current window pointer (CWP) field in the processor state register (PSR) keeps track of which window is currently active.

The current window pointer is decremented when the processor executes a call to a subroutine and is incremented when the processor returns.



0144-3

The registers in each window are divided into ins, outs, and locals. The eight global registers are shared by all windows and appear as registers 0–7 in each window. Registers 8–15 serve as outs, registers 16–23 as locals, and 24–36 as ins. Each window shares its ins and outs with adjacent windows. The outs of a previous window are the ins of the current window, and the outs of the current window are the ins of the next window. The globals are equally available to all windows and the locals are unique to each window. The windows are joined together in a circular stack where the outs of window 7 are the ins of register 0.

Multitasking Support

The CY7C601 supports a multitasking operating system by providing user and supervisor modes. Some instructions are privileged and can only be executed while the processor is in supervisor mode. Changing from user to supervisor mode requires taking a hardware interrupt or executing a trap instruction.

In addition, multiprocessing is supported by the CY7C605 CMU.

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DATEL

GENERAL PURPOSE A/D CONVERTERS

Model	Resolution	Conversion Time (Max)	Linearity (Max)	Input Range	Package	Temp Range[1] C/I/M	MIL STD 883 QL
ADC-EH8B2	8-Bits	2 µs	± ½ LSB	0 to + 10V ± 5V	2 × 2 × 0.375 in.	C	
ADC-EH8B1		4 µs					
ADC-847A	8-Bits	9 µs	± 1 LSB	0 to + 5V, + 10V ± 5V, ± 10V	18-pin DIP	C	
ADC-847B			± ¼ LSB				
ADC-830C	8-Bits	100 µs	± ½ LSB	0 to + 5V	20-pin DIP	C	
ADC-EK8B	8-Bits	1.8 ms	± ½ LSB	0 to + 10V, ± 5V	24-pin DIP	C	
ADC-ET-8	8-Bits	1.8 ms	± ½ LSB	0 to + 10V, ± 5V	24-pin DIP	C,M	
ADC-EH10B2	10-Bits	2 µs	± ½ LSB	0 to + 10V, ± 5V	3 × 2 × 0.375 in.	C	
ADC-EH10B1		4 µs					
ADC-EK10B	10-Bits	6 ms	± ½ LSB	0 to 10V, ± 5V	24-pin DIP Monolithic	C,M	
ADC-856	10-Bits	1 µs/LSB	± ½ LSB	0 to + 5V, + 10V ± 2.5V, ± 5V, ± 10V	28-pin DIP	C,M	
ADC-EH12B3	12-Bits	2 µs	± ½ LSB	0 to 10V ± 5V	4 × 2 × 0.375 in.	C	
ADC-EH12B2		4 µs					
ADC-EH12B1		8 µs					
ADC-HZ12	12-Bits	8 µs	± ½ LSB	0 to + 5V, + 10V ± 2.5V, ± 5V, ± 10V	32-pin DIP	C,M	883,QL
ADC-5211	12-Bits	13 µs	± ½ LSB	± 5V	24-pin DIP	C,M	QL
ADC-5212	12-Bits	13 µs	± ½ LSB	± 10V	24-pin DIP	C,M	QL
ADC-5214	12-Bits	13 µs	± ½ LSB	± 5V	24-pin DIP	C,M	QL
ADC-5215	12-Bits	13µs	± ½ LSB	± 10V	24-pin DIP	C,M	QL
ADC-5216	12-Bits	13 µs	± ½ LSB	0 to + 10V	24-pin DIP	C,M	QL
ADC-HX12	12-Bits	20 µs	± ½ LSB	0 to + 5V, + 10V ± 2.5V, ± 5V, ± 10V	32-pin DIP	C,M	883,QL
ADC-HC12BMC	12-Bits	300 µs	± ½ LSB	0 to + 5V, ± 10V ± 2.5V, ± 5V, ± 10V	32-pin DIP	C,M	QL
ADC-EK12D	3½ Digits	12 ms	± ½ LSB	0 to + 10V	24-pin DIP	C,I,M	
ADC-EK12B	12-Bits	24 ms	± ½ LSB	0 to + 10V, ± 5V	24-pin DIP	C	
ADC-ET12B	12-Bits	24 ms	± 1½ LSB	0 to + 10V, ± 5V	24-pin DIP	C,I,M	
			± ½ LSB				
			± ½ LSB				
ADC-7109	12-Bits	33 ms	1 Count	V+ to V−	40-pin DIP	C	

HIGH SPEED A/D CONVERTERS

Model	Resolution	Conversion Time (Max)	Linearity (Max)	Input Range	Package	Temp Range[1] C,M	MIL-STD-883 QL
ADC-815	8 Bits	700 ns	± ½ LSB	0 to + 5V, + 10V, + 20V ± 2.5V, ± 5V, ± 10V	24-pin DIP	C,M	QL
ADC-5101	8 Bits	900 ns	± ½ LSB	0 to − 5V, − 10V, − 20V 0 to + 5V, + 10V, + 20V ± 2.5V, ± 5V, ± 10V	24-pin DIP	C,M	QL
ADC-5101H							
ADC-825	8 Bits	1 µs	± ½ LSB	0 to + 5V, + 10V, + 20V ± 2.5V, ± 5V, ± 10V	24-pin DIP	C,M	QL
ADC-881	8 Bits	1 µs	± 0.04 LSB	± 5V	MODULE	C	
ADC-510	10 Bits	425 ns	± ½ LSB	0 to + 10V, + 20V ± 10V	32-pin DIP	C,M	QL
ADC-515	10 Bits	650 ns	± ½ LSB	0 to + 10V, + 20V ± 10V	32-pin DIP	C,M	QL
ADC-816	10 Bits	800 ns	± ½ LSB	0 to − 10V, − 20V ± 2.5V, ± 5V, ± 10V	32-pin DIP	C,M	883,QL
ADC-826	10 Bits	1.4 µs	± ½ LSB	0 to − 5V, − 10V, − 20V ± 2.5V, ± 5V, ± 10V	32-pin DIP	C,M	QL
ADC-868	12 Bits	500 ns	± ½ LSB	0 to ± 5V, ± 2.5V	MODULE	C	
ADC-500BMC	12 Bits	500 ns	0.0125% FSR ± ½ LSB	0 to + 10V ± 10V	32-pin DIP	C,M	QL
ADC-500BMM		500 ns					
ADC-505BMC		550 ns					
ADC-505BMM		550 ns					
ADC-508BMC		700 ns					
ADC-508BMM		700 ns					

[1]C = 0°C to 70°C I = − 25°C to + 85°C M = − 55°C to + 125°C

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HIGH SPEED A/D CONVERTERS

Model	Resolution	Conversion Time (Max)	Linearity (Max)	Input Range	Package	Temp Range[2] C,M	MIL STD 883 QL
ADC-520	12 Bits	800 ns	±½ LSB	0 to +10V, +20V, −20V ±10V	32-pin DIP	C,M	QL
ADC-521				0 to +5V, ±2.5			
ADC-511	12 Bits	1 µs	±¾ LSB	0 to +10V ±5V	24-pin DIP	C,M	
ADC-810	12 Bits	2 µs	±1 LSB	0 to +10V, +20V	32-pin DIP	C,M	
ADC-817A	12 Bits	2 µs	±1 LSB	0 to −5V, −10V ±2.5V, ±5V, ±10V	32-pin DIP	C,M	
ADC-827A	12 Bits	3 µs	±1 LSB	0 to −5V, −10V ±2.5V, ±5V, ±10V	32-pin DIP	C,M	
ADC-811	12 Bits	3 µs	±1 LSB	0 to +10V, +20V ±5V, ±10V	32-pin DIP	C,M	
ADC-800	15 Bits	400 ms	2 LSB	−Vs +1.5V to +Vs −1.5V	40-pin DIP	C	
ADC-974	16 Bits	2.5 µs	±½ LSB @ 14 Bits	±5V	MODULE	C	

FLASH A/D CONVERTERS

Model	Resolution	Conversion Time (Max)	Linearity (Max)	Input Range	Temp Range[1] C,M	MIL STD 883 QL
ADC-207	7 Bits	50 nS	±½ LSB	0 to +5V	C,M	883
ADC-303	8 Bits	10 nS	±½ LSB	0 to −2V	C	—
ADC-302	8 Bits	20 nS	±½ LSB	0 to −2V	C	—
ADC-301	8 Bits	33 nS	±½ LSB	0 to −2V	C	—
ADC-300	8 Bits	50 nS	±½ LSB	0 to −2V	C	—
ADC-208	8 Bits	50 nS	±0.6 LSB	0 to +5V	C,M	883
ADC-310	10 Bits	50 nS	±1.75 LSB	0 to −2V	C	

SAMPLING A/D CONVERTERS

Model	Resolution	Throughput	Linearity (Max)	Input Range	Package	Temp Range[1] C,M	MIL STD 883 QL
ADS-115	10 Bits	1 MHz	±½ LSB	0 to +10V	32-pin DIP	C,M	QL
ADS-116	10 Bits	1 MHz	±½ LSB	−10 to +10V	32-pin DIP	C,M	QL
ADS-21	12 Bits	1.3 MHz	±0.0125% FSR ±½ LSB	0 to +10V, 0 to −5V, −10V, −20V ±5V, ±10V	46-pin DIP	C	
ADS-22	12 Bits	1 MHz	±0.0125% FSR ±½ LSB	0 to +10V, 0 to −5V, −10V, −20V ±5V, ±10V	46-pin DIP	C	
ADS-105	12 Bits	1 MHz	±0.0125% FSR ±½ LSB	0 to +10V	32-pin DIP	C,M	QL
ADS-106	12 Bits	1 MHz	±0.0125% FSR ±½ LSB	±10V	32-pin DIP	C,M	QL
ADS-125	12 Bits	700 kHz	±½ LSB	0 to +10V, ±10V	32-pin DIP	C,M	QL
ADS-126	12 Bits	700 kHz	±½ LSB	0 to +5V, ±2.5V	32-pin DIP	C,M	
ADS-111	12 Bits	500 kHz	±¾ LSB	0 to +10V, ±5V	24-pin Dlp	C,M	
ADC-HS12	12 Bits	66 kHz	±½ LSB	0 to +5V, +10V ±2.5V, ±5V, ±10V	32-pin DIP	C,M	
ADC-674ZA	12 Bits	55 kHz	±1 LSB ±½ LSB	0 to +10V, +20V ±5V, ±10V	28-pin DIP	C,M	
ADC-674ZB							
ADC-674ZC							
ADC-574ZA	12 Bits	35 kHz	±1 LSB	0 to +10V, +20V ±5V, ±10V	28-PIN DIP	C	
ADC-574ZB			±½ LSB				
ADC-574ZC			±½ LSB				
ADC-B207/208	7/8 Bits	20 MHz	±0.6 LSB	0 to +5V	6.3 × 4 in.	C	
ADC-B303E	8 Bits	100 MHz	±½ LSB	0 to +1V ±0.5V	Eurocard size Pin connector	C	
ADC-B302E	8 Bits	50 MHz	±½ LSB			C	
ADC-B301E	8 Bits	30 MHz	±½ LSB			C	
ADC-B304E	8 Bits	20 MHz	±½ LSB			C	
ADC-B10E	10 Bits	12 MHz	±1.75 LSB			C	
ADC-B500	12 Bits	1.25 MHz	±0.0125% FSR ±½ LSB	0 to −5V, −10V, 0 to −20V, +10V ±5V, ±10V	3.8 × 4.5 in Board	C	
ADC-B500-1							
ADC-B505	12 Bits	1.1 MHz	±0.0125% FSR ±½ LSB	0 to −5V, −10V, 0 to −20V +10V, ±5V, ±10V	3.8 × 4.5 Board	C	

*Includes ADC-500 and SHM-45 [1]C = 0°C to 70°C I = −25°C to +85°C M = −55°C to +125°C

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D/A CONVERTERS

Model	Resolution	Settling Time (Max)	Linearity Error (Max)	Output Range	Package	Temp Range[1] C,M	MIL STD 883 QL
DAC-8303	8 Bits	7.5 ns	± ½ LSB	0 to −1.054V	2 × 3 × 0.375 in. (50 × 75 × 10 mm) Module	C	
DAC-0805	8 Bits	8 ns	± ½ LSB	0 to −637.5 mV	24-pin DIP Hybrid	I	
DAC-HF8	8 Bits	25 ns	± ½ LSB	0 to +5 mA ±2.5 mA	24-pin DIP Hybrid	C,M	QL
DAC-08	8 Bits	150 ns	± ½ LSB	0 to −2 mA	16-pin DIP Monolithic	C,M	
DAC-7523	8 Bits	200 ns	± ½ LSB	± Vref / Rin	16-pin DIP Monolithic	C	
DAC-IC8BC	8 Bits	300 ns	± ½ LSB	0 to −2 mA	16-pin DIP Monolithic	C,M	
DAC-608C	8 Bits	1 µs	± ½ LSB	$\frac{\text{Vref}}{15\text{k}\Omega}\ \frac{\text{D}}{256}$	20-pin DIP Monolithic	C	
DAC-UP8	8 Bits	2 µs	± ½ LSB	0 to +10V ±5V	22-pin DIP Monolithic	C,M	
DAC-330	10 Bits	4.7 ns	±1 LSB	0 to −1V	28-pin DIP Monolithic	C	
DAC-HF10	10 Bits	25 ns	± ½ LSB	0 to +5 mA ±2.5 mA	24-pin DIP Hybrid	C,M	QL
DAC-IC10	10 Bits	250 ns	± ½ LSB ±1 LSB ± ½ LSB	0 to −4 mA	16-pin DIP Monolithic	C,M	
DAC-610C	10 Bits	500 ns	± ½ LSB	$\frac{\text{Vref}}{15\text{k}\Omega}\ \frac{\text{D}}{256}$	20-pin DIP Monolithic	C	
DAC-7533	10 Bits	800 ns	±0.1%	± Vref / Rin	16-pin DIP Monolithic	C	
DAC-HF12B	12 Bits	50 ns	± ½ LSB	0 to +5 mA ±2.5 mA	24-pin DIP Hybrid	C,M	QL
DAC-562C DAC-562M	12 Bits	400 ns	± ½ LSB ± ¼ LSB	0 to −2 mA ±1 mA	24-pin DIP Hybrid	C,M	
DAC-DG12B1 DAC-DG12B2	12 Bits	50 ns	± ½ LSB	0 to −10, ±5V, ±10V ±5V, ±10V	4 × 2 × 0.4 in. (102 × 51 × 10 mm)	C	
DAC-612C	12 Bits	1 µs	± ½ LSB	$\frac{\text{Vref}}{15\text{k}\Omega}\ \frac{\text{D}}{4096}$	24-pin DIP Hybrid	C	
DAC-7541	12 Bits	1 µs	±0.012%	± Vref / Rin	18-pin DIP Monolithic	C	
DAC-7134BJ DAC-7134UJ	12 Bits	3 µs	± ½ LSB	± Vref / Rin Vref/Rin	28-pin DIP Monolithic	C	
DAC-HK12	12 Bits	3 µs	± ½ LSB	0 to +5V, +10V ±2.5V, ±5V, ±10V	24-pin DIP Hybrid	C,M	883, QL
DAC-HZ12	12 Bits	3 µs	± ½ LSB	0 to ±5V, ±10V ±2.5V, ±5V, ±10V	24-pin DIP Hybrid	C,M	883, QL
DAC-HZ12D	3 Digits	3 µs	± ¼ LSB	0 to 2.5V 0 to +5V 0 to +10V	24-pin DIP Hybrid	C,M	
DAC-7134BK DAC-7134UK	13 Bits	3 µs	± ½ LSB	± Vref / Rin Vref / Rin	28-pin DIP Hybrid	C	
DAC-7134BL DAC-7134UL	14 Bits	3 µs	± ½ LSB	± Vref / Rin Vref/Rin	28-pin DIP Hybrid	C	
DAC-HP16B	16 Bits	15 µs	0.003%	0 to ±10V 0 to ±5V	24-pin DIP Hybrid	C,M	883, QL

[1] C = 0°C to 70°C I = −25°C to +85°C M = −55°C to +125°C

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SAMPLE/HOLD AMPLIFIERS

Model	Linearity	Acquisition Time	Aperture Delay	Input Range	Hold-Mode Droop	Bandwidth	Package	Temp Range[1] C,M	MIL STD 883 QL
SHM-91	0.003%	2 μs	15 ns	±10V	5 μV/μs	1 MHz	24-pin DIP	C,M	QL
SHM-45	0.01%	200 ns	6 ns	±5, ±10V	0.5 μV/μs	16 MHz	24-pin DIP	C,M	QL
SHM-4860	0.01%	200 ns	6 ns	±10V	0.5 μV/μs	16 MHz	24-pin DIP Hybrid	C,M	QL
SHM-5	0.01%	350 ns	20 ns	±10V	20 μV/μs	5 MHz	2×2×0.375 in (50×50×10 mm) Module	C	
SHM-20C	0.01%	1 μs	30 ns	±10V	0.08 μV/μs	2 MHz	14-pin DIP Monolithic	C	
SHM-IC-1	0.01%	5 μs	50 ns	±10V	50 μV/ms	2 MHz	14-pin DIP Monolithic	C,M	
SHM-LM-2	0.01%	6 μs	200 ns	±10V	0.2mV/ms	1 MHz	8-pin TO-99 Monolithic	C	
SHM-6	0.02%	2 μs	20 ns	±10V	10 μV/μs	5 MHz	32-pin DIP Hybrid	C,M	QL
SHM-9	0.01%	6 μs	200 ns	±11.5V	0.2 mV/ms	4 MHz	16-pin DIP Hybrid	C,M	QL
SHM-UH3	0.05%	30 ns	5 ns	±5V	50 μV/μs	45 MHz	2×2×0.375 in (50×50×10 mm) Module	C	
SHM-HU	0.1%	25 ns	6 ns	±2.5V	50 μV/μs	50 MHz	24-pin DIP Hybrid	C	QL
SHM-7MC	0.1%	40 ns	3 ns	±5V, ±2.5V	100 μV/μs	40 MHz	24-pin DIP Hybrid	C	
SHM-40	0.1%	40 ns	3 ns	±2.5V	100 μV/μs	40 MHz	24-pin DIP Hybrid	C,M	QL
SHM-360	0.15%	20 ns	—	±3V	10 mV/μs	25 MHz	24-pin DIP Monolithic	C	
SHM-361		12 ns				55 MHz			
SHM-30C	0.01%	500 ns	20 ns	±10V	0.01 μV/μs	4.5 MHz	14-pin DIP Monolithic	C	

DATA ACQUISITION SUBSYSTEMS

Model	Resolution	Channels	Through-Put Rate	Linearity (Max)	Gain Range	Input Range	Package	Temp Range[1]	MIL STD 883 QL
DAS-952R	8 Bits	16 Single Ended	17 kHz	±½ LSB	—	0 to +5V	40-pin DIP Monolithic	I	
HDAS-8	12 Bits	8 Diff.	50 kHz	±¾ LSB	1 to 200	0 to +50 mV 0 to +10V ±50 mV to ±10V	62-pin Hybrid	C,M	883, QL
HDAS-16	12 Bits	16 Single Ended	50 kHz	±¾ LSB	1 to 200	0 to +50 mV 0 to +10V ±50 mV to ±10V	62-pin Hybrid	C,M	883, QL
MDAS-8D	12 Bits	8 Diff.	50 kHz	±1 LSB	—	0 to +5V 0 to +10V ±2.5V, ±5V, ±10V	Module	C	
MDAS-16	12 Bits	16 Single Ended	50 kHz	±1 LSB	—	0 to +5V 0 to +10V ±2.5V, ±5V, ±10V	Module	C	
MDAS-940D	12 Bits	8 Diff.	33 kHz	±½ LSB	1, 2, 4, 8	0 to +5V 0 to +10V ±5V, ±10V	Module	C	
MDAS-940S	12 Bits	16 Single Ended	33 kHz	±½ LSB	1, 2, 4, 8	0 to +5V 0 to +10V ±5V, ±10V	Module	C	

Output logic for all devices is three-state TTL. [1]C = 0°C to 70°C I = −25°C to +85°C M = −55°C to +125°C

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OPERATIONAL AMPLIFIERS

Model	DC Open Loop Gain (V/V)	Settling Time 10V to 0.1%	Slew Rate (V/μSec)	Gain Bandwidth	Offset Drift (μV/°C)	Output	Package	Temp Range[1] C,M	MIL STD 883 QL
AM-427-1A	6.3×10^5		1.7	5 MHz	1.8	±11V/±18 mA	8-pin DIP	C	
AM-427-1B	10^6				0.6				
AM-427-2A	6.3×10^5		1.7	5 MHz	1.8	±11V/±18 mA	8-pin TO-99	C	
AM-427-2B	10^6				0.6				
AM-430A	100K	11 μs	0.5	2.5 MHz	1.3	+10V/+25 mA	8-pin TO-99	C	
AM-430B					0.6				
AM-450-2	25K	330 ns	30	12 MHz	20	±10V/±10 mA	8-pin TO-99	C,M	
AM-452-2	15K	200 ns	120	20 MHz	30	±10V/±10 mA	8-pin TO-99	C,M	
AM-453-2C	100K	—	13	10 MHz	30	±12V/±20 mA	8-pin TO-99	C,M	
AM-460-2C	150K	1.5 μs	7	12 MHz	10	±10V/±10 mA	8-pin TO-99	C	
AM-462-2	150K	1.0 μs	35	100 MHz	15	±10V/±10 mA	8-pin TO-99	C	
AM-464-2	100K	—	5	4 MHz	15	±35V/±10 mA	8-pin TO-99	C	
AM-500GC	10^6	200 ns to 0.01%	1000	100 MHz	5	±10V/±50 mA	14-pin DIP	C,M	QL
AM-500MC					7				
AM-500MM					10				
AM-1435	10^5	70 ns to 0.01%	300	1000 MHz	5	±7V/±14 mA	14-pin DIP	C,M	QL
AM-7650-1	10^6	—	2.5	2 MHz	0.05	±4.7V	14-pin DIP 8-pin TO-99	C	
AM-7650-2									

INSTRUMENTATION AMPLIFIERS

Model	Description	Gain Range	Gain Non-Linearity	Settling Time	Input Impedance	Output	Common Mode Rejection	Package	Temp Range C,M
AM-543MC	High Performance Hybrid Digitally Selectable Gain Ranges	1 to 128	0.01%	6 μsec.	$10^{12}\Omega$	±11V at ±1 mA	86 dB	24-pin DIP	C,M
AM-551MC	Low Cost, High Performance Hybrid	1 to 1000	0.01%	2 μsec.	$10^{12}\Omega$	±11V at ±5 mA	100 dB	16-pin DIP	C,M

SIGNAL CONDITIONING AND ISOLATION AMPLIFIERS

Model	Description	Isolation Voltage	Gain Range	Gain Non-Linearity	Input Resistance	Common Mode Rejection	Input Offset Voltage	Output	Temp Range C,M
AM-227	Low-cost Precision Isolation Amplifier	±1000V dc	10 to 1000	±0.005%	100 MΩ	176 dB	±150 μV	±10V at ±5 mA	C
SCM-100A	Low-Cost, Four Channel Isolation Amplifier	±1000V dc	1 to 1000	±0.03%	100 MΩ	156 dB	±20 μV	±5V at ±5 mA	C
SCM-100B				±0.02%		145 dB	±50 μV		
SCM-101									
SCM-103	4-chan Strain gage cond.	None	166.6 V/V or 50 V/V	±0.01%	100 MΩ	94 dB	±150 μV	±5V at ±5 mA	C

[1]C = 0°C to 70°C I = −25°C to +85°C M = −55°C to +125°C

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ACTIVE FILTERS

MODEL	NO. OF POLES	BUTTERWORTH	BESSEL	ELLIPTICAL	LOW PASS	HIGH PASS	BAND PASS	BAND REJECT	RESISTOR TUNING	DIGITAL TUNING	VOLTAGE TUNING	ACCURACY	FREQUENCY PS
FLJ-DC	2	•	•	•	•	•	•			•		0.1%	Note 1
FLJ-D1	2	•	•	•	•	•	•			•		0.1%	1-1.6 kHz
FLJ-D2	2	•	•	•	•	•	•			•		0.1%	100-160 kHz
FLJ-D5LA1	5			•	•					•		3%	10 Hz-2 kHz
FLJ-D5LA2	5			•		•				•		3%	100 Hz-20 kHz
FLJ-D6LA1	6			•	•					•		3%	10 Hz-2 kHz
FLJ-D6LA2	6			•		•				•		3%	100 Hz-20 kHz
FLJ-R3BA1	3					•			•			2%	10 Hz-2 kHz
FLJ-R3BA2						•			•			2%	100 Hz-20 kHz
FLJ-R8LA1	8			•	•				•			2%	10 Hz-2 kHz
FLJ-R8LA2	8			•	•				•			2%	100 Hz-20 kHz
FLJ-R8LB1	8			•					•			2%	10 Hz-2 kHz
FLJ-R8LB2	8			•					•			2%	100 Hz-20 kHz
FLJ-UR1BA1	1	•					•		•			3%	40 Hz-1.6 kHz
FLJ-UR1BA2	1	•					•		•			3%	400 Hz-10 kHz
FLJ-UR2BA1	2	•					•		•			3%	40 Hz-1.6 kHz
FLJ-UR2BA2	2	•					•		•			3%	400 Hz-10 kHz
FLJ-UR2EA1	2	•						•	•			3%	40 Hz-1.6 kHz
FLJ-UR2EA2	2	•						•	•			3%	400 Hz-10 kHz
FLJ-UR2LH1	2	•			•	•			•			3%	40 Hz-1.6 kHz
FLJ-UR2LH2	2	•			•	•			•			3%	400 Hz-20 kHz
FLJ-UR4HA1	4	•				•			•			3%	40 Hz-1.6 kHz
FLJ-UR4HA2	4	•				•			•			3%	400 Hz-5 kHz
FLJ-UR4HB1	4			•		•			•			3%	40 Hz-1.6 kHz
FLJ-UR4HB2	4			•		•			•			3%	400 Hz-20 kHz
FLJ-UR4LA1	4	•			•				•			3%	40 Hz-1.6 kHz
FLJ-UR4LA2	4	•			•				•			3%	400 Hz-20 kHz
FLJ-UR4LB1	4	•			•				•			3%	40 Hz-1.6 kHz
FLJ-UR4LB2	4	•			•				•			3%	400 Hz-20 kHz
FLJ-VB	2	•					•				•	±3%	200 Hz-20 kHz
FLJ-VH	4	•				•					•	±3%	20 Hz-20 kHz
FLJ-VL	4	•			•						•	±3%	100 Hz-100 kHz
FLT-U2	2	•			•	•	•		•			±5%	0.001Hz-200 kHz
FLT-C1	7			•	•								78 Hz-20 kHz

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ANALOG MULTIPLEXERS

Model	Channels	Settling Time 20V to 0.01%	Access Time	Input Voltage Range	Package	Temp Range[1] C,M	Features
MV-808	8 Single Ended	2.8 µs	350 ns	± 15V	16-pin DIP	C	Low ON Resistance Dielectrically Isolated CMOS
MV-1606	16 Single Ended	2.4 µs	300 ns	± 15V	28-pin DIP	C,M	
MVD-409	4 Differential	2.8 µs	350 ns	± 15V	16-pin DIP	C	
MVD-807	8 Differential	2.4 µs	300 ns	± 15V	28-pin DIP	C	
MX-808	8 Single Ended	3 µs	500 ns	± 15V	16-pin DIP	C	Overvoltage Protected
MX-818	8 Single Ended or 4 Differential	800 ns	125 ns	± 15V	18-pin DIP	C,M	High Speed
MX-1606	16 Single Ended	3 µs	500 ns	± 15V	28-pin DIP	C,M	Overvoltage Protected
MX-1616	16 Single Ended or 8 Differential	800 ns	150 ns	± 15V	28-pin DIP	C,M	High Speed
MXD-409	4 Differential	3 µs	500 ns	± 15V	16-pin DIP	C	Overvoltage Protected
MXD-807	8 Differential	3 µs	500 ns	± 15V	28-pin DIP	C	

[1]C = 0°C to 70°C I = −25°C to +85°C M = −55°C to +125°C

VOLTAGE INVERTERS

Model	Description	Package	Temperature Range
VI-7660-1	CMOS VOLTAGE CONVERTERS INPUT RANGE +1.5V to +10.0V	TO-99 Monolithic 8-pin DIP	0° to +70°C
VI-76602			

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VOLTAGE REFERENCES

Model	Nonlinearity % of F.S.	Drift	Package	Temperature Range	Description
VR-182A	± 1.43%	100 ppm/°C	2-LEAD TO-18 Monolithic	0° to +70°C	2.455V PRECISION BANDGAP VOLTAGE REFERENCE
VR-182B		50 ppm/°C			
VR-182C		30 ppm/°C			

VOLTAGE-TO-FREQUENCY CONVERTERS

Model	Description	Non-Linearity % of F.S.	Drift	Package	Technology	Operating Temperature Range (°C)
VFQ-1C	V/F, F/V Converter Operates to 100 kHz	0.05%	40 ppm/°C	14-pin DIP	Monolithic	0 to +70
VFQ-1R		0.05%				−25 to +85
VFQ-2C		0.01%				0 to +70
VFQ-3C		0.25%				0 to +70

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SRAM MONOLITHICS - DIP/LCC

Part Number	Organization	Speed min. (ns)	Typical DC Current I_{CC1} (mA)	Typical DC Current I_{SB1} (mA)	Typical DC Current I_{CCDR} (µA)	Dimensions (inches)	Package
DPS9167*	16K x 1	35	40	0.01	1	1.000 x 0.300 x 0.200	20-PIN DIP
DPS9167G*	16K x 1	35	40	0.01	1	0.420 x 0.290 x 0.085	20-PAD LCC
DPS9168*	4K x 4	25	50	0.02	15	1.000 x 0.300 x 0.200	20-PIN DIP
DPS9168G*	4K x 4	25	50	0.02	15	0.420 x 0.290 x 0.085	20-PAD LCC
DPS9116*	2K x 8	35	30	1	50	1.200 x 0.600 x 0.200	24-PIN DIP
DPS9116G*	2K x 8	35	30	1	50	0.550 x 0.450 x 0.085	32-PAD LCC
DPS9287*	64K x 1	25	50	1	5	1.100 x 0.300 x 0.200	22-PIN DIP
DPS9287G*	64K x 1	25	50	1	5	0.490 x 0.290 x 0.085	22-PAD LCC
DPS9788*	16K x 4	25	60	0.02	10	1.100 x 0.300 x 0.200	22-PIN DIP
DPS9788G*	16K x 4	25	60	0.02	10	0.490 x 0.290 x 0.085	22-PAD LCC
DPS9264	8K x 8	35	30	0.05	10	1.400 x 0.600 x 0.200	28-PIN DIP
DPS9264G	8K x 8	35	30	0.05	10	0.550 x 0.450 x 0.850	32-PAD LCC
DPS8181*	256K x 1	45	60	1	200	1.200 x 0.400 x 0.200	24-PIN DIP
DPS8181G*	256K x 1	45	60	1	200	0.550 x 0.350 x 0.085	28-PAD LCC
DPS8186*	64K x 4	55	60	5	200	1.400 x 0.600 x 0.200	28-PIN DIP
DPS8186G*	64K x 4	55	60	5	200	0.550 x 0.450 x 0.850	32-PAD LCC
DPS92256	32K x 8	85	40	1	10	1.400 x 0.600 x 0.200	28-PIN DIP
DPS92256G	32K x 8	85	40	1	10	0.550 x 0.450 x 0.085	32-PAD LCC
DPS921024*	128K x 8	100	-	-	-	1.600 x 0.600 x 0.200	32-PIN DIP
DPS921024G*	128K x 8	100	-	-	-	-	-

Dense-Pac

DRAM MONOLITHICS - DIP/LCC

Part Number	Organization	Speed min. (ns)	Typical DC Current I_{CC1} (mA)	Typical DC Current I_{SB1} (mA)	Dimensions (inches)	Package
DPD91256*	256K x 1	100	60	1	0.800 x 0.300 x 0.200	16-PIN DIP
DPD91256G*	256K x 1	100	60	1	-	16-PAD LCC
DPD91644*	64K x 4	100	60	1	0.900 x 0.300 x 0.200	18-PIN DIP
DPD91644G	64K x 4	100	60	1	0.435 x 0.290 x 0.080	18-PAD LCC
DPD9001*	1MB x 1	100	60	1	0.900 x 0.300 x 0.200	18-PIN DIP
DPD9001G*	1MB x 1	100	60	1	0.435 x 0.290 x 0.080	18-PAD LCC
DPD92654*	256K x 4	100	60	1	0.900 x 0.300 x 0.200	18-PIN DIP
DPD92654G*	256K x 4	100	60	1	0.435 x 0.290 x 0.080	18-PAD LCC

EPROM MONOLITHICS - DIP/LCC

Part Number	Organization	Speed min. (ns)	Typical DC Current I_{CC1} (mA)	Typical DC Current I_{SB1} (mA)	Dimensions (inches)	Package
DPV27C256*	32K x 8	120	60	1	1.400 x 0.600 x 0.200	28-PIN DIP
DPV27C256G*	32K x 8	120	60	1	0.550 x 0.450 x 0.130	32-PAD LCC
DPV27C512*	64K x 8	120	60	1	1.400 x 0.600 x 0.200	28-PIN DIP
DPV27C512G*	64K x 8	120	60	1	0.550 x 0.450 x 0.130	32-PAD LCC
DPV27C101	128K x 8	170	60	1	1.400 x 0.600 x 0.200	32-PIN DIP
DPV27C101G	128K x 8	170	60	1	0.550 x 0.450 x 0.130	32-PAD LCC
DPV27C1024*	64K x 16	120	60	1	2.000 x 0.600 x 0.200	40-PIN DIP
DPV27C1024G*	64K x 16	120	60	1	0.650 x 0.650 x 0.130	44-PAD LCC

* Monolithic devices packaged upon request.

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16Kx1 SRAM BASED MODULES

Part Number	Organization	Speed min. (ns)	Typical DC Current			Dimensions (inches)	Package
			I_{CC1} (mA)	I_{SB1} (mA)	I_{CCDR} (µA)		
DPS8132*	32K x 1	20	55	0.2	2	1.100 x 0.300 x 0.150	22-PIN DIP
DPS81C64*	64K x 1	20	85	0.4	4	2.600 x 0.480 x 0.185	26-PIN SIP
DPS166167	256K x 1	20	65	0.16	16	1.980 x 0.900 x 0.295	40-PIN DIP
DPS166167	128K x 2	20	290	0.16	16	1.980 x 0.900 x 0.295	40-PIN DIP
DPS7M464	16K x 4	20	160	0.04	4	1.100 x 0.400 x 0.340	22-PIN DIP
DPS8M464	16K x 4	20	160	0.04	4	1.100 x 0.400 x 0.340	22-PIN DIP
DPS16X4	16K x 4	20	160	0.04	4	2.800 x 0.440 x 0.120	28-PIN SIP
DPS257	64K x 4	20	340	0.16	16	1.980 x 0.900 x 0.295	40-PIN DIP
DPS16X5	16K x 5	20	200	0.05	5	2.800 x 0.400 x 0.200	28-PIN SIP
DPS257	32K x 8	20	440	0.16	16	1.980 x 0.900 x 0.295	40-PIN DIP
DPS129	16K x 8	20	320	0.08	8	3.600 x 0.450 x 0.200	36-PIN SIP
DPS288	32K x 9	20	495	0.18	18	2.500 x 0.900 x 0.220	50-PIN DIP
DPS257	16K x 16	20	640	0.16	16	1.980 x 0.900 x 0.295	40-PIN DIP
DPS288	16K x 18	20	720	1.0	18	2.500 x 0.900 x 0.220	50-PIN DIP

4Kx4 SRAM BASED MODULES

Part Number	Organization	Speed min. (ns)	Typical DC Current			Dimensions (inches)	Package
			I_{CC1} (mA)	I_{SB1} (mA)	I_{CCDR} (µA)		
DPS84H08	8K x 4	25	65	0.4	30	1.100 x 0.300 x 0.145	22-PIN DIP
DPS88H04	4K x 8	25	100	0.4	30	1.200 x 0.300 x 0.145	24-PIN DIP
DPS88H08	8K x 8	25	130	1.2	60	1.400 x 0.600 x 0.280	28-PIN DIP
DPS88H16	16K x 8	25	190	2.4	120	1.400 x 0.600 x 0.280	28-PIN DIP
DPS4X16	4K x 16	25	200	1.2	60	1.850 x 0.350 x 0.350	36-PIN ZIP
DPS4H16*	4K x 16	25	200	1.2	60	2.000 x 0.300 x 0.180	36-PIN SIP
DPS266*	16K x 16	25	200	3.2	240	2.100 x 0.900 x 0.240	40-PIN DIP
DPS4X32*	4K x 32	25	400	2.4	120	2.800 x 0.400 x 0.240	56-PIN ZIP

64Kx1 SRAM BASED MODULES

Part Number	Organization	Speed min. (ns)	Typical DC Current			Dimensions (inches)	Package
			I_{CC1} (mA)	I_{SB1} (mA)	I_{CCDR} (µA)		
DPS8256	256K x 1	15	125	0.4	20	2.800 x 0.125 x 0.435	30-PIN SIP
DPS5122*	1MB x 1	15	425	1.6	80	2.100 x 0.900 x 0.240	42-PIN DIP
DPS5122*	512K x 2	15	450	1.6	80	2.100 x 0.900 x 0.240	42-PIN DIP
DPS86M44*	64K x 4	15	200	0.4	20	1.200 x 0.400 x 0.240	24-PIN DIP
DPS8644	64K x 4	15	200	0.4	20	3.000 x 0.435 x 0.125	30-PIN SIP
DPS8645	64K x 4	15	200	0.4	20	2.800 x 0.425 x 0.125	28-PIN SIP
DPS1024	256K x 4	15	500	1.6	80	2.150 x 0.900 x 0.240	42-PIN DIP
DPS1026	256K x 4	15	500	1.6	80	2.150 x 0.900 x 0.240	40-PIN DIP
DPS1027	256K x 4	15	500	1.6	80	2.150 x 0.900 x 0.240	40-PIN DIP
DPS320	64K x 5	15	250	0.5	25	4.000 x 0.480 x 0.185	40-PIN SIP
DPS384	64K x 6	15	300	0.6	30	4.000 x 0.480 x 0.185	40-PIN SIP
DPS6408	64K x 8	15	400	0.8	40	2.150 x 0.900 x 0.240	40-PIN DIP
DPS8524*	64K x 8	15	400	0.8	40	3.150 x 0.900 x 0.240	30-PIN SIP
DPS8589*	64K x 9	15	450	0.9	45	3.400 x 0.400 x 0.240	32-PIN SIP
DPS1152	128K x 9	15	675	1.8	90	2.500 x 0.900 x 0.240	50-PIN DIP
DPS1024	128K x 8	15	600	1.6	80	2.100 x 0.900 x 0.240	42-PIN DIP
DPS1025	128K x 8	15	600	1.6	80	2.100 x 0.900 x 0.240	40-PIN DIP
DPS1026	128K x 8	15	600	1.6	80	2.100 x 0.900 x 0.240	40-PIN DIP
DPS1027	128K x 8	15	600	1.6	80	2.100 x 0.900 x 0.240	40-PIN DIP
DPS6410*	64K x 10	15	500	1.0	50	1.800 x 0.900 x 0.240	36-PIN DIP
DPS6412*	64K x 12	15	600	1.2	60	1.800 X 0.900 X 0.240	36-PIN DIP
DPS1024	64K x 16	15	800	1.6	80	2.100 x 0.900 x 0.240	42-PIN DIP
DPS1025	64K x 16	15	800	1.6	80	2.100 x 0.900 x 0.240	40-PIN DIP
DPS1026	64K x 16	15	800	1.6	80	2.100 x 0.900 x 0.240	40-PIN DIP
DPS1027	64K x 16	15	800	1.6	80	2.100 x 0.900 x 0.240	40-PIN DIP
DPS1152	64K x 18	15	900	1.8	90	2.500 x 0.900 x 0.220	50-PIN DIP

* Substrate designed upon request.
Dense-Pac offers lower power modules at slower speeds.

2Kx8 SRAM BASED MODULES

Part Number	Organization	Speed min. (ns)	Typical DC Current I_{CC1} (mA)	Typical DC Current I_{SB1} (mA)	Typical DC Current I_{CCDR} (µA)	Dimensions (inches)	Package
DPS8808*	8K x 8	35	65	0.01	48	1.400 x 0.600 x 0.240	28-PIN DIP
DPS2X16*	2K x 16	35	40	0.01	16	2.000 x 0.600 x 0.150	40-PIN DIP
DPS2X32*	2K x 32	35	140	0.11	16	2.000 x 0.600 x 0.150	56-PIN DIP

8Kx8 SRAM BASED MODULES

Part Number	Organization	Speed min. (ns)	Typical DC Current I_{CC1} (mA)	Typical DC Current I_{SB1} (mA)	Typical DC Current I_{CCDR} (µA)	Dimensions (inches)	Package
DPS41129	16K x 8	45	40	0.05	20	1.400 x 0.600 x 0.240	28-PIN DIP
DPS41193	24K x 8	45	45	0.15	30	1.400 x 0.600 x 0.240	28-PIN DIP
DPS41257	32K x 8	45	50	2.00	40	1.400 x 0.600 x 0.240	28-PIN DIP
DPS1124	128K x 8	70	180	1.60	64	2.800 x 1.500 x 0.240	56-PIN DIP
DPS1224	128K x 8	70	180	1.60	64	2.400 x 1.400 x 0.240	48-PIN DIP
DPS91288	128K x 8	100	45	1.00	16	3.400 x 1.200 x 0.240	68-PIN DIP
DPS8M628	8K x 16	45	65	0.10	20	2.000 x 0.600 x 0.240	40-PIN DIP
DPS8M656	16K x 16	45	75	0.20	40	2.000 x 0.600 x 0.130	40-PIN DIP
DPS1124	64K x 16	70	210	1.60	64	2.800 x 1.500 x 0.240	56-PIN DIP
DPS91288	64K x 16	100	75	1.00	120	3.400 x 1.500 x 0.130	68-PIN DIP

16Kx4 SRAM BASED MODULES

Part Number	Organization	Speed min. (ns)	Typical DC Current I_{CC1} (mA)	Typical DC Current I_{SB1} (mA)	Typical DC Current I_{CCDR} (µA)	Dimensions (inches)	Package
DPS32H8*	32K x 8	25	150	2.0	80	1.400 x 0.600 x 0.240	28-PIN DIP
DPS16X17	32K x 8	25	150	4.0	64	1.800 x 0.300 x 0.500	36-PIN DSIP
DPS16X16	16K x 16	25	240	4.0	64	1.900 x 0.300 x 0.360	38-PIN DSIP
DPS16X17	16K x 16	25	240	4.0	64	1.800 x 0.300 x 0.500	36-PIN DSIP
DPS3216*	32K x 16	25	300	10.0	128	2.400 x 0.600 x 0.240	44-PIN DIP

64Kx4 SRAM BASED MODULES

Part Number	Organization	Speed min. (ns)	Typical DC Current I_{CC1} (mA)	Typical DC Current I_{SB1} (mA)	Typical DC Current I_{CCDR} (µA)	Dimensions (inches)	Package
DPS5124	512K x 4	55	50	10	6	2.695 x 0.600 x 0.270	54-PIN DIP
DPS5124	256K x 8	55	100	10	6	2.695 x 0.600 x 0.270	54-PIN DIP
DPS6432	256K x 8	55	100	10	6	2.995 x 0.600 x 0.270	60-PIN DIP
DPS6432	128K x 16	55	200	10	6	2.995 x 0.600 x 0.270	60-PIN DIP
DPS6432	64K x 32	55	400	10	6	2.995 x 0.600 x 0.270	60-PIN DIP
DPS12832*	128K x 32	55	500	10	6	3.200 x 1.200 x 0.270	64-PIN DIP

32Kx8 SRAM BASED MODULES

Part Number	Organization	Speed min. (ns)	Typical DC Current I_{CC1} (mA)	Typical DC Current I_{SB1} (mA)	Typical DC Current I_{CCDR} (µA)	Dimensions (inches)	Package
DPS4648	64K x 8	85	22	0.2	25	1.600 x 0.600 x 0.295	32-PIN DIP
DPS4968	96K x 8	85	24	0.3	35	1.600 x 0.600 x 0.295	32-PIN DIP
DPS41288	128K x 8	85	26	1.6	50	1.600 x 0.600 x 0.295	32-PIN DIP
DPS42568*	256K x 8	85	40	1.6	40	2.700 x 0.600 x 0.240	64-PIN DSIP
DPS6433	256K x 8	100	25	5.0	40	3.000 x 0.600 x 0.270	60-PIN DIP
DPS256P8	256K x 8	70	80	4.0	20	3.500 x 0.550 x 0.258	35-PIN SIP
DPS256Q8	256K x 8	70	25	5.0	20	1.100 x 1.400 x 0.260	42-PIN QIP
DPS96122	512K x 8	85	40	5.0	90	3.400 x 1.200 x 0.310	68-PIN DIP
DPS45128	512K x 8	100	40	5.0	75	2.400 x 1.400 x 0.240	48-PIN DIP
DPS8M612	32K x 16	85	64	0.2	25	2.000 x 0.600 x 0.240	40-PIN DIP
DPS8M624	64K x 16	85	68	0.4	50	2.000 x 0.600 x 0.240	40-PIN DIP
DPS42568*	128K x 16	85	60	1.6	75	2.700 x 0.600 x 0.240	64-PIN DSIP
DPS6433	128K x 16	100	60	5.0	40	3.000 x 0.600 x 0.270	60-PIN DIP
DPS45129*	256K x 16	100	80	5.0	120	2.800 x 1.400 x 0.240	48-PIN DIP
DPS96122	256K x 16	85	52	5.0	90	3.400 x 1.200 x 0.310	68-PIN DIP
DPS6433	64K x 32	100	80	5.0	40	3.000 x 0.600 x 0.270	60-PIN DIP

* Substrate designed upon request.
Dense-Pac offers lower power modules at slower speeds.

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256Kx1 SRAM BASED MODULES

Part Number	Organization	Speed min. (ns)	Typical DC Current I_{CC1} (mA)	Typical DC Current I_{SB1} (mA)	Typical DC Current I_{CCDR} (µA)	Dimensions (inches)	Package
DPS10241*	1024K x 1	35	35	0.4	16	3.000 x 0.400 x 0.200	30-PIN SIP
DPS20482*	4MB x 1	35	45	1.6	64	2.200 x 0.900 x 0.240	44-PIN DIP
DPS20482*	2MB x 2	35	75	1.6	64	2.200 x 0.900 x 0.240	44-PIN DIP
DPS2564*	256K x 4	35	120	0.4	16	3.000 x 0.400 x 0.200	30-PIN SIP
DPS25616*	1MB x 4	35	135	1.6	64	2.200 x 0.900 x 0.240	44-PIN DIP
DPS2568*	256K x 8	35	240	0.8	32	4.400 x 0.400 x 0.240	44-PIN DIP
DPS25616*	512K x 8	35	240	1.6	64	2.200 x 0.900 x 0.240	44-PIN DIP
DPS2569*	256K x 9	35	270	0.9	36	2.200 x 0.400 x 0.240	44-PIN DIP
DPS25618*	512K x 9	35	270	1.8	64	2.500 x 0.900 x 0.240	54-PIN DIP
DPS25616*	256K x 16	35	480	1.6	64	2.200 x 0.900 x 0.240	44-PIN DIP
DPS25618*	256K x 18	35	540	1.8	64	2.500 x 0.900 x 0.240	54-PIN DIP

128Kx8 SRAM BASED MODULES

Part Number	Organization	Speed min. (ns)	Typical DC Current I_{CC1} (mA)	Typical DC Current I_{SB1} (mA)	Typical DC Current I_{CCDR} (µA)	Dimensions (inches)	Package
DPS9512P8*	512K x 8	70	300	15	300	TBD	TBD - DIP
DPS1024P8*	1MB x 8	70	600	30	600	3.800 x 1.600 x 0.300	38-PIN SIP
DPS96488*	2MB x 8	70	1200	60	1200	3.400 x 1.200 x 0.310	68-PIN DIP
DPS512P8*	512K x 8	70	300	15	300	3.800 x 1.600 x 0.300	38-PIN DIP
DPS96488*	1MB x 16	70	1200	60	1200	3.400 x 1.200 x 0.310	68-PIN DIP

NOVRAMS

512x8 NOVRAM BASED MODULES

Part Number	Organization	Speed min. (ns)	Typical DC Current I_{CC1} (mA)	Typical DC Current I_{SB1} (mA)	Dimensions (inches)	Package
DPN18	1K x 8	250	310	220	1.400 x 0.600 x 0.150	28-PIN DIP
DPN28	2K x 8	250	530	440	1.400 x 0.600 x 0.240	28-PIN DIP
DPN88	8K x 8	250	970	880	2.400 x 1.400 x 0.240	48-PIN DIP

DRAMS

64Kx1 DRAM BASED MODULES

Part Number	Organization	Speed min. (ns)	Typical DC Current I_{CC1} (mA)	Typical DC Current I_{SB1} (mA)	Dimensions (inches)	Package
DPD4256	256K x 1	100	36	2	2.200 x 0.300 x 0.140	22-PIN SIP
DPD4464	64K x 4	100	144	8	2.200 x 0.300 x 0.140	22-PIN SIP
DPD4848	64K x 8	100	288	16	3.000 x 0.625 x 0.150	30-PIN SIP
DPD4849	64K x 9	100	324	18	3.000 x 0.625 x 0.150	30-PIN SIP

256Kx1 DRAM BASED MODULES

Part Number	Organization	Speed min. (ns)	Typical DC Current I_{CC1} (mA)	Typical DC Current I_{SB1} (mA)	Dimensions (inches)	Package
DPD411M*	1MB x 1	100	42	8	2.400 x 0.300 x 0.140	22-PIN SIP
DPD5124*	512K x 4	100	144	16	2.400 x 0.400 x 0.240	24-PIN SIP
DPD44256*	256K x 4	100	144	8	2.400 x 0.300 x 0.140	22-PIN SIP
DPD45256*	256K x 5	100	180	10	2.600 x 0.300 x 0.140	26-PIN SIP
DPD42568*	256K x 8	100	288	16	3.000 x 0.625 x 0.150	30-PIN SIP
DPD45269*	256K x 9	100	324	18	3.000 x 0.625 x 0.150	30-PIN SIP
DPD42568LL*	256K x 8	100	288	16	3.000 x 0.625 x 0.150	30-PIN SIP
DPD42569LL*	256K x 9	100	324	18	3.000 x 0.625 x 0.150	30-PIN SIP
DPD42568LP*	256K x 8	100	288	16	3.000 x 0.425 x 0.150	30-PIN SIP
DPD42569LP*	256K x 9	100	324	18	3.000 x 0.425 x 0.150	30-PIN SIP

* Substrate designed upon request.
Dense-Pac offers lower power modules at slower speeds.

1MBx1 DRAM BASED MODULES

Part Number	Organization	Speed min. (ns)	Typical DC Current I_{CC1} (mA)	Typical DC Current I_{SB1} (mA)	Dimensions (inches)	Package
DPD414M*	4MB x 1	100	50	8	1.500 x 0.500 x 0.240	30-PIN SIP
DPD441M*	1MB x 4	100	200	8	1.500 x 0.500 x 0.240	30-PIN SIP
DPD4M8*	4MB x 8	100	400	64	3.000 x 1.200 x 0.240	60-PIN DIP
DPD1M8*	1MB x 8	100	400	16	3.200 x 0.725 x 0.240	30-PIN SIP
DPD1M9*	1MB x 9	100	415	20	3.200 x 0.725 x 0.240	30-PIN SIP

256Kx4 DRAM BASED MODULES

Part Number	Organization	Speed min. (ns)	Typical DC Current I_{CC1} (mA)	Typical DC Current I_{SB1} (mA)	Dimensions (inches)	Package
DPD51240*	512K x 40	100	500	40	3.000 x 0.700 x 0.275	60-PIN DIP

VIDEO RAMS

64Kx1 VIDEO RAM BASED MODULES

Part Number	Organization	Speed min. (ns)	Typical DC Current I_{CC1} (mA)	Typical DC Current I_{SB1} (mA)	Dimensions (inches)	Package
DPO10V24	64K x 16	100	640	160	2.600 x 0.900 x 0.240	52-PIN DIP

64Kx4 VIDEO RAM BASED MODULES

Part Number	Organization	Speed min. (ns)	Typical DC Current I_{CC1} (mA)	Typical DC Current I_{SB1} (mA)	Dimensions (inches)	Package
DPO2564*	256K x 4	100	80	6	2.600 x 0.900 x 0.240	52-PIN SIP
DPO5124*	512K x 4	100	100	24	3.400 x 0.900 x 0.240	76-PIN SIP
DPO3848*	384K x 8	100	100	24	2.900 x 0.500 x 0.800	56-PIN DIP

EEPROMS

8Kx8 EEPROM BASED MODULES

Part Number	Organization	Speed min. (ns)	Typical DC Current I_{CC1} (mA)	Typical DC Current I_{SB1} (mA)	Dimensions (inches)	Package
DPE41129	16K x 8	60	48	6	1.400 x 0.600 x 0.240	28-PIN DIP
DPE40128	16K x 8	60	48	6	1.400 x 0.600 x 0.240	28-PIN DIP
DPE41193	24K x 8	60	51	9	1.400 x 0.600 x 0.240	28-PIN DIP
DPE40192	24K x 8	60	51	9	1.400 x 0.600 x 0.240	28-PIN DIP
DPE40256	32K x 8	60	54	12	1.400 x 0.600 x 0.240	28-PIN DIP
DPE41257	32K x 8	60	54	12	1.400 x 0.600 x 0.240	28-PIN DIP
DPE1224	128K x 8	85	90	48	2.400 x 1.400 x 0.240	48-PIN DIP
DPE1124	128K x 8	85	90	48	2.800 x 1.400 x 0.240	56-PIN DIP
DPE8M628	8K x 16	60	48	6	2.000 x 0.600 x 0.240	40-PIN DIP
DPE8M656	16K x 16	60	96	12	2.000 x 0.600 x 0.240	40-PIN DIP

* Substrate designed upon request.
Dense-Pac offers lower power modules at slower speeds.

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32Kx8 EEPROM BASED MODULES

Part Number	Organization	Speed min. (ns)	Typical DC Current I_{CC1} (mA)	Typical DC Current I_{SB1} (mA)	Dimensions (inches)	Package
DPE4648	64K x 8	85	48	6	1.600 x 0.600 x 0.295	32-PIN DIP
DPE4968	96K x 8	85	51	9	1.600 x 0.600 x 0.295	32-PIN DIP
DPE41288	128K x 8	85	54	12	1.600 x 0.600 x 0.295	32-PIN DIP
DPE51288	128K x 8	85	54	12	1.600 x 0.600 x 0.295	32-PIN DIP
DPE6433	256K x 8	100	110	42	3.000 x 0.600 x 0.270	60-PIN DIP
DPE42568*	256K x 8	85	40	2	3.200 x 0.600 x 0.240	64-PIN DSIP
DPE45128	512K x 8	100	90	48	2.400 x 1.400 x 0.240	48-PIN DIP
DPE8M612	32K x 16	85	55	6	2.000 x 0.600 x 0.275	40-PIN DIP
DPE8M624	64K x 16	85	110	12	2.000 x 0.600 x 0.275	40-PIN DIP
DPE42568*	128K x 16	85	60	2	3.200 x 0.600 x 0.240	64-PIN DSIP
DPE6433	128K x 16	100	170	42	3.000 x 0.600 x 0.270	60-PIN DIP
DPE45129*	256K x 16	120	135	48	2.800 x 1.400 x 0.240	48-PIN DIP
DPE6433	64K x 32	100	290	42	3.000 x 0.600 x 0.270	60-PIN DIP

EPROMS

8Kx8 EPROM BASED MODULES

Part Number	Organization	Speed min. (ns)	Typical DC Current I_{CC1} (mA)	Typical DC Current I_{SB1} (mA)	Dimensions (inches)	Package
DPV8X16*	8K x 16	150	60	2	2.000 x 0.600 x 0.240	40-PIN DIP
DPV8X24*	8K x 24	150	90	3	2.400 x 0.600 x 0.240	48-PIN DIP
DPV8X32*	8K x 32	150	120	4	2.800 x 0.600 x 0.240	56-PIN DIP

32Kx8 EPROM BASED MODULES

Part Number	Organization	Speed min. (ns)	Typical DC Current I_{CC1} (mA)	Typical DC Current I_{SB1} (mA)	Dimensions (inches)	Package
DPV32X16*	32K x 16	150	60	2	2.000 x 0.600 x 0.240	40-PIN DIP
DPV128X16	128K x 16	150	70	8	2.800 x 1.500 x 0.240	56-PIN DIP
DPV32X24*	32K x 24	150	90	3	2.400 x 0.600 x 0.240	48-PIN DIP
DPV32X32*	32K x 32	150	120	4	2.800 x 0.600 x 0.240	56-PIN DIP

64Kx8 EPROM BASED MODULES

Part Number	Organization	Speed min. (ns)	Typical DC Current I_{CC1} (mA)	Typical DC Current I_{SB1} (mA)	Dimensions (inches)	Package
DPV512X8*	512K x 8	150	40	8	2.800 x 1.500 x 0.240	56-PIN DIP
DPV64X24*	64K x 24	150	90	3	2.400 x 0.600 x 0.240	48-PIN DIP
DPV64X32*	64K x 32	150	120	4	2.800 x 0.600 x 0.240	56-PIN DIP

128Kx8 EPROM BASED MODULES

Part Number	Organization	Speed min. (ns)	Typical DC Current I_{CC1} (mA)	Typical DC Current I_{SB1} (mA)	Dimensions (inches)	Package
DPV1048X8*	1048K x 8	150	45	8	2.200 x 1.300 x 0.240	44-PIN DIP
DPV128X16B*	128K x 16	150	60	2	2.400 x 0.600 x 0.240	48-PIN DIP
DPV512X16B*	512K x 16	150	70	8	2.600 x 1.500 x 0.240	48-PIN DIP
DPV128X24B*	128K x 24	150	90	3	2.800 x 0.600 x 0.240	56-PIN DIP
DPV128X32*	128K x 32	150	120	4	3.200 x 0.600 x 0.240	64-PIN DIP
DPV256X32*	256K x 32	150	140	8	3.200 x 1.500 x 0.240	64-PIN DIP

* Substrate designed upon request.
Dense-Pac offers lower power modules at slower speeds.

VERSAPAC SRAM BASED MODULES

Part Number	Organization	Speed min. (ns)	Typical DC Current			Dimensions (inches)	Package
			I_{CC1} (mA)	I_{SB1} (mA)	I_{CCDR} (µA)		
DPS832V	32K x 8	35	82	1.0	60	1.090 x 1.090 x 0.300	66-PIN PGA
DPS3232V	128K x 8	35	92	2.0	120	1.090 x 1.090 x 0.300	66-PIN PGA
DPS832V	16K x 16	35	160	1.0	60	1.090 x 1.090 x 0.300	66-PIN PGA
DPS3232V	64K x 16	35	182	2.0	120	1.090 x 1.090 x 0.300	66-PIN PGA
DPS832V	8K x 32	35	320	1.0	60	1.090 x 1.090 x 0.300	66-PIN PGA
DPS3232V	32K x 32	35	360	2.0	120	1.090 x 1.090 x 0.300	66-PIN PGA

VERSAPAC EEPROM BASED MODULES

Part Number	Organization	Speed [2] min. (ns)	Typical DC Current		Dimensions (inches)	Package
			I_{CC1} (mA)	I_{SB1} (mA)		
DPE832V	32K x 8	55	75	12	1.090 x 1.090 x 0.300	66-PIN PGA
DPE3232V	128K x 8	70	80	20	1.090 x 1.090 x 0.300	66-PIN PGA
DPE832V	16K x 16	55	136	12	1.090 x 1.090 x 0.300	66-PIN PGA
DPE3232V	64K x 16	70	140	20	1.090 x 1.090 x 0.300	66-PIN PGA
DPE832V	8K x 32	55	260	12	1.090 x 1.090 x 0.300	66-PIN PGA
DPE3232V	32K x 32	70	260	20	1.090 x 1.090 x 0.300	66-PIN PGA

VERSAPAC EPROM BASED MODULES

Part Number	Organization	Speed [1] min. (ns)	Typical DC Current		Dimensions (inches)	Package
			I_{CC1} (mA)	I_{SB1} (mA)		
DPV3232V	128K x 8	70	75	60	1.090 x 1.090 x 0.330	66-PIN PGA
DPV6432V	256K x 8	70	46	8	1.090 x 1.090 x 0.330	66-PIN PGA
DPV12832V	512K x 8	200	33	4	1.090 x 1.090 x 0.330	66-PIN PGA
DPV3232V	64K x 16	70	90	60	1.090 x 1.090 x 0.330	66-PIN PGA
DPV6432V	128K x 16	200	84	8	1.090 x 1.090 x 0.330	66-PIN PGA
DPV12832V	256K x 16	70	62	4	1.090 x 1.090 x 0.330	66-PIN PGA
DPV3232V	32K x 32	70	120	60	1.090 x 1.090 x 0.330	66-PIN PGA
DPV6432V	64K x 32	70	160	8	1.090 x 1.090 x 0.330	66-PIN PGA
DPV12832V	128K x 32	200	120	4	1.090 x 1.090 x 0.330	66-PIN PGA

NOTE:
1. Read Access Speeds.

Dense-Pac offers lower power modules at slower speeds.

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DUAL-PORTED RAMS

DUAL-PORTED RAM MODULES - Advanced Information

Part Number	Organization	Speed min. (ns)	Typical DC Current			Dimensions (inches)	Package
			I_{CC1} (mA)	I_{SB1} (mA)	I_{CCDR} (µA)		
DPP2X8*	2K x 8	35	TBD	TBD	TBD	TBD	TBD
DPP4X8*	4K x 8	35	TBD	TBD	TBD	TBD	TBD
DPP8X8*	4K x 8	35	TBD	TBD	TBD	TBD	TBD
DPP16X8*	16K x 8	35	TBD	TBD	TBD	TBD	TBD
DPP32X8*	32K x 8	35	TBD	TBD	TBD	TBD	TBD
DPP128X8*	128K x 8	35	TBD	TBD	TBD	TBD	TBD
DPP2X16*	2K x 16	35	TBD	TBD	TBD	TBD	TBD
DPP4X16*	4K x 16	35	TBD	TBD	TBD	TBD	TBD
DPP8X16*	8K x 16	35	TBD	TBD	TBD	TBD	TBD
DPP16X16*	16K x 16	35	TBD	TBD	TBD	TBD	TBD
DPP32X16*	32K x 16	35	TBD	TBD	TBD	TBD	TBD
DPP64X16*	64K x 16	35	TBD	TBD	TBD	TBD	TBD
DPP2X32*	2K x 32	35	TBD	TBD	TBD	TBD	TBD
DPP4X32*	4K x 32	35	TBD	TBD	TBD	TBD	TBD
DPP8X32*	8K x 32	35	TBD	TBD	TBD	TBD	TBD
DPP16X32*	16K x 32	35	TBD	TBD	TBD	TBD	TBD
DPP32X32*	32K x 32	35	TBD	TBD	TBD	TBD	TBD
DPP64X32*	64K x 32	35	TBD	TBD	TBD	TBD	TBD

FLASH EEPROMS

FLASH EEPROM MODULES - Advanced Information

Part Number	Organization	Speed min. (ns)	Typical DC Current		Dimensions (inches)	Package
			I_{CC1} (mA)	I_{SB1} (mA)		
DPZ8M628*	8K x 16	170	TBD	TBD	TBD	40-PIN DIP
DPZ8M656*	16K x 16	170	TBD	TBD	TBD	40-PIN DIP
DPZ8M612*	32K x 16	170	TBD	TBD	TBD	40-PIN DIP
DPZ8M624*	64K x 16	170	TBD	TBD	TBD	40-PIN DIP
DPZ48C512*	64K x 8	170	TBD	TBD	TBD	32-PIN DIP
DPZ48C1024*	128K x 8	170	TBD	TBD	TBD	32-PIN DIP
DPZ48C2048*	256K x 8	170	TBD	TBD	TBD	32-PIN DIP
DPZ48C4096*	512K x 8	170	TBD	TBD	TBD	32-PIN DIP
DPZ20488*	2048K x 8	170	TBD	TBD	TBD	48-PIN DIP

FIFO MODULES

FIFO MODULES - Advanced Information

Part Number	Organization	Speed min. (ns)	Typical DC Current		Dimensions (inches)	Package
			I_{CC1} (mA)	I_{SB1} (mA)		
DPF2X9*	2K x 9	35	TBD	TBD	TBD	TBD
DPF4X9*	4K x 9	35	TBD	TBD	TBD	TBD
DPF8X9*	4K x 9	35	TBD	TBD	TBD	TBD
DPF16X9*	16K x 9	35	TBD	TBD	TBD	TBD
DPF32X9*	32K x 9	35	TBD	TBD	TBD	TBD
DPF2X18*	2K x 18	35	TBD	TBD	TBD	TBD
DPF4X18*	4K x 18	35	TBD	TBD	TBD	TBD
DPF8X18*	8K x 18	35	TBD	TBD	TBD	TBD
DPF16X18*	16K x 18	35	TBD	TBD	TBD	TBD
DPF32X18*	32K x 18	35	TBD	TBD	TBD	TBD
DPF64X18*	64K x 18	35	TBD	TBD	TBD	TBD
DPF2X36*	2K x 36	35	TBD	TBD	TBD	TBD
DPF4X36*	4K x 36	35	TBD	TBD	TBD	TBD
DPF8X36*	8K x 36	35	TBD	TBD	TBD	TBD

* Substrate designed upon request.
Dense-Pac offers lower power modules at slower speeds.

STANDARD PART NUMBERING SYSTEM

DP	S	92256	G	-	85	M
PREFIX		FAMILY			SPEED	
DEVICE TYPE		FAMILY SUFFIX			TEMP./SCREEN	

DEVICE TYPE
- S - SRAM
- D - DRAM
- E - EEPROM
- V - EPROM
- N - NOVRAM
- O - VIDEORAM
- P - DUAL-PORTED RAMS
- Z - FLASH EEPROMS
- F - FIFO

FAMILY SUFFIX
- G - LCC PACKAGE
- * - VENDOR SPECIFICATION
- V - VERSAPAC
- P - PLASTIC MODULE (may appear in family number)

TEMP./SCREEN
- C - 0°C to +70°C
- I - -40°C to +85°C, plus Burn-In
- M - -55°C to +125°C, MIL Processed
- B - -55°C to +125°C, MIL Processed to Methods 5004 and 5005

MIXED-TECHNOLOGY VERSAPAC PART NUMBERING SYSTEM

		M0		M1		M2		M3			
DP	0	0	0	0	4	1	7	1	V	-	M
PREFIX											
LCC CODE									TEMP./SCREEN		
SPEED CODE									VERSAPAC SUFFIX		

LCC CODE
- 0 - 8Kx8 SRAM
- 1 - 32Kx8 SRAM
- 2 - 128Kx8 SRAM
- 3 - 8Kx8 EEPROM
- 4 - 32Kx8 EEPROM
- 5 - 128Kx8 EEPROM
- 6 - 8Kx8 EPROM
- 7 - 32Kx8 EPROM
- 8 - 128Kx8 EPROM

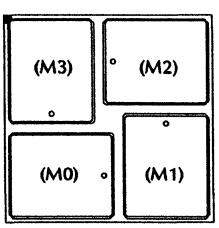
SPEED CODE:

	SRAM	EEPROM	UVPROM
0 -	150ns	300ns	300ns
1 -	120ns	250ns	250ns
2 -	100ns	200ns	200ns
3 -	85ns	150ns	170ns
4 -	70ns	120ns	150ns
5 -	55ns	90ns	120ns
6 -	45ns	70ns	90ns
7 -	35ns	55ns	70ns
8 -	25ns	45ns	55ns
9 -	20ns	35ns	45ns

TEMPERATURE/SCREEN
- C - 0°C to +70°C
- I - -40°C to +85°C, plus Burn-In
- M - -55°C to +125°C, MIL Processed
- B - -55°C to +125°C, MIL Processed to Methods 5004 and 5005

EXAMPLE:

1 32Kx8 SRAM @ 70ns in position M0.
1 8Kx8 EEPROM @ 250ns in positions M1.
1 32Kx8 EEPROM @ 250ns in position M2.
1 128Kx8 EPROM @ 300ns in position M3.



PART NUMBER WOULD BE:

DP	14	31	41	80	V-C
	M0	M1	M2	M3	TEMP.

STANDARD PART NUMBERING SYSTEM

This system is used for all of the products offered by Dense-Pac Microsystems, Inc. with the exception of mixed technology Versapac modules *(described below)*. Dense-Pac product part numbers always begin with the letters "DP" *(Dense-Pac)* followed by a letter indicating the device type or technology. The part number itself usually reflects the organization of the memory and is sometimes followed by a letter representing the manufacturer of the monolithic device used *(in the case of modules)* or the package type *(in the case of monolithics)*. The dash number at the end identifies the speed of the module followed by the letter representing the grade.

SEMICUSTOM - VERSAPAC PART NUMBERING SYSTEM

The Versapac module requires a new system for the products that mix SRAM, EEPROM, and EPROM on the same substrate. This new system allows customers to pick and choose module configuration and still maintain a standard manufacturer's part number as opposed to generating Source Control Drawings.

This Short Form Catalog is designed as an overview of products that are currently available as well as products that are potentially available. Please contact your sales representatives for further information about products contained herein. Specified parameters are subject to change without notice.

Dense-Pac

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Analog Signal Processing Integrated Circuits

Device	Pkg Pins	Max Cutoff or Center (KHz)	Max Ext. Clk (MHz)	Supply Voltage Range (V)	Dynamic Range (dB)	Description
▼ *General Purpose Filters (Switched Capacitor)*						
RM5604A	16	10	1.4	±5 to ±10	73	Triple 1/3 octave bandpass filter
RM5605A	16	10	1.1	±5 to ±10	73	Double 1/2 octave bandpass filter
RM5606A	16	10	1.1	±5 to ±10	73	Single 1 octave bandpass filter
RF5609A	8	25	2.5	±5 to ±10	70	7th order elliptical lowpass
RF6609A	8	25	2.5	±4 to ±6	80	CMOS 7th order elliptic lowpass
RF5611A	8	5	2.5	±5 to ±10	62	5th order Chebychev highpass
RF5612A	8	2.5	2.5	±5 to ±10	62	4th order Notch
RF5613A	8	19.5	2.5	±5 to ±10	60	7th order linear phase lowpass
RF5614A	8	18	1	±5 to ±10	70	6th order single 1/3 octave bandpass
RF5615A	8	18	1	±5 to ±10	70	6th order single 1/2 octave bandpass
RF5616A	8	18	1	±5 to ±10	70	6th order single 1 octave bandpass
RF5651A	24	10	3.58	±5 to ±10	70	C-message/1010 Hz notch/program weighting combo
▼ *Modem Filters (Switched Capacitor)*						
RM5630A	16	2.1/1.1	1	±5 to ±10	58 **	Bell 103 compatible, 300 baud, full duplex
RM5631A	16	1.8/1.1	1	±5 to ±10	66	CCITT V.21 compatible, 200/300 baud, full duplex
RM5635A	16	2.4/1.2	1536	±5 to ±10	50 **	CCITT V.22 Bis compatible, 2400 bps, full duplex
RM5636B	22	1.8	3.6864	±5 to ±10	72	Bell 201/CCITT V.26 compatible, 2400 bps filter combo
RM5637A	22	1.8	3.6864	±5 to ±10	70	Bell 208/CCITT V.27 compatible, 4800 bps filter combo
RM5638A	16	1.8	3.6864	±5	50 **	Bell 209/CCITT V.29 compatible, 9600 bps filter combo. Contains a receiver bandpass filter, a fixed compromise delay equalizer filter, and a transmit lowpass filter.
▼ Universal Filters (Switched Capacitor)						
RU5620A	18	20	1.25	±5 to ±10	80	2nd order filter, digitally programmable (f_o) and Q)
RU5621A	14	30	.75	±5 to ±10	70	Two 2nd order sections, resistor programmable
RU5622A	20	30	.75	±5 to ±10	75	Four 2nd order sections
▼ *Transversal Filters/Special Signal Processing*						
RT5601BB	22	5	10	8 to 22	60	Buried-channel windowed DFT processor
RT5602AA	16	125	4	14 to 16	60	64-stage lowpass transversal filter
RT5602AC	16	250	4	14 to 16	60	64-stage bandpass transversal filter
RT5602AG	16	500	4	14 to 16	60	Hanning-windowed sine chirp (64 stages)
RT5602AH	16	500	4	14 to 16	60	Hanning-windowed cosine chirp (64 stages)
▼ *Audio Delay Lines*						
RD5106A	8	167	1.0	+5 to 13	50*	256 sample audio delay with driver and S/H output. Delay from 512 µsec to 1 sec.
RD5107A	8	167	1.0	+5 to 13	50*	512 sample audio delay with driver and S/H output. Delay from 1.024 msec to 2 sec.
RD5108A	8	167	1.0	+5 to 13	50*	1024 sample audio delay with driver and S/H output. Delay from 2.048 msec to 4 sec.

** Appropriate filtering and clock rate can provide S/N ≥65 dB*
*** Worst-case test limits. Typical values on actual devices are 65 dB or better.*

The part numbers shown are not the complete part numbers needed for ordering. Many products are available in multiple package types and/or test specifications. Refer to a recent price list or contact your local EG&G Solid State Products Group sales office for details.

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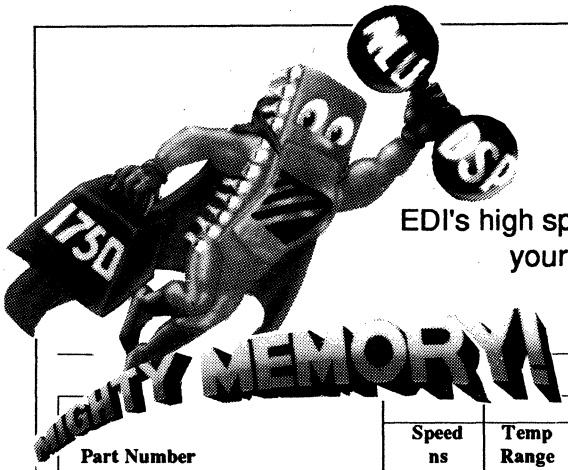

EDI
The future...today.

EDI's high speed 256K CMOS SRAMs are perfect partners for your advanced architecture design projects, including Military 1750, DSP, ALU, and other high performance 32 bit micro design applications.

256K Monolithic CMOS Static RAMs

Part Number	Speed ns	Temp Range	Max Current Consumption ICC1 mA	ICC3 mA	IDR µA	Package Type/Pins	Dimensions L x W x H (in)
256Kx1							
EDI81256C25LB	25	MIL	120	10	—	LCC/28	0.55 x 0.350 x 0.082
EDI81256C35LB	35	MIL	120	10	—	LCC/28	0.55 x 0.350 x 0.082
EDI81256C45LB	45	MIL	120	10	—	LCC/28	0.55 x 0.350 x 0.082
EDI81256C55LB	55	MIL	120	10	—	LCC/28	0.55 x 0.350 x 0.082
EDI81256C35QB	35	MIL	120	10	—	DIP/24	1.20 x 0.350 x 0.145
EDI81256C45QB	45	MIL	120	10	—	DIP/24	1.20 x 0.350 x 0.145
EDI81256C55QB	55	MIL	120	10	—	DIP/24	1.20 x 0.350 x 0.145
256Kx1, Low Power							
EDI81256P25LB	25	MIL	120	3	500	LCC/28	0.55 x 0.350 x 0.082
EDI81256P35LB	35	MIL	120	3	500	LCC/28	0.55 x 0.350 x 0.082
EDI81256P45LB	45	MIL	120	3	500	LCC/28	0.55 x 0.350 x 0.082
EDI81256P55LB	55	MIL	120	3	500	LCC/28	0.55 x 0.350 x 0.082
EDI81256P35QB	35	MIL	120	3	500	DIP/24	1.20 x 0.350 x 0.145
EDI81256P45QB	45	MIL	120	3	500	DIP/24	1.20 x 0.350 x 0.145
EDI81256P55QB	55	MIL	120	3	500	DIP/24	1.20 x 0.350 x 0.145
64Kx4							
EDI8464C35LB	35	MIL	120	10	—	LCC/28	0.55 x 0.350 x 0.082
EDI8464C45LB	45	MIL	120	10	—	LCC/28	0.55 x 0.350 x 0.082
EDI8464C55LB	55	MIL	120	10	—	LCC/28	0.55 x 0.350 x 0.082
EDI8465C25QB	25	MIL	120	10	—	DIP/24	1.20 x 0.350 x 0.145
EDI8465C35QB	35	MIL	120	10	—	DIP/24	1.20 x 0.350 x 0.145
EDI8465C45QB	45	MIL	120	10	—	DIP/24	1.20 x 0.350 x 0.145
EDI8465C55QB	55	MIL	120	10	—	DIP/24	1.20 x 0.350 x 0.145
EDI8465C25LB	25	MIL	120	10	—	LCC/28	0.55 x 0.350 x 0.082
EDI8465C35LB	35	MIL	120	10	—	LCC/28	0.55 x 0.350 x 0.082
EDI8465C45LB	45	MIL	120	10	—	LCC/28	0.55 x 0.350 x 0.082
EDI8465C55LB	55	MIL	120	10	—	LCC/28	0.55 x 0.350 x 0.082
64Kx4, Low Power							
EDI8464P35LB	35	MIL	120	3	500	LCC/28	0.55 x 0.350 x 0.082
EDI8464P45LB	45	MIL	120	3	500	LCC/28	0.55 x 0.350 x 0.082
EDI8464P55LB	55	MIL	120	3	500	LCC/28	0.55 x 0.350 x 0.082
EDI8465P25QB	25	MIL	120	3	500	DIP/24	1.20 x 0.350 x 0.145
EDI8465P35QB	35	MIL	120	3	500	DIP/24	1.20 x 0.350 x 0.145
EDI8465P45QB	45	MIL	120	3	500	DIP/24	1.20 x 0.350 x 0.145
EDI8465P55QB	55	MIL	120	3	500	DIP/24	1.20 x 0.350 x 0.145
EDI8465P25LB	25	MIL	120	3	500	LCC/28	0.55 x 0.350 x 0.082
EDI8465P35LB	35	MIL	120	3	500	LCC/28	0.55 x 0.350 x 0.082
EDI8465P45LB	45	MIL	120	3	500	LCC/28	0.55 x 0.350 x 0.082
EDI8465P55LB	55	MIL	120	3	500	LCC/28	0.55 x 0.350 x 0.082

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EDI has been the the leading supplier of bytewide SRAMs for Military applications since it introduced the industry's first Military 64K Static RAM, an 8Kx8 module, in 1983.

Bytewide, 256K Monolithic CMOS Static RAMs

Part Number	Speeds	Temp	Max Current Consumption			Package	
	ns	Range	ICC1	ICC3	IDR	Type/Pins	Dimensions
			mA	mA	µA		L x W x H (in)
32Kx8							
EDI8832C45CB	45	MIL	95	1.5	600	DIP/28	1.40x.600x.180
EDI8832C55CB	55	MIL	95	1.5	600	DIP/28	1.40x.600x.180
EDI8832C60CB	60	MIL	95	1.5	600	DIP/28	1.40x.600x.180
EDH8832C-70KMHR	70	MIL	95	1	500	DIP/28	1.40x.600x.180
EDH8832C-85KMHR	85	MIL	95	1	500	DIP/28	1.40x.600x.180
EDH8832C-10KMHR	100	MIL	95	1	500	DIP/28	1.40x.600x.180
EDH8832C-12KMHR	120	MIL	95	1	500	DIP/28	1.40x.600x.180
EDH8832C-15KMHR	150	MIL	95	1	500	DIP/28	1.40x.600x.180
EDI8832C45LB	45	MIL	95	1.5	600	LCC/32	0.45x.550x.090
EDI8832C55LB	55	MIL	95	1.5	600	LCC/32	0.45x.550x.090
EDI8832C60LB	60	MIL	95	1.5	600	LCC/32	0.45x.550x.090
EDH8832C-70JMHR	70	MIL	95	1	500	LCC/32	0.45x.550x.090
EDH8832C-85JMHR	85	MIL	95	1	500	LCC/32	0.45x.550x.090
EDH8832C-10JMHR	100	MIL	95	1	500	LCC/32	0.45x.550x.090
EDH8832C-12JMHR	120	MIL	95	1	500	LCC/32	0.45x.550x.090
EDH8832C-15JMHR	150	MIL	95	1	500	LCC/32	0.45x.550x.090
EDH8832C-70QMHR	70	MIL	95	1	500	DIP/28	1.40x.300x.180
EDH8832C-85QMHR	85	MIL	95	1	500	DIP/28	1.40x.300x.180
EDH8832C-10QMHR	100	MIL	95	1	500	DIP/28	1.40x.300x.180
EDH8832C-12QMHR	120	MIL	95	1	500	DIP/28	1.40x.300x.180
EDH8832C-15QMHR	150	MIL	95	1	500	DIP/28	1.40x.300x.180
32Kx8, Low Power							
EDH8832P-70KMHR	70	MIL	95	0.25	150	DIP/28	1.40x.600x.180
EDH8832P-85KMHR	85	MIL	95	0.25	150	DIP/28	1.40x.600x.180
EDH8832P-10KMHR	100	MIL	95	0.25	150	DIP/28	1.40x.600x.180
EDH8832P-12KMHR	120	MIL	95	0.25	150	DIP/28	1.40x.600x.180
EDH8832P-15KMHR	150	MIL	95	0.25	150	DIP/28	1.40x.600x.180
EDH8832P-70JMHR	70	MIL	95	0.25	150	LCC/32	0.45x.550x.090
EDH8832P-85JMHR	85	MIL	95	0.25	150	LCC/32	0.45x.550x.090
EDH8832P-10JMHR	100	MIL	95	0.25	150	LCC/32	0.45x.550x.090
EDH8832P-12JMHR	120	MIL	95	0.25	150	LCC/32	0.45x.550x.090
EDH8832P-15JMHR	150	MIL	95	0.25	150	LCC/32	0.45x.550x.090
EDH8832P-70DMHR	70	MIL	95	0.25	150	CERDIP/28	1.40x.600x.180
EDH8832P-85DMHR	85	MIL	95	0.25	150	CERDIP/28	1.40x.600x.180
EDH8832P-10DMHR	100	MIL	95	0.25	150	CERDIP/28	1.40x.600x.180
EDH8832P-12DMHR	120	MIL	95	0.25	150	CERDIP/28	1.40x.600x.180
EDH8832P-15DMHR	150	MIL	95	0.25	150	CERDIP/28	1.40x.600x.180
EDH8832P-70QMHR	70	MIL	95	0.25	150	DIP/28	1.40x.300x.180
EDH8832P-85QMHR	85	MIL	95	0.25	150	DIP/28	1.40x.300x.180
EDH8832P-10QMHR	100	MIL	95	0.25	150	DIP/28	1.40x.300x.180
EDH8832P-12QMHR	120	MIL	95	0.25	150	DIP/28	1.40x.300x.180
EDH8832P-15QMHR	150	MIL	95	0.25	150	DIP/28	1.40x.300x.180

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DESC Approved Static RAMs

EDI has an active program to be listed as an approved source on the Defense Electronics Supply Center (DESC) Standard Military Drawings for microcircuits and has been listed as an approved source for 8Kx8, 32Kx8, 64Kx4 and 256Kx1 devices. Please contact EDI or your local EDI rep for up-to-date DESC- SMD listings.

DESC Drawing No.	Description
5962-85525	8Kx8
5962-88552	32Kx8, Low Power
5962-88662	32Kx8, Standard Power
5962-88545	64Kx4, Low Power
5962-88681	64Kx4, Standard Power
5962-88544	256Kx1, Low Power
5962-88xxx*	256Kx1, Standard Power

*Source approval pending at publication.

64K Monolithic CMOS Static RAMs

Part Number	Speeds ns	Temp Range	Max Current Consumption ICC1 mA	ICC3 mA	IDR µA	Package Type/Pins	Dimensions L x W x H (in)
64Kx1							
EDI8164C35QB	35	MIL	100	9	—	DIP/22	1.10x.295x.150
EDI8164C45QB	45	MIL	100	9	—	DIP/22	1.10x.295x.150
EDI8164C55QB	55	MIL	100	9	—	DIP/22	1.10x.295x.150
EDI8164C35LB	35	MIL	100	9	—	LCC/22	.490x.290x.070
EDI8164C45LB	45	MIL	100	9	—	LCC/22	.490x.290x.070
EDI8164C55LB	55	MIL	100	9	—	LCC/22	.490x.290x.070
64Kx1, Low Power							
EDI8164P35QB	35	MIL	100	9	600	DIP/22	1.10x.295x.150
EDI8164P45QB	45	MIL	100	9	600	DIP/22	1.10x.295x.150
EDI8164P55QB	55	MIL	100	9	600	DIP/22	1.10x.295x.150
EDI8164P35LB	35	MIL	100	9	600	LCC/22	.490x.290x.070
EDI8164P45LB	45	MIL	100	9	600	LCC/22	.490x.290x.070
EDI8164P55LB	55	MIL	100	9	600	LCC/22	.490x.290x.070
16Kx4							
EDI8416C35QB	35	MIL	90	20	—	DIP/22	1.10x.295x.150
EDI8416C45QB	45	MIL	90	20	—	DIP/22	1.10x.295x.150
EDI8416C55QB	55	MIL	90	20	—	DIP/22	1.10x.295x.150
EDI8416C35LB	35	MIL	90	20	—	LCC/22	.490x.290x.070
EDI8416C45LB	45	MIL	90	20	—	LCC/22	.490x.290x.070
EDI8416C55LB	55	MIL	90	20	—	LCC/22	.490x.290x.070
16Kx4, with Output Enable Function							
EDI8417C35QB	35	MIL	95	20	—	DIP/24	1.10x.300x.145
EDI8417C45QB	45	MIL	95	20	—	DIP/24	1.10x.300x.145
EDI8417C55QB	55	MIL	95	20	—	DIP/24	1.10x.300x.145
EDI8417C35LB	35	MIL	95	20	—	LCC/28	.550x.350x.082
EDI8417C45LB	45	MIL	95	20	—	LCC/28	.550x.350x.082
EDI8417C55LB	55	MIL	95	20	—	LCC/28	.550x.350x.082

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64K Monolithic CMOS Static RAMs

Part Number	Speeds	Temp	Max Current Consumption			Package	
	ns	Range	ICC1	ICC3	IDR	Type/Pins	Dimensions
			mA	mA	µA		L x W x H (in)
8Kx9							
EDI8908C35CB	35	MIL	140	1	200	DIP/28	1.40x.600x.180
EDI8908C45CB	45	MIL	140	1	200	DIP/28	1.40x.600x.180
EDI8908C55CB	55	MIL	140	1	200	DIP/28	1.40x.600x.180
EDI8908C35QB	35	MIL	140	1	200	DIP/28	1.40x.300x.180
EDI8908C45QB	45	MIL	140	1	200	DIP/28	1.40x.300x.180
EDI8908C55QB	55	MIL	140	1	200	DIP/28	1.40x.300x.180
EDI8908C35LB	35	MIL	140	1	200	LCC/32	0.45x.550x.090
EDI8908C45LB	45	MIL	140	1	200	LCC/32	0.45x.550x.090
EDI8908C55LB	55	MIL	140	1	200	LCC/32	0.45x.550x.090
EDI8908C35L28B	35	MIL	140	1	200	LCC/28	.550x.350x.082
EDI8908C45L28B	45	MIL	140	1	200	LCC/28	.550x.350x.082
EDI8908C55L28B	55	MIL	140	1	200	LCC/28	.550x.350x.082
8Kx8							
EDI8808C35CB	35	MIL	140	1	200	DIP/28	1.40x.600x.180
EDI8808C45CB	45	MIL	140	1	200	DIP/28	1.40x.600x.180
EDI8808C55CB	55	MIL	140	1	200	DIP/28	1.40x.600x.180
EDI8808C35QB	35	MIL	140	1	200	DIP/28	1.40x.300x.180
EDI8808C45QB	45	MIL	140	1	200	DIP/28	1.40x.300x.180
EDI8808C55QB	55	MIL	140	1	200	DIP/28	1.40x.300x.180
EDI8808C35LB	35	MIL	140	1	200	LCC/32	0.45x.550x.090
EDI8808C45LB	45	MIL	140	1	200	LCC/32	0.45x.550x.090
EDI8808C55LB	55	MIL	140	1	200	LCC/32	0.45x.550x.090
8Kx8, 6T CMOS							
EDH8808ACL-10KMHR	100	MIL	70	0.1	50	DIP/28	1.40x.600x.180
EDH8808ACL-12KMHR	120	MIL	70	0.1	50	DIP/28	1.40x.600x.180
EDH8808ACL-15KMHR	150	MIL	70	0.1	50	DIP/28	1.40x.600x.180
EDH8808ACL-20KMHR	200	MIL	70	0.1	50	DIP/28	1.40x.600x.180
EDH8808ACL-10DMHR	100	MIL	70	0.1	50	CERDIP/28	1.40x.600x.180
EDH8808ACL-12DMHR	120	MIL	70	0.1	50	CERDIP/28	1.40x.600x.180
EDH8808ACL-15DMHR	150	MIL	70	0.1	50	CERDIP/28	1.40x.600x.180
EDH8808ACL-20DMHR	200	MIL	70	0.1	50	CERDIP/28	1.40x.600x.180
EDH8808ACL-10JMHR	100	MIL	70	0.1	50	LCC/32	0.45x.550x.090
EDH8808ACL-12JMHR	120	MIL	70	0.1	50	LCC/32	0.45x.550x.090
EDH8808ACL-15JMHR	150	MIL	70	0.1	50	LCC/32	0.45x.550x.090
EDH8808ACL-20JMHR	200	MIL	70	0.1	50	LCC/32	0.45x.550x.090

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EDI is continuing its leadership in the manufacture of Static RAM modules by incorporating each new advance in SRAM technology to provide today's designers with next generation technology.

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Megabit Density Static RAM Modules

Part Number	Speeds	Temp	Max Current Consumption			Package	
	ns	Range	ICC1	ICC3	IDR	Type/Pins	Dimensions
			mA	mA	µA		L x W x H (in)
64Kx16, High Speed, Programmable							
EDH816H64C-35CC	35	COM	1380	85	—	DIP/40	2.20x.900x.270
EDH816H64C-45CC	45	COM	1380	85	—	DIP/40	2.20x.900x.270
EDH816H64C-55CC	55	COM	1380	85	—	DIP/40	2.20x.900x.270
EDH816H64C-70CC	70	COM	1380	85	—	DIP/40	2.20x.900x.270
EDH816H64C-35CMHR	35	MIL	1380	85	—	DIP/40	2.20x.900x.270
EDH816H64C-45CMHR	45	MIL	1380	85	—	DIP/40	2.20x.900x.270
EDH816H64C-55CMHR	55	MIL	1380	85	—	DIP/40	2.20x.900x.270
EDH816H64C-70CMHR	70	MIL	1380	85	—	DIP/40	2.20x.900x.270
64Kx16, JEDEC Standard Pinout							
EDI8M1664C60CC	60	COM	240	10	2500	DIP/40	2.20x.900x.270
EDI8M1664C70CC	70	COM	240	10	2500	DIP/40	2.20x.900x.270
EDI8M1664C85CC	85	COM	195	3	1500	DIP/40	2.20x.900x.270
EDI8M1664C100CC	100	COM	195	3	1500	DIP/40	2.20x.900x.270
EDI8M1664C70CB	70	MIL	240	10	2500	DIP/40	2.20x.900x.270
EDI8M1664C85CB	85	MIL	195	3	1500	DIP/40	2.20x.900x.270
EDI8M1664C100CB	100	MIL	195	3	1500	DIP/40	2.20x.900x.270
128Kx8, JEDEC Standard Pinout							
EDI8M8128C60CC	60	COM	120	10	2500	DIP/32	1.60x.600x.275
EDI8M8128C70CC	70	COM	120	10	2500	DIP/32	1.60x.600x.275
EDI8M8128C80CC	80	COM	120	10	2500	DIP/32	1.60x.600x.275
EDI8M8128C90CC	90	COM	195	3	1500	DIP/32	1.60x.600x.275
EDI8M8128C100CC	100	COM	195	3	1500	DIP/32	1.60x.600x.275
EDI8M8128C120CC	120	COM	195	3	1500	DIP/32	1.60x.600x.275
EDI8M8128C150CC	150	COM	195	3	1500	DIP/32	1.60x.600x.275
EDI8M8128C70CB	70	MIL	120	10	2500	DIP/32	1.60x.600x.275
EDI8M8128C80CB	80	MIL	120	10	2500	DIP/32	1.60x.600x.275
EDI8M8128C90CB	90	MIL	195	3	1500	DIP/32	1.60x.600x.275
EDI8M8128C100CB	100	MIL	195	3	1500	DIP/32	1.60x.600x.275
EDI8M8128C120CB	120	MIL	195	3	1500	DIP/32	1.60x.600x.275
EDI8M8128C150CB	150	MIL	195	3	1500	DIP/32	1.60x.600x.275
128Kx8, JEDEC Standard Pinout, Low Power							
EDI8M8128P90CC	90	COM	95	0.9	500	DIP/32	1.60x.600x.275
EDI8M8128P100CC	100	COM	95	0.9	500	DIP/32	1.60x.600x.275
EDI8M8128P120CC	120	COM	95	0.9	500	DIP/32	1.60x.600x.275
EDI8M8128P150CC	150	COM	95	0.9	500	DIP/32	1.60x.600x.275
EDI8M8128P90CB	90	MIL	95	0.9	500	DIP/32	1.60x.600x.275
EDI8M8128P100CB	100	MIL	95	0.9	500	DIP/32	1.60x.600x.275
EDI8M8128P120CB	120	MIL	95	0.9	500	DIP/32	1.60x.600x.275
EDI8M8128P150CB	150	MIL	95	0.9	500	DIP/32	1.60x.600x.275

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512 K Density, High Performance CMOS Static RAM Modules

Part Number	Speeds	Temp	Max Current Consumption			Package	
	ns	Range	ICC1	ICC3	IDR	Type/Pins	Dimensions
			mA	mA	µA		L x W x H (in)
64Kx8							
EDI8M864C60CC	60	COM	120	5	2500	DIP/32	1.60x.600x.230
EDI8M864C70CC	70	COM	120	5	2500	DIP/32	1.60x.600x.230
EDI8M864C80CC	80	COM	120	5	2500	DIP/32	1.60x.600x.230
EDI8M864C90CC	90	COM	95	1.5	750	DIP/32	1.60x.600x.230
EDI8M864C100CC	100	COM	95	1.5	750	DIP/32	1.60x.600x.230
EDI8M864C120CC	120	COM	95	1.5	750	DIP/32	1.60x.600x.230
EDI8M864C150CC	150	COM	95	1.5	750	DIP/32	1.60x.600x.230
EDI8M864C70CB	70	MIL	120	5	2500	DIP/32	1.60x.600x.230
EDI8M864C80CB	80	MIL	120	5	2500	DIP/32	1.60x.600x.230
EDI8M864C90CB	90	MIL	95	1.5	750	DIP/32	1.60x.600x.230
EDI8M864C100CB	100	MIL	95	1.5	750	DIP/32	1.60x.600x.230
EDI8M864C120CB	120	MIL	95	1.5	750	DIP/32	1.60x.600x.230
EDI8M864C150CB	150	MIL	95	1.5	750	DIP/32	1.60x.600x.230

256K Density High Performance CMOS Static RAM Modules

16Kx16							
EDH816H16C-25CC-Z	25	COM	440	65	—	ZIP/36	1.70x.292x.500
EDH816H16C-35CC-Z	35	COM	440	65	—	ZIP/36	1.70x.292x.500
EDH816H16C-45CC-Z	45	COM	440	65	—	ZIP/36	1.70x.292x.500
64Kx4							
EDH84H64C-35CC-D3	35	COM	345	8	600	DIP/24	1.30x.600x.270
EDH84H64C-45CC-D3	45	COM	325	8	600	DIP/24	1.30x.600x.270
EDH84H64C-55CC-D3	55	COM	305	8	600	DIP/24	1.30x.600x.270
EDH84H64C-35CMHR-D3	35	MIL	345	10	800	DIP/24	1.30x.600x.270
EDH84H64C-45CMHR-D3	45	MIL	325	10	800	DIP/24	1.30x.600x.270
EDH84H64C-55CMHR-D3	55	MIL	305	10	800	DIP/24	1.30x.600x.270
EDH84H64C-70CMHR-D3	70	MIL	285	10	800	DIP/24	1.30x.600x.270

µPak MicroController Modules

EDI's exclusive µPak (micropak) line offers complete 80C31 micro-computer systems with 64K to 320K bits of external program and data memory in a package and pin configuration equivalent to that of a single microprocessor.

EDI685C31
80C31 based with 64K SRAM and 64K EEPROM

EDI687C31
80C31 based with 64K SRAM and 64K UVEPROM

EDI697C31
80C31 based with 64K SRAM and 256K UVEPROM

Speeds:	8/12 MHz		
Temp Ranges:	COM, IND, MIL		
Packages:	COM	DIP/40	2.05x.700x.365
	IND, MIL	DIP/40	2.05x.700x.288

Electronic Designs Incorporated
42 South Street, Hopkinton, MA 01748-2280 USA (508)435-2341, TFX:(508)4356302, TLX:948004
Electronic Designs Europe Ltd., Shelley House, The Avenue, Lightwater, Surrey GU18 5RF
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EXAR

Communication Circuits

Telecom Circuits

PCM Repeaters	Types of Applications
XR-C240 PCM Repeater XR-C262 High Performance PCM Repeater XR-C262Z High Performance PCM Repeater XR-C277 Low Power PCM Repeater XR-C277-5F Low Power PCM Repeater(2mBit) XR-T5620 T148 PCM Repeater AC/DC Test XR-T56L22 Ultra Low Power Repeater/Receiver	PCM repeater with transmission rate of 1.544 or 2.048 MBits/s T1, T148C, transmission lines.
T1 Line Interface	
XR-T5650 PCM Line Receiver XR-T5750 Crystal Version of T5650	T1 line receiver, positive and negative data recovery, NRZ data format recovery, clock and data separator.
XR-T5670 B8ZS/AMI Transcoder	B8ZS and AMI coding and decoding, code error detection.
XR-T5675 Line Driver	High current driver, relay driver, PCM line driver, lamp driver.
Interface	
XR-T3588/3589 V.35 Interface Receiver/Transmitter	High speed DTE to DCE interface.
XR-T5681 PCM Line Interface Chip 2Mbit XR-T5683 PCM Line Interface Chip 8Mbit XR-T5684 Digital PCM Line Interface Chip T1	T1 PCM receiver for short haul (up to 800 ft).
XR-T5690 Serial T1 Transceiver	T1 D4 and ESF framing and coding.

Datacom Circuits

UARTS	Types of Applications
XR-16C450 Asynchronous Receiver &Transmitter (UART) XR-82C684 CMOS Quad Channel (QUART) XR-88C681/68C681/CMOS Dual Channel UART (DUART)	Asynchronous data communication
Modems	
XR-14412 FSK Modem System XR-2103 FSK Modem Filter XR-2120 PSK Modem Filter XR-2121 Bell 212A Modulator XR-2122 Bell 212A Modulator XR-2123 PSK Modulator/Demodulator XR-2125 Bell 212A Data Buffer XR-2127 Bell 212A/V.22 Modem Filters with Analog Loopback (ALB) XR-2128 Bell 212A/V.22 Modem Filters with ALB and Enhanced CPM XR-2129 Bell 212A/V.22 Modem Filters with ALB and Enhanced CPM XR-2400 V.22 Modem Chip Set XR-2100 V.21 Modem	FSK, PSK, Modems (low/medium speed) PBX, data terminals.

Exar

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EXAR

General Purpose Standard Products

	Types of Applications
Phase Locked Loops & Tone Decoders	
XR-210 FSK Modulator/Demodulator	For FM to audio conversion, frequency synthesis, FSK generation, tracking filter, tone decoding, signal conditioning, FM demodulation.
XR-215 General Purpose Phase-Locked Loop	
XR-2211 FSK Demodulator/Tone Decoder	
XR-2212 Precision Phase-Locked Loop	
XR-567 Tone Decoder	
XR-2567 Dual Monolithic Tone Decoder	
XR-L567 Micropower Tone Decoder	
Function/Waveform Generators & VCOs	
XR-205 Waveform Generator	Voltage and Current-to-Frequency conversion, wave-form generator (sine-square-triangle) phase-locked loop generation, tone generator.
XR-2206 Monolithic Function Generator	
XR-2207 Voltage Controlled Oscillator	
XR-2209 Precision Oscillator	
XR-8038 Precision Waveform Generator	
XR-8038A Precision Waveform Generator w/Low $\Delta THD/\Delta T$	
Timing Circuits	
XR-555 Timing Circuit	Clock generation, time delay generation, memory refresh for micorprocessors, pulse shaping, missing pulse detection.
XR-L555 Micropower Timing Circuit	
XR-556 Dual Timing Circuit	
XR-2240 Programmable Timer/Counter	
XR-2242 Long Range Timer	
XR-2243 Micropower Long Range Timer	
XR-2556 Dual Timing Circuit	
XR-L556 Micropower Dual Timing Circuit	
Voltage Regulator	
XR-1468 Dual Polarity Tracking Voltage Regulator	On card regulation in analog and digital systems, main regulation in small instruments, DC to DC switching regulators transformers.
XR-4194 Dual Tracking Voltage Regulator	
XR-4195 ±15V Dual Tracking Voltage Regulator	
XR-494 Pulse-Width Modulating Regulator	
XR-495 Pulse-Width Modulating Regulator with On-Chip 39V Zener	
XR-1524/2524/3524 Pulse Width Modulating Regulator	
XR-1525A/2525A/3525A Pulse Width Modulating Regulator	
XR-1527A/2527A/3527A Pulse Width Modulating Regulator	
XR-1543 Power Supply Supervisory	
XR-T469 Primary Side Pulse Width Modulator	
Operational Amplifiers	
XR-146/246/356 Programmable Quad Bipolar Op Amp	Signal conditioning, active filters for audio, signal amplification and processing.
XR-3403 Quad Operational Amplifier	
XR-4136 Quad Operational Amplifier	
XR-4741 Quad Operational Amplifier	
XR-4558 Dual Operational Amplifier	
XR-4739 Dual Low Noise Operational Amplifier	
XR-082/3 Dual Bipolar JFET Operational Amplifier	
XR-084 Quad Bipolar JFET Operational Amplifier	
XR-34074 Quad High Performance Operational Amplifier	
Display Drivers	
XR-2201/2/3/4 High Voltage, High Current Darlington Array	LED, driver, alpha numeric and fluorescent display up to 85V. 5V-15V CMOS to PMOS level shifter, and solenoid driver. RS-232 Line driver/receiver.
XR-6118 Fluorescent Display Driver	
XR-2001/2/3/4 High Voltage, High Current Darlington Array	
XR-2011/2/3/4 High Voltage, High Current Darlington Array	
XR-1488 Quad Line Driver	
XR-1489A Quad Line Receiver	
General Purpose Switched Capacitor Filters	
XR-1001/8 General Purpose Low Pass Filters	Removes noise from desired signal. Select particular tone from a spectrum. Signal conditioning for digital processing, detection of harmonic in vibrational analysis. C-message noise measurement in telecom systems.
XR-1010 Second Order Switched Capacitor Filters	
XR-1015/1016 Seventh Order Switched Capacitor Filters	
XR-1020A Telecom Instrumentation Filter	

Disk Drives Circuits

EXAR offers a wide selection of products specifically designed for hard disk, floppy disk and magnetic tape drives. Our years of experience in designing and manufacturing standard integrated circuits for the magnetic storage industry is complemented by our custom and semi-custom experience and capabilities, which have produced user specific proprietary integrated circuits for major disk drive functions.

	XR-117	XR-501	XR-510A	XR-511
High Bandwidth Preamplifier (>50MHz)	*	*	*	*
Full Writing Functions	*	*	*	*
Low Noise Preamplifier (<2nV/ Hz)	*			
Very Low Noise Preamplifier (<1nV/ Hz)		*	*	*
Unsafe Condition Indicator	*	*	*	*
Low Voltage Inhibit		*	*	*
Optional Internal Damping Resistors	*	*	*	*
2 Head Version	*		*	
4 Head Version	*		*	*
6 Head Version	*	*	*	*
8 Head Version		*		*
DIP Packaging	*	*	*	*
PLCC Packaging	*	*	*	*
JEDEC S.O. Packaging	*	*	*	*

Exar

Pulse Detector Circuits

The Pulse Detector takes the analog read signal from the Read/Write preamplifier and converts it into digital data at standard TTL levels. EXAR pulse detectors also include additional circuitry to "pre-qualify" the analog data to eliminate errrors.

	XR-541	XR-8464B
Interfaces directly with all EXAR Read/Writes	*	*
High Performance AGC	*	*
Amplitude Signal Qualification	*	*
Compatible with MFM Clock Encoding	*	*
Compatible with RLL Clock Encoding	*	*
AGC Hold for Embedded Servo Applications	*	
Single +12V Power Supply		*
Standard +5V/+12V Power Supplies	*	
DIP Packaging	*	*
PLCC Packaging	*	*
JEDEC S.O. Packaging	*	

XR-532* RLL Data Separator

*Available Janurary 1989

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883C E² FROM EXEL

EXEL ESTABLISHED ITS 883C COMPLIANCE IN 1987. WE OFFER MILITARY PRODUCTS THAT CONFORM TO EITHER 883C OR STANDARD MILITARY DRAWINGS.

AVAILABLE NOW

XL 2864 FAMILY, NMOS, 8K x 8, E² PROM, PIN 1 OPEN

XLM2864AY-300A883C	300NS	600MIL, CERAMIC DIP
XLM2864AY-350A883C	350NS	
XLM2864AY-450A883C	450NS	

XL 2865 FAMILY, NMOS, 8K x 8, E²PROM, PIN 1 READY/BUSY

XLM2865AY-300A883C	300NS	600MIL, CERAMIC DIP
XLM2865AY-350A883C	350NS	
XLM2865AY-450A883C	450NS	

XL 78C800 FAMILY, CMOS, E²PLD, 600-800 NOR GATES

XLM78C800L-45A883C	45NS	300MIL, CERAMIC DIP

Exel

AVAILABLE SOON – CONSULT FACTORY

XL 2864 FAMILY IN 32 LEAD LCC (Z PKG)
XL 2816 FAMILY IN 24 LEAD CERAMIC DIP (J PKG)
XL 78C800 FAMILY IN 300 MIL, CERAMIC DIP 25NS, 35NS
XL 46C15 FAMILY, CMOS, 16K, E²PROM, BIPOLAR PROM PINOUTS IN BOTH THE 28 LEAD LCC (3 PKG) AND 24 LEAD CERAMIC DIP

FOR MORE INFORMATION CONTACT YOUR LOCAL EXEL DISTRIBUTOR, EXEL REPRESENTATIVE OR EXEL SALES DEPARTMENT.

EXEL MICROELECTRONICS, 2150 COMMERCE DR, SAN JOSE, CA 95161
PHONE: 408/432-0500 FAX: 408/432-8710

EXEL

XL93C46

93C46 1024-Bit Serial Electrically Erasable Programmable Memory (5V only)

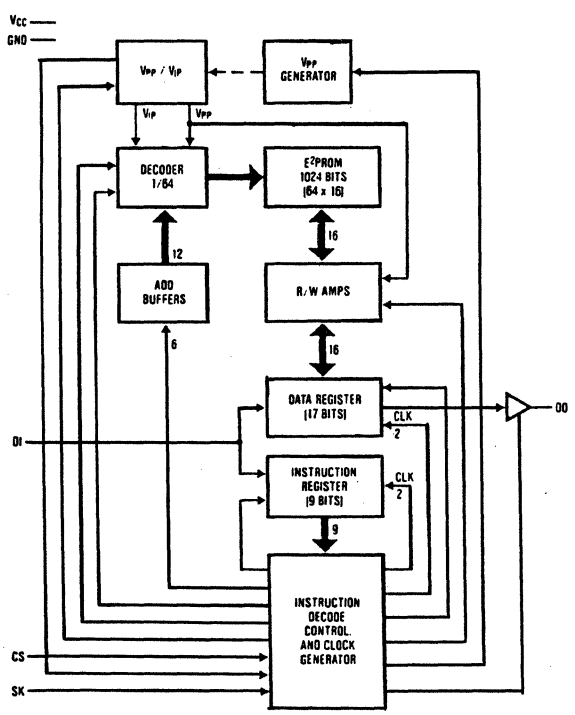
General Description

The 93C46 is a 1024-bit non-volatile, sequential EEPROM, fabricated using advanced CMOS EEPROM technology. It is an external memory with the 1024 bits of read/write memory divided into 64 registers of 16 bits each. Each register can be serially read or written by a 4-bit or 8-bit controller device, such as a COP4XX, 8048,8096 or TMS1000, or by a standard microprocessor. Written information is stored in a floating gate cell until it is updated by an erase and write cycle. The 93C46 has been designed for applications requiring up to 10000 erase/write cycles per register. A power-down mode is provided by CS to reduce power consumption by 83 percent with TTL levels and 87 percent with CMOS levels, when compared to a NMOS part in standby mode.

Features

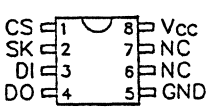
- CMOS
- Low Cost
- TTL compatible
- 5V only erase and write (5V = 10%)
- 64 x 16 serial read/write memory
- Simple interfacing
- Low standby power
- Non-volatile erase and write
- Reliable floating gate technology
- Self-timed programming cycle
- Device status signal
- Compatible with NMC9306, NMC9346, COP494 and COP495

Block Diagram

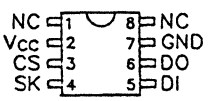


PIN CONFIGURATIONS

Plastic Dual-in-line Package



Small Outline Package



Pin Names

CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
V_{CC}	Power Supply
GND	Ground
NC	Not Connected

EXEL Microelectronics, Inc.
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2150 Commerce Drive • P.O. Box 49038 • San Jose, CA 95161-9038
PHONE 408 432-0500 • FAX 408 432-8710 • TWX 910 338-23116 • TLX 17339

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FUJITSU

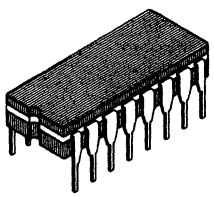
ULTRA HIGH SPEED ECL ICs

MB 810A/MB 811A
MB 813A/MB 814A

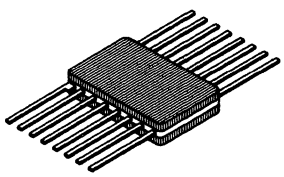
March 1987
Edition 1.0

ULTRA HIGH SPEED ECL FAMILY

The Fujitsu MB 810A series is an ultra high speed logic designed for high speed digital systems. The MB 810A series is suitable not only for a high speed transmission equipment, a radio installation, a high speed logic treatment equipment, a high performance measuring instrument but for high speed gate array peripherals. The inputs/outputs level and power supply voltage are compatible with ECL 10 kH series. The MB 810A series devices are housed in 16-pin mini-flat packages and 16-pin dual-in-line packages.



CERAMIC PACKAGE
DIP-16C-C01



CERAMIC PACKAGE
FPT-16C-C01

- Ultra high speed:
  Propagation delay time – 400 ps/gate typ.
- ECL Interface level:
  10 kH ECL compatible inputs and outputs
- Output rising/falling time – 350 ps typ.
- Max. clock frequency: 1.5 GHz typ.
- Emitter Follower Output: Wired OR capability, 50 Ω line drivability
- Stable bias circuit for the changeable power supply voltage

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply (V_{CCS} = V_{CCF} = 0)	V_{EE}	–7.0 to 0	V
Input Voltage (V_{CCS} = V_{CCF} = 0)	V_{IN}	–3.0 to 0	V
Output Current	I_{OUT}	–50 to 0	mA
Operating Ambient Temperature	T_A	–30 to +125	°C
Storage Temperature	T_{STG}	–55 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Fujitsu Microelectronics

FUJITSU

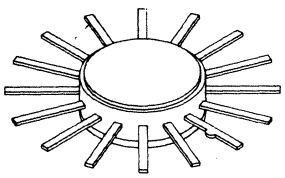
ULTRA HIGH SPEED ECL ICs

MB881/MB882
MB883/MB884
MB885/MB886

June 1988
Edition 2.0

ULTRA HIGH SPEED ECL FAMILY

The Fujitsu MB 880 series is a family of ultra high speed ECL integrated circuits. It is useful for Giga-bits fiber communication systems, and electrical measuring instruments. The inputs/outputs interface and power voltage are compatible with ECL 10K series. The MB 880 series devices are packaged in the compact circular ceramic flat packages that are convenient for mounting a high speed and high density printed circuit board.

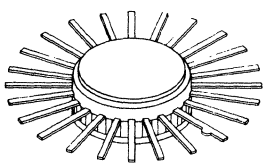


CERAMIC PACKAGE
FPT-16C-A01

- Ultra High Speed:
  Propagation delay time — 150 ps/gate typ.
- ECL Interface Level:
  10K ECL compatible inputs and outputs

Input/Output Characteristic

Parameter	Temperature Coefficient	V_{EE} Coefficient
V_{OH}	1.6 mV/°C typ.	20 mV/V typ.
V_{OL}	0.4 mV/°C typ.	250 mV/V typ.
Input threshold voltage	1.1 mV/°C typ.	140 mV/V typ.



CERAMIC PACKAGE
FPT-24C-A03

- Single Power Supply:
  -5.2 V for V_{EE}, -2.0 V for output load terminations
- Emitter Follower Output:
  Wired OR capability, 50 Ω line drivability
- Compact Circular Flat Package:
  Low thermal resistance (10°C/W typ. (junction to case) for FPT-16C-A01, 6°C/W typ. (junction to case) for FPT-24C-A03C), high density mounting capability.
- 2 Pins for 1 Input:
  Having 2 pins for each input makes it easy to design the signal patterns on the printed circuit board.

ABSOLUTE MAXIMUM RATINGS (V_{CC} = 0 V)

Parameter	Symbol	Rating	Unit
Supply Voltage	V_{EE}	-7.0 to 0	V
Input Voltage	V_I	-5.5 to 0	V
Output Current	I_{OUT}	50	mA
Case Temperature	T_C	-30 to 125	°C
Storage Temperature	T_{STG}	-55 to 150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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FUJITSU

ECL 4096-BIT BIPOLAR RANDOM ACCESS MEMORY

MBM 10474A-5
MBM 10474A-7

June 1987
Edition 1.0

4096-BIT BIPOLAR ECL RANDOM ACCESS MEMORY

The Fujitsu MBM 10474A is fully decoded 4096-bit ECL read/write random access memory designed for high-speed scratch pad, control and buffer storage applications. This device is organized as 1024 words by 4 bits, and it features on-chip voltage compensation for improved noise margin.

The MBM 10474A offers extremely small cell and chip size, realized through the use of Fujitsu's patented DOPOS (Doped Polysilicon), as well as U-Fox (U-groove isolation with thick field oxide) processing. As a result, very fast access time with high yields and outstanding device reliability are achieved in volume production.

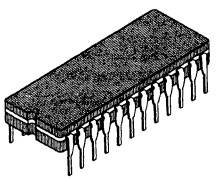
Operation for the MBM 10474A is specified over a temperature range of from 0° to 75°C (T_A for DIP, T_C for Flat Package and LCC). It also features 24-pin DIP, Flat Package, or LCC. It is fully compatible with industry-standard 10 K-series ECL families.

- 1024 words x 4 bits organization
- On-chip voltage compensation for improved noise margin
- Fully compatible with industry-standard 10 K-series ECL families
- Address access time: 5 ns max. (MBM 10474A-5)
  7 ns max. (MBM 10474A-7)
- Chip select access time: 3 ns max. (MBM 10474A-5)
  5 ns max. (MBM 10474A-7)
- Open emitter output for ease of memory expansion
- Low power dissipation of 0.33 mW/bit typ. (MBM 10474A-5)
  0.24 mW/bit typ. (MBM 10474A-7)
- DOPOS and U-Fox processing
- Pin compatible with the F10474

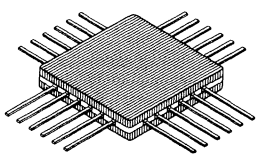
ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating	Symbol	Value	Unit
V_{EE} Pin Potential to Ground Pin	V_{EE}	+0.5 to -7.0	V
Input Voltage	V_{IN}	+0.5 to V_{EE}	V
Output Current (DC, Output High)	I_{OUT}	-30	mA
Temperature under Bias	T_A for DIP	-55 to +125	°C
	T_C for Flat Package and LCC	-55 to +125	
Storage Temperature	T_{STG}	-65 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet.



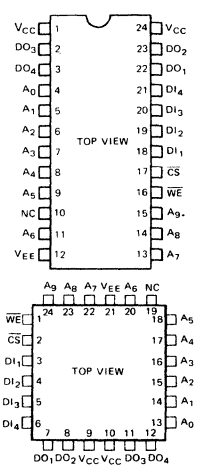
CERAMIC PACKAGE
DIP-24C-C05



CERAMIC PACKAGE
FPT-24C-C02

LCC-24C-F02: See page 10

PIN ASSIGNMENT



V_{CC} grounded
LCC PAD CONFIGURATION : See page 10

Small geometry bipolar integrated circuits are occasionally susceptible to damage from static voltages or electric fields. It is therefore advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this device.

Fujitsu Microelectronics

FUJITSU

ECL 16384-BIT BIPOLAR RANDOM ACCESS MEMORY

MBM10484A-8

October 1987
Edition 1.0

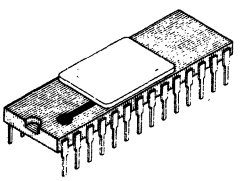
16384-BIT BIPOLAR ECL RANDOM ACCESS MEMORY

The Fujitsu MBM 10484A is fully decoded 16384-bit ECL read/write random access memory designed for high-speed scratch pad, control and buffer storage applications. This device is organized as 4096 words by 4 bits, and it features on-chip voltage compensation for improved noise margin.

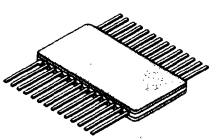
The MBM 10484A offers extremely small cell and chip size, realized through the use of Fujitsu's patented DOPOS (Doped Polysilicon), as well as IOP-II (Isolation by Oxide and Polysilicon) processing. As a result, very fast access time with high yields and outstanding device reliability are achieved in volume production.

Operation for the MBM 10484A is specified over a temperature range of from 0°C to 55°C (T_A for DIP T_C for Flat Package and LCC). It also features 28-pin ceramic DIP, Flat package, or LCC and is fully compatible with industry-standard 10K-series ECL families.

- 4096 words x 4 bits organization
- On-chip voltage compensation for improved noise margin
- Fully compatible with industry-standard 10 K-series ECL families
- Address access time: 8 ns max.
- Chip select access time: 4 ns max.
- Open emitter output for ease of memory expansion
- Low power dissipation of 0.10 mW/bit typ.
- DOPOS and IOP-II processing



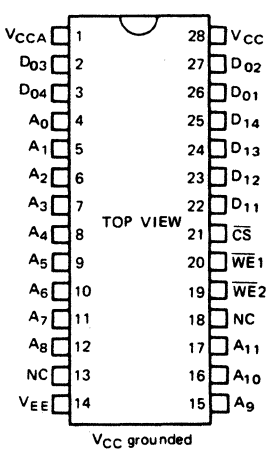
CERAMIC PACKAGE
DIP-28C-A06



CERAMIC PACKAGE
FPT-28C-C03

LCC-28C-F02: See Page 10

PIN ASSIGNMENT



LCC PAD CONFIGURATION: See Page 10

ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating	Symbol	Value	Unit
V_{EE} Pin Potential to Ground Pin	V_{EE}	+0.5 to -7.0	V
Input Voltage	V_{IN}	+0.5 to V_{EE}	V
Output Current (DC, Output High)	I_{OUT}	-30	mA
Temperature under Bias	T_A for DIP	-55 to +125	°C
	T_C for Flat Package and LCC	-55 to +125	
Storage Temperature	T_{STG}	-65 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Fujitsu Microelectronics

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FUJITSU

BICMOS 262144-BIT ECL RANDOM ACCESS MEMORY

MBM100C500-15

May 1988
Edition 1.0

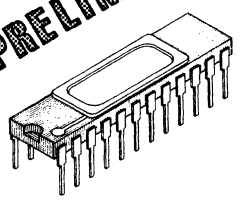
262144-BIT BICMOS ECL RANDOM ACCESS MEMORY

The Fujitsu MBM100C500 is fully decoded 262144 bit BICMOS ECL random access memory designed for main memory, control and buffer storage applications. This device is organized as 262144 words by one bit, and it features on chip voltage compensation for improved noise margin.

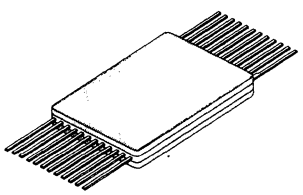
Operation for the MBM100C500 is specified over an ambient temperature range of from 0°C to 85°C (TA). It is packaged in 24-pin ceramic DIP, flatpackage, or LCC and fully compatible with industory standard 100K series ECL families.

- 262144 words by 1 bit organization
- On-chip voltage/temperature compensation for improved noise margin
- Fully compatible with industory standard 100K series ECL families
- Address access time: 15ns max
  Chip select access time: 15ns max
- Power dissipation: 550mW typ
- Open emitter output for ease of memory expansion
- BICMOS Processing

PRELIMINARY



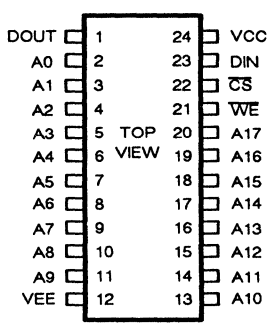
DIP-24C-A09

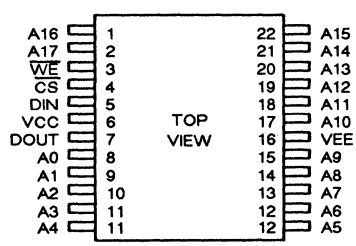


FPT-24C-C04

LCC-24C-A02: See page 7

PIN ASSIGNMENT





LCC Pad Configuration: See page 7

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

ABSOLUTE MAXIMUM RATINGS (see NOTE)

Rating	Symbol	Value	Unit
VEE Pin Potential to ground Pin	V_{EE}	+0.5 to -7.0	V
Input Voltage	V_{IN}	+0.5 to VEE	V
Output Current (DC, Output High)	I_{OUT}	-30	mA
Temperature under Bias	T_A	-55 to +125	°C
Storage Temperature	T_{STG}	-65 to +150	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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FUJITSU

CMOS UV ERASABLE 262144-BIT READ ONLY MEMORY

MBM 27C256H-10
MBM 27C256H-12

June 1986
Edition 1.0

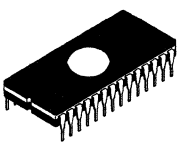
CMOS 262144 BIT UV ERASABLE AND ELECTRICALLY PROGRAMMABLE READ ONLY MEMORY

PRELIMINARY

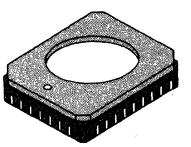
The Fujitsu MBM 27C256H is a 262,144 bits high speed CMOS erasable and electrically reprogrammable read only memory (EPROM). It is especially well suited for application where rapid turn-around and/or bit pattern experimentation, and low-power consumption are important.

A 28-pin dual-in line package with a transparent lid and 32-pad Leadless Chip Carrier (LCC) are used to package the MBM 27C256H. The transparent lid allows the user to expose the device to ultra violet light in order to erase the memory bit pattern previously programmed. At the completion of erasure, a new pattern can then be written into the memory.

The MBM 27C256H is fabricated using CMOS double polysilicon gate technology with single transistor stacked gate cells. It is organized as 32,768 words by 8 bits for use in microprocessor applications. Single +5V operation greatly facilitates its use in systems.



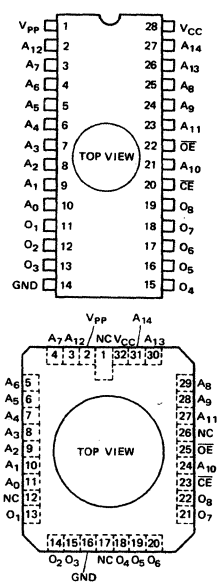
CERAMIC PACKAGE
DIP-28C-C01



CERAMIC PACKAGE
LCC-32C-F01

- CMOS power consumption
  Standby: 550 μW max.
  Active: 330 mW max.
- 32,768 words x 8 bits organization, fully decoded
- Single location programming
- Programmable utilizing the Quick Pro™ algorithm
- Programming voltage: 12.5V
- No clocks required (fully static operation)
- Fast access time:
  100 ns max. (MBM 27C256H-10)
  120 ns max. (MBM 27C256H-12)
- TTL compatible inputs/outputs
- Three-state output with OR-tie capability
- Single +5V supply, ±10% tolerance
- Standard 28-pin ceramic
  DIP: Suffix-Z
- Standard 32-pad ceramic
  LCC: Suffix-TV

PIN ASSIGNMENT



ABSOLUTE MAXIMUM RATINGS (see NOTE)

Rating	Symbol	Value	Unit
Temperature under Bias	T_{BIAS}	-25 to +85	°C
Storage Temperature	T_{STG}	-65 to +125	°C
All Inputs/Outputs Voltage with respect to GND	V_{IN}, V_{OUT}	-0.6 to $+V_{CC}$ + 0.6	V
Voltage on A_9 with respect to GND	V_{A9}	-0.6 to +13.5	V
V_{PP} Voltage with respect to GND	V_{PP}	-0.6 to +13.5	V
Supply Voltage with repsect to GND	V_{CC}	-0.6 to +7	V

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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FUJITSU

CMOS 1,048,576 BIT UV ERASABLE READ ONLY MEMORY (EPROM)

MBM 27C1001-20
MBM 27C1001-25

March 1987
Edition 1.0

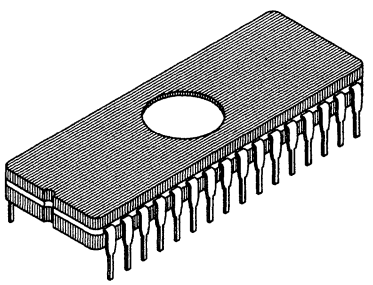
CMOS 1,048,576 BIT UV ERASABLE READ ONLY MEMORY (EPROM)

PRELIMINARY

The Fujitsu MBM 27C1001 EPROM is a high speed read-only static memory that is UV-erasable and reprogrammable. The device contains 1,048,576 programmable or reprogrammable bits organized in a 131,072-byte/8-bit format. The MBM 27C1001 is housed in a 32-pin DIP with a transparent lid; when the lid is properly exposed to an ultraviolet light source, a previously programmed bit pattern is erased in approximately 15-to-21 minutes. A new bit pattern can then be written into memory.

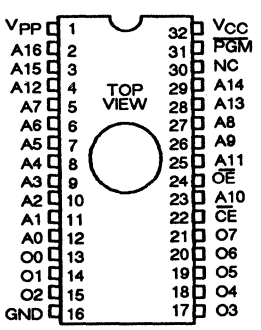
The MBM 27C1001 EPROM is fabricated using CMOS double poly-silicon gate technology with stacked single-transistor gate cells. The MBM 27C1001 is an excellent choice for system development work and in other applications where program changes are frequently necessary. Once programmed, the device requires only a single +5V power supply; the current requirements are exceptionally low in both the active and standby modes of operation.

- 131,072-byte/8-bit organization with on-chip decoding
- Single-byte or four-byte programming capability with Quick Pro™ algorithm
- Static operation (no clocks required)
- Upward compatible with 256K/512K EPROMS
- Fast access time:
  MBM 27C1001-20 = 200 ns (max)
  MBM 27C1001-25 = 250 nx (max)
- Easy and simple memory expansion via @pin
- Three-state output for wired-OR capability
- TTL-compatible inputs/outputs
- Single =5V (+10%) power supply with low current drain:
  Active operation = 30 mA (max)
  Standby operation = 0.1 mA (max)
- Programming voltage: +12.5V
- JEDEC-approved pin assignments
- 32-pin CERDIP



CERAMIC PACKAGE
DIP-32C-C01

PIN ASSIGNMENT



ABSOLUTE MAXIMUM RATINGS (see NOTE)

Rating	Symbol	Value	Unit
Supply Voltage with respect to ground	V_{CC}	-0.6 to + 7.0	V
Programming Voltage with respect to ground	V_{PP}	-0.6 to + 14.0	V
Input/Output Voltage (except for A_9 with respect to ground)	$V_{IN\ 1}$	-0.6 to V_{CC} + 0.6	V
Programming Voltage with respect to ground	$V_{IN\ 2}$	-0.6 to + 13.5	V
Temperature under Bias	T_{BIAS}	-25 to + 85	°C
Storage Temperature Range	T_{STG}	-65 to + 125	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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FUJITSU

CMOS 1048576-BIT FAST PAGE DYNAMIC RAM

MB81C1000-10
MB81C1000-12
MB81C1000-15

July 1987
Edition 3.0

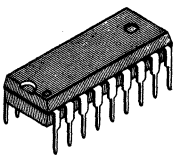
CMOS 1,048,576 x 1 BIT FAST PAGE DYNAMIC RAM

The Fujitsu MB 81C1000 is CMOS fully decoded dynamic RAM organized as 1,048,576 words x 1 bit. The MB 81C1000 has been designed for mainframe memories, buffer memories, and video image memories requiring highspeed, high-band width output with low power dissipation, as well as for memory systems of handheld computers which need very lower power dissipation.

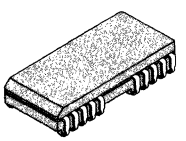
Fujitsu's advanced three-dimensional stacked capacitor cell technology makes the MB 81C1000 high α-ray soft error immunity and long refresh time.

Since the CMOS circuits are used for peripheral circuits, low power dissipation and high speed operation are realized.

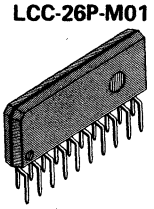
The CMOS standby current is about one-tenth that of the conventional NMOS DRAM, so large capacity memory systems such as semiconductor disks with less power and battery backup becomes possible, i.e., low standby current makes the RAM applicable as non-volatile memories. RAM not requiring large cooling mechanisms are also ideal for equipment which need to work quietly.



PLASTIC PACKAGE
DIP-18P-M04



PLASTIC PACKAGE
LCC-26P-M01

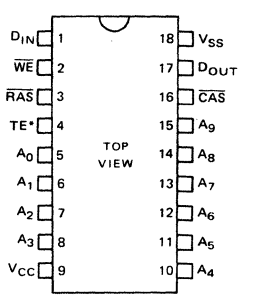


PLASTIC PACKAGE
ZIP-20P-M02

DIP-18C-A01: See Page 17
LCC-26C-A01: See Page 18

- 1,048,576 x 1 CMOS DRAM, 18-pin DIP, 26-pin SOJ, and 20-pin ZIP
- Silicon gate, CMOS, 3D-Stacked Capacitor Cell
- Row Access Time (t_{RAC}),
  100 ns max. (MB 81C1000-10)
  120 ns max. (MB 81C1000-12)
  150 ns max. (MB 81C1000-15)
- Random Cycle Time (t_{RC}),
  180 ns min. (MB 81C1000-10)
  210 ns min. (MB 81C1000-12)
  260 ns min. (MB 81C1000-15)
- Column Access Time (t_{CAC}),
  30 ns max. (MB 81C1000-10)
  35 ns max. (MB 81C1000-12)
  40 ns max. (MB 81C1000-15)
- Fast Page Mode Cycle Time (t_{PC}),
  60 ns min. (MB 81C1000-10)
  70 ns min. (MB 81C1000-12)
  80 ns min. (MB 81C1000-15)
- Single 5V±10% Supply
- Low Power Dissipation
  330 mW max. (MB 81C1000-10)
  275 mW max. (MB 81C1000-12)
  220 mW max. (MB 81C1000-15)
  11 mW max. (TTL level input)
  5.5 mW max. (CMOS level input)
- 512 refresh cycles every 8.2 ms
- $\overline{RAS}$-only, $\overline{CAS}$-before-$\overline{RAS}$, or Hidden Refresh
- Early Write and Delayed Write
- Fast Page Mode Read-Modify-Write capability.
- Common I/O capability by using early write

PIN ASSIGNMENT



*: Test Enable (will be available)

Pin Assignment
For SOJ: See Page 15/18

Pin Assignment
For ZIP: See Page 16

ABSOLUTE MAXIMUM RATINS (See NOTE)

Rating		Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS}		V_{IN}, V_{OUT}	-1 to +7	V
Voltage on V_{CC} Relative to V_{SS}		V_{CC}	-1 to +7	V
Storage Temperature	Ceramic	T_{STG}	-55 to +150	°C
	Plastic		-55 to +125	
Power Dissipation		P_D	1.0	W
Short Circuit Output Current		–	50	mA

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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FUJITSU

CMOS 262,144 BIT STATIC RANDOM ACCESS MEMORY

MB81C81A-35
MB81C81A-45

May 1988
Edition 1.0

262,144 WORDS x 1 BIT HIGH SPEED CMOS STATIC RANDOM ACCESS MEMORY

The Fujitsu MB81C81A is 262,144 words x 1 bit static random access memory fabricated with a CMOS technology.

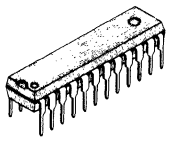
Since MB81C81A consists of NMOS cells and CMOS peripherals, it is packaged in 300 mil DIP and reached low power dissipation such as 550 mW.

It uses fully static circuitry and therefore requires no clocks or refreshing to operate.

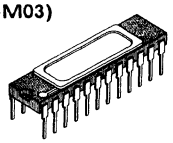
The MB81C81A is designed for memory applications where high performance, low cost, large bit storage and simple interfacing are required.

MB81C81A is compatible with TTL logic families in all respects; input, output and a single +5 V supply.

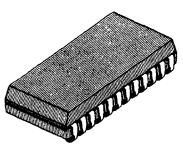
- Organization: 262,144 words x 1 bit
- Static operation: No clocks or refresh required
- Fast access time: 35 ns max. (MB81C81A-35)
  45 ns max. (MB81C81A-45)
- Single +5V supply ±10% tolerance
- Separate data input and output
- TTL compatible inputs and output
- Three-state output with OR-tie capability
- Chip select for simplified memory expansion, automatic power down
- All inputs and output have protection against static charge
- 300 mil width 24-pin Dual In-Line Package
  (Suffix: Plastic DIP; P-SK, Ceramic DIP; C-SK)
  24 pad LCC (Suffix: CV)
  24 pad SOJ (Suffix: PJ)



PLASTIC PACKAGE
(DIP-24P-M03)



CERAMIC PACKAGE
(DIP-24C-A08)



PLASTIC PACKAGE
(LCC-24P-M01)

LCC-24C-A02, See page 11

ABSOLUTE MAXIMUM RATINGS (see NOTE)

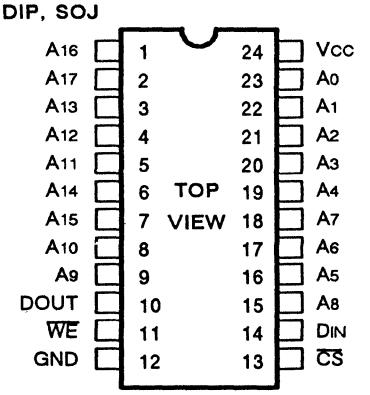
Rating		Symbol	Value	Unit
Supply Voltage		V_{CC}	-0.5 to +7	V
Input Voltage on any pin with to GND		V_{IN}	-3.5* to +7	V
Output Voltage on any pin with to GND		V_{OUT}	-0.5 to +7	V
Output Current		I_{OUT}	±20	mA
Power Dissipation		P_D	1.0	W
Temperature under Bias		T_{BIAS}	-10 to +85	°C
Storage Temperature	CERAMIC	T_{STG}	-65 to +150	°C
	PLASTIC		-45 to +125	

* DC: min. = -0.5 V

NOTE:
Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN ASSIGNMENT

DIP, SOJ



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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FUJITSU

CMOS 262144-BIT STATIC RANDOM ACCESS MEMORY

MB81C84A-35
MB81C84A-45

April 1988
Edition 2.0

64K x 4 BIT(262, 144-BIT) HIGH SPEED STATIC RANDOM ACCESS MEMORY WITH AUTOMATIC POWER DOWN

The Fujitsu MB81C84A is a 65,536-words by 4-bits static random access memory fabricated with a CMOS silicon-gate process. To make power dissipation lower, peripheral circuits consist of CMOS technology, and to obtain smaller chip size, cells consist of NMOS transistors and resistors. MB81C84A has 300mil plastic DIP and 300mil plastic small outline J-lead (SOJ) as package option. The memory utilizes asynchronous circuitly and requires +5V power supply. All pins are TTL compatible.

The MB81C84A is ideally suited for use in large computer systems and other applications where fast access time, large capacity and ease of use are required. All devices offer the advantages of low power dissipation, low cost and high performance.

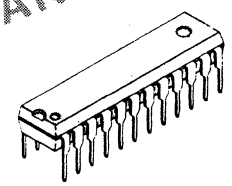
- Organization: 65,536 words x 4 bits
  Fast access time: $t_{AA} = t_{ACS}$ = 35 ns max. (MB81C84A-35)
  $t_{AA} = t_{ACS}$ = 45 ns max. (MB81C84A-45)
- Completely static operation: No clock required
- TTL compatible inputs/outputs
- Three-state output
- Common data input/output
- Single +5V power supply, ±10% tolerance
- Low power standby: 660 mW max. (Active)
  165 mW max. (Standby, TTL level)
  83 mW max. (Standby, CMOS level)
- Standard 24-pin PLASTIC DIP package (300mil) : Suffix -P-SK
- Standard 24-pin PLASTIC SOJ package (300mil) : Suffix -PJ

ABSOLUTE MAXIMUM RATINGS (See NOTE)

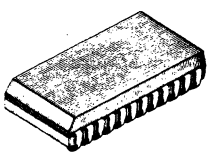
Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.5 to +7.0	V
Input Voltage	V_{IN}	−3.0 to +7.0	V
Output Voltage	V_{OUT}	−0.5 to +7.0	V
Output Current	I_{OUT}	±20	mA
Power Dissipation	P_D	1.0	W
Temperature Under Bias	T_{BIAS}	−10 to +85	°C
Storage Temperature Range	T_{STG}	−45 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ADVANCE INFO.

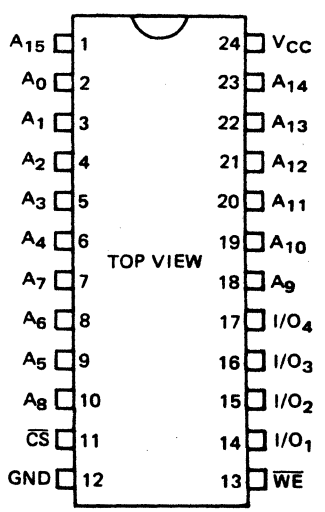


PLASTIC PACKAGE
(DIP-24P-M03)



PLASTIC PACKAGE
(LCC-24P-M01)

PIN ASSIGNMENT



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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SCSI (Small Computer Systems Interface)

Device	Description	Package
MB87030CR	High Performance SCSI Protocol Controller. Asynchronous and synchronous transfer capability. • Transfer Speeds of 4.0MB/sec Synchronous and 2.0MB/sec Asynchronous • 8 Byte FIFO • 24-Bit Transfer Byte Counter • Optimized for Differential Drivers (External)	RIT-88C
MB87031PF	Same as MB87030 except for package	FPT-100P
MB87033PD	Same as MB87030 except: • 24-Bit Transfer Byte Counter • 48mA Single-Ended Drivers On-Chip	LCC-84P
MB89351	Asynchronous only version of the MB87030. • Transfer Speeds of 2.0MB/sec • 8 Byte FIFO • 24-Bit Transfer Byte Counter	SDIP-64P, FPT-64P
MB89352	Same as MB89351except: • 48mA Single-Ended Drivers On-Chip	SDIP-64P, FPT-64P

Floppy Disk Controller

Device	Description	Alternate Source	Package
MB8876A	Floppy Disk Formatter/Controller	FD1791-02	DIP-40P, DIP-40C
MB8877A	Floppy Disk Formatter/Controller	FD1793-02	DIP-40P, DIP-40C
MB89311A	Enhanced 8877A. Supports 3.5",5.25",8" Drives		DIP-28P
MB4107	VFO Oscillator for MB89311		DIP-24P

Hard Disk Controller

Device	Description	Package
MB89342	Single-Chip ESDI Hard Disk Controller	DIP-28P

DRAM Controllers

Device	Description	Package
MB1422	256K or 64K Dynamic RAM Controller	DIP-42P
MB1430	1M Dynamic RAM Controller With Nibble Mode Capability	DIP-48P
MB1431	1M Dynamic RAM Controller With Page Mode Capability	DIP-48P

DSP (Digital Signal Processors)

Device	Description	Package
MB8764	CMOS 16-Bit Fixed Point DSP (100ns Multiply Accumulate Function)	PGA-88P/C, LCC-84C
MB87064	Low-Cost Mask Only Version MB8764	DIP-42P/C
MB86220	Low-Cost CMOS 24-Bit Floating Point DSP (75ns Cycle Time)	PGA-135C, FPT80P
MB86232	High-Performance CMOS 32-Bit Floating Point DSP (75ns Cycle Time)	PGA-208C
MB87069	CCMOS Serial Interface Adaptor for MB8764/064	RIT-64P

IPC (Integrated Peripheral Chip)

Device	Description	Package
MB89396	PC/XT, PC/AT Chip Set Integrates Peripheral Controller Functions in 80286/386 PC Systems: 2x MB89237A (DMA Controller) 2x MB89259A (Interrupt Controller) 1x MB89254 (Interval Timer) DMA Address Latches	FPT-120P

Notes:
FPT: Plastic Flat Package
LCC-xxxC:Leadless ChipCarrier/Leaded Chip Carrier
LCC-xxxP:Plastic Leaded Chip Carrier
RIT: Repeated-In-Line or PGA (Pin Grid Array)
SDIP: Skinny Dual-In-Line Package

Prescalers

MB400/500 Series (BIPolar Technology)

Device	Notes	Max Freq	ICC	VCC	Package
MB467	Low Speed/Low Cost	200 MHz	6mA	5V	DIP-08P, FPT-08P
MB501	Standard Version	1.0 GHz	30mA	5V	DIP-08P, FPT-08P
MB501L	Low-Power Version MB501	1.1 GHz	10mA	5V	DIP-08P, FPT-08P
MB501LV	Low-Voltage Version MB501	1.1 GHz	12mA	5V	DIP-08P, FPT-08P
MB501SL	Super Low-Power Version MB501	1.1 GHz	5mA	5V	DIP-08P, FPT-08P
MB503	Low Speed/Low Cost	200 MHz	8mA	5V	DIP-08P, FPT-08P
MB504	Standard Version	520 MHz	10mA	5V	DIP-08P, FPT-08P
MB504L	Low-Power Version MB504	520 MHz	5mA	5V	DIP-08P, FPT-08P
MB504LV	Low-Voltage Version MB504	520 MHz	6mA	5V	DIP-08P, FPT-08P
MB505-16		1.6 GHz	9mA	5V	DIP-08P, FPT-08P
MB506		2.4 GHz	18mA	5V	DIP-08P, FPT-08P
MB507		1.6 GHz	18mA	5V	DIP-08P, FPT-08P
MB508		2.3 GHz	24mA	5V	DIP-08P, FPT-08P
MB509	Low-Power Stand-by Mode	1.1 GHz	10mA	5V	DIP-08P, FPT-08P

MB50200 Series (GaAs Technology)

Device	Recommended Prescaler	Max Freq	IDD	VDD	Package
MB50201	MB87001A	1.0 GHz	5mA	5V	FPT-08P
MB50202	MB87001A	1.6 GHz	9mA	5V	FPT-08P

MB1500 Series (Single-chip Prescaler and PLL)

Device	Divide Ratio	Freq	ICC	VCC	Package
MB1501	64/65, 128/129	1.1 GHz	15mA	3V	DIP-16P, FPT-16P
MB1504	32/63, 64/65	520 MHz	10mA	3V	DIP-16P, FPT-16P

PLL (Phase Lock Loop) Devices

MB87000 Series

Device	Compatible With	Freq	VDD	IDD	Package
MB87001A		25 MHz	5V	3mA	DIP-16P, FPT-16P
MB87006A	Motorola MC 145158	25 MHz	3-5V	3.5mA	DIP-16P, FPT-16P
MB87014		250 MHz	4-5V	8mA	DIP-16P, FPT-16P
MB87073		25 MHz	3-5V	3mA	DIP-16P, FPT-16P
MB87086		130 MHz	5V	8mA	DIP-16P, FPT-16P

CODECs (Coder/Decoders)

Device	Companding Law	Operation	Alternate Source	Package
MB6021	μ-Law	Sync/Async	HD44234	DIP-16P, DIP-16C
MB6022	A-Law	Sync/Async	HD44233	DIP-16P, DIP-16C
MB6025	μ-Law	Sync	HD44232	DIP-16P, DIP-16C
MB6026	A-Law	Sync	HD44231	DIP-16P, DIP-16C

LAN (Local Area Network)

Device	Description	Package
MB8795B	Ehernet Data Link Controller (IEEE 802.3 CSMA/CD Compatible)	PGA-64C
MB87012	Low-Cost Ethernet Data Link Controller (IEEE 802.3 CSMA/CD Compatible)	DIP/FPT64P,PGA-64C
MB502A	Manchester Encoder/Decoder for MB8795C/MB87012	DIP-24C

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MBL80286
Microprocessors and Peripherals

Device	Description	Package
MBL80286-6 MBL80286-8 MBL80286-10	6 MHz 16-Bit MPU 8 MHz 16-Bit MPU 10 MHz 16-Bit MPU	LCC-68C, LCC-68P,RIT-68C
MBL82284-6 MBL82284-8 MBL82284-1	Clock Generator (6 MHz) Clock Generator (8 MHz) Clock Generator (10 MHz)	DIP-18P, DIP-18C
MBL82288-6 MBL82288-8 MBL82288-1	Bus Controller (6 MHz) Bus Controller (8 MHz) Bus Controller (10 MHz)	DIP-20P, DIP-20C

MBL8086/8088/80186/80188
Microprocessors and Peripherals

Device	Description	Package
MBL80186-6 MBL80186-8 MBL80186-10	6 MHz 16-Bit MPU 8 MHz 16-Bit MPU 10 MHz 16-Bit MPU	LCC-68C, RIT-68C LCC-68P
MBL8086-6 MBL8086-2 MBL8086-1	6 MHz 16-Bit MPU 8 MHz 16-Bit MPU 10 MHz 16-Bit MPU	DIP-40P, DIP-40C
MBL80188 MBL80188-10	8 MHz 16-Bit MPU 10 MHz 16-Bit MPU	LCC-68C, RIT-68C
MBL8088 MBL8088-2 MBL8088-1	5 MHz 8-Bit MPU 8 MHz 8-Bit MPU 10 MHz 8-Bit MPU	DIP-40P, DIP-40C
MBL8089 MBL8089-2	5 MHz I/O Processor 8 MHz I/O Processor	DIP-40C
MBL8259A MBL8259A-2	5 MHz Int Controller 8 MHz Int Controller	DIP-28P,DIP-28C DIP-28P,DIP-28C
MBL8282	Octal Latch	DIP-20C
MBL8283	Octal Latch	DIP-20C
MBL8284A MBL8284A-1	Clock Generator (8MHz) Clock Generator (10MHz)	DIP-18C
MBL8286	Bus Transceiver	DIP-18C
MBL8287	Bus Transceiver	DIP-18C
MBL8288	Bus Controller	DIP-20C
MBL8289 MBL8289-1	Bus Arbiter (8MHz) Bus Arbiter (10MHz)	DIP-20P,DIP-20C

8-Bit Microcomputers and Peripherals

Device	Description	Package
MBL8035N/E/H	NMOS 8-Bit MCU	DIP-40P, DIP-40C
MBL8048N/E/H	NMOS 8-Bit MCU	DIP-40P, DIP-40C
MBL8039N/E/H	NMOS 8-Bit MCU	DIP-40P, DIP-40C
MBL8049N/E/H	NMOS 8-Bit MCU	DIP-40P, DIP-40C
MBL8749H/N	NMOS 8-Bit MCU	DIP-40C
MBL80C39H/N	CMOS 8-Bit MCU	40 Pin C/P-DIP/P-FLAT
MBL80C49H/N	CMOS 8-Bit MCU	40 Pin C/P-DIP/P-FLAT
MBL8031AH	NMOS 8-Bit MCU	DIP-40P, DIP-40C
MBL8051AH	NMOS 8-Bit MCU	DIP-40P, DIP-40C
MBL8243	NMOS I/O Expander	DIP-24P, DIP-24C
MBL82C43	CMOS I/O Expander	DIP-24P, DIP-24C,FPT-24P

Universal Peripheral Interface Controllers

Device	Description	Package
MBL8041A	NMOS 8-Bit	DIP-40P, DIP-40C
MBL8042H/N	ROM version of 8742	DIP-40P, DIP-40C
MBL8742H/N	8-Bit EPROM version	DIP-40C

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Video Controllers

Device	Description	Alternate Source	Package
MB88303	T.V. Display Controller 64 CHAR, 20 x 9		DIP-22P
MB88313	T.V. Display Controller 32 CHAR, 8 x 2 or 16 x 1		DIP-16P, FPT-16P
MB88321	T.V. Display Controller 64 CHAR, 20 x 9 (RGB)		
MB88323	T.V. Display Controller 64 CHAR, 20 x 9		DIP-22P, FPT-24P
MB88324	T.V. Display Controller 64 CHAR, 20 x 9		DIP-22P, FPT-24P
MB88325	T.V. Display Controller 127 CHAR, 24 x 12		
MB89321A	CRT Controller	MC68B45, HC68B45	DIP-40P
MB89321B	CRT Controller	MC68B45, HC68B45	DIP-40P
MB89322A	CRT Controller (Intel Interface Logic)		DIP-40P
MB89322B	CRT Controller (Intel Interface Logic)		DIP-40P

CRT Controller Comparison Chart

	Motorola MC6845	Hitachi HC6845	Hitachi HC6345	Fujitsu MB89321BP	Fujitsu MB89322BP	Fujitsu MB89321AP	Fujitsu MB893222AP
Standard 6845 Features Motorola Bus	X	X	X	X			
Standard 6845 Features Intel Bus					X		
Standard 6845 Features Motorola Bus Plus: • Smooth Scroll • 4-Screen Partitions (Scroll Independent)						X	
Standard 6845 Features Intel Bus Plus: • Smooth Scroll • 4-Screen Partitions (Scroll Independent)							X
CMOS			X	X	X	X	X
100% 6845 Software Compatible	X	X		X	X		
6845 Pin Compatible	X	X		X		X	

CMOS 8-Bit Flexible Micro controllers

Device	Description	Package
MB89713	8K bytes ROM, 260 bytes RAM 8-Channel/8-bit A/D, PWM-D/A Real Time I/O, Full Duplex UART Serial I/O, 0.5uS instruction time 128K off-board addressable memory	SDIP-64, FPT-64
MB89715	16K bytes ROM, 516 bytes RAM 8-Channel/8-bit A/D, PWM-D/A Real Time I/O, Full Duplex UART Serial I/O, 0.5uS instruction time 128K off-board addressable memory	SDIP-64, FPT-64
MB89T713 MB89T715 MB89P713 MB89P715	ROM-less version of MB89713 ROM-less version of MB89715 OTP version of MB89713 OTP version of MB89715	SDIP-64, FPT-64
MB89W715	Windowed EPROM version of MB89715	DIP-64,
MB89PV715	Piggyback device for MB89713/ MB89715	DIP-64,
MB2120	Development system for MB89713/89715 series using PC or VAx as host, plus C-Compiler, Macro-Assembler, Linker, Library Manager, Software Simulator, and Host Emulator software.	

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CD4000B and CD4000A Series CMOS Logic ICs

The RCA CD4000-Series CMOS Logic IC product line covers a broad range of SSI, MSI, and LSI functions from simple gates to complex counters, registers, and arithmetic circuits, and includes both standard circuit types for commercial and industrial applications and high-reliability slash (/) series types for aerospace, military, and critical industrial applications. Types in plastic and in frit-seal ceramic packages are also available with burn-in for applications requiring reliability beyond that of standard commercial product.

Specific design features for CMOS devices and the performance advantages of CMOS technology—low power consumption, high noise immunity, high speed, high fanout, TTL and DTL logic compatibility, excellent temperature stability, and fully protected inputs and outputs—allow the system designer to achieve outstanding performance, high reliability, and simplified circuitry in a wide variety of equipment designs.

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CD4000B-Series Features

- 20-volt rating
- 100% tested for quiescent current at 20 V
- Maximum input current (leakage) of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V at 25°C
- Standardized symmetrical output characteristics
- 5-V, 10-V, and 15-V parametric ratings
- Noise margin (over full package-temperature range): 1 V at V_{DD} = 5 V, 2 V at V_{DD} = 10 V, 2.5 V at V_{DD} = 15 V
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

Function	Type No.	No. of Pins
Gates		
NOR/NAND		
2-Input NOR, 2-Input NAND	**CD4572UB**	16
Dual 4-input NOR	**CD4002B**	14
	CD4002UB	14
Dual 4-input NAND	**CD4012B**	14
	CD4012UB	14
	CD4012A	14
Triple 3-input NOR	**CD4025B**	14
	CD4025UB	14
Triple 3-input NAND	**CD4023B**	14
	CD4023UB	14
Quad 2-input NOR	**CD4001B**	14
	CD4001UB	14
	CD4001A	14
Quad 2-input NAND	**CD4011B**	14
	CD4011UB	14
	CD4011A	14
8-input NOR/OR	**CD4078B**	14
8-input NAND/AND	**CD4068B**	14
Dual 3-input NOR plus inverter	**CD4000B**	14
	CD4000UB	14
Dual 2-input NAND buffer driver	**CD40107B**	8, 14
OR/AND		
Dual 4-input OR	**CD4072B**	14
Dual 4-input AND	**CD4082B**	14
Triple 3-input OR	**CD4075B**	14
Triple 3-input AND	**CD4073B**	14
Quad 2-input OR	**CD4071B**	14
Quad 2-input AND	**CD4081B**	14
Buffers and Inverters		
Dual complementary pair plus inverter	**CD4007UB**	14
	CD4007A	14
Quad Inverter	**CD4572UB**	16
Hex inverter	**CD4069UB**	14
Hex inverter/buffer (3-state)	**CD4502B**	16
Hex buffer (3-state non-inverting)	**CD4503B**	16
Hex buffer/converter (inverting)	**CD4009UB**	16
	CD4009A	16
Hex buffer/converter (inverting)	**CD4049UB**	16
	CD4049A	16
Hex buffer/converter (non-inverting)	**CD4010B**	16
	CD4010A	16
Hex buffer converter (non-inverting)	**CD4050B**	16
Quad true/complement buffer	**CD4041UB**	14
Dual 2-input NAND buffer driver	**CD40107B**	8, 14
Multifunction/AOI		
Quad exclusive-OR	**CD4030B**	14
	CD4030A	14

Function	Type No.	No. of Pins
Gates (cont'd)		
Quad exclusive-OR	**CD4070B**	14
Quad exclusive-NOR	**CD4077B**	14
	CD4519B	16
Quad AND/OR Select	**CD4019B**	16
	CD4019A	16
Dual 2-wide, 2-input AND/OR invert (AOI)	**CD4085B**	14
Expandable 4-wide, 2-input AND/OR invert (AOI)	**CD4086B**	14
Multifunctional expandable 8-input (3-state output)	**CD4048B**	16
	CD4048A	16
Decoders/Encoders		
BCD-to-decimal decoder	**CD4028B**	16
	CD4028A	16
8-input priority encoder	**CD4532B**	16
10-line to 4-line BCD priority encoder	**CD40147B**	16
4-bit latch 4-to-16 line decoder (outputs high)	**CD4514B**	24
4-bit latch 4-to-16 line decoder (outputs low)	**CD4515B**	24
Dual 1-of-4 decoder/demultiplexer (outputs high)	**CD4555B**	16
Dual 1-of-4 decoder/demultiplexer outputs low)	**CD4556B**	16
Schmitt Trigger		
Quad 2-input NAND	**CD4093B**	14
Hex	**CD40106B**	14
Interface		
Quad low-to-high voltage	**CD40109B**	16
Hex high-to-low voltage (inverting)	**CD4009UB**	16
	CD4009A	16
	CD4049UB	16
	CD4049A	16
Hex high-to-low voltage (non-inverting)	**CD4010B**	16
	CD4010A	16
	CD4050B	16
Hex voltage-level shifter TTL-CMOS or CMOS-CMOS operation	**CD4504B**	16
Dual 2-input NAND buffer driver	**CD40107B**	8, 14
8-bit bidirectional CMOS-to-TTL level converter	**CD40116** ▽#	22
Programmable dual 4-bit terminator	**CD40117B**▽	14

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CD4000B and CD4000A Series CMOS Logic ICs (Cont'd)

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Function	Type No.	No. of Pins
Multivibrators		
Monostable astable	**CD4047B**	14
	CD4047A	14
Dual monostable	**CD4098B**	16
Dual precision monostable	**CD4538B**	16
Flip-Flops		
Dual "D" with set/reset capability	**CD4013B**	14
	CD4013A	14
Dual "J-K" with set/reset capability	**CD4027B**	16
	CD4027A	16
Gated "J-K" (non-inverting)	**CD4095B**	14
Gated "J-K" (inverting and non-inverting)	**CD4096B**	14
Hex "D"	**CD40174B**	16
4-bit "D" with 3-state outputs	**CD4076B**	14
Quad "D"	**CD40175B**	16
Latches		
Quad clocked "D"	**CD4042B**	16
	CD4042A	16
Quad NOR R S (3-state outputs)	**CD4043B**	16
Quad NAND R S (3-state outputs)	**CD4044B**	16
Dual 4-bit	**CD4508B**	24
8-bit addressable	**CD4099B**	16
	CD4724B	16
Registers		
Shift Registers-Static		
Dual 4-stage with serial input parallel output	**CD4015B**	16
18-stage	**CD4006B**	14
64-stage	**CD4031B**	16
Dual 64-bit	**CD4517B**	16
8-stage with synchronous parallel or serial input/serial output	**CD4014B**	16
8-stage with asynchronous parallel input or synchronous serial input/serial output	**CD4021B**	16
4-stage parallel-in/parallel-out with J-K input and true/complement output	**CD4035B**	16
4-bit universal bidirectional with 3-state outputs	**CD40104B**	16
4-bit universal bidirectional with asynchronous master reset	**CD40194B**	16
8-stage bidirectional parallel or serial input/parallel output	**CD4034B**	24
32-bit left/right	**CD40100B**	16
8-stage shift-and-store bus	**CD4094B**	16
Shift Registers-Dynamic		
200-stage	**CD4062A**	12
Storage Registers		
8-bit addressable latch	**CD4099B**	16
	CD4724B	16
4-bit "D"-type with 3-state outputs	**CD4076B**	16
4 x 4 Multiport	**CD40108B**	24
4 x 4 Multiport	**CD40208B**	24
FIFO Buffer Registers		
4-bit x 16 word	**CD40105B**	16

Function	Type No.	No. of Pins
Counters		
Binary Ripple		
7-stage	**CD4024B**	14
	CD4024A	14
12-stage	**CD4040B**	16
14-stage	**CD4020B**	16
	CD4020A	16
24-stage frequency divider with oscillator	**CD4521B**	16
14-stage counter/divider and oscillator	**CD4060B**	16
	CD4060A	16
Timers		
21-stage	**CD4045B**	14
Industrial time-base generator	**CD4566B**	16
Programmable	**CD4536B**	16
	CD4541B	14
Synchronous		
Decade counter/divider plus 10 decoded decimal outputs	**CD4017B**	16
	CD4017A	16
Divide-by-8 counter/divider with 8 decminal outputs	**CD4022B**	16
Presettable divide-by- "N" counter, fixed or programmable	**CD4018B**	16
	CD4018A	16
Programmable BCD divide-by- "N" counter	**CD4522B**	16
Programmable divide-by- "N" counter	**CD4059A**	24
Presettable up/down counter, binary or BCD-decade	**CD4029B**	16
	CD4029A	16
Presettable 4-bit BCD up/down counter	**CD4510B**	16
Presettable 4-bit binary up/down counter	**CD4516B**	16
Presettable 2-decade BCD down counter	**CD40102B**	16
Presettable 8-bit binary down counter	**CD40103B**	16
Presettable 4-bit BCD up/down counter	**CD40192B**	16
Presettable 4-bit binary up/down counter	**CD40193B**	16
Dual BCD up counter	**CD4518B**	16
Dual binary up counter	**CD4520B**	16
Programmable 4-Bit Counters:		
Decade with asynchronous clear	**CD40160B**	16
Binary with asynchronous clear	**CD40161B**	16
Decade with synchronous clear	**CD40162B**	16
Binary with synchronous clear	**CD40163B**	16
Display Drivers		
With Counter		
Decade counter/divider with 7-segment display outputs and display enable	**CD4026B**	16
Decade counter/divider with 7-segment display outputs and ripple blanking	**CD4033B**	16

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Function	Type No.	No. of Pins
Display Drivers		
With Counter (Cont'd)		
Decade Up/Down Counter/Latch/ Display-Driver	**CD40110B**	16
For Liquid-Crystal-Display Driver		
4-segment display driver	**CD4054B**	16
BCD-to-7-segment decoder/driver with "display-frequency" output	**CD4055B**	16
BCD-to-7-segment decoder/driver with strobed-latch function	**CD4056B**	16
	CD4543B	16
4-digit decoder/driver with hexidecimal display	**CD7211**▽	40
4-digit decoder/driver with decimal display	**CD7211A**▽	40
4-digit decoder/driver with hexidecimal display	**CD7211M**▽	40
4-digit decoder/driver with decimal display	**CD7211AM**▽	40
For Light-Emitting-Diode Drive		
BCD-to-7-segment latch decoder/ driver	**CD4511B**	16
Multiplexers/Demultiplexers		
Analog		
Triple 2-channel	**CD4053B**	16
Differential 4-channel	**CD4052B**	16
Single 8-channel	**CD4051B**	16
Differential 8-channel	**CD4097B**	24
Single 16-channel	**CD4067B**	24
Quad bilateral switch	**CD4016B**	14
	CD4016A	14
Quad bilateral switch	**CD4066B**	14
	CD4066A	14
Digital (Data Selectors)		
Quad AND/OR select	**CD4019B**	16
4-bit AND/OR Selector Quad 2-Channel Data Selector	**CD4519B**	16
Dual 1-of-4 decoder/demultiplexer (outputs high)	**CD4555B**	16
Dual 1-of-4 decoder/demultiplexer (outputs low)	**CD4556B**	16
Quad 2-line-to-1-line	**CD40257B**	16
8-channel	**CD4512B**	16
Analog (Data Selector) Dual 4-channel	**CD4529B**	16

Function	Type No.	No. of Pins
Phase-Locked Loop		
Micropower	**CD4046B**	16
	CD4046A	16
Arithmetic Circuits		
Adders/Comparators		
4-bit full adder with parallel carry out	**CD4008B**	16
NBCD adder with 4 sum outputs, plus carry out	**CD4560B**	16
Triple serial adder, positive logic	**CD4032B**	16
Triple serial adder, negative logic	**CD4038B**	16
4-bit magnitude comparator	**CD4063B**	16
	CD4585B	16
Quad exclusive-OR gate	**CD4030B**	14
	CD4070B	14
Quad exclusive-NOR gate	**CD4077B**	14
	CD4519B	16
ALU/Rate Multipliers		
4-bit arithmetic logic unit	**CD40181B**	24
	CD4057A	28
BCD rate multiplier	**CD4527B**	16
Binary rate multiplier	**CD4089B**	16
Look-ahead-carry block	**CD40182B**	16
Parity Generator/Checker		
9-bit	**CD40101B**	14
Multiport Register		
4 x 4	**CD40108B**	24
4 x 4	**CD40208B**	24
8 x 1	**CD4034B**	24
8 x 1	**CD4034A**	24
Quad Bilateral Switches		
For transmission or multiplexing of analog or digital signals	**CD4016B**	14
	CD4016A	14
	CD4066B	14
	CD4066A	14

▽ Indicates types designed for special applications. Ratings and characteristics data for these types differ in some aspects from the standardized data for A- and B-series types. Refer to data pages on these types for specific differences.

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CD54/74HC/HCT-Series High-Speed CMOS Logic ICs

The RCA HC/HCT series of high-speed CMOS logic integrated circuits include an extensive line of products that are pin compatible with many existing bipolar 54/74 LSTTL and CMOS 4000 series of digital logic types. The new HC/HCT series ICs provide high-speed CMOS replacements for the most popular LSTTL devices in existing designs and also offer low-power all-CMOS designs for new digital systems.

For information on RCA high-speed CMOS products, refer to "QMOS Product Line" brochure, HSC-220A; to the RCA technical data sheets on specific types; or to the RCA DATABOOK "High-Speed CMOS Logic ICs", SSD-290C. A general information "QMOS" brochure, QAB-500, and a "QMOS Reliability" brochure, QRB-510, are also available.

CMOS Logic		TTL Logic		Description	No. of Pins
Plastic Pkg.	CERDIP	Plastic Pkg.	CERDIP		
CD74HC00E, M	CD54HC00F	CD74HCT00E, M	CD54HCT00F	Quad 2-Input NAND Gate	14
CD74HC02E, M	CD54HC02F	CD74HCT02E, M	CD54HCT02F	Quad 2-Input NOR Gate	14
CD74HC03E, M	CD54HC03F	CD74HCT03E, M	CD54HCT03F	Quad 2-Input NAND Gate with Open Drain	14
•CD74HC04E, M	•CD54HC04F	CD74HCT04E, M	CD54HCT04F	Hex Inverter/Buffer	14
CD74HC08E, M	CD54HC08F	CD74HCT08E, M	CD54HCT08F	Quad 2-Input AND Gate	14

•CD54/74HCU04, unbuffered version also available.

RCA Products

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CD54/74HC/HCT-Series High-Speed CMOS Logic ICs (Cont'd)

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CMOS Logic		TTL Logic		Description	No. of Pins
Plastic Pkg.	CERDIP	Plastic Pkg.	CERDIP		
CD74HC10E, M	CD54HC10F	CD74HCT10E, M	CD54HCT10F	Triple 3-Input NAND Gate	14
CD74HC11E, M	CD54HC11F	CD74HCT11E, M	CD54HCT11F	Triple 3-Input AND Gate	14
CD74HC14E, M	CD54HC14F	CD74HCT14E, M	CD54HCT14F	Hex Inverting Schmitt Trigger	14
CD74HC20E, M	CD54HC20F	CD74HCT20E, M	CD54HCT20F	Dual 4-Input NAND Gate	14
CD74HC21E, M	CD54HC21F	CD74HCT21E, M	CD54HCT21F	Dual 4-Input AND Gate	14
CD74HC27E, M	CD54HC27F	CD74HCT27E, M	CD54HCT27F	Triple 3-Input NOR Gate	14
CD74HC30E, M	CD54HC30F	CD74HCT30E, M	CD54HCT30F	8-Input NAND Gate	14
CD74HC32E, M	CD54HC32F	CD74HCT32E, M	CD54HCT32F	Quad 2-Input OR Gate	14
CD74HC42E, M	CD54HC42F	CD74HCT42E, M	CD54HCT42F	BCD-to-Decimal Decoder (1-to-10)	16
CD74HC73E, M	CD54HC73F	CD74HCT73E, M	CD54HCT73F	Dual J-K Flip-Flop w/RESET	14
CD74HC74E, M	CD54HC74F	CD74HCT74E, M	CD54HCT74F	Dual D Flip-Flop w/SET and RESET	14
CD74HC75E, M	CD54HC75F	CD74HCT75E, M	CD54HCT75F	Dual 2-Bit Bistable Transparent Latch	16
CD74HC85E, M	CD54HC85F	CD74HCT85E, M	CD54HCT85F	4-Bit Magnitude Comparator	16
CD74HC86E, M	CD54HC86F	CD74HCT86E, M	CD54HCT86F	Quad 2-Input EXCLUSIVE-OR Gate	14
CD74HC93E, M	CD54HC93F	CD74HCT93E, M	CD54HCT93F	4-Bit Binary Ripple Counter	14
CD74HC107E, M	CD54HC107F	CD74HCT107E, M	CD54HCT107F	Dual J-K Flip-Flop w/RESET	14
CD74HC109E, M	CD54HC109F	CD74HCT109E, M	CD54HCT109F	Dual J-K Flip-Flop w/SET and RESET, Positive Edge Trigger	16
CD74HC112E, M	CD54HC112F	CD74HCT112E, M	CD54HCT112F	Dual J-K Flip-Flop w/SET and RESET, Negative Edge Trigger	16
CD74HC123E, M	CD54HC123F	CD74HCT123E, M	CD54HCT123F	Dual Retriggerable Monostable Multivibrator w/RESET	16
CD74HC125E, M	CD54HC125F	CD74HCT125E, M	CD54HCT125F	Quad 3-State Buffer	14
CD74HC126E, M	CD54HC126F	CD74HCT126E, M	CD54HCT126F	Quad 3-State Buffer	14
CD74HC132E, M	CD54HC132F	CD74HCT132E, M	CD54HCT132F	Quad 2-Input NAND Schmitt Trigger	14
CD74HC137E, M	CD54HC137F	CD74HCT137E, M	CD54HCT137F	3-to-8 Line Decoder w/Latch, Inverting	16
CD74HC138E, M	CD54HC138F	CD74HCT138E, M	CD54HCT138F	3-to-8 Line Decoder/Demultiplexer, Inverting	16
CD74HC139E, M	CD54HC139F	CD74HCT139E, M	CD54HCT139F	Dual 2-of-4 Line Decoder/Demultiplexer	16
CD74HC147E, M	CD54HC147F	CD54HC147E, M	CD54HCT147F	10-to-4 Line-Priority Encoder	16
CD74HC151E, M	CD54HC151F	CD74HCT151E, M	CD54HCT151F	8-Input Multiplexer	16
CD74HC153E, M	CD54HC153F	CD74HCT153E, M	CD54HCT153F	Dual 4-Input Multiplexer	16
CD74HC154E, M, EN	CD54HC154F	CD74HCT154E, M	CD54HCT154F	4-to-16 Line Decoder/Demultiplexer	24
CD74HC157E, M	CD54HC157F	CD74HCT157E, M	CD54HCT157F	Quad 2-Input Multiplexer, Non-Inverting	16
CD74HC158E, M	CD54HC158F	CD74HCT158E, M	CD54HCT158F	Quad 2-Input Multiplexer, Inverting	16
CD74HC160E, M	CD54HC160F	CD74HCT160E, M	CD54HCT160F	Synchronous BCD Decade Counter, Asynchronous Reset	16
CD74HC161E, M	CD54HC161F	CD74HCT161E, M	CD54HCT161F	Synchronous 4-Bit Binary Counter, Asynchronous Reset	16
CD74HC162E, M	CD54HC162F	CD74HCT162E, M	CD54HCT162F	Synchronous BCD Decade Counter, Synchronous Reset	16
CD74HC163E, M	CD54HC163F	CD74HCT163E, M	CD54HCT163F	Synchronous 4-Bit Binary Counter, Synchronous Reset	16
CD74HC164E, M	CD54HC164F	CD74HCT164E, M	CD54HCT164F	8-Bit Serial-In Parallel-Out Shift Register	14
CD74HC165E, M	CD54HC165F	CD74HCT165E, M	CD54HCT165F	8-Bit Parallel-In Serial-Out Shift Register	16
CD74HC166E, M	CD54HC166F	CD74HCT166E, M	CD54HCT166F	8-Bit Parallel-In Serial-Out Shift Register	16
CD74HC173E, M	CD54HC173F	CD74HCT173F, M	CD54HCT173F	Quad D-Type Flip-Flop, 3-State, Positive Edge Triggered	16
CD74HC174E, M	CD54HC174F	CD74HCT174E, M	CD54HCT174F	Hex D-Type Flip-Flop w/RESET	16
CD74HC175E, M	CD54HC175F	CD74HCT175E, M	CD54HCT175F	Quad D-Type Flip-Flop w/RESET	16
CD74HC181E, M, EN	CD54HC181F	CD74HCT181E, M	CD54HCT181F	4-Bit Arithmetic Logic Unit	24
CD74HC182E, M	CD54HC182F	CD74HCT182E, M	CD54HCT182F	Look-Ahead Carry Generator	16
CD74HC190E, M	CD54HC190F	CD74HCT190E, M	CD54HCT190F	Presettable Synchronous BCD Decade Up/Down Counter	16
CD74HC191E, M	CD54HC191F	CD74HCT191E, M	CD54HCT191F	Synchronous 4-Bit Binary Up/Down Counter	16
CD74HC192E, M	CD54HC192F	CD74HCT192E, M	CD54HCT192F	Presettable Synchronous 4-Bit BCD Decade Up/Down Counter	16
CD74HC193E, M	CD54HC193F	CD74HCT193E, M	CD54HCT193F	Presettable Synchronous 4-Bit Binary Up/Down Counter	16
CD74HC194E, M	CD54HC194F	CD74HCT194E, M	CD54HCT194F	4-Bit Bidirectional Universal Shift Register	16
CD74HC195E, M	CD54HC195F	CD74HCT195E, M	CD54HCT195F	4-Bit Parallel Access Shift Register	16
CD74HC221E, M	CD54HC221F	CD74HCT221E, M	CD54HCT221F	Dual Monostable Multivibrator w/RESET	16
CD74HC237E, M	CD54HC237F	CD74HCT237F, M	CD54HCT237F	3-to-8 Line Decoder/Demultiplexer w/Address Latches	16
CD74HC238E, M	CD54HC238F	CD74HCT238E, M	CD54HCT238F	3-to-8 Line Decoder/Demultiplexer, Inverting and Non-Inverting	16
CD74HC240E, M	CD54HC240F	CD74HCT240E, M	CD54HCT240F	Octal Buffer Line Driver, 3-State, Inverting	20
CD74HC241E, M	CD54HC241F	CD74HCT241E, M	CD54HCT241F	Octal Buffer Line Driver, 3-State, Non-Inverting	20
CD74HC242E, M	CD54HC242F	CD74HCT242E, M	CD54HCT242F	Quad-Bus Transceiver, 3-State, Inverting and Non-Inverting	14
CD74HC243E, M	CD54HC243F	CD74HCT243E, M	CD54HCT243F	Quad-Bus Transceiver, 3-State, Non-Inverting	14
CD74HC244E, M	CD54HC244F	CD74HCT244E, M	CD54HCT244F	Octal-Buffer Line Driver, 3-State	20
CD74HC245E, M	CD54HC245F	CD74HCT245E, M	CD54HCT245F	Octal-Bus Transceiver, 3-State, Non-Inverting	20
CD74HC251E, M	CD54HC251F	CD74HCT251E, M	CD54HCT251F	8-Input Multiplexer, 3-State	16
CD74HC253E, M	CD54HC253F	CD74HCT253E, M	CD54HCT253F	Dual 4-Input Multiplexer, 3-State	16
CD74HC257E, M	CD54HC257F	CD74HCT257E, M	CD54HCT257F	Quad 2-Input Multiplexer, 3-State, Non-Inverting Outputs	16
CD74HC258E, M	CD54HC258F	CD74HCT258E, M	CD54HCT258F	Quad 2-Input Multiplexer, 3-State, Inverting Outputs	16
CD74HC259E, M	CD54HC259F	CD74HCT259E, M	CD54HCT259F	8-Bit Addressable Latch	16
CD74HC273E, M	CD54HC273F	CD74HCT273 E, M	CD54HCT273F	Octal D-Type Flip-Flop w/RESET	20
CD74HC280E, M	CD54HC280F	CD74HCT280E, M	CD54HCT280F	9-Bit Odd/Even Parity Generator/Checker	14
CD74HC283E, M	CD54HC283F	CD74HCT283E, M	CD54HCT283F	4-Bit Full Adder w/Fast Carry	16
CD74HC297E, M	CD54HC297F	CD74HCT297E, M	CD54HCT297F	Digital Phase-Locked Loop Filter	16
CD74HC299E, M	CD54HC299F	CD74HCT299E, M	CD54HCT299F	8-Bit Universal Shift Register, 3-State	20
CD74HC354E, M	CD54HC354F	CD74HCT354E, M	CD54HCT354F	8-Input Multiplexer/Register, 3-State●	20
CD74HC356E, M	CD54HC356F	CD74HCT356E, M	CD54HCT356F	8-Input Multiplexer/Register, 3-StateΔ	20

●Transparent data and select latches
ΔEdge-triggered data flip-flops, transparent select latches.

For other Harris Semiconductor Products, see pages 2715 thru 2775.

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CD54/74HC/HCT-Series High-Speed CMOS Logic ICs (Cont'd)

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CMOS Logic		TTL Logic		Description	No. of Pins
Plastic Pkg.	CERDIP	Plastic Pkg.	CERDIP		
CD74HC365E, M	CD54HC365F	CD74HCT365E, M	CD54HCT365F	Hex Buffer/Line Driver, 3-State, Non-Inverting	16
CD74HC366E, M	CD54HC366F	CD74HCT366E, M	CD54HCT366F	Hex Buffer/Line Driver, 3-State, Inverting	16
CD74HC367E, M	CD54HC367F	CD74HCT367E, M	CD54HCT367F	Hex Buffer/Line Driver, 3-State, Non-Inverting	16
CD74HC368E, M	CD54HC368F	CD74HCT368E, M	CD54HCT368F	Hex Buffer/Line Driver, 3-State, Inverting	16
CD74HC373E, M	CD54HC373F	CD74HCT373E, M	CD54HCT373F	Octal Transparent Latch, 3-State	20
CD74HC374E, M	CD54HC374F	CD74HCT374E, M	CD54HCT374F	Octal D Flip-Flop, 3 State	20
CD74HC377E, M	CD54HC377F	CD74HCT377E, M	CD54HCT377F	Octal D-Type Flip-Flop with Data Enable	20
CD74HC390E, M	CD54HC390F	CD74HCT390E, M	CD54HCT390F	Dual Decade Ripple Counter	16
CD74HC393E, M	CD54HC393F	CD74HCT393E, M	CD54HCT393F	Dual 4-Bit Binary Ripple Counter	14
CD74HC423E, M	CD54HC423F	CD74HCT423E, M	CD54HCT423F	Dual Retriggerable Monostable Multivibrator with Reset	16
CD74HC533E, M	CD54HC533F	CD74HCT533E, M	CD54HCT533F	Octal Transparent Latch, 3-State, Inverting	20
CD74HC534E, M	CD54HC534F	CD74HCT534E, M	CD54HCT534F	Octal D Flip-Flop, 3-State, Inverting	20
CD74HC540E, M	CD54HC540F	CD74HCT540E, M	CD54HCT540F	Octal Buffer Line Driver, 3-State, Inverting	20
CD74HC541E, M	CD54HC541F	CD74HCT541E, M	CD54HCT541F	Octal Buffer Line Driver, 3-State	20
CD74HC563E, M	CD54HC563F	CD74HCT563E, M	CD54HCT563F	Octal Transparent Latch, 3-State, Inverting	20
CD74HC564E, M	CD54HC564F	CD74HCT564E, M	CD54HCT564F	Octal D Flip-Flop, 3-State, Inverting	20
CD74HC573E, M	CD54HC573F	CD74HCT573E, M	CD54HCT573F	Octal Transparent Latch, 3-State	20
CD74HC574E, M	CD54HC574F	CD74HCT574E, M	CD54HCT574F	Octal D Flip-Flop, 3-State	20
CD74HC583E, M	CD54HC583F	CD74HCT583E, M	CD54HCT583F	4-Bit BCD Full Adder w/Fast Carry	16
CD74HC597E, M	CD54HC597F	CD74HCT597E, M	CD54HCT597F	8-Bit Shift Register with Input Storage	16
CD74HC640E, M	CD54HC640F	CD74HCT640E, M	CD54HCT640F	Octal Bus Transceiver, 3-State, Inverting	20
CD74HC643E, M	CD54HC643F	CD74HCT643E, M	CD54HCT643F	Octal Bus Transceiver, 3-State, True/Inverting	20
CD74HC646E, M, EN	CD54HC646F	CD74HCT646E, M	CD54HCT646F	Octal Bus Transceiver/Register, 3-State	24
CD74HC647EN, M	CD54HC647F	CD74HCT647EN, M	CD54HCT647F	Octal Bus Transceiver/Register, 3-State, with Open-Drain, Non-Inverting	24
CD74HC648E, M, EN	CD54HC648F	CD74HCT648E, M	CD54HCT648F	Octal Bus Transceiver/Register, 3-State, Inverting	24
CD74HC649EN, M	CD54HC649F	CD74HCT649EN, M	CD54HCT649F	Octal Bus Transceiver/Register, 3-State, Inverting, with Open-Drain	24
CD74HC651EN, M	CD54HC651F	CD74HCT651EN, M	CD54HCT651F	Octal Bus Transceiver/Register. 3-State, Inverting	24
CD74HC652EN, M	CD54HC652F	CD74HCT652EN, M	CD54HCT652F	Octal Bus Transceiver/Register, 3-State, Non-Inverting	24
CD74HC653EN, M	CD54HC653F	CD74HCT653EN, M	CD54HCT653F	Octal Bus Transceiver/Register, Open Drain (A Side), 3-State (B Side), Inverting	24
CD74HC654EN, M	CD54HC654F	CD74HCT654EN, M	CD54HCT654F	Octal Bus Transceiver/Register, Open Drain (A Side), 3-State (B Side), Non-Inverting	24
CD74HC670E, M	CD54HC670F	CD74HCT670E, M	CD54HCT670F	4 x 4 Register File, 3-State	16
CD74HC688E, M	CD54HC688F	CD74HCT688E, M	CD54HCT688F	8-Bit Magnitude Comparator	20
CD74HC4002E, M	CD54HC4002F	CD74HCT4002E, M	CD4HCT4002F	Dual 4-Input NOR Gate	14
CD74HC4015E, M	CD54HC4015F	CD74HCT4015E, M	CD54HCT4015F	Dual 4-Stage Static Shift Register	16
CD74HC4016E, M	CD54HC4016F	CD74HCT4016E, M	CD54HCT4016F	Quad Bilateral Switch	14
CD74HC4017E, M	CD54HC4017F	CD74HCT4017E, M	CD54HCT4017F	Decade Counter/Divider with 10 Decoded Outputs	16
CD74HC4020E, M	CD54HC4020F	CD74HCT4020E, M	CD54HCT4020F	14-Stage Binary Ripple Counter	16
CD74HC4024E, M	CD54HC4024F	CD74HCT4024E, M	CD54HCT4024F	7-Stage Binary Ripple Counter	16
CD74HC4040E, M	CD54HC4040F	CD74HCT4040E, M	CD54HCT4040F	12-Bit Binary Counter	16
CD74HC4046AE, M	CD54HC4046AF	CD74HCT4046AE, M	CD54HCT4046AF	Phase-Locked Loop with VCO	16
CD74HC4049E, M	CD54HC0409AF	—	—	Hex Inverting HIGH-to-LOW Level Shifter	16
CD74HC4050E, M	CD54HC4050F	—	—	Hex HIGH-to-LOW Level Shifter	16
CD74HC4051E, M	CD54HC4051F	CD74HCT4051E, M	CD54HCT4051F	8-Channel Analog Multiplexer/Demultiplexer	16
CD74HC4052E, M	CD54HC4052F	CD74HCT4052E, M	CD54HCT4052F	Dual 4-Channel Analog Multiplexer/Demultiplexer	16
CD74HC4053E, M	CD54HC4053F	CD74HCT4053E, M	CD54HCT4053F	Triple 2-Channel Analog Multiplexer/Demultiplexer	16
CD74HC4059E, M, EN	CD54HC4059F	CD74HCT4059E, M	CD54HCT4059F	Programmable Divide by "N" Counter	24
CD74HC4060E, M	CD54HC4060F	CD74HCT4060E, M	CD54HCT4060F	14-Stage Binary Counter w/Oscillator	16
CD74HC4066E, M	CD54HC4066F	CD74HCT4066E, M	CD54HCT4066F	Quad Bilateral Switch	14
CD74HC4067E, M, EN	CD54HC4067F	CD74HCT4067E, M	CD54HCT4067F	16-Channel Analog Multiplexer/Demultiplexer	24
CD74HC4075E, M	CD54HC4075F	CD74HCT4075E, M	CD54HCT4075F	Triple 3-Input OR Gate	14
CD74HC4094E, M	CD54HC4094F	CD74HCT4094E, M	CD54HCT4094F	8-Stage Shift-and-Store Bus Register	16
CD74HC4316E, M	CD54HC4316F	CD74HCT4316E, M	CD54HCT4316F	Quad Analog Switch, Multiplexer/Demultiplexer	16
CD74HC4351E, M	CD54HC4351F	CD74HCT4351E, M	CD54HCT4351F	8-Channel Analog MUX/DEMUX w/Latch	20
CD74HC4352E, M	CD54HC4352F	CD74HCT4352E, M	CD54HCT4352F	Dual 4-Channel Analog MUX/DEMUX w/Latch	20
CD74HC4353E, M	CD54HC4353F	CD74HCT4353E, M	CD54HCT4353F	Triple 2-Channel Analog MUX/DEMUX w/Latch	20
CD74HC4510E, M	CD54HC4510F	CD74HCT4510E, M	CD54HCT4510F	Presettable Sync. 4-Bit, Up/Down Counter, BCD	16
CD74HC4511E, M	CD54HC4511F	CD74HCT4511E, M	CD54HCT4511F	BCD-to-7-Segment Latch/Decoder/Driver	16
CD74HC4514E, M, EN	CD54HC4514F	CD74HCT4514E, M	CD54HCT4514F	4-to-16 Line Deocoder/Demultiplexer w/Input Latch	24
CD74HC4515E, M, EN	CD54HC4515F	CD74HCT4515E, M	CD54HCT4515F	4-to-16-Line Decoder with Input Latches	24
CD74HC4516E, M	CD54HC4516F	CD74HCT4516E, M	CD54HCT4516F	Presettable Sync. 4-Bit, Up/Down Counter, Binary	16
CD74HC4518E, M	CD54HC4518F	CD74HCT4518E, M	CD54HCT4518F	Dual 4-Bit Synchronous BCD Counter	16
CD74HC4520E, M	CD54HC4520F	CD74HCT4520E, M	CD54HCT4520F	Dual 4-Bit Synchronous Binary Counter	16
CD74HC4538E, M	CD54HC4538F	CD74HCT4538E, M	CD54HCT4538F	Dual Precision Monostable Multivibrator	16
CD74HC4543E, M	CD54HC4543F	CD74HCT4543E, M	CD54HCT4543F	BCD-to-7-Segment Latch/Decoder/Driver for LCDs	16
CD74HC7030E	—	CD74HCT7030E	—	9-Bit x 64 Word FIFO Register, 3-State	28
CD74HC7038E, M, EN	CD54HC7038F	CD74HCT038E, M	CD54HCT7038F	9-Bit Bus Transceiver w/Latch	24

For other Harris Semiconductor Products, see pages 2715 thru 2775.

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CD54/74HC/HCT Series High-Speed CMOS Logic ICs (Cont'd)

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CMOS Logic		TTL Logic		Description	No. of Pins
Plastic Pkg.	CERDIP	Plastic Pkg.	CERDIP		
CD74HC7046E, M	CD54HC7046F	CD74HCT7046E, M	CD54HCT7046F	Phase-Locked Loop with VCO and In-Lock Detector	16
CD74HC7266E, M	CD54HC7266F	—	—	Quad Exclusive NOR Gate	14
CD74HC40102E, M	CD54HC40102F	CD74HCT40102E, M	CD54HCT40102F	8-Bit Synchronous 2-Decade BCD Down Counter	16
CD74HC40103E, M	CD54HC40103F	CD74HCT40103E, M	CD54HCT40103F	8-Bit Synchronous Binary Down Counter	16
CD74HC40104E, M	CD54HC40104F	CD74HCT40104E, M	CD54HCT40104F	4-Bit Bidirectional Universal Shift Register, 3-State	16
CD74HC40105E, M	CD54HC40105F	CD74HCT40105E, M	CD54HCT40105F	4 Bits x 16 Words FIFO Register	16
CD74HCUO4E, M	CD54HCU04F	—	—	Hex Inverter (Unbuffered)	14

Note: Add package suffix code to part number on all orders.
E or EN = Dual-In-Line Plastic Package — Temp. Range = -40° to +125°C.
F = Dual-In-Line Frit-Seal Ceramic Package (CERDIP) — Temp. Range = -55° to +125°C.
H = Chip — Temp. Range = -55° to +125°C.
M = Dual-In-Line Surface-Mounted Package — Temp. Range = -40° to +125°C.

CD54/74AC/ACT Series Advanced CMOS Logic ICs

The RCA AC/ACT series of Advanced CMOS Logic ICs include a broad line of products that match bipolar FAST* products in speed, performance, and logic-type output drive, but at CMOS power levels. This product line consists of CD54/74AC-series types, which feature CMOS input-voltage-level compatibility, and CD54/74ACT-series types, which are input-voltage-level-compatible with LSTTL devices.

For information on Advanced CMOS Logic ICs, refer to the product brochure "RCA Advanced CMOS Logic ICs," ACL-285B, to the technical data sheets on specific types; and to the DATABOOK "RCA Advanced CMOS Logic ICs," SSD-283A.

*FAST is a registered trademark of Fairchild Semiconductor Corp.

GE/RCA Solid State

AC/ACT Type (For High-Reliability Versions, See Footnote*)		Description	No. of Pins	Data Bulletin File No.
Dual In-Line Plastic Pkg.	Small-Outline Plastic Pkg.			
CD74AC/ACT00E	CD54AC/ACT00M	Quad 2-Input NAND Gate	14	1855
CD74AC/ACT02E	CD54AC/ACT02M	Quad 2-Input NOR Gate	14	1978
CD74AC/ACT04E	CD54AC/ACTT04M	Hex Inverter/Buffer	14	1945
CD74AC/ACT05E	CD54AC/ACT05M	Hex Inverter/Buffer with Open-Drain Outputs	14	1945
CD74AC/ACT08E	CD54AC/ACT08M	Quad 2-Input AND Gate	14	1950
CD74AC/ACT10E	CD54AC/ACT10M	Triple 3-Input NAND Gate	14	1977
CD74AC/ACT14E	CD54AC/ACT14M	Hex Inverting Schmitt Trigger	14	1984
CD74AC/ACT20E	CD54AC/ACT20M	Dual 4-Input NAND Gate	14	1976
CD74AC/ACT32E	CD54AC/ACT32M	Quad 2-Input OR Gate	14	1951
CD74AC/ACT74E	CD45AC/ACT74M	Dual D Flip-Flop w/Set and Reset	14	1881
CD74AC/ACT86E	CD54AC/ACT86M	Quad 2-Input Exclusive-OR Gate	14	1952
CD74AC/ACT109E	CD54AC/ACT109M	Dual J-K Flip-Flop w/Set and Reset, Positive Edge Trigger	16	1967
CD74AC/ACT112E	CD54AC/ACT112M	Dual J-K Flip-Flop w/Set and Reset, Negative Edge Trigger	16	1967
CD74AC/ACT138E	CD54AC/ACT138M	3-to-8 Line Decoder/Demultiplexer, Inverting	16	1909
CD74AC/ACT139E	CD54AC/ACT139M	Dual 2-to-4 Line Decoder/Demultiplexer	16	1953
CD74AC/ACT151E	CD54AC/ACT151M	8-Input Multiplexer	16	1980
CD74AC/ACT153E	CD54AC/ACT153M	Dual 4-Input Multiplexer	16	1966
CD74AC/ACT157E	CD54AC/ACT157M	Quad 2-Input Multiplexer	16	1910
CD74AC/ACT158E	CD54AC/ACT158M	Quad 2-Input Multiplexer, Inverting	16	1910
CD74AC/ACT161E	CD54AC/ACT161M	Synchronous 4-Bit Binary Counter, Asynchronous Reset	16	1959
CD74AC/ACT163E	CD54AC/ACT163M	Synchronous 4-Bit Binary Counter, Synchronous Reset	16	1959
CD74AC/ACT164E	CD54AC/ACT164M	8-Bit Serial-In Parallel-Out Shift Register	14	1954
CD74AC/ACT174E	CD54AC/ACT174M	Hex D-Type Flip-Flop w/Reset	16	1973
CD74AC/ACT175E	CD54AC/ACT175M	Quad D-Type Flip-Flop w/Reset	16	1964
CD74AC/ACT191E	CD54AC/ACT191M	†Synchronous 4-Bit Binary Up/Down Counter	16	1911
CD74AC/ACT193E	CD54AC/ACT193M	†Synchronous 4-Bit Binary Up/Down Counter w/Reset	16	1947
CD74AC/ACT238E	CD54AC/ACT238M	3-to-8 Line Decoder/Demultiplexer	16	1909
CD74AC/ACT240E	CD54AC/ACT240M	Octal Buffer Line Driver, 3-State, Inverting	20	1856
CD74AC/ACT241E	CD54AC/ACT241M	Octal Buffer Line Driver, 3-State, Non-Inverting	20	1856
CD74AC/ACT244E	CD54AC/ACT244M	Octal Buffer Line Driver, 3-State, Non-Inverting	20	1856
CD74AC/ACT245E	CD54AC/ACT245M	Octal Bus Transceiver, 3-State	20	1907
CD74AC/ACT251E	CD54AC/ACT251M	8-Input Multiplexer, 3-State	16	1981
CD74AC/ACT253E	CD54AC/ACT253M	Dual 4-Input Multiplexer, 3-State	16	1985
CD74AC/ACT257E	CD54AC/ACT257M	Quad 2-Input Multiplexer, 3-State, Non-Inverting	16	1955
CD74AC/ACT258E	CD54AC/ACT258M	Quad 2-Input Multiplexer, 3-State, Inverting	16	1955

For other Harris Semiconductor Products, see pages 2715 thru 2775.

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CD54/74AC/ACT Series Advanced CMOS Logic ICs (Cont'd)

HARRIS SEMICONDUCTOR
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AC/ACT Type (For High-Reliability Versions, See Footnote*)		Description	No. of Pins	Data Bulletin File No.
Dual In-Line Plastic Pkg.	Small-Outline Plastic Pkg.			
CD74AC/ACT273E	CD54AC/ACT273M	Octal D-Type Flip-Flop w/Reset	20	1979
CD74AC/ACT280E	CD54AC/ACT280M	9-Bit Odd/Even Parity Generator/Checker	14	1957
CD74AC/ACT283E	CD54AC/ACT283M	4-Bit Full Adder w/Fast Carry	16	1912
CD74AC/ACT297E	CD54AC/ACT297M	Digital Phase-Locked-Loop Filter	16	—
CD74AC/ACT299E	CD54AC/ACT299M	8-Bit Universal Shift Register, 3-State, Asynchronous Reset	20	1958
CD74AC/ACT323E	CD54AC/ACT323M	8-Bit Universal Shift Register, 3-State, With Synchronous Reset	20	1958
CD74AC/ACT373E	CD54AC/ACT373M	Octal Transparent Latch, 3-State	20	1882
CD74AC/ACT374E	CD54AC/ACT374M	Octal D-Type Flip-Flop, 3-State	20	1883
CD74AC/ACT533E	CD54AC/ACT533M	Octal Transparent Latch, 3-State, Inverting	20	1882
CD74AC/ACT534E	CD54AC/ACT534M	Octal D-Type Flip-Flop, 3-State, Inverting	20	1883
CD74AC/ACT540E	CD54AC/ACT540M	Octal Buffer Line Driver, 3-State, Inverting	20	1857
CD74AC/ACT541E	CD54AC/ACT541M	Octal Buffer Line Driver, 3-State, Non-Inverting	20	1857
CD74AC/ACT563E	CD54AC/ACT563M	Octal Transparent Latch, 3-State, Inverting	20	1956
CD74AC/ACT564E	CD54AC/ACT564M	Octal D-Type Flip-Flop, 3-State, Inverting	20	1948
CD74AC/ACT573E	CD74AC/ACT573M	Octal Transparent Latch, 3-State, Non-Inverting	20	1956
CD74AC/ACT574E	CD74AC/ACT574M	Octal D-Type Flip-Flop, 3-State	20	1948
CD74AC/ACT623E	CD54AC/ACT623M	Octal Bus Transceiver, 3-State, Non-Inverting	20	1968
CD74AC/ACT646EN	CD54AC/ACT646M	Octal Bus Transceiver/Register, 3-State	24	1970
CD74AC/ACT647EN	CD54AC/ACT647M	Octal Bus Transceiver/Register, 3-State, with Open-Drain, Non-Inverting	24	1982
CD74AC/ACT648EN	CD54AC/ACT648M	Octal Bus Transceiver/Register, 3-State, Inverting	24	1970
CD74AC/ACT649EN	CD54AC/ACT649M	Octal Bus Transceiver/Register, 3-State, Inverting with Open-Drain	24	1982
CD74AC/ACT651EN	CD54AC/ACT651M	Octal Bus Transceiver/Register, 3-State, Inverting	24	1974
CD74AC/ACT652EN	CD54AC/ACT652M	Octal Bus Transceiver/Register, 3-State, Non-Inverting	24	1974
CD74AC/ACT653EN	CD54AC/ACT653M	Octal Bus Transceiver/Register, Open Drain (A Side), 3-State (B Side), Inverting	24	1975
CD74AC/ACT654EN	CD54AC/ACT654M	Octal Bus Transceiver/Register, Open Drain (A Side), 3-State (B-Side), Non-Inverting	24	1975
CD74AC/ACT7060E	CD54AC/ACT7060M	14-Stage Binary Counter with Oscillator	20	2062
CD74AC/ACT7061E	CD54AC/ACT7061M	14-Stage Binary Counter with Oscillator (Reset will not disable oscillator)	20	—
CD74AC/ACT7201E	CD54AC/ACT7201M	512 x 9-Bit Parallel In-Out FIFO	28	1983
CD74AC/ACT7202E	CD54AC/ACT7202M	1024 x 9-Bit Parallel In-Out FIFO	28	1983
CD74AC/ACT7623E	CD54AC/ACT7623M	Octal Bus Transceiver, 3-State (B Side), Open Drain (A Side), Non-Inverting	20	1969

*High-reliability versions of these AC/ACT types are available in dual-in-line frit-seal ceramic (CERDIP) packages ("F" suffix) and are screened to class/3A (Class B MIL-STD-883 Compliant) level for military, aerospace, and critical industrial applications.

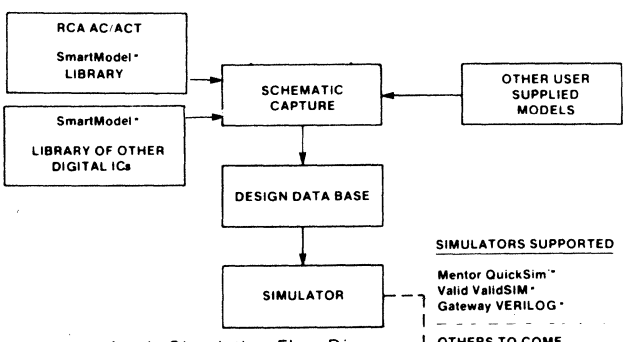
† — Presettable

Package Suffix Letters: "E", "EN" — Dual-In-Line Plastic (DIP)
"M" — Dual-In-Line Surface-Mount Plastic Small Outline (SO).

Behavioral Models of RCA AC/ACT Logic

Logic Automation Inc. provides behavioral language models, called SmartModels®, that include built-in component data on RCA AC/ACT Advanced CMOS Logic IC's to simulate complex system operation. This built-in knowledge (data information on the components and their design use) permits the system designer to perform virtually error-free design verification without system interruption.

®SmartModel is a trademark of Logic Automation, Inc.
*QuickSim is a trademark of Mentor Graphics Corp
*ValidSim is a trademark of Valid Logic Systems
*VERILOG is a trademark of Gateway Design Automation Corp



Logic Simulation Flow Diagram

For other Harris Semiconductor Products, see pages 2715 thru 2775.

RCA Products

GE/RCA Solid State

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The RCA CMOS line of microprocessor, microcomputer, memory, and peripheral integrated circuits are intended for use in a broad range of diverse industrial, consumer, and military applications.

The circuits include central-processing units (CPUs), custom and standard read-only memories (ROMs), mask-programmable read-only memories (PROMs), random-access memories (RAMs) and a wide variety of peripherals including a multiply/divide unit (MDU), programmable IUs, keyboard interface circuits, latches and decoders and UARTS.

For information on these circuits, refer to the GE Solid State DATABOOK, "CMOS Microprocessors, Peripherals, RAMs, ROMs," SSD-260C.

Part Number	Description
Microprocessors	
CDP1802A, AC	8-Bit
CDP1802BC	8-Bit
CDP1805AC	8-Bit with RAM and Counter/Timer
CDP1806AC	8-Bit with RAM and Counter/Timer
CDP6805E2, C	8-Bit with RAM, I/O, Counter/Timer
CDP6805E3, C	8-Bit with RAM, I/O, Counter/Timer
Microcomputers	
CDP1804AC	8-Bit with RAM, ROM, Counter/Timer
CDP68HC05C4	8-Bit with RAM, ROM, I/O, Counter/Timer
CDP68HC05C8	8-Bit with RAM, ROM, I/O, Counter/Timer
CDP68HC05D2	8-Bit with RAM, ROM, I/O, Counter/Timer
CDP6805F2, C	8-Bit with RAM, ROM, I/O Counter/Timer
CDP6805G2, C	8-Bit with RAM, ROM, I/O Counter/Timer
Emulators	
CDP68EM05C4	8-Bit Microcomputer Piggyback
CDP68EM05D2	8-Bit Microcomputer Piggyback
RAMs	
CDP1822, C	256 x 4
CDP1823, C	128 x 8
CDP1824, C	32 x 8
CDP1826C	64 x 8
CDM6116A	2K x 8
CDM6264	8K x 8
CDM62256	32 x 8
MWS5101	256 x 4
MWS5101A	256 x 4
MWS5114	1K x 4
CDP68HC68R1	SPI RAM 128-Bytes
CDP68HC68R2	SPI RAM 256-Bytes

Part Number	Description
Mask-Programmable ROMs	
CDM5332	4K x 8
CDM5333	4K x 8
CDM5364, A	8K x 8
CDM5365	8K x 8
CDM53128	16K x 8
CDM53256	32K x 8
CDM53256A-20	32K x 8
CDP1831, C	512 x 8
CDP1832, C	512 x 8
CDP1833, C, BC	1K x 8
CDP1834, C	1K x 8
CDP1835C	2K x 8
CDP1837C	4K x 8
Peripherals	
CDP1851, C	Programmable I/O Interface
CDP1852, C	Byte-Wide I/O Port
CDP1872C	8-Bit Input Port
CDP1874C	8-Bit Input Port
CDP1875C	8-Bit Output Port
CDP68HC68P1	8-Bit Single I/O Port
CDP6823	Parallel Interface
CDP1853, C	1 of 8 Decoder
CDP1859, C	4-Bit Bus Buffer Separator
CDP1881, C	6-Bit Latch & Decoder
CDP1882, C	6-Bit Latch & Decoder
CDP1883, C	7-Bit Latch & Decoder
CDP1854A, C	Programmable UART
CDP1857C	4-Bit Bus Buffer Separator
CDP6402, C	Programmable UART
CDP65C51-1, CDP65C51-2, CDP65C51-4	Asynchronous Communications Interface Adapter
CDP65C51A-1, CDP65C51A-2, CDP65C51A-4	Asynchronous Communications Interface Adapter
CDP6853-1, CDP6853-2, CDP6853-4	Asynchronous Communications Interface Adapter (ACIA), Motel Bus
CDP1855, C	8-Bit Programmable Multiply/Divide Unit (MDU)
CDP1871A, C	Keyboard Encoder, ASCII Hex
CDP1878, C	Dual Counter/Timer
CDP1879, C-1	Real-Time Clock
CDP6818	Real-Time Clock with RAM, Motel Bus
CDP6818A	Real-Time Clock Plus RAM
CDP68HC68S1	Serial Bus Interface Chip
CDP68HC68T1	SPI Real-Time Clock
CDP68HC68W1	Serial Digital Pulse Width Modulator
CDP1877, C	Programmable Interrupt Controller
CDP68HC68A2	SPI 10-Bit A/D Converter

For other Harris Semiconductor Products, see pages 2715 thru 2775.

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Telecommunications ICs

The RCA Telecommunications product line has the resources to meet the challenges of modern telecommunications systems. The product line of RCA offers system designers an extensive array of diverse solid-state components that may be used advantageously in a wide variety of telecommunication circuit functions.

The expanding applications of telephone terminals and transmission equipment have brought about a technological transformation from analog to digital in telecommunication equipment. Not only are people making more telephone calls, but businesses also are substantially increasing their volume of digital data transmission. This increased traffic is placing a heavy burden on existing analog telecommunications facilities. One significant way of easing this burden is the ongoing conversion of voice signals to digital format. In this format, by means of multiplexing techniques, information is compressed in both the time and the frequency domains. As a result, it is possible to increase system utilization many times while improving data integrity and analog fidelity.

RCA CMOS Single-Chip Full-Feature PCM CODECS
Complete CODEC and Filtering Systems for Telephone Systems Applications

Type No.	Description	Features					Pkg. No. of Pins
		Power Supply Range (V)	Operating Modes	Power Dissipation (Typ.) (mW)	Variable Clock Rates	Compatible Logic Interface	
CD-22352°	μ-Law CODEC like CD22354, CD22357 but meets D3/D4 channel specifications and has transmit and receive A/B signaling capabilities	4.75 to 5.25	Asynchronous or Synchronous	75	64 kHz to 2.048 MHz	TTL or CMOS	18E
CD-22354°	Provides AT&T μ-Law companding characteristic						16E
CD-22357°	Provides CCITT A-Law companding characteristic	•Adjustable gain for transmit input •Stable on-chip precision voltage reference					16E

Operating Temperature Range (T_A): -25 to +85°C
°Meets CCITT recommendations

RCA CMOS Crosspoint Switches with Control Memory

Type	Switch Array Configuration	Switch Characteristics (T_A = 25°C)					Pkg. No. of Pins
		ON Resistance (V_{DD} = 12 V)		Linearity (Distortion)•	Signal Crosstalk (Attenuation of -40 dB)	DC Supply Voltage Range°	
		ΔR_{ON}	R_{ON}				
		Ω (Typ)		% (Typ)	MHz (Typ)	(V)	
CD22100	4x4x1	18	75	0.5	1.5▲	3-18	16D, E, F
CD22101	4x4x2	8	75	0.25	2.5•	3-18	24D, E, F
CD22102	4x4x2	8	75	0.25	2.5•	3-18	24D, E, F
CD54/74 HC 22106	8x8x1	23 (V_{CC} = 9V)	40	0.12Δ	20 (75Ω)	2-10	28E, F,M
CD54/74 HCT 22106	8x8x1	25 (V_{CC} = 4.5V)	58	0.12Δ	20 (75Ω)	4.5-5.5	28E, F,M

• 600Ω, 1 V Rms, 10-V Supply
▲ 1 kΩ, 1 V Rms, 10-V Supply
Δ fis = 1kHz, R_L = 600Ω, V_{IN} = 7 V p-p, V_{CC} = 4.5 V
°T_A Range: D and F Package, -55 to +125°C
E Package, -40 to +85°C

RCA 5-Volt Low-Power DTMF Receivers

Type	Power Supply	Features					Pkg. No. of Pins
		Low Power Consumption	Detects	Type of Code	Outputs 3-State Enabled	Interface	
CD-22202•	Single, Low-Tolerance (10%) 5-Volt	50mW typ.	Either 12 or 16 Standard DTM Digits	4-Bit Hexadecimal or Binary Coded 2 of 8	To facilitate microprocessor bus-oriented architecture	(Synchronous or Handshake #) Directly to CD4000-Series and HC-Series CMOS	18E
CD-22203•			CD22203 is like the CD22202 but has early detect output on Pin 6.				18E
CD-22204•			All 16 Standard DTMF Digits	4-Bit Hexadecimal			14E

•Interchangeable with SSI types SSI 202, 203, 204 but with improved epitaxial process #CD22202 and CD22203 only.
Operating Temperature Range (T_A): 0 to +70°C

GE/RCA Solid State

RCA Products

For other Harris Semiconductor Products, see pages 2715 thru 2775.

RCA CMOS Modems

Type No.	Title	Supply Voltage Range (V)	Power Consumption Typ. (mW)	Compat-Logic Interface	Data Rate	Operating Modes	Interfaces Directly with	Pkg. No. of Pins
CD 22212E• CD 22212Q•	Single-Chip 1200 BPS Full-Duplex Bell 103/212A Compatible	9.6 to 13.2	180	TTL and CMOS	Full Duplex 0-300 BPS (FSK) and 1200 BPS (DPSK)	Asynchronous Synchronous	Standard μps (80C48 80C51 8749 typ.)	22, 28 DIP 28 PCC
CD-22223▲	1200 Baud FSK Type For European and closed systems use designed to meet CCITT V.23 signaling frequencies	4.5 to 13	2mA @ 5V		1200 Baud full or half duplex			16-DIP

•Pin and software compatible with SSIK212, K221, K222, K224 one-chip modems.
▲Interchangeable with the SSI type SSI223
Operating-Temperature Range (T_A): CD22212, -40 to +85°C, CD2223, -25 to +75°C

RCA Dual-Tone Multifrequency (DTMF) Tone Generator

Type No.	Application	Features			Pkg. No. of Pins
		DC Supply Voltage (V)	Device Power	3.58-MHz Crystal Control	
CD22859	For dual-tone telephone dialing systems	2.5 to 10■	Unregulated DC or telephone loop current	Provides high accuracy and stability for all frequences	16 D, E
		• Mute driver output on chip • Built-in pull ups on inputs			

Operating Temperature Range (T_A): -40 to +85°C
■Tone Generation mode

RCA 16-Channel Precision Timer/Driver

Type No.	Application	DC Supply Voltage (V)	Function	Pkg. No. of Pins
CD22401	Timer/Driver	5 ± 0.5	Interface circuit for critically timed output pulses for high-speed printers	40 E

For Digital Transmission Systems in Telephone Networks
RCA CMOS HDB3 (High-Density Bipolar 3) Transcoder

Type No.	Application	DC Supply Voltage Range (V)	Functions		Pkg. No. of Pins
CD22103A	For 2.048/8.448 Mb/s Transmission	4.5 to 5.5	Performs — HDB3/AMI transmission coding and reception decoding For Data Rates — from 50 kbs to 10 Mb/s consistent with CCITT G703 recommendations	With code error detection, in independent coder and decoder sections	16 D, E

RCA PCM Line Repeater

CD22301	For PCM Carrier Systems operating with 1.544 (T1) and 2.048 Mb/s bipolar pulse trains For T148 Carrier Systems operating with 2.37 Mb/s ternary pulse trains	5.1 V ± 5% externally regulated supply	• Signal equalization and amplification • Automatic line build-out (ALBO) • Threshold Detection • Pulse Timing • Clock Extraction • Buffered Output Formation	18 E

Operating Temperature Range (T_A):
CD22103A: -55 to +125°C, -40 to +85°C
CD22301: -40 to +85°C

GE/RCA Solid State

RCA Products

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RCA Operational Amplifiers

Electrical Characteristics, T_A = 25°C

Type	V_{IO} Max. mV	I_I Max. nA	I^+ Max. Ma	Max. V^+, V^-	A_{OL} (Min.) dB	Unity Gain BW Typ. MHz	SR (Typ.) V/μs	Pkg. No. of Pins
General-Purpose Types Single-Unit Types								
CA081•	15	50pA	2.8	±18	88	5	13	8E
CA081A•	6	40pA	2.8	±18	94	5	13	8E
CA101	5	0.05	2.5	±44	94	1	—	8E,S,T
CA201, LM201†	7.5	0.15	3	±44	85	1	—	8E,S, T
CA301A, LM301A†	7.5	0.025	3	±36	88	1	10	8E,S, T
CA307, LM307†	7.5	250	3	±36	88	1	—	8E,S, T
CA741, LM741†	5	500	2.8	±44	94	1	0.5	8E,S, T
CA741C, LM741C†	6	500	2.8	±36	86	1	0.5	10T, 14E
CA748, LM748†	5	500	2.8	±44	94	1	0.5	8E, S, T
CA748C, LM748C†	6	500	2.8	±35	86	1	0.5	8E, S, T
CA3193•	0.5	40	3.5	±18	100	1.2	0.25	8E,S,
CA3193A•	0.2	20	3.5	±18	110	1.2	0.25	T
CA3420•	10	5pA	0.65	±11	80	0.5*	0.5	8E,S,
CA3420A•	5	5pA	0.65	±11	86	0.5*	0.5	T
CA3440•	10	50pA	0.017	±12.5	80	63kHz	0.03	8E,S
CA3440A•	5	40pA	0.017	±12.5	80	63kHz	0.03	T
CA3450	15	350	35	±8.5	60	220	330	16E
CA3493•	0.5	40	3.5	±18	100	1.2*	0.25	8E,S,
CA3493A•	0.2	20	3.5	±18	110	1.2*	0.25	T
CA6741	Low-Noise CA741	See Note 1						
Dual-Unit Types								
CA082•	15	50pA	5.6	±18	88	5	13	8E
CA082A•	6	40pA	5.6	±18	94	5	13	8E
CA158	5	150	1.2	±13	94	1	—	8E,S,
CA158A	2	50	1.2	±13	94	1	—	T
CA258	5	150	1.2	±13	94	1	—	8E,S,
CA258A	3	80	1.2	±13	94	1	—	T
CA358, LM358†	7	250	1.2	±13	88	1	—	8E,S, T
CA358A	3	100	1.2	±13	88	1	—	8E,S,T
CA747	5	500	2.8	±44	94	1	0.5	10T,
CA747C	6	500	2.8	±36	86	1	0.5	14E
CA1458, LM1458†	6	500	2.8	±36	86	1	0.5	8E,S, T
CA1558, LM1558†	5	500	2.8	±44	94	1	0.5	8E,S, T
CA2904, LM2904†	7	250	1.2	±13	100*	1	—	8E,S, T
CA5422• Ampl A	10	5pA	0.7	±11	60	160 kHz	0.25	14E
Ampl B	20	25pA	0.7		50	800 kHz	1	
Quad-Unit Types								
CA084•	15	50pA	11.2	±18	88	5	13	14E
CA084A•	6	40pA	11.2	±18	94	5	13	14E
CA124	5	150	2	±16	94	1	—	14E
CA224	7	250	2	±16	88	1	—	14E
CA324, LM324†	7	250	2	±16	86	1	—	14E
CA3401	—	300	10	±18	60	5	0.6	14E
CA3410•	15	40	12	±18	86	5.4	10	16E
CA3410A•	8	30	10	±18	86	5.4	10	16E

Type	V_{IO} Max. mV	I_I Max. nA	I^+ Max. Ma	Max. V^+, V^-	A_{OL} (Min.) dB	Unity Gain BW Typ. MHz	SR (Typ.) V/μs	Pkg. No. of Pins
Wideband Single-Unit Types								
CA3010	5	12 μA	2.5	±8	66	16	3	12T
CA3010A	2	4 μA	3.3	±8	66	16	3	12T
CA3015	5	24 μA	7.3	±16	72	60	7	12T
CA3015A	2	6 μA	7.3	±16	72	60	7	12T
CA3029	5	12 μA	2.5	±8	60	16	3	14E
CA3029A	2	4 μA	3.5	±8	60	16	3	14E
CA3030	5	24 μA	7.3	±16	72	60	7	14E
CA3030A	2	6 μA	7.3	±16	72	60	7	14E
CA3037	5	12 μA	2.5	±8	60	16	3	14D
CA3037A	2	4 μA	3.3	±8	60	16	3	14D
CA3038	5	24 μA	7.3	±16	72	60	7	14D
CA3038A	2	6 μA	7.3	±16	72	60	7	14D
CA3100•	5	2000	10.5	±18	56	38*	70	8E,S,T
CA3130•	15	50pA	15	±8	94	15	30	8E,M,
CA3130A•	5	30pA	15	±8	94	15	30	S,T
CA3140•	15	50pA	6	±18	86	4.5*	9	8E,S,
CA3140A•	5	30pA	6	±18	86	4.5*	9	T,M
CA3160•	15	50pA	15	±8	94	4*	10	8E,S,
CA3160A•	5	30pA	15	±8	94	4*	10	T,M
CA3450▲	15	130	35	±8.5	60	220	330	16E
Wideband Dual-Unit Types								
CA3240•	15	50pA	12	±18	86	4.5*	9	8E,8T
CA3240A•	5	40pA	12	±18	86	4.5*	9	8S,14EI
CA3260•	15	50pA	15.5	±8	94	4*	10	8E,M,
CA3260A•	5	30pA	15.5	±8	94	4*	10	T,S
Wideband High-Slew Rate Types (>50 V/μs)								
CA3080	5	5000	1.2	±18	□	2#	50	8E,S,
CA3080A	2	5000	1.2	±18	□	2#	50	T
CA3100•	5	2000	10.5	±18	56	38#	70	8E,S,T
CA3280	3	5000	4.8	±18	94	9#	125	16E
CA3280A	0.5	5000	4.8	±18	94	9#	125	16E
CA3450	15	350	35	±8.5	60	220	330	16E
5-Volt BiMOS Microprocessor Types for Low-Supply Voltage, Low-Input-Current Applications°								
CA5130	10	15pA	0.4	±8	85	15	30	8E,M
CA5130A	4	10pA	0.4	±8	90	15	30	S,T
CA5160	10	15pA	0.4	±8	85	3*	8	8E,S,
CA5160A	4	10pA	0.4	±8	90	3*	8	T
CA5260	15	15pA	1.8	±8	80	3*	8	8E,M,
CA5260A	4	15pA	1.8	±8	83	3*	8	S,T
CA5420	10	2pA	0.5	±11	85	0.5	0.5	8E, S,T
CA5420A	5	1pA	0.5	±11	85	0.5	0.5	8E, S,T
CA5422 Ampl. A	10	5pA	0.7	±11	60	160 kHz	0.25	14E
Ampl. B	20	25pA	0.7		50	800 kHz	1	
OTAs (Programmable, Variable) Micropower (Single-Unit Types)								
CA3060††	5	5000	3.6	±18	100	1.5	8	16E
CA3078	4.5	32	0.13	±7	88	0.8	1.5	8E,T
CA3078A	3.5	12	0.025	±18	92	0.8	1.5	8E,T
CA3080	5	5000	1.2	±18	100	2#	50	8E,S,
CA3080A	2	5000	1.2	±18		2#	50	T

•BiMOS type * ft Δ pA # Open-Loop BW

Note: 1: "Popcorn" (Burst) Noise. Device rejected if total noise voltage (burst + 1/f) referred to input exceeds 20 μV peak during 30-second test period.

†Technical data on LM Branded Types are identical to the corresponding CA Branded Types: †† Triple unit.

GE/RCA Solid State

RCA Products

For other Harris Semiconductor Products, see pages 2715 thru 2775.

RCA Operational Amplifiers

Electrical Characteristics, T_A = 25°C

Type	V_{IO} Max. mV	I_I Max. nA	I^+ Max. Ma	Max. V^+, V^-	A_{OL} (Min.) dB	Unity Gain BW Typ. MHz	SR (Typ.) V/μs	Pkg. No. of Pins
CA3440•	10	50pA	0.017	±12.5	80	63kHz	0.03	8E,S,
CA3440A•	5	40pA	0.017	±12.5	80	63kHz	0.03	T
CA6078A	Low-noise CA3078A		"Popcorn" (Burst) Noise. Device rejected if total noise voltage (burst + off) referred to input exceeds 20 μV peak during 30-second test period.					
Dual-Unit Types								
CA3280	3	5000	4.8	±18	94	9#	125	16E
CA3280A	0.5	5000	4.8	±18	94	9#	125	16E
High-Current Types								
CA3094	5	5000	0.4	±12	86	30	50	8E, S,T
CA3094A	5	5000	0.4	±18	86	30	50	
CA3049B	5	5000	0.4	±22	86	30	50	

•BiMOS type † kHz †† Triple Unit # Open-Loop BW
°Can also operate at higher and lower voltage depending on type
T_A Range: All types -55 to 125° except CA311 (0 to +70°C)

RCA BIMOS-E Operational Amplifiers

Internal Compensation

Type	V_{IO} Max. mV	I_I Max. pA	I^+ Max. Ma	Max. V^+, V^-	A_{OL} (Min.) dB	Unity Gain BW Typ. MHz	SR (Typ.) V/μs	Pkg. No. of Pins
General-Purpose Quad-Unit Types								
CA5470■	15	10	6	±18	80	14	5	14E,M
CA5470□	18	11 nA	7	±8	80	12	5	14E,M
High-Speed Wideband Dual-Unit Types (Preliminary)								
CA5202△	3	0.1 nA	8	±8	65	50	100	8E,M 8T,S

■T_A = 25°C □T_A = -55 to +125°C △T_A = -40 to +85°C

RCA Comparators

General-Purpose Types

Electrical Characteristics, T_A = 25°C

Type	V_{IO} Max. mV	I_I Max. nA	I^+ Max. Ma	Max. V^+, V^-	A_{OL} (Min.) dB	Unity Gain BW Typ. MHz	SR (Typ.) V/μs	Pkg. No. of Pins
Single-Unit Types								
CA311	7.5	250	8	±18	106	Response Time[1]		8E,S,T
Dual-Unit Types								
CA3290	20	50pA	3	±18	88	Response Time[2]		8E,S,T
CA3290A	10	40pA	3	±18	88			14EI

RCA Comparators (Cont'd)

General-Purpose Types

Type	V_{IO} Max. mV	I_I Max. nA	I^+ Max. mA	Max. V^+, V^-	A_{OL} (Min.) dB	Unity Gain BW Typ. MHz	SR (Typ.) V/μs	Pkg. No. of Pins
Quad-Unit Types								
CA139	5	100	8	±18	—	Response Time[3]		14E
CA139A	2	100	8	±18	94			14E
CA239	5	250	2	±18	—			14E
CA239A	2	250	2	±18	94			14E
CA339	5	250	2	±18	94			14E
CA339A	2	250	2	±18	94			14E

Response Time
1 = 200 ns
2 = t_r = 1.2 μs, t_f = 200 ns
3 = t_r = 1.3 μs, t_f = 300 ns

T_A Range: All types -55 to +125°C except CA311 (0 to +70°C)

Programmable Types with Memory

Type	V_{IO} Max mV		V_{IO} (Min) mV	I_{IB} (Max) mA		I_O (Min) mA	Switching Times (Typ.) ns				Pkg. No. of Pins
	LR	HR	(Hyst.)				t_d	t_f	t_r	t_s	
CA3098	6	10	20	100 pnp	100 npn	100	600	50	500	4500	8E, S,T

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Differential Amplifiers

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RCA differential amplifiers are intended for differential signal processing over a wide input voltage range in communications systems operating at frequencies up to 500 MHz.

Type	Description	Freq. Range DC to MHz	A (typ.) dB	BW (3dB Point) (Typ.) kHz	I/F NF (Typ.) dB	AGC Range (Typ.) dB	Pkg. No. of Pins
CA3000	DC Amplifier	30	37	650	—	90	10 T
CA3001	Video & Wideband Amplifier	29	19	29■	5	60	12T
CA3002	IF Amplifier	20	24	11■	4#	—	10T
CA3005	RF Amplifiers	100	16	—	7.8#	-60•	12T
CA3006		100	16	—	7.8#	-60•	
CA3026	Dual Independent	120	32□	550†	3.25	75	12T
CA3028A	Differential /Cascode Amplifiers	120	40□	—	7.2#	62	8C, S,T
CA3028B		120	40	8	7.2#	62	
CA3040	Video & Wideband Amplifier	55	37	5.5	7.5	—	12T
CA3049	Dual High-Frequency	500	22	1.35▲	53	75	12T
CA3050	Dual Differential Amplifiers	20	—	4.3•/ 600†	—	60	14 D, E
CA3051		20	—	4.3•/ 600†	—	60	
CA3053	Differential /Cascode Amplifier	120	40	Recommended for IF Amplifier Applications			8E, S,T
CA3054	Dual Independent	120	32	550†	3.25	75	14E
CA3102	Dual High-Frequency	500	22	1.35▲	1.5	7.5	14E

•Min ■RMS ▲GHZ #NF °Transistor Array † f_T (mHz)
□G_P Min. at 100 MHz: Cascode. 16dB, Diff Ampl. 14 dB

V_{OUT} (p-p Volts): CA3000, 6.4 CA3001, 5 CA3002, 5.5 CA3028B, 11.5 CA3040, 05. (RMS)
T_A Range: -55 to +125° C except for types CA3051, CA3054 (-40 to +85° C)

IC Arrays

RCA High-Speed CMOS Arrays

20-Lead (E), (F) and (M) Packages

Type V_{CC} = 4.5V	V_{IH} Min. V	V_{IL} Max. V	V_{OH} Min. V	V_{OL} Max. V	I_I Max. μA	I_{CC} Max. μA	Switching Characteristics C_L = 50 pF, t_r, t_f = 6 ns		
							t_{PLH} t_{PHL}• Max. ns	t_{TLH} t_{THL}• Max. ns	C_I Max. pF
CD54/74 HC688	3.15	1.35	4.4/ 3.98*	0.1/ 0.26*	±0.1†	8†	34/ 24‡	15	10
CD54/74 HCT688	2	0.8	4.4/ 3.98*	0.1/ 0.26*	±0.1†	8†	34/ 24‡	15	10

*CMOS/TTL loads †V_{CC} = 6 V
‡ Rand B data to output/enable to output

Note: For information on Power Darlington Transistor/Arrays, see section on Bipolar Power Transistors

IC Arrays (Cont'd)

RCA Diode Arrays

Electrical Characteristics at T_A = 25° C. Apply for Each Diode

Type	Description	$V_{(BR)R}$ (Min.) V	I_R (Max.) μA	C_D (Typ.) pF	V_{F1} - V_{F2} (Max.) mV	Pkg. No. of Pins
CA3019	Quad Plus 2 Uncommitted	4	10	1.8	5 (I_F = 1 mA)	10T
		• Ultra-fast low-capacitance matched diodes				
CA3039	6 Individual	5	0.1	0.65	5 (I_F = 1 mA)	12T
		• Ultra-fast low-capacitance matched diodes				
CA3141	10 High Reverse Breakdown Voltage Diodes □□	30	0.1	0.3	0.55 (typ.) (each diode pair)	16E
		• Low-noise performance • Low-leakage current				

□□ Six connected to form 3 common-cathode diode pairs.
Four connected to form 2 common-anode diode pairs.

RCA CMOS ARRAYS

Electrical Characteristics at T_A = 25° C

Type	Description	Features	Pkg. No. of Pins
CA3600	Three CMOS Pairs	R_I = 100 GΩ, high voltage gain = 53 dB typ. (per CMOS stage) Low gate terminal current = 10 pA typ. Specified and tested for linear circuit operation at frequencies up to 5 MHz (untuned).	14E
CD54/74 HC U04	QMOs Hex Inverter (Unbuffered) Linear Wide-band Amplifier	t_{PLH}, t_{PHL} = 6 ns @ V_{CC} = 5V 2-6 volt operation T_A = -40 to +85° C	14E, M
		For application information, refer to RCA Application Note, ICAN7637 "Linear Application of the CD74HCU04 QMOS Inverter."	

GE/RCA Solid State

RCA Products

For other Harris Semiconductor Products, see pages 2715 thru 2775.

IC Arrays (Cont'd)

HARRIS SEMICONDUCTOR
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RCA Transistor Arrays

Electrical Characteristics at T_A = 25°C

Type	Description	$V_{(BR)CEO}$ (Min.) V	$V_{(BR)CBO}$ (Min.) V	h_{FE} (Min.)	I_C (Max.) mA	Pkg. No. of Pins
CA3018	Two Isolated Transistors plus a Darlington Pair	15	20	30	50	12T
CA3018A		15	30	60	50	
		h_{FE} matched ± 10%, V_{BE} matched ±2 mV and ±5 mV max. Operation from dc to 120 MHz.				
CA3045	Three Transistors plus a Differential Pair	15	20	40	50	14D, F
CA3046		15	20	40	50	14E
		f_t > 300 MHz 2 matched pairs, ±5 mV				
CA3050	Dual Differential Amplifiers plus Diode Bias String	15	20	f_T▲600 MHz (typ.)	50	14D
CA3051		15	20		50	14E
		I_{IO} = 70 nA max., I_{IB} = 500 nA max. V_{IO} = 5 mV max.				
CA3081	General-Purpose n-p-n High-Current Transistors	16	20	40	100	16E, F
		Seven Common-Emitter				
CA3082		16	20	40	100	16E, F
		Seven Common-Collector				
CA3083		15	20	40	100	16E 16F
		Five independent transistors Q_1 and Q_2 matched: (I_{IO} at 1 mA,) 2.5 μA max.				
CA3086	Three Isolated Transistors plus a Differential Pair	15	20	40	50	14E, 14F
		f_T > 550 MHz typ. Operation from dc to 120 MHz.				
CA3127	Five Independent Transistors	15	20	40	20/ trans.	16E, 16F
		f_T > 1 GHz Operation from dc to 500 MHZ.				
CA3146	Three Transistors plus a Differential Pair	30	40	30	50	16E
CA3146A		40	50	30	50	
		f_t > 500 MHz typ. Operation from dc to 120 MHz.				
CA3183	Five High-Current Transistors	30	40	40	75	16E
CA3183A		40	50	40	75	
		High-voltage versions of CA3083 Trans. Q_1 & Q_2 matched at 1 mA.				
CA3227	Five Independent Transistors	8	12	40	20/ trans.	16E
		f_t = 3 GHz typ. Operation from dc to 1.5 GHz.				
CA3246	Three Independent Transistors plus a Differential Pair	8	12	40	20	14E
		f_t = 3 GHz typ. Operation from dc to 1.5 GHz.				
CA3250	General-Purpose n-p-n High-Current Transistors	20	20	40	100	18E, 18F
		Eight Common-Collector				
CA3251		20	20	40	100	
		Eight Common-Emitter				

▲For single transistor

Type	Description	$V_{(BR)CEO}$ (Min.) V n-p-n/ p-n-p	$V_{(BR)CBO}$ (Min.) V n-p-n/ p-n-p	h_{FE} (Min.) n-p-n/ p-n-p	I_C (Max.) mA n-p-n/ p-n-p	Pkg. No. of Pins
CA3096	Five Independent Transistors, 3 n-p-n, 2 p-n-p	35/–40	45/–40	150/20	50/–10	16E
CA3096A		35/–40	45/–40	150/20	50/–40	
CA3096C		24/–24	30/–24	100/15	50/–10	
		n-p-n		p-n-p		
		$\|V_{IO}\|$ = 5 mV max.		5 mV max.		
		$\|I_{IO}\|$ 0.6 μA max.		0.25 μA max.		
CA3097	Thyristor/ Transistor Array 1 n-p-n, 1 n-p-n/p-n-p trans. pair, 1 zener, 1 PUT, 1 SCR	30/–40	50/–50	n-p-n/ p-n-p pair 8000 typ.	100/–10	16E
		PUT: I_P = 15 nA, V_{AK} = ±30 V Zener V_Z = 8 V ± 10% Z_Z = 15 Ω typ. at 10 mA				

RCA Amplifier Arrays Electrical Characteristics at T_A 25°C

Type	Description	f_T MHz	A_{OL} (Typ.) dB	NF (Typ.) dB	Push-Pull Input & Output	Pkg. No. of Pins
CA3026	Dual Independent Differential Amplifiers	550■	32	3.25■	X	12T
CA3054		Maximum input offset voltage ±5 mV. Useful from dc to 120 MHz. Types are indentical except for package and substrate connection				14E
CA3048	Four Independent AC Amplifiers	12	58	2 @ 1 kHz	—	16E
		Operates from single-ended supply.				
CA3049	Dual High-Frequency Differential Amplifiers	1350	23†	4.6†	X	12T
CA3102		Independently accessible inputs and outputs. Useful from dc to 500 MHz. CA3102 like the CA3049 except that it has a separate substrate connection.				14E
CA3052	Four Independent AC Amplifiers	12	58‡	V_O = 2 V rms min.		16E
		Operates from single-ended supply				
CA3060	Three, Independent, Identical OTA Arrays	Includes unique zener diode regulator system. For data, see OP Amp Section.			X	16E

† At 200 MHz
* 1/f at 1 kHz
■ For single transistor
Δ AT 100 kHz
‡ Each amplifier

RCA Products

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Power-Control Circuits

RCA Voltage Regulators

Electrical Characteristics at T_A = 25°C

Type	V_I Range V	V_O Range V	I_O (max.) mA	Load Regulation % V_O (max.)	V_I-V_O V (min.)	Short-Circuit Current Limit mA (typ.)	Pkg. No. of Pins
CA3085	7.5 to 30	1.8 to 26	12•	0.1	4	96	8T,
CA3085A	7.5 to 40	1.7 to 36	100	0.15	4	96	8S,
CA3085B	7.5 to 50	1.7 to 46	100	0.15	3.5	96	8E
CA723	9.5 to 40	2 to 37	150	0.03	3	65	10T,
CA723C	9.5 to 40	2 to 37	150	0.03	3	65	14E

•This value may be extended to 100 mA; however, regulation is not specified beyond 12 mA.
Operating temperature range (T_A): −55 to +125°C

RCA Voltage-Regulator Control Circuit Variable-Interval Pulse Regulator

Operating Temperature Range (T_A): 0 to +70°C

Typical Electrical Characteristics at T_A = 25°C	V_{CC} (Pin 7) V	V_{CC} Range V	I_{CC} mA	Error Voltage Ref. (Pin 1) V	Pulse Output V_{OL} (Pin 6) V	Pulse Output V_{OH} (Pin 6) V	Max. Load Duty Cycle %
	13	10-15	27	6.5	1.0	12	50

Features
- *Operation up to 200 kHz*
- *ESD Protection: Pins are protected against ESD*
- *Remote ON/OFF: Activates regulator*
- *Slow start with Reset: Soft start ensured at power-up and restart*
- *Over-current sensing: Protects power device from over-dissipation over-current trip (Pin), 1.25 volts)*
- *Supply voltage monitor: Locks out the drive unit until V_{SUPPLY} has reached 9 V*
- *Bandgap reference voltage (internal): Provides temperature-compensated 1.2 V and 6.8 V references*
- *Lower peak currents than PWM regulator: Less prone to magnetic saturation*

14-Lead Dual-In-Line (E) Package

RCA Regulating Pulse-Width Modulators

Electrical Characteristics at V^+ = 20 V, f = 20 kHz
T_A = −55 to +125°C for CA1524;
0 to +70°C for CA2524, CA3534
16-Lead Dual-In-Line (E) and (F) Packages

Type	V^+ Range V	V_O Range V	Load Regulation % V_O (Typ.)	Ripple Rejection db (Typ.)	Total Standby Current Is (mA) (Max.)	$V_{CE\ SAT}$ V (Typ.)
CA1524	8 to 40	4.8 to 5.2	0.2	66	10	0.8
CA2524	8 to 40	4.8 to 5.2	0.2	66	10	0.8
CA3524	8 to 40	4.6 to 5.4	0.2	66	10	0.8

Short-Circuit current limit, 100mA typ.
Temperature Stability, 1% max.

RCA Zero-Voltage Switches

Electrical Characteristics at T_A = 25°C
14-Lead Dual-In-Line (E) Package

Type	AC Input Voltage @ 50-60 and 400 Hz (VAC)	Max. DC Supply Volts (V)	Max. Input Current (μA)	Sensor Range (R_x) kΩ	Control Current To Thyristor Gate (mA)
CA3059	24	14	1	2 to 100	Up to 124 with internal supply; up to 240 with one external supply
CA3079	120 208/ 230 277	10	2	2 to 50	

Operating temperature range (T_A): −55 to +125°C

RCA Quad-Gated Power Drives

For Interfacing Low-Level Logic to High-Current Loads
Electrical Characteristics at T_A = 25°C, V_{CC} = 5V;
T_A Range: −40 to +85°C

Type	Features	I_{CEX} Max. (V_{CE} = 50V) μA	$V_{CE\ SUS}$ Min. (I_C = 100 mA) V	$V_{CE\ (sat)}$ Max. (I_C = 600 mA) V	I^+ Max. I_C = 700mA V_{CC} + 5.5V mA	I_R Max. (V_R = 50V) μA	t_{PHL}, t_{PLH} Max. μs	Pkg. No. of Pins
Inverting Types								
CA3262	Independent over-current limiting for each output •(0.7 min. A). Independent over-temperature limiting for each output (155 typ. °C)	100#	25#	0.7Δ	80□ 5■	100	10	16E
CA3242	Overload protection circuitry	100Δ	25Δ	0.8#	80□ 5■	100	20	16E
Non Inverting Types								
CA3219A	Fast t_{PHL}, t_{PLH} (typically 3 μs)	100#	25#	0.7Δ	80□ 5■	100	10	16E
CA3252	Input latch with external feedback resistor	100Δ	25Δ	0.7#	80□ 5■	100	30	16E

□All outputs ON ■All outputs OFF #V_{IN} = 0.8V ΔV_{IN} = 2.4 V •V_{OUT} = 4.5 to 24.5 volts

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RCA Solenoid and Motor Driver (½ H Drive) CA3169

Electrical Characteristics at T_A = 25°C, V_{CC} = 10.5 to 18 V
Versa V1 TO-220 Style Package

Characteristics		Limits			Units
		Min.	Typ.	Max.	
Output Leakage Current (Pin 2 or Pin 3)		-110	±0.5	110	μA
Quiescent Current (Pin 1): Input Terminals Shorted	V_{CC} =	—	70	100	mA
Input Terminals Open	14 V	—	17	40	mA
Overvoltage Shutdown Circuit (Pin 1) Upper Trip Point		20	25	27	V
Lower Trip Point		18	21.4	23	V
Source Output Short Circuit Current (Pin 2-G)		0.65	1.11	2.6	A
Sink Output (I_{SINK} 600 mA) Output Saturation Voltage		—	0.3	0.85	V

Operating temperature range: -40 to +85°C

RCA Operational Amplifier/Comparator CA3177

Electrical Characteristics at T_A = 25°C, T_A Range: 0 to +70°C

Sections	Features	V_{IO} Max. mV	I_{IB} Max. μA	V_{ICR} Max. V	I^+ Max. mA	h_{FE}	$V_{CE(sat)}$ Max. V	Pkg. No. of Pins
Operational Amplifier	Has shut-down control and Isolated Transistor	100	15	12 2•	10 3•			8EI
Q14 Amplifier						45 Note 1	0.6 Note 2	
Q1 Amplifier	High Output Current 50 mA Max.						0.4 Note 3	

Note 1: V_{CE} = 10V, I_6 = 0.1 mA and 2 mA
Note 2: I_7 = 0.2 mA, I_6 = 2mA
Note 3: I_8 = 0.15 mA, I_1 = 30 mA
•Min.

RCA Multi-Purpose Wideband Power Amplifiers CA3020, CA3020A

Typical Electrical Characteristics at T_A = 25°C
12-Lead (T) Package

Characteristics	CA3020	CA3020A	Units
Maximum Power Output (P_O) at THD = 10%	550	1000	mW
Sensitivity (C_{IN})	35	45	mV
Power Gain (G_P)	75	75	dB
Input Resistance (R_{IN})	55	55	kΩ
Signal-to-Noise Ratio (I/N)	70	66	dB
Total Harmonic Distortion at 150 mW (THD)	3.1	3.3	%
Bandwidth (-3-db point) (BW)	8	8	MHz

Operating temperature range (T_A): -55 to +125°C

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GE/RCA Type	Description
Engine and Drive Train Controls	
CA324	Quad Operational Amplifier
CA339	Quad Voltage Comparator
CA358	Dual Operational Amplifier
CD3165	Electronic Switching Circuit
CA3169	Solenoid and Motor Driver
CA3219A	Quad-Power NAND Driver
CA3242	Quad-Gated Inverting Power Driver
CA3252	Quad-Gated Non-Inverting Power Driver
CA3262	Quad-Gated Inverting Power Driver
CD4538B	CMOS Dual Precision Monostable Multivibrator
CDP1802A	8-Bit Microprocessor
CDP1804A	8-Bit Microcomputer
CDP1805A	8-Bit Microprocessor
CDP6805E2	8-Bit Microprocessor
CDP6805E3	8-Bit Microprocessor
CDP6805F2	8-Bit Microcomputer
CDP6805G2	8-Bit Microcomputer
CDP6823	Parallel Interface
CDP68HC05C4	8-Bit Microcomputer
CDP68HC05D2	8-Bit Microcomputer
CDP68HC68A2	SPI A/D Converter
CDP68HC68R1	SPI RAM 128 Bytes
CDP68HC68R2	SPI RAM 256 Bytes
Features (Optional Equipment)	
CA3169	Solenoid and Motor Driver
CD3219A	Quad-Gated Non-Inverting Power Driver
CA3228	Speed Control System
CA3232	÷20 Prescaler
CA3242	Quad-Gated Inverting Power Driver
CA3252	Quad-Gates Non-Inverting Power Driver
CA3259	Stereo Sound Volume/Tone Control
CD4517B	CMOS Dual 64-Stage Static Shift Register
CD40106B	CMOS High-Speed 8-Bit Bidirectional CMOS/TTL Interface Level Converter
CDP68HC05D2	8-Bit Microcomputer
CDP68HC05F2	8-Bit Microcomputer
Multiplex Communications	
CD4016B	CMOS Quad Bilateral Switch
CD4006B	CMOS 18-Stage Static Shift Register
CD4512B	CMOS 8-Channel Data Selector
CD54/74HC/HCT157	Quad 2-Input Multiplexer
CD54/74HC/HCT257	Quad 2-Input Multiplexer, 3-State
CDP1802A	8-Bit Microprocessor
CDP1804A	8-Bit Microcomputer
CDP1805A	8-Bit Microprocessor
CDP1863	8-Bit Programmable Counter
CDP6402	Programmable UART
CDP6823	Parallel Interface
CDP6853	Asynchronous Communications Interfacce Adapter
CDP6805E2	8-Bit Microprocessor
CDP6805E3	8-Bit Microprocessor
CDP6805F2	8-Bit Microcomputer
CDP6805G2	8-Bit Microcomputer
CDP65C51E1	Asynchronous Communications Interface Adapter
CDP65C51E2	Asynchronous Communications Interface Adapter
CDP68HC05D2	8-Bit Microcomputer

GE/RCA Type	Description
Multiplex Communications (Cont'd)	
CDP68HC68A2	SPI A/D Converter
CDP68HC68R1	SPI RAM 128 Bytes
CDP68HC68R2	SPI RAM 256 Bytes
Body Computer	
CD54/74HC/HCT00	Quad 2-Input NAND Gate
CD54/74HC/HCT244	Octal Buffer/Line Driver; 3-State
CD54/74HC/HCT245	Octal Bus Transceiver; 3-State
CD54/74HC/HCT373	Octal Transparent Latch; 3-State
CD54/74HC/HCT374	Octal D-Type Flip-Flop; Positive-Edge Trigger; 3-State
CDM5364	8K x 8 ROM
CDM5365	8K x 8 ROM
CDM6116	2K x 8 RAM
CDM6264	8K x 8 RAM
CDM53128	16K x 8 ROM
CDM53256	32K x 8 ROM
CDP1851	Programmable I/O Interface
CDP1852	Byte-Wide I/O Port
CDP1855	8-Bit Programmable Multiply/Divide Unit
CDP1863	8-Bit Programmable Counter
CDP6818	Real Time Clock, MOTEL Bus
CDP68HC05C4	8-Bit Microcomputer
CDP68HC05D2	8-Bit Microcomputer
CDP68HC68R1	SPI RAM 128 Bytes
CDP68HC68R2	SPI RAM 256 Bytes
CDP68HC68T1	SPI Real-Time Clock
Entertainment	
CA3088	AM Receiver Subsystem and General Purpose Amplifier Array
CA3089	FM IF System
CA3130	BiMOS Op Amp
CA3189	FM IF System
CA3195	RC Phase-Lock-Loop Stereo Decoder
CA3257	PLL FM Multiplex Stereo Demodulator
CA3258	Noise Blanker
CA3259	Stereo Sound/Volume Tone Control
CA3209	FM IF System
CD4052	CMOS Analog Multiplexer/Demultiplexer
CDP6818	Real Time Clock, MOTEL Bus
CDP68HC05D2	8-Bit Microcomputer
CDP68HC68R2	SPI RAM 256 Bytes
CDP68HC68T1	SPI Real Time Clock
Driver Information/Display	
LCD	
CD4054B	4-Segment Display Driver
CD4055B	BCD-to-7-Segment Decoder/Driver with Display freq. output
CD4056B	BCD-to-7 Segment Decoder/Driver with Strobed-Latch Function
CD4543B	BCD-to-7 Segment Decoder/Driver with Strobed-latch Function
CD7211	Four-Digit LCD Decoder/Driver
CD7211A	Four-Digit LCD Decoder/Driver
CD7211M	Four-Digit LCD Decoder/Driver
CD7211AM	Four-Digit LCD Decoder/Driver
CD54/4HC/HCT4543	BCD-to-7 Segment Latch/Decoder/Driver
LED	
CA3081	Common-Emitter Transistor Array
CA3082	Common-Collector Transistor Array
CA3083	High-Current NPN Transistor Array
CA3161	BCD-to-7 Segment Decoder/Driver, Current Output Driver, Common Anode

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Automotive Circuits (Cont'd)

RCA CA3165
Electronic Switching Circuit For Ignition Applications

Electrical Characteristics at T_A = 25°C, V = 13 V

Operating Temperature Range: -40 to +85°C

Characteristics	Test Period	Limits						Units
		CA3165E1			CA3165E			
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Current at Term*	Dwell	—	18.4	—	—	18.4	—	mA
	Spark	—	17.5	—	—	17.5	—	
Output Voltage at Term 4 V_4	Dwell	12.8	—	—	12.8	—	—	V
	Spark	—	—	0.5	—	—	0.5	
Output Voltage at Term 7 V_7	Dwell	—	—	1	—	—	—	V
Output Voltage at Term 8 V_8	Dwell	—	—	0.9				V
	Portion of Spark	1.2	—	—	—	—	—	
Oscillator Voltage at Term 2 V_2	Dwell	—	4.4	—	—	4.4	—	V_{p-p}
	Spark	—	0.6	—	—	0.6	—	

Package: 8E, 14E

*CA3165E Term 7 I_7
CA3161E1 Term 12 I_{12}

RCA CA3228
Speed-Control System

Typical Switching Characteristics
Driver Command Input Hold Times:
(Based on 0.68 μF capacitor on Pin 4)

Accel. (ms)	Coast (ms)	Resume (ms)	On (ms)	Off (ms)
50	50	330	50	50

Internal Oscillator Frequency, f_{osc} = 10 kHz
(Based on 0.001 μF capacitor on Pin 5)

Typical Performance Characteristics
(f_{osc} = 50 kHz; fs/Speed Ratio, 2.22 Hz/mph)

Speed Sensor Input Frequency Range (fs) at Pin 8 (Hz)	Speed Resolution (mph)	Min. Operating Speed (mph)	Max. Stored Speed (mph)	Redundant Brake Speed (mph)
62 to 222	0.45	25	100	11

Operating Temperature Range: -40 to +85°C
Package: 24E

RCA Quad-Gated Power Driver

For Interfacing Low-Level Logic to High-Current Loads
Electrical Characteristics at T_A = 25°C, V_{CC} = 5V;
T_A Range: -40 to +85°C

Type	Features	I_{CEX} Max. (V_{CE} = 50V) μA	$V_{CE\ SUS}$ Min. (I_C = 100 mA) V	$V_{CE\ (sat)}$ Max. (I_C = 600 mA) V	I^+ Max. (I_C = 700mA V_{CC} = 5.5V) mA	I_R Max. (V_R = 50V) μA	t_{PHL}, t_{PLH} Max. μs	Pkg. No. of Pins
Inverting Types								
CA3262	Independent over-current limiting for each output •(0.7 min. A). Independent over-temperature limiting for each output (155 typ. °C)	100	25	0.7	80□ 5■	100	10	16E

•V_{OUT} = 4.5 V to 24.5 V □All outputs ON ■All outputs OFF

GE/RCA Solid State

RCA Products

For other Harris ASIC Products, see pages 4244 thru 4253.

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RCA Video/Monitor Circuits

HARRIS SEMICONDUCTOR
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Type No.	Description	Pkg. No. of Pins
Signal Transmission Modulator		
CA1890	TV Video/Audio, RF Modulator	14E
Demodulators		
CA3049	Dual High-Frequency Differential Amplifier	12T
CA3052	Four Independent AC Amplifiers	16E
CA3102	Dual High-Frequency Differential Amplifier. Like the CA3049 but has a Separate Substrate Connection for Greater Design Flexibility	14E
RF/IF		
CA7607	Video IF Amplifier System Suitable for FET Applications	16E
CA7611	Video IF Amplifier System for N-P-N Tuner Stages	16E
LM1822N	Video IF Amplifier/PLL Detector System	24E
LM1823N	Like LM 1822N but Intended for Cable TV	24E
Video/ Chroma/ Luma Processing		
CA3126	TV Chroma Processor	16E, Q
CA3217	Single-Chip TV Chroma/Luminance Processor	28E
Video Switches Analog Multiplexers/ Demultiplexers		
CA3256	CMOS/BiMOS Analog Video Switch and Amplifier	18E
CD4016B	CMOS Quad Bilateral Switch	14•
CD4051B	CMOS Single 8-Channel Analog Multiplexer/Demultiplexer	16•
CD4052B	CMOS Differential 4-Channel Analog Multiplexer/Demultiplexer	16•
CD4053B	CMOS Triple 2-Channel Analog Multiplexer/Demultiplexer	16•
CD4066B	CMOS Quad Bilateral Switch	14•
CD4067B	CMOS Single 16-Channel Analog Multiplexer/Demultiplexer	24•
CD4097B	CMOS Differential 8-Channel Analog Multiplexer/Demultiplexer	24•
Video Switches Analog Multiplexers/ Demultiplexers (Cont'd)		
CD54/74-HC/HCT4016	High-Speed CMOS Quad Bilateral Switch	14°
HC/HCT4051	High-Speed CMOS Single 8-Channel Analog Multiplexer/Demultiplexer	16°
HC/HCT4052	High-Speed CMOS Differential 4-Channel Analog Multiplexer/ Demultiplexer	16°
HC/HCT4053	High-Speed CMOS Triple Two-Channel Analog Multiplexer/Demultiplexer	16°
HC/HCT4067	High-Speed CMOS 16-Channel Analog Multiplexer/Demultiplexer	24°
HC/HCT4097	High-Speed CMOS Differential 8-Channel Analog Multiplexer/ Demultiplexer	24°

Type No.	Description	Pkg. No. of Pins
	Video Switches Analog Multiplexers/ Demultiplexers (Cont'd)	
HC/HCT4316	High-Speed CMOS Quad Analog Switch Multiplexer/Demultiplexer with Separate Analog and Digital Power Supplies	16°
HC/HCT4351	High-Speed CMOS 8-Channel Analog Multiplexer/Demultiplexer with Address Latch	18°
HC/HCT4352	High-Speed CMOS Dual 4-Channel Analog Multiplexer/Demultiplexer with Address Latch	18°
HC/HCT4353	High-Speed CMOS Triple 2-Channel Analog Multiplexer/Demultiplexer with Latch	18°
Mixers		
CA3253	Video Processor	24E
CA3256	CMOS/BiMOS Analog Video Switch and Amplifier	18E
CA3450	Video Line Driver, High-Speed Operational Amplifier	16E
CD4016B	CMOS Quad Bilateral Switch	14•
CD4051B	CMOS 8-Channel Analog Multiplexer/ Demultiplexer	16•
CD4052B	CMOS Differential 4-Channel Analog Multiplexer/Demultiplexer	16•
CD4053B	CMOS Triple 2-Channel Analog Multiplexer/Demultiplexer	16•
CD4066B	CMOS Quad Bilateral Switch	14•
CD4067B	CMOS Single 16-Channel Analog Multiplexer/Demultiplexer	24•
CD4097B	CMOS Differential 8-Channel Analog Multiplexer/Demultiplexer	24•
CD54/74-HC/HCT4016	High-Speed CMOS Quad Bilateral Switch	14°
HC/HCT4051	High-Speed CMOS Single 8-Channel Analog Multiplexer/Demultiplexer	16°
HC/HCT4052	High-Speed CMOS Differential 4-Channel Analog Multiplexer/ Demultiplexer	16°
HC/HCT4053	High-Speed CMOS Triple 2-Channel Analog Multiplexer/Demultiplexer	16°
HC/HCT22106	High-Speed CMOS 8x8x1 Crosspoint Switch with Memory Control	28E
Sync Generators		
CD22402	CMOS LSI Sync Generator	24D, E
CA3254	RS-170 Sync Generator (EIA RS-170 Standard with 2:1 Interlace) for 525-Line, 60-Hz Systems	24E
CA3255	Like CA3254 but Designed for Use in 625-Line, 50-Hz Systems	24E
Video Processors		
CA3054	Dual Independent Differential Amplifier Transistor Array	14E
CA3100	Wide-Band Operational Amplifier	8E,S,T
CA3102	Dual High-Frequency Differential Amplifier	14E
CA3127	High-Frequency N-P-N Transistor Array	16E, F
CA3135	TV Luminance Processor	16E
CA3156	Video/Chroma Processor	16E
CA3194	Single-Chip PAL Luminance/Chroma Processor	24E

RCA Products

For other Harris Semiconductor Products, see pages 2715 thru 2775.

RCA Video/Monitor Circuits (Cont'd)

HARRIS SEMICONDUCTOR
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Type No.	Description	Pkg. No. of Pins
Video Processors (Cont'd)		
CA3227	High-Frequency N-P-N Transistor Array	16E
CA3246	High-Frequency N-P-N Transistor Array	14E
CA3253	Video Processor for Video Camera Applications	24E
CA3256	CMOS/BiMOS Analog Video Switch and Amplifier	18E
CD54/74-HCU04	High-Speed CMOS Hex Inverter (Unbuffered)	14°
Sync Processors		
CA555	Precision Timer and Oscillator	8E,S,T
CA3142	TV Sync Processor	16E
CA3202	TV Horizontal/Vertical Countdown Digital Sync System	14E
CA3210	TV Horizontal/Vertical Countdown Digital Sync System for 525-Line Operation	24E
CA3218	TV Horizontal/Vertical Countdown Digital Sync System	16E
CA3236	TV Horizontal/Vertical Countdown Digital Sync System Complete Decoder for NTSC or PAL 525-Line Operation	28E
CA3241	Like CA3236 but for 625-Line Operation	28E
CA3223	Like CA3210 but for 625-Line Operation	24E
CD4013B	CMOS Dual "D" Type Flip Flop	14•
CD4046B	CMOS Micropower Phase-Locked Loop	16•
CRT Drive CRT Bias		
CA3224	Automatic Picture Tube Bias Circuit	22E
Horizontal-Vertical Scan		
CA555	Precision Timer and Oscillator	8E,S,T
CA1391	TV Horizontal Processor (Positive Horizontal Sawtooth Input)	8E
CA1394	Like CA1391 but with Negative Horizontal Sawtooth Input	8E
CA3094	Programmable Power Switch Amplifier	8E,S,T
CA3154	TV Sync/AGC/Horizontal Sync Processor	16E
CA3177	Operational Amplifier/Comparator	8E
CA3218	TV Horizontal/Vertical Countdown Digital Sync System	16E
CA3261	AFC Horizontal Oscillator Signal Processor with Sync Separator and AGC	18E
CA3210	TV Horizontal/Vertical Countdown Digital Sync System	24E
CA3223	Like CA3210 but Intended for 625-Line Operation	24E
CA3236	TV Horizontal/Vertical Countdown Digital Sync System Complete Decoder for NTSC or PAL (525-Line Operation)	28E
CA3241	Like CA3236 but for 625-Line Operation	28E
CD4040B	CMOS Ripple-Carry Binary Counter/Divider	14•
Display Drivers		
CD4054B	CMOS 4-Segment LCD Display Driver	16•
CD4055B	CMOS BCD-to-7-Segment LCD Display Decoder/Driver with "Display-Frequency" Output	16•
CD4056B	CMOS BCD-to-7-Segment LCD Display Decoder/Driver with Strobed-Latch Function	16•
CD4094B	CMOS 8-Stage Shift and Store Bus Register	16•
CD4511B	CMOS BCD-to-7-Segment Latch/Decoder/Driver for LED and Other Displays	16•

Type No.	Description	Pkg. No. of Pins
Display Drivers (Cont'd)		
CD4543B	CMOS BCD-to-7-Segment Latch/Decoder/Driver for LCD Displays	16•
CD4543B	CMOS BCD-to-7-Segment Latch/Decoder/Driver for LCD Displays	16•
CD54/74-HC/HCT4511	High-Speed CMOS BCD-to-7-Segment Latch/Decoder/Driver for LED and Other Displays	16E,F,M
HC/HCT4543	High-Speed CMOS BCD-to-7-Segment Latch/Decoder/Driver for LCD Displays	16E,F,M
CD7211 CD7211A CD7211M CD7211AM	CMOS 4-Digit LCD Decoder Drivers Decode Multiplexed Binary to Hexadecimal (CD7211, CD7211M) and decimal (CD7211A, CD7211AM) outputs	40E
CA3081	General-Purpose High-Current N-P-N 7-Transistor Common-Emitter Array	16E, F
CA3082	General-Purpose High-Current N-P-N 7-Transistor Common-Collector Array	16E, F
CA3083	General-Purpose High-Current N-P-N Transistor Array	16F
CA3161	BCD-to-7-Segment Decoder Driver	16E
CA3168	2-Digit BCD-to-7-Segment Decoder Driver	24E
CA3207	BiMOS Sequencer Driver	22E
CA3208	BiMOS Segment Latch-Driver	22E
CA3250	General-Purpose, High-Current N-P-N 8-Transistor Common-Collector Array	18E, F
CA3251	General-Purpose, High-Current N-P-N 8-Transistor Common-Emitter Array	18E, F
CD4026B	CMOS Decade Counter/Divider	16•
CD4083B	CMOS Decade Counter/Divider	16•
CD40110B	Decade Up/Down Counter/Latch/Display Driver	16•
CD4041UB	Quad Time/Complement Buffer	14•
CD4049UB	Hex Buffer/Converter	16•
CD4050B	Hex Buffer/Converter	16•
CD54/74 HC/HCT4049	Hex Inverting High to Low Level Shifter	16E,F,M
HC/HCT4051	Hex High-to-Low Level Shifter	16E,F,M

Note: Package designator (T) indicates TO-5 package with straight leads.
•D, E, F, and K packages
°E, F, M packages

GE/RCA Solid State

RCA Products

For other Harris Semiconductor Products, see pages 2715 thru 2775.

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RCA Radio/Communications Circuits

HARRIS SEMICONDUCTOR
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Type No.	Description	Pkg. No. of Pins
RF Modulators		
CA1890	TV Video/Audio, RF Modulator	14E
CA3049	Dual High-Frequency Differential Amplifier	12T
CA3102	Like CA3049 but Has a Separate Substrate Connection for Greater Design Flexibility	14E
IR Preamplifier		
CA3237	IR Remote Control Amplifier	9 SIP
Differential Amplifiers and Arrays		
CA3005	RF Amplifier	12T
CA3006	Identical to CA3005 except for Input Offset Voltage	12T
CA3028	Differential/Cascode Amplifier	8E,S,T
CA3049	Dual High-Frequency Differential Amplifier	12T
CA3053	Identical to CA3028 except for 100-MHz Noise Specification	8E,S,T
CA3102	Dual High-Frequency Differential Amplifier	14E
CA3227	High-Frequency N-P-N Transistor Array	16E
CA3246	High-Frequency N-P-N Transistor Array	14E
Tuning Control		
CA3140	BiMOS Operational Amplifier	8E,S,T
CA3163	1.25 GHz ÷ 64/÷ 256 Dual-Mode VHF/UHF Prescaler	14E
CA3179	1.25 GHz ÷ 64/÷ 256 Dual-Mode Prescaler	14E
CA3199	1.25 GHz ÷ 4 Prescaler	8E
CA3232	200 MHz ÷ 20 Prescaler	8E
CA3263	Bandswitch Operational Amplifier	
CA3247	Analog Interface Unit (AIU)	40E
CDP6805	CMOS 8-Bit Microprocessor	40D, E, Q
Display		
CA3081	General-Purpose High-Current N-P-N 7-Transistor Common-Emitter Array	16E, F
CA3082	General-Purpose High-Current N-P-N 7-Transistor Common-Collector Array	16E, F
CA3161	BCD-to-7-Segment Decoder Driver	16E
CA3168	2-Digit BCD-to-7-Segment Decoder Driver	24E
CA3207	BiMOS Sequencer Driver	22E
CA3208	BiMOS Segment Latch-Driver	22E
CA3250	General-Purpose, High-Current N-P-N 8-Transistor Common-Collector Array	18E, F
CA3251	General-Purpose, High-Current N-P-N 8-Transistor Common-Emitter Array	18E, F
CD4054B	CMOS 4-Segment LCD Display Driver	
CD4055B	CMOS BCD-to-7-Segment LCD Display Decoder/Driver with "Display-Frequency" Output	16•
CD4056B	CMOS BCD-to-7-Segment LCD Display with Strobed-Latch Function	16•
CD4094B	8-Stage Shift and Store Bus Register	16•
CD4511B	CMOS BCD-to-7-Segment Latch/Decoder/Driver for LED and Other Displays	16•
CD4543B	CMOS BCD-to-7-Segment Latch/Decoder/Driver for LCD Displays	16•
CD54/74-HC/HCT4511	High-Speed CMOS BCD-to-7-Segment Latch/Decoder/Driver for LED and Other Displays	16E,F,M
HC/HCT4543	High-Speed CMOS BCD-to-7-Segment Latch/Decoder/Driver for LCD Displays	16E,F,M

Type No.	Description	Pkg. No. of Pins
Power Supply Regulators		
CA723	Voltage Regulator	10T,14E
CA1523	Voltage Regulator Control Circuit for Variable Switching Regulator	14E
CA3085	Positive Voltage Regulator	8E,S,T
CA3130	BiMOS Operational Amplifier	8E,S,T
CA3524	Regulating Pulse-Width Modulator	16E, F
2N3053	High-Speed Switching N-P-N Power Transistor	TO-39
2N3055H	General-Purpose Silicon N-P-N Power Transistor	TO-204 MA
AM/FM Radio AM Radio		
CA3088	AM Receiver Subsystem and General-Purpose Amplifier Array	16E
PLL IF with Detector		
CA3215	FM/IF Amplifier/Detector Limiter	16E
IF Without Detector		
CA3002	IF Amplifier	10T
CA3011	Wide-Band Amplifier	10T
CA3012	Wide-Band Amplifier	10T
IF with Detector		
CA2111A	FM/IF Amplifier-Limiter and Quadrature Detector	14E, Q
CA2136A	FM/IF Amplifier-Limiter and Quadrature Detector	14E, Q
CA3013	Wide-Band Amplifier Discriminator	10T
CA3014	Wide-Band Amplifier Discriminator	10T
CA3089	FM/IF System	16E
CA3189	Like CA3089 but Particularly Suitable for High-Fidelity FM and Electronically Tuned Radios	16E
CA3209	FM/IF System for Search and Scan.	16E
Audio		
CA3020	Multipurpose Wide-Band Power Amplifier	12T
CA3048	Four Independent AC Amplifiers	16E
CA3052	Schematically Identical with CA3048, but Each Amplifier is Tightly Specified for Equivalent Output Noise	16E
CA3094	Programmable Power Switch/Amplifier	8E,S,T
CA3259	Stereo Sound Volume/Tone Control	18E
Stereo Demodulators		
CA3195	RC Phase-Lock-Loop Stereo Decoder	16E
CA3257	PLL FM Multiplex Stereo Demodulator	16E
CA3258	Noise Blanker	16E

•D, E, F, and K packages

Note: Package designator (T) indicates TO-5 package with straight leads.

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RCA Products

For other Harris Semiconductor Products, see pages 2715 thru 2775.

RCA TV/CATV Circuits

Type No.	Description	Pkg. No. of Pins
Tuner Control		
CA3140	BiMOS Operational Amplifier	8E, S, T
CA3163	1.25 GHz ÷ 64/÷ 250 Dual Mode VHF/UHF Prescaler	14E
CA3199	1.25 GHz ÷ 4 Prescaler	8E
CA3247	Analog Interface Unit (AIU)	40E
CDP6805	CMOS 8-Bit Microprocessor	40D, E, Q
IR Preamplifier		
CA3237	IR Remote-Control Amplifier	9 SIP
Video IF (PIX)		
LM1822N	Video IF Amplifer/PLL Detector System	24E
LM1823N	Like LM1822N but intended for Cable TV Systems	24E
CA7607	Video IF Amplifier System for FET Applications	16E
CA7611	Video IF Amplifier System for NPN Tuner Stages	16E
AFT		
LM1822N	Video IF Amplifier/PLL Detector System	24E
LM1823N	Like LM1822N but Intended for Cable TV Systems	24E
CA7607	Video IF Amplifier System Suitable for FET Applications	16E
CA7611	Video IF Amplifier Systems for N-P-N Tuner Stages	16E
Display Drivers		
CA3081	General-Purpose High-Current N-P-N 7-Transistor Common-Emitter Array	16E, F
CA3082	General-Purpose High-Current N-P-N 7-Transistor Common-Collector Array	16E, F
CA3161	BCD-to-7-Segment Decoder Driver	16E
CA3168	2-Digit BCD-to-7-Segment Decoder Driver	24E
CA3207	BiMOS Sequencer Driver	22E
CA3208	BiMOS Segment Latch-Driver	22E
CA3250	General-Purpose High-Current N-P-N 8-Transistor Common-Collector Array	18E, F
CA3251	General-Purpose High-Current N-P-N 8-Transistor Common-Emitter Array	18E, F
CD4054B	CMOS 4-Segment LCD Display Driver	16•
CD4055B	CMOS BCD-to-7-Segment LCD Display Decoder/Driver with "Display-Frequency" Output	16•
CD4056B	CMOS BCD-to-7-Segment LCD Display Decoder/Driver with Strobed-Latch Function	16•
CD4094B	CMOS 8-Stage Shift and Store Bus Register	16•
CD4511B	CMOS BCD-to-7-Segment Latch/ Decoder/Driver for LED and Other Displays	16•
CD4543B	CMOS BCD-to-7-Segment Latch/ Decoder/Driver for LCD Displays	16•
Sound IF Detector/Audio		
CA1190	Sound IF and Audio Output Subsystem	16Q
CA1191	Like CA1190 but with Integral Bent-Down Wing Tab Heat Sink	16E
CA2111A	FM/IF Amplifier-Limiter and Quadrature Detector	14E, Q
CA2136A	FM/IF Amplifier-Limiter and Quadrature Detector	14E, Q
CA3012	Wide-Band Amplifier	10T
CA3013	Wide-Band Amplifier Discriminator	10T
CA3014	Wide-Band Amplifier Discriminator	10T
CA3065	IF Amplifier-Limiter, FM Detector, Electronic Attenuator, Audio Driver	14E, Q

Type No.	Description	Pkg. No. of Pins
Sound IF Detector/Audio (Cont'd)		
CA3089	FM/IF System	16E
CA3189	Like CA3089 but Particularly Suitable for High-Fidelity FM and Electronically Tuned Radios	16E
CA3209	FM/IF System for Search and Scan	16E
CA3215	FM/IF Amplifier/PLL Detector	16E
Stereo Sound/ SAP Detector		
CA324	Quad Operational Amplifier	14E
CA3260	BiMOS Operational Amplifier	8E, S, T
CA3215	FM/IF Amplifier/PLL Detector	16E
Audio Amplifier/ Processor		
CA324	Quad Operational Amplifier	14E
CA3048	Four Independent AC Amplifiers	16E
CA3052	Schematically Identical with CA3048, but Each Amplifier is Tightly Specified for Equivalent Output Noise	16E
CA3260	BiMOS Operational Amplifier	8E, S, T
CA3259	Stereo Sound Volume/Tone Control	18E
Audio Output		
CA1191	Like CA1190 but with Integral Bent-Down Wing-Tab Heat Sink	16E
CA3134	Sound IF and Audio Output Subsystem	16EM, QM
Audio/Video Selector/ Amplifier		
CA3256	CMOS/BiMOS Analog Video Switch and Amplifier	18E
CD4016B	CMOS Quad Bilateral Switch	14•
CD4051B	CMOS 8-Channel Analog Multiplexer/ Demultiplexer	16•
CD4052B	CMOS Differential 4-Channel Analog Multiplexer/Demultiplexer	16•
CD4053B	CMOS Triple 2-Channel Analog Multiplexer/Demultiplexer	16•
CD4066B	CMOS Quad Bilateral Switch	14•
CD54/74-HC/HCTU04	High-Speed CMOS Hex-Inverter (Unbuffered)	14E,F,M
HC/HCT4016	High-Speed CMOS Quad Bilateral Switch	14E,F,M
HC/HCT4052	High-Speed CMOS Differential 4-Channel Analog Multiplexer/ Demultiplexer	16E,F,M
HC/HCT4053	High-Speed CMOS Triple 2-Channel Analog Multiplexer/Demultiplexer	16E,F,M
HC/HCT4066	High-Speed CMOS Quad Bilateral Switch	14E,F,M
Chroma/Luma Processors		
CA1398	TV Chroma Processor	14E
CA3070	TV Chroma System (Complete Subcarrier Regeneration System)	16E
CA3071	TV Chroma Amplifier System	14E
CA3072	TV Chroma System (Performs Demodulation Function	14E
CA3121	TV Chroma Amplifier/Demodulator	16E
CA3126	TV Chroma Processor	16E, Q
CA3135	TV Luminance Processor	16E
CA3151	Single-Chip TV Chroma Processor/ Demodulator	24E

Note: Package designator (T) indicated TO-5 package with straight leads.
•D, E, F, and K packages

RCA Products

For other Harris Semiconductor Products, see pages 2715 thru 2775.

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RCA TV/CATV Circuits (Cont'd)

Type No.	Description	Pkg. No. of Pins
Chroma/Luma Processors (Cont'd)		
CA3156	Video/Chroma Processor	16E
CA3170	TV Chroma System	16E
CA3194	Single-Chip PAL Luminance/Chroma Processor	24E
CA3217	Single-Chip TV Chroma/Luminance Processor	28E
Deflection Circuits Horizontal and Vertical		
CA3202	TV Horizontal/Vertical Countdown Digital Sync System	14E
CA3210	TV Horizontal/Vertical Countdown Digital Sync System for 525-Line Operation	24E
CA3218	TV Horizontal/Vertical Countdown Digital Sync System for 525-Line Operation	16E
CA3223	Like CA3210 but for 625-Line Operation	24E
CA3236	TV Horizontal/Vertical Countdown Digital Sync System for 525-Line Operation	28E
CA3241	Like CA3236 but for 625-Line Operation	28E
Horizontal		
CA1391	TV Horizontal Processor with Positive Horizontal Sawtooth Input	8E
CA1394	Like CA1391 but with Negative Horizontal Sawtooth Input	8E
CA3154	TV Sync/AGC/Horizontal Signal Processor	16E
CA3261	AFC/Horizontal Oscillator Signal Processor with Sync Separator and AGC	18E
Sync		
CA3142	TV Sync Processor	16E
Power Supply Regulators		
CA723	Voltage Regulator	10T,14E
CA1523	Voltage Regulator Control Circuit for Variable Switching Regulator	14E
CA3085	Positive Voltage Regulator	8E,S,T
CA3130	BiMOS Operational Amplifier	8E,S,T
CA3524	Regulating Pulse-Width Modulator	16E, F
2N3053	High-Speed Switching N-P-N Power Transistor	TO-39
2N3055H	General-Purpose Silicon N-P-N Power Transistor	TO-204 MA

•D, E, F, and K packages
Note: Package designator (T) indicated TO-5 package with straight leads.

Special Analog Function Circuits

RCA BiMos Single-Chip Detector/Alarm System

Type No.	Description	Electrical Characteristics @ T_A = 25°C				Pkg. No. of Pins
		Operating Voltage Range (V)	Input Leakage Current Max. (pA)	Standby Battery Current Typ. (μA)	Available Reference Source Current Min. (μA)	
CA3164A	With Integral Drivers for Mechanical or Piezoelectric Horn Alarms	7-11	1	8•	5	14E

Operating Temperature Range (T_A): 0 to +50°C
•Adjustable to 5 μA

RCA Four Quadrant Multiplier

Type No.	Description	Electrical Characteristics @ T_A = 25°C					Pkg. No. of Pins
		Power Operation Capability (V)	Power Supply Sensitivity Typ. (mV/V)	Accuracy Max. (%)	Linearity Max. (%)	Bandwidth -3dB Typ. MHz	
CA3091	• Multiplier • Divider • Squarer • Square Rooter • Provides Output Voltage that is the Product of Two Input Voltages	±6 (4mW drain)	36	±4	3.0	4.4	14D

Operating Temperature Range (T_A): -55 to +125°C

GE/RCA Solid State

RCA Products

For other Harris Semiconductor Products, see pages 2715 thru 2775.

Military and Aerospace Products

GE Solid State is a leading supplier of high-reliability integrated circuits to the military and aerospace community. Years of commitment, dedication, experience, and know-how make possible shipment of hundreds of thousands of quality high-reliability microcircuits annually.

MIL-Specification Product JAN, SMD, and DESC Specifications

GE Solid State offers the following RCA CMOS ICs as JAN product (MIL-M-38510) as a first option to a customer. When JAN product is not available, Standard Military Drawings product (SMD) and DESC/MIL Drawing product are offered.

The CD4000B Series of High-Voltage CMOS Logic ICs, is offered in a number of JAN Class S and Class B MIL-M-38510 slash-sheet types. The CD54HC/HCT series of High-Speed CMOS Logic ICs is also available as JAN, SMD, and DESC product. The CD54AC/ACT Series of Advanced CMOS Logic ICs is now available as a standard military drawing product. JAN product for these ICs is being considered for early availability.

CMOS Integrated Circuits

RCA JAN Qualified-Parts Listing and MIL-M-38510 Detail Specifications (Slash Sheets)

Detail Specification	RCA Type	Available JAN Devices				Detail Specification	RCA Type	Available JAN Devices			
		S	B	1 x 10^5 Rad Si	1 x 10^6 Rad Si			S	B	1 x 10^5 Rad Si	1 x 10^6 Rad Si
MIL-M-38510/65001	CD54HC00		A			MIL-M-38510/05701	CD4006A		A		
65002	CD54HC10		I			02	CD4014A		A		
65101	CD54HC02		I			03	CD4015A		A		
65201	CD54HC32		I			04	CD4021A		A		
65203	CD54HC08		I			05	CD4031A		A		
65403	CD54HC373		I			06	CD4034A				
65701	CD54HC04		I			51	CD4006B				
65705	CD54HC244		I			52	CD4014B	A	A	A	A
65755	CD54HCT244		I			53	CD4015B	A	A	A	A
MIL-M-38510/05001	CD4011A		A			54	CD4021B	A	A	A	
02	CD4012A		A			55	CD4031B				
03	CD4023A		A			56	CD4034B				
51	CD4011B	A	A	A	A	MIL-M-38510/05801	CD4016A				
52	CD4012B	A	A	A	A	02	CD4066A				
53	CD4023B	A	A	A	A	51	CD4016B				
MIL-M-38510/05101	CD4013A		A			52	CD4066B	A	A	A	A
02	CD4027A		A			MIL-M-38510/05901	CD4028A				
03	CD4043A					51	CD4028B	A	A	A	
51	CD4013B	A	A	A	A	MIL-M-38510/17001	CD4081B	A	A	A	
52	CD4027B	A	A	A	A	02	CD4082B		A	A	
53	CD4043B					03	CD4073B		A	A	
MIL-M-38510/05201	CD4000A		A			MIL-M-38510/17101	CD4071B	A	A	A	A
02	CD4001A		A			02	CD4072B		A	A	
03	CD4002A		A			03	CD4075B	I	A	A	A
04	CD4025A		A			MIL-M-38510/17201	CD4085B	A	A	A	A
51	CD4000B					02	CD4086B	A	A	A	A
51	CD4001B	A	A	A		03	CD4070B	I	A	A	A
53	CD4002B	A	A	A		04	CD4077B		A	A	
54	CD4025B	A	A	A	A	MIL-M-38510/17301	CD4514B				
MIL-M-38510/05301	CD4007A		A			02	CD4515B				
02	CD4019A		A			03	CD4532B				
03	CD4030A					04	CD4555B				
04	CD4048A					05	CD4556B				
51	CD4007UB	A	A	A	A	MIL-M-38510/17401	CD4069UB	A	A	A	A
52	CD4019B	A	A	A		02	CD40107B				
53	CD4030B	A	A	A	A	03	CD4502B	A	A	A	
54	CD4048B					04	CD40109B				
MIL-M-38510/05401	CD4008A					MIL-M-38510/17501	CD4076B				
51	CD4008B	A	A	A		02	CD4095B				
MIL-M-38510/05501	CD4009A					03	CD4096B				
02	CD4010A					04	CD4098B		A	A	
03	CD4049A		A	A		05	CD40174B				
04	CD4050A		A	A		MIL-M-38510/17601	CD4099B		A	A	
05	CD4041A					02	CD4508B				
51	CD4009UB					MIL-M-38510/17701	CD4093B				
52	CD4010B					02	CD40106B				
53	CD4049UB	A	A	A	A	MIL-M-38510/17801	CD4067B				
54	CD4050B	A	A	A	A	02	CD4097B				
55	CD4041UB	A	A	A		03	CD40257B				
MIL-M-38510/05601	CD4017A		A								
02	CD4018A										
03	CD4020A		A								
04	CD4022A		A								
05	CD4024A		A								
51	CD4017B	A	A	A							
52	CD4018B	A	A	A	A						
53	CD4020B	A	A	A	A						
54	CD4022B	A	A	A	A						
55	CD4024B	A	A	A							

A = available P = proposed qual. I = in process (MIL-M-38510 detailed electrical test programs are available.)

RCA Products

For other Harris Semiconductor Products, see pages 2715 thru 2775.

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Military and Aerospace Products

RCA Compliance to MIL-STD-883, Rev. C

GE Solid State provides the RCA CD4000B, CD54HC/HCT, and CD54AC/ACT CMOS IC Series parts that are in full compliance with MIL-STD-883C. Paragraph 1.2.1 Class S and Class B product are provided that meet the requirements of this paragraph and are designated as follows:

a) Slash MS (....MS) parts meet Class S requirements when Group B conformance testing is performed.
b) Slash 3A (....3A) parts meet Class B requirements. RCA also provides parts that meet the requirements of MIL-STD-883, Paragraph 1.2.2. These CMOS IC parts have the designation Slash 3 (..../3) and meet most of the requirements of a Class B part.

High-Reliability CD4000B-Series High-Voltage CMOS ICs

The RCA high-reliability CD4000B series of high-voltage CMOS integrated circuits consists of a broad range of SSI, MSI-1, and MSI-2 (LSI) functions from simple gates to complex counters, registers, and arithmetic circuits. Specific design features for CMOS devices and the performance advantages of CMOS technology — low power consumption, high noise immunity, high speed, high fanout, TTL and DTL logic compatibility, excellent temperature stability, and fully protected inputs and outputs — provide the logic system designer with a capability to achieve outstanding performance, high reliability, and simplified circuitry in a wide variety of equipment designs.

GE Solid State offers radiation-hardened RCA CD4000-series CMOS integrated circuits tested to withstand total ionizing radiation dosages of 1 x 10^5 rads (Si) — R-suffix types, and 1 x 10^5 rads (Si) — H-suffix types. These radiation tolerances are achieved by special process controls imposed during wafer fabrication.

RCA radiation-hardened types may be screened to MIL-M-38510 Class S. The specified levels of radiation resistance are verified Group E Sub-group 2 of Method 5005 and tested according to Method 1019 of MIL-STD-883.

Features

- 100% tested for quiescent current at 20V
- Maximum input current (leakage) of 1μA at 18 V over full package-temperature range; 100 nA at 18 V at 25°C
- Standardized symmetrical output characteristics
- 5-V, 10-V, and 15-V parametric ratings
- Noise margin (over full package-temperature range): 1 V at V_{DD} = 5 V, 2 V at V_{DD} =10 V, 2.5 V at V_{DD} = 15 V
- Meets all requirements of JEDEC Standard No. 13B, "Standard Specifications for description of 'B' Series CMOS Devices"

The 54HC/HCT High-Reliability Product Line

The RCA HC/HCT series of high-speed CMOS integrated circuits includes a functionally complete set of LSTTL equivalent types and selected equivalent CMOS CD4000 series types. The CD4000 series types selected are unique to the CMOS process. These types are readily produced by the highly versatile CMOS technology, but cannot be implemented by the more restrictive bipolar technology. Each CMOS circuit function is offered in two basic logic series, as follows:

1. **CD54/HCTXXXX-series types** — feature LSTTL input-voltage-level compatibility and provide high-speed CMOS direct drop-in replacements of LSTTL devices.
2. **CD54/HCXXXX-series types** — feature CMOS input-voltage-level compatibility and are intended for use in new second-generation all-CMOS systems.

In addition, the RCA high-speed family contains a third category, **CD54/HCUXX**, which includes unbuffered types intended for linear or high-speed oscillator applications.

The HC/HCT family consists of a comprehensive set of buffers, transceivers, and registers that are popular in computer systems. A wide variety of popular logic, MUX's, encoders/decoders, counters, arithmetic units, multivibrators, display drivers, and phase-lock loops complete the family.

HC/HCT FAMILY FEATURES

- *Functionally and pin compatible with industry 54 and CD4000B-series types.*
- *CMOS outputs for maximum noise margins.*
- *Fan-out (over temperature):*
  Standard Outputs - 10 LSTTL loads
  Bus-Driver Outputs - 15 LSTTL loads
- *Military temperature range:*
  CD54HC/HCT/HCU: -55 to +125°C
- *Balanced propagation and transition times.*
- *Significant power reduction compared to LSTTL logic.*

CD54HCXXXX
- *2 to 6V operation.*
- *High noise immunity: N_{IL} = 30%, N_{IH} = 30% at V_{CC} = 5V.*

CD54HCTXXXX
- *4.5 to 5.5V operation.*
- *Direct LSTTL input logic compatibility*
  V_{IL} = 0.8V (max), V_{IH} = 2.0V (min)
- *CMOS input compatibility*
  I_{IL}, $I_{IH} \leq 1\mu A$ at V_{OL}, V_{OH}

RCA Products

For other Harris Semiconductor Products, see pages 2715 thru 2775.

Military and Aerospace Products

The 54AC/ACT High-Reliability Product Line

The RCA-Series of Advanced CMOS Logic Integrated Circuits is comprised of a broad range of logic types equivalent in performance and speed to FAST*, AS† (Advanced Schottky), and S† (Schottky) bipolar types, but superior in that they require substantially less power in logic operations. Each CMOS circuit function is offered in two basic logic series, as follows:

1. **CD54ACTXXX/3A-series types.** These types feature TTL input-voltage-level compatibility and, using the same standardized pin-outs, provide reduced power-consumption alternatives to the very high power consumption of the FAST, AS, and S bipolar logic series types.
2. **CD54ACXXX/3A-series types.** These types feature CMOS input-voltage-level compatibility and, using the same standardized pin-outs, provide enhanced system performance (better system noise margin) at speeds similar to those of FAST, AS, and S logic series types.

The AC/ACT family consists of a comprehensive set of octal buffers, octal latches, octal flip-flops, octal transceivers in both the classic 200-series pin-out and the newer 500-series flow-through pin-out. In addition, selected SSI inverters, gates, flip-flops, Schmitt triggers, plus selected MSI counters, registers, multiplexers, decoders, arithmetic functions, and FIFO's are included for a total of 126 circuits, in both the ACT and AC series; more types are planned.

*FAST is a Trademark of Fairchild Semiconductor Corp.
†AS and S are Trademarks of Texas Instruments.

AC Series Features

Following are the special features of the AC series of Advanced CMOS Logic ICs.

- 1.5- to 5.5-volt operation
- High noise immunity:
  $N_{IL} = N_{IH} = 30\%$ for $V_{CC} = 3$ to 5 volts
  $N_{IL} = N_{IH} = 20\%$ for $V_{CC} = 1.5$ to 3 volts

/3A Family Features

Following is a listing of the features of the ACL family of logic devices.

- Fully compliant to MIL-STD-883, Para. 1.2.1.
- Functionally and pin-compatible with industry 54 bipolar types in the FAST, AS, and S series.
- CMOS rail-to-rail output swing for maximum noise margins.
- Fanout (over temperature):
  2400 ACL Loads
  15 FAST Loads
  48 AS Loads
- Military operating-temperature range
  Ceramic (CERDIP) 54 series: -55 to +125°C
  NOTE: FAST, AS, and S series types are rated for only 0 to +70°C.
- Balanced propagation and output transition times.
- Significant power reduction compared to FAST, AS, and S TTL logic, resulting in improved equipment reliability.
- Outputs reliably drive 75-ohm lines (54 series) without need for terminations.
- Meets JEDEC Standard No. 20; presently, in draft (non-issued) form.
- Octal types have typically a 1-volt peak simultaneous switching-voltage transient, similar to FAST series.
- CMOS input compatible.

ACT Series Features

Following are the special features of the ACT series of Advanced CMOS Logic ICs.

- 4.5 to 5.5-volt operation
- Direct TTL input logic compatible:
  V_{IL} = 0.8 volt (max.); V_{IH} = 2 volts (min.)
- Similar to FAST specifications except for the 64 milliampere I_{OL} of FAST drivers

High-Reliability Slash-Series LSI Products

The RCA high-reliability slash-series of CMOS LSI microprocessors, memories, and peripherals are ideally suited for military applications such as mobile ground equipment that must be battery operated and exposed to harsh environments. Use of a highly reliable, all CMOS LSI technology provides low power operation throughout the military temperature range.

The 'Slash 3' suffix following the type designation indicates that the devices are screened to military specifications as described in the screening sequence.

Features:

- Low power consumption
- Fully static
- Single power supply
- Full temperature range
- High noise immunity
- Complete family which includes RAMs, ROMs, and I/Os
- Full CMOS CDP1802A microprocessor

CDP1800 Series

The RCA CDP1800 series offers a complete line of CMOS microprocessor and associated memory and peripheral devices. The heart of the series is the CDP1802A central processing unit (CPU). This unit, which features CMOS register-based architecture, offers 16 internal registers to facilitate data manipulation and to reduce the need for additional devices. The need for external devices is even further reduced by use of on-chip clock, DMA, and single-phase operation.

The microprocessor uses CMOS technology, designed on a single chip to maintain low power drain intended for multi-system applications requiring general-purpose CPUs, large memory address space, and extensive external I/O for use with optimized peripherals.

The RCA CDP1800-series memory/microprocessor product line offers the system designer exceptional flexibility in hardware/software tradeoffs. In addition this product line includes a programmable I/O, universal asynchronous receiver-transmitter (UART), directly interfaceable random-access memories (RAMs) and read-only memories (ROMs).

RCA Products

For other Harris Semiconductor Products, see pages 2715 thru 2775.

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Military and Aerospace Products

The RCA CDP1800 slash(/) series memories are designed for use in memory systems where high speed, low operating current, and simplicity in use are desirable. These devices feature excellent noise immunity. These types have separate data inputs and outputs and utilize a single power supply.

General-Purpose Memories

In addition to the memories designed to interface directly with CDP1800-series, a complete line of RCA general-purpose memories are also available. These memories include industry-standard ROMs that can be mask-programmed to meet customer application requirements. These ROMs feature low-power CMOS technology with high-noise immunity and full-temperature-range characteristics.

The list of memories also includes fully static CMOS RAMs with densities up to 32k-bytes, low operating power, low standby current, and memory retention for 2- to 2.5-volt minimum standby battery voltage.

Radiation-Hardened CMOS/SOS Static RAMs

RCA Rad-Hard memories use CMOS/SOS technology and are designed for use in memory systems where low power and simplicity in use are desired. The CMM5114 and CMM5104 have TTL compatibility on all I/O terminals. The CMM6167 is CMOS compatible.

Radiation Features

CMOS/SOS technology permits operation in high-radiation environments. It is insensitive to neutrons, cannot latch up at any dose rate and is resistant to single-event upset caused by cosmic rays or heavy ions.

Total Dose	$\geq 1 \times 10^5$ Rads (Si)
*Latchup	Not Possible
*Transient Upset	$\geq \times 10^{10}$ Rads (Si)/Second
*Transient Survival	$\geq 1 \times 10^{12}$ Rads (Si)/Second
Single-Event-Upset (SEU)	Less than 10^{-9} Errors/Bit-Day (Typically)

*Inherent property of SOS

The Epic Family

The emulation and programmable IC family, composed of several CMOS/SOS chips, is a high-performance microcomputer "building block" set which can be used to replace existing minicomputers by emulating (adapting) the minicomputers' software for a wide variety of new applications with unique architecture, at comparable or increased speed and greatly reduced power.

The EPIC family contains a number of LSI CMOS/SOS chips which, in various combinations, can be configured into microprogrammable computers with great flexibility of architecture, data format, and overall capability. In addition to all the advantages of CMOS technology, the SOS technology offers excellent tolerance to radiation, an important factor in aerospace applications.

The EPIC family centers around an 8-bit slice, two controllers or sequencers, an interrupt controller, an 8 x 8 bit multiplier slice, RAM and ROM, and a number of automated gate arrays that integrate the logic required to join the major system blocks into a minimum parts computer system.

Available Devices

General Processor	GP001
Mask-Programmable ROM (512 x 8)	GP301
Mask-Programmable ROM (256 x 16)	GP302
Mask-Programmable ROM (512 x 16) with Pipeline Register	GP305
Emulating Controller	GP501
"2910" Type Controller	GP502
Multiplier (8 x 8)	GP503
Voltage Level Converter and Buffer	GP511
Double Address Select Unit	GP514
Double Register Select Unit	GP515
Bus Interface Unit	GP516
Interrupt Control Unit	GP517

Applicable Memories: Static CMOS/SOS

RAM (4096 x 1)	CMM5104/1RZ
RAM (1024 x 4)	CMM5114/1RZ
RAM (16384 x 1)	CMM6167/1RZ

Rad-Hard High-Speed CMOS/SOS Logic-HCS/HCTS

The high speeds and low quiescent power dissipation that characterize the RCA HC/HCT family are made possible by utilizing a three-micron, self-aligned silicon-gate CMOS process. The three-micron process minimizes the internal parasitic capacitances of the circuit, which results in increased switching speed.

The polysilicon gates of the transistors are deposited over a thin gate oxide before the source and drain diffusions are defined. Ion implantation is then used to form the source and drain areas, with the polysilicon gates acting as a mask for the implantation. The source and drain are automatically aligned to the gate, hence the expression "self-aligned-gate" process. In this manner, gate-to-source and gate-to-drain capacitances are minimized.

HCS/HCTS Structure

The basic polysilicon gate structure described above, is used for the HCS/HCTS (CMOS/SOS) family except that the devices are made on epitaxial Si islands on a sapphire substrate. This technique greatly reduces device capacitance and completely eliminates latch-up. A special SOS process is also used to achieve the megarad hardness levels.

Circuit functions are offered in two basic logic series, as follows:

1. HCTSXXXX-series types — feature LSTTL input-voltage-level compatibility and provide high-speed CMOS direct drop-in replacements of LSTTL devices.
2. HCSXXXX-series types — feature CMOS input-voltage-level compatibility and are intended for use in CMOS systems.

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HCS/HCTS Derived from HC/HCT Layouts

- Optimized output device size ratios for CMOS/SOS process parameters
- Optimized input device size ratios to meet:
  V_{IH} = 2.5 Volts
  V_{IL} = 0.8 Volts
- ESD protection by use of "closed" (edgeless) input and output transistors as well as CMOS/SOS-compatible resistor/diode circuitry
- 125 functions from six basic masks

HCS/HCTS Family Features

- New High-Speed, Low-Power Radiation-Hardened CMOS Logic Family
- 20X Faster Than 4000 Series
- SOS Based
- Wide Choice of Logic Functions Based on Bulk High-Speed CMOS Family
- Class S Qualified

GE/RCA Application Specific ICs (ASICs)

The GE/RCA semicustom and custom programs provide the hardware and software systems needed to automate the design of application-specific integrated circuits (ASICs). The ASIC devices described are supplied in high-reliability versions processed and screened to MIL-STD-883, Class S and B requirements.

Full Range of Cost-Effective Design Elements

Standard Cells

• SC1000	6-micron, high-voltage library, 12-volt operation
• SC2000	CMOS II, single-level metal, 2.5 micron▲, 2-ns gate delays
• SC2500	CMOS II, double-level metal, 2.5 micron▲, 2-ns gate delays
• SC2800	SOS, rad-hard library, 2.5 micron▲, 2-ns gate delays
• SC3000	CMOS III, double-level metal, 1.5 micron▲, 1-ns gate delays
• SC3500	CMOS IIIA, double-level metal, 1.25 micron▲, 0.8 ns gate delays.
• SC4000	CMOS IV, double-level metal, 1.0 micron▲, 0.75-ns gate delays

Gate Arrays

• PA30000 Series	2 micron▲, double-level metal, SOS
• PA40000 Series	3 micron, single-level metal, bulk Si
• PA50000 Series	3 micron, double-level metal, bulk Si
• PA60000 Series	4 micron, single-level metal, SOS
• CGA10 Series	2 micron, double-level metal, bulk Si
• CGA200 Series	1.5 micron, double-level metal, bulk Si

▲Effective Channel Length

Fully Supported Design Automation Software

MIMIC — Logic simulation, automatic test pattern generation and fault analysis plus user-definable behavioral modeling with the industry's most extensive hazard analysis.

FASTRACK — The most automated design system in the industry. Converts logic net list to pattern generator types.

MP2D — Automated placement and routing of interconnections for Standard Cells.

MERLYN — Automatic placement and routing of interconnections for Gate Arrays with utilization capability exceeding 75 percent.

AFTER — Test program generation.

CONCERT — Connectivity check and parasitic capacitance and resistance extraction of interconnects for both single- and double-level metal.

Accessible from Daisy Systems, Valid Logic, and Mentor Graphics workstations as well as P-CAD and Futurenet on IBM PC.

Gate Arrays

Through the gate-array approach, designers customize gate arrays, which are matrices of uncommitted transistors, to individual circuits by specifying metal interconnections among transistors in an array.

A GE/RCA gate array is a CMOS LSI chip consisting of p devices, n devices, and tunnels in a repetitive-ordered structure on either a silicon or a sapphire substrate. All device nodes (gates, drains, and sources) are accessible. Gate arrays are available for both double-level and single-level metallization.

In double-level-metal gate arrays, a sequence of four "personalization" masks (contact, first metal, via, and second metal) defines the interconnect pattern that implements the required logic function. In single-level-metal gate arrays, a single personalization metal mask defines the logic function.

Although some number of gates may be inaccessible because of interconnect restrictions, the GE/RCA automatic design process permits utilization of 80% of the total gates available for any one application with single-level metal and in some instances as high as 95% with double-level metal (PA50000).

Gate arrays are a proven high-reliability, low-cost solution to semicustom LSI circuit design. Because gate arrays use standard chips customized by one or four personalization masks, design turnaround time is short and the correction of potential system-integration errors or design change is easily accomplished.

Standard Cells

In the standard-cell approach, designers prepare a logic diagram using the functions available in the cell library; each cell has been predesigned and laid out using individual transistors. The logic design is then entered into the computer system and verified through simulation Placement of the cells in rows with variable-width channels between them for interconnections and routing of interconnections are performed automatically with a more efficient use of silicon. When the standard-cell circuit is manufactured, each of its layers is fabricated independently.

Standard cells usually provide greater flexibility, versatility, and performance compared to gate arrays.

RCA Products

For other Harris Semiconductor Products, see pages 2715 thru 2775.

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Military and Aerospace Products

Radiation-Hardened CMOS/SOS ASICs

The RCA high-reliability radiation-hardened CMOS silicon-on-sapphire (CMOS/SOS) makes possible the design of Application Specific Integrated Circuits (ASICs) capable of withstanding severe radiation and environmental effects encountered in such demanding applications as strategic missiles and survivable military satellite systems.

CMOS/SOS ASICs are designed to withstand total dose radiation of at least 100 krads (Si) and can be screened to modified MIL-M-38510, Class S requirements. CMOS/SOS ASICs can also be screened to modified Class B levels for ASIC products required to withstand less demanding conditions, such as battlefield tactical radiation levels and avionic system requirements, at considerably lower cost.

We welcome your inquiries on custom LSI. Our extensive experience, on both military and commercial programs, can provide the necessary background in design, processing, and testing to assure a scheduled, on-budget, successful custom high-reliability radiation-hardened CMOS/SOS ASIC.

Radiation-Hardened Gate Arrays

Gate Array Series	Technology	Typical Gate Delay at 5 V (ns)	Operating Voltage Range (V)	Total Number of Gates	RCA Family Series Number
PA60000	4-micron Single-level Metal, Si-Gate CMOS/SOS	2	3-10	1313	61200
PA30000	2-micron (Leff) Double-Level Metal, Si-Gate CMOS/SOS	1.8	4.5-5.5	2224 3192 4202 6000	32200 33200 34200 36000

Radiation-Hardened Standard Cells

Standard Cell Family	Features	
SC2800 Family Single-Level Metal, Si-Gate CMOS/SOS	Gate Length	3 μm
	Gate Oxide Thickness	500 A
	Number of Cells	46 MP2D
	Performance	2 ns at 5.0 V, 25°C typical 1 ns at 7.5 V, 25°C typical
	Operating Voltage	4 - 8 volts
	Interconnect	SLM, N+ Poly with 20 ohms/square
	Chip Size	
	Density	8 mil^2/transistor
	Gates	3300 max.
	Pads	132 max.
	Area	320 x 320 mils

RCA High-Reliability CA3000 Slash-Series Linear ICs

RCA-CAXXXX "Slash" (/) Series types are high-reliability linear integrated circuits intended for applications in aerospace, military, and industrial equipment. These devices are electrically and mechanically similar to the standard types described in commercial databook SSD-240C entitled "Integrated Circuits for Linear Applications," but are specially processed and tested to meet the electrical, mechanical, and environmental test methods and procedures established for microcircuit devices.

Screening levels /1, /3, and /3W are based on guidelines established for military product. Chip versions of the standard product and quality conformance tests are offered on a custom basis only.

Radiation Effects on Linear ICs

There is no dedicated process for radiation hardening of the Linear ICs. Gammacell exposure of various devices representing both the bipolar and BiMOS wafer technologies has resulted in the following information which is useful for design guidance when considering radiation hardness.

Devices processed under bipolar technologies tend to withstand Gamma radiation to exposure levels of 1 x 10^5 rads (Si) prior to experiencing significant parameter degradation, while those processed with BiMOS techniques can withstand Gamma Ray exposure levels up to 1 x 10^4 rads(Si) before significant parameter degradation takes place. We do not guarantee rad-hard levels for linear ICs.

RCA Products

For other Harris Semiconductor Products, see pages 2715 thru 2775.

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Digital to Analog Converters

Intersil supplies digital-to-analog converters (D/A converters) with 8-bit, 10-bit, 12-bit, 14-bit and 16-bit resolution. All are four-quadrant multiplying D/A converters using thin-film resistors and CMOS circuitry for high accuracy and low power dissipation. All are microcomputer compatible, with input protection against damage from electrostatic discharge.

Type	Digital Input Format	Settling Time (To 0.05% FS)	Output Current (Max)	Non Linearity% FS (Suffix)	Gain Error (% FS)	Gain Linearity Tempo PPM/°C	Power Supply $V_{(Typ)}$ I(Max)
8-BIT							
AD7523	Binary/ Offset Binary	200 ns (Max)	$\frac{\pm V_{REF}}{10K\Omega}$ A	0.2% (J) 0.1% (K) 0.05% (L)	1.5% (Max)	10 2	$\frac{+15V}{100\mu A}$
10-BIT							
AD7520* AD7530	Binary/ Offset Binary	500 ns (Typ)	$\frac{\pm V_{REF}}{10K\Omega}$ A	0.2% (J) 0.1% (K) 0.05% (L)	0.3% (Max)	10 2	$\frac{+15V}{2mA}$
AD7533	Binary/ Offset Binary	600 ns (Typ)	$\frac{\pm V_{REF}}{10K\Omega}$ A	0.2% (J) 0.1% (K) 0.05% (L)	1.4% (Max)	10 2	$\frac{+15V}{2mA}$
12-BIT							
AD7521* AD7531	Binary/ Offset Binary	500 ns (Typ)	$\frac{\pm V_{REF}}{10K\Omega}$ A	0.2% (J) 0.1% (K) 0.05% (L)	0.3% (Typ)	10 2	$\frac{+15V}{2mA}$
AD7541	Binary/ Offset Binary	1 μs (Max)	$\frac{\pm V_{REF}}{10K\Omega}$ A	0.02% (J) 0.01% (K) 0.01% (L)	0.3% (Max)	— 2	$\frac{+15V}{2mA}$
14-BIT							
ICL7134	Binary μ 2's Complement B	3 μs (Max)	$\frac{\pm V_{REF}}{10K\Omega}$ A	0.1% (J) 0.006% (K) 0.003% (L)	0.02% (J) 0.012% (K) 0.006% (L)	5 1	$\frac{+15V}{0.5mA}$

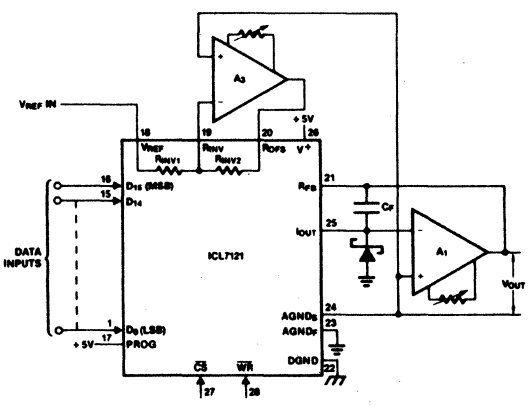
*AD7530 and AD7531 are identical to AD7520 and AD7521, respectively, except for output leakage current and feed-through specifications.

GE/RCA Solid State

ICL7121
16-Bit μP-Compatible D/A Converter

This high-performance 16-bit D/A converter achieves 0.003% linearity without laser trimming by combining the converter with a unique on-chip PROM-controlled correction circuit. This insures long-term stability and accuracy even over the full military temperature range. Silicon-gate CMOS circuitry keeps the power dissipation to a very low 25 mW.

Designed and programmed for bipolar operation, it can be connected to provide a true 2's complement input transfer function without any external resistors. Microprocessor bus interfacing is eased by standard memory WRite cycle timing and control signal use. The device is available in a 28-pin CERDIP package in both 0°C to +70°C, and −55°C to +125°C temperature ranges.



ICL7121 Example of Bipolar, Four Quadrant Operation

For other Harris Semiconductor Products, see pages 2715 thru 2775.

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The proliferation of microprocessors and the general swing to digital signal processing has caused an explosion in the need for data acquisition products. In turn, the associated data translation requirements from the analog world to digital format, and vice versa, have spurred considerable effort toward making A/D-D/A converters progressively smaller, cheaper, and more reliable. Toward that end, Intersil has developed a family of integrated circuits designed to meet the varying requirements of the system designer.

All of Intersil's converters are fabricated using CMOS technology, which equates, inherently, to extremely low power consumption. All maximize on-chip componentry for the intended application in order to reduce the external component requirements to a minimum.

To facilitate acquaintance with Intersil products, a number of A/D converters are available in the form of low-cost Evaluation Kits. The Kits combine the specified converter with a number of additional components required to assemble a functional subsystem. They include components PC board and appropriate assembly instructions.

Content:

A/D Converter Systems
- Digital Multimeter
- Instrumentation
- Bargraph

A/D Converters
- Display Type
- μP Type
- Evaluation Kits

D/A Converters

Analog To Digital Converters

A/D Converters with Display Drivers

Integrating A/D Converters are characterized by high inherent accuracy, excellent noise rejection, non-critical associated components and low cost. They are relatively slow with conversion rates up to 30 conversions per second. All Intersil integrating converters provide fully precise Auto-Zero, Auto-Polarity (including ± null indication), single reference operation, very high input impedance, true input integration over a constant period (for maximum EMI rejection), fully ratiometric operation, overrange indication and a medium-quality built-in reference.

3¾ Digit LCD 7-Segment Displays — ICL7139
For Low-Cost Autoranging Digital Multimeters — ICL7149

These monolithic autoranging multimeter circuits always display the results of a conversion on the correct range. Measure AC and DC voltage, DC current and resistance in the following ranges:

DC Voltage — 400mV, 4V, 40V, 400V
AC Voltage — 400V (ICL7139)
(Optional ac circuit with 2 ranges (ICL7149))
DC Current — 4mA, 40mA, 400mA, 4A
Resistance — 4K, 40K, 400K, 4M

On-chip duplex display drive includes three decimal points and 11 annunciators. Less than 20mW power dissipation provides 1000 hours typical battery life. Continuity output drives piezoelectric beeper. Guaranteed zero reading for 0 Volts input on all ranges.

101-Segment LCD Bargraph A-D Converter — ICL7182

The ICL7182 is a complete analog-to-digital converter that directly drives a multiplexed liquid crystal display. Included are a charge-balance A/D converter, a 2.56V bandgap reference, display decode and driver, and a 50KHz oscillator. A complete analog bargraph generator requires only the addition of an external display, two passive components and a 350μA, 5V power source.

For other Harris Semiconductor Products, see pages 2715 thru 2775.

4½ Digit LCD 7-Segment Displays — ICL7129
For High Quality Battery Operated Instruments

Very high performance A/D Converter for direct drive of multiplexed LCDs. Ideal for high-resolution, hand-held digital multimeters and other battery powered (9V) instruments. Accuracy is better than 0.005% of full scale, with resolution down to 10μV per count. Overrange and underrange outputs permit design of autoranging instruments with 10:1 range changing input. Instant continuity check gives both visual indication and a logic-level output for enabling an external audible transducer. Provisions for detection and indication of Low Battery condition.

For 3½ Digit LCD/LED 7-Segment Displays — ICL7106/7116, ICL7136/7126, ICL7137-7107, ICL7117

These 3½-digit A/D Converters contain all the necessary active devices on a single CMOS integrated circuit. Included are A/D Converters, 7-segment decoders, display drivers, a reference and a clock. All feature auto-zero to less than 10μV, zero-input drift of less than 1μV/°C, input bias current of 10pA max., and rollover and linearity errors of less than one count. True differential inputs and reference provide wide applications versatility over a temperature range from 0 to +70°C.

For Liquid Crystal Displays	**ICL7106** — Direct drive; 0.1 to 15 conversions per second; supply current = 1.8mA max. **ICL7116** — Similar to above, but features a Hold Reading input which allows indefinite retention of a display reading. **ICL7136** — Low-power version of ICL7106, but with maximum supply current of only 100μA gives 8000 hours typical 9V battery life. 0.1 to 4 conversions per second. **ICL7126** — Earlier version of ICL7136. Recommended for exact replacement requirement only.
For LED Displays	**ICL7137** — Low-power, direct drive ADC for common anode, 7-segment LED displays. Requires positive and negative 5V supply voltages, with supply current of less than 200μA. 0.1 to 4 conversions per second. **ICL7107** — Direct drive ADC for common anode, 7-segment LED displays. Requires positive and negative 5V supply voltages. **ICL7117** — Similar to ICL7137, but requires 1.8mA (max.) of supply current and provides up to 15 conversions per second. Hold Reading allows indefinite retention of display reading.

A/D Converter Evaluation Kits

The following Evaluation Kits are available to permit rapid assembly, testing and evaluation of specific A/D converters. Each Kit comes complete with a prewired printed circuit board and all necessary components (except batteries) for a suitable demonstration circuit. Assembly and operating instruction are supplied.

ICL7129EV/Kit

This Kit permits evaluation of the Intersil ICL7129 4½ digit, LCD, 7-segment display in a functional DC digital voltmeter circuit. It includes the A/D converter IC, a liquid crystal display, a 120KHz crystal, a voltage reference IC and all necessary passive components and hardware items.

ICL7139EV/Kit
ICL7106/07EV/Kit
ICL7136EV/Kit

ICL7106EV/Kit, ICL7107EV/Kit

To ease evaluation of these unique circuits, Intersil offers kits which contain all the necessary components to build a 3½ digit panel meter. Two kits are offered, the ICL7106EV/Kit and the ICL7107EV/Kit. Both contain the appropriate IC, a circuit board, a display (LCD for the ICL7106EV/Kit, LEDs for the ICL7107EV/Kit), passive components, and miscellaneous hardware.

ICL7136EV/Kit

Intersil's ICL7136 is a low-power version of the 3½ digit LCD A/D converters. This Kit contains all the components necessary to build a battery-operated 3½ digit panel meter. It includes the A/D converter IC, a circuit board, liquid crystal display, passive components, and miscellaneous hardware.

ICL7139EV/Kit

This Kit uses the Intersil ICL7139 to build a complete 3¾ digit autoranging multimeter, capable of directly measuring voltage, current, and resistance. Included in the Kit are the ICL7139 IC, circuit board, liquid crystal display, and all necessary passive components and hardware.

ICL7182EV/Kit

With this Kit, the user can easily evaluate a 101 segment LCD bargraph A/D converter using Intersil's ICL7182. Everything necessary to build the completed circuit is included in the Kit: The ICL7182 IC, circuit board, 101 segment LCD, passive components, and miscellaneous hardware.

GE/RCA Solid State

Intersil offers a family of 4, 6, and 8-bit video-speed flash A/D converters designed for applications demanding both low-power consumption and high-speed digitization. Manufactured in CMOS/SOS technology provides superior power/speed performance.

Type	Resolution	Clock Rate	Power Dissipation	Integral Linearity	Differential Linearity
CA3304	4-bit	20MHz	30mW	¼ LSB	¼ LSB
CA3304A	4-bit	25MHz	35mW	¼ LSB	¼ LSB
CA3306L	6-bit	10MHz	55mW	½ LSB	½ LSB
CA3306	6-bit	15MHz	70mW	½ LSB	½ LSB
CA3306A	6-bit	15MHz	70mW	¼ LSB	¼ LSB
CA3318C	8-bit	15MHz	150mW	1½ LSB	+1/−.8 LSB
CA3318	8-bit	15MHz	150mW	1½ LSB	±0.8 LSB

For other Harris Semiconductor Products, see pages 2715 thru 2775.

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μP Compatible A/D Converters

Integrating

Intersil integrating μP-Compatible A/D Converters contain both monolithic versions and 2-chip sets, with up to 16-bit resolution. All utilize CMOS processing for lowest power consumption, and all have a guaranteed accuracy of 1 count.

4½ Digit A/D Converter with Multiplexed BCD Output — ICL7135

This precision A/D Converter is suitable for display applications as well as microprocessor and UART interface. Count accuracy of ±1 in 20,000 makes it ideal for the visual display DVM/DPM market, while added functions such as Strobe, Run/Hold, Busy, Overrange and Underrange allow operation in more sophisticated systems. Chip contains all necessary active devices except display drivers, reference and clock. All outputs are TTL compatible.

12-Bit μP-Compatible A/D Converter — ICL7109

This monolithic 12-bit binary A/D converter may be directly accessed under control of two byte-Enable inputs, and a Chip Select input, for a simple parallel-bus interface. A UART handshake mode operates in conjunction with industry-standard UARTs to provide serial data transmission. Operates at up to 30 conversions per second. Available in three temperature ranges: −55°C to +125°C, −25°C to +85°C, and 0°C to +70°C.

14/16-Bit μP-Compatible Two-Chip A/D Converter Sets — ICL8052/ICL7104, ICL8068/ICL7104

Available with 14-bit and 16-bit resolution, this two-chip set performs the analog signal processing on one chip (ICL8052 or ICL8068) and the switching and digital functions on the other (ICL7104). A combination of chips may be ordered for either 14-bit or 16-bit operation and for low-noise or low-leakage alternatives. All combinations, however, offer three-state, latched, binary outputs plus Polarity and Overrange. All combinations operate over a temperature range of 0°C to +70°C.

ICL7104-14 14-Bit ADC
ICL7104-16 16-Bit ADC
ICL8052 Low input leakage current (30pA max.) analog processing circuit. Typical noise = 30μV.
ICL8068 — Low noise (2μV typical) analog processing circuit. Input leakage current = 165pA.

Successive Approximation

Successive Approximation Converters are generally associated with high speed, ranging up to 100,000 conversions per second. All Intersil Successive Approximation Converters are μP compatible.

8-Bit A/D Converters for 8080A MPU Interface — ADC0802, ADC0803, ADC0804

This Successive Approximation A/D Converter was designed to operate with the 8080A or Z-80 microprocessor control bus via three-state outputs with no additional interfacing requirements, but permits easy interface to most other microprocessors. Differential analog input range is 0 to 5V with a single +5V supply. With a conversion time of less than 100 μs, it provides up to 8888 conversions per second with a clock frequency of 640KHz.

ADC0802 Total unadjusted error = ± 1/2LSB
ADC0803 Total full-scale adjust error = ± 1/2LSB
ADC0804 Total unadjusted error = ± 1LSB

14-Bit High-Speed A/D Converter — ICL7115

With a conversion speed of 40μs (max), this 14-bit ADC has a byte organized digital output for bus interface to 8 and 16-bit microprocessor systems. CMOS circuitry, thin-film resistors and an on-chip PROM calibration table combine to achieve 13-bit linearity (without laser trimming) and a very low (60mW) power dissipation. Available in three temperature ranges: 0°C to +70°C, −25°C to +85°C, and −55°C to +125°C.

Type	Resolution	Linearity	Output	Conversion Time	Power Supply Current from ±5V	Temp Range
ADC0804	8-bit	½ LSB	TTL, 3-State	100μS	+2.5mA	0 to +70° & −40 to +85° & −55 to +125°
ICL7109	±12-bit	1 LSB	TTL, 3-State	30mS	±1.5mA	0 to 70° & −25 to +85° & −55 to +125°
ICL7112	12-bit	½, 1 LSB	TTL, 3-State	30μS	±4mA	0 to 70° & −25 to +85° & −55 to +125°
ICL7115	14-bit	1, 2, 3 LSB	TTL, 3-State	30μS	±4mA	0 to 70° & −25 to +85° & −55 to +125°
ICL7104/8052	16-bit	1 LSB	TTL, 3-State	300mS	+15, 15mA −15, 14.2mA +5.6mA	0 to 70°
ICL7151	10-bit	½, 1 LSB	TTL, 3-State	10μS	+30, −15mA	0 to 70° & −40 to +85°
ICL7152	10-bit	½, 1 LSB	TTL, 3-State	5μS	+30, −15mA	0 to 70° & −40 to +85° & −55 to +125°
CA3310	10-bit	½, 1 LSB	TTL, 3-State	13μS	+3mA	

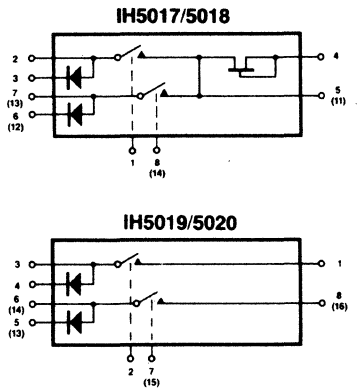
For other Harris Semiconductor Products, see pages 2715 thru 2775.

GE/RCA Solid State

Virtual Ground Switches, JFETs (P-Channel)

Each package contains up to four channels of analog gating designed to eliminate the need for external drivers. The odd-numbered devices are designed to be driven directly from TTL open-collector logic (15V). Each channel simulates a SPDT switch. The parts are intended for high-performance multiplexing and commutating use. All have turn-on/turn-off times of 500 ns and a leakage current ($I_{D(off)}$) of 0.2 nA.

Switch Configuration				Special Features	Switch Type	$r_{DS(on)}$ (Ω Max)
SPST	Dual SPST	Triple SPST	Quad SPST			
IH5021	IH5017	IH5013	IH5009	Common Output	P-JFET	100
IH5022	IH5018	IH5014	IH5010			150
IH5023	IH5019	IH5015	IH5011	Separate Output		100
IH5024	IH5020	IH5016	IH5012			150

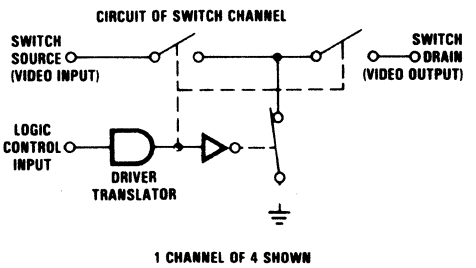


Examples of Common Output and Separate Output Switch Configurations

RF/Video Switches, CMOS

Designed for high-frequency operation, these switches utilize a "T" configuration where a shunt switch is closed when the switch is open. This provides superior isolation between input and output and greatly improves performance in the video and RF region. Switch attenuation varies less than 3 dB from dc to 100 MHz. Available in three (commercial and military) temperature ranges and in 14-pin plastic DIP and 10-pin TO-100 metal package.

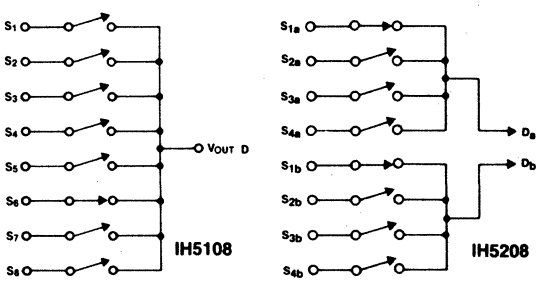
Switch Configuration		$r_{DS(on)}$ (Ω Max)	$I_{D(off)}$ (nA Max)	t_{ON} (ns Max)	t_{OFF} (ns Max)
Dual SPST	Quad SPST				
IH5341	IH5352	75	1.0	300	150



Internal Switch Configuration

Multiplexers

Intersil provides three multiplexer families — a standard IH6000 Family featuring low $r_{DS(ON)}$; an equivalent fault-protected IH5000 series which ensures that an OFF channel will remain OFF when the input exceeds the supply rails by up to ± 25 V, even with the supply voltage at zero; a multiplex/demultiplex unit with on-board data latches and control pins for microprocessor interface. All utilize CMOS technology for extremely low quiescent operating current.



Examples of Single-Ended and Differential Configurations

Mux Family	Special Features	$r_{DS(ON)}$ (Ω Max)	$I_{D(OFF)}$ (nA Max)	t_{ON} (ns Max)	t_{OFF} (ns Max)	Analog Voltage Range V_{Supply} = (±15V)	Configuration: 8 Channel Single Ended	Configuration: 4 Channel Differential	Configuration: 16 Channel Single Ended	Configuration: 8 Channel Differential
IH5000 Series	Industry standard pinouts, fault protection up to ±25V input, low leakage, low input current	900	1.0	1500	1000	−25 to +25 (Input)	IH5108	IH5208		
		1000	1.0	1500	1000	−25 to +25 (Input)			IH5116	IH5216
IH6000 Series	Industrial standard pinouts, low leakage, low $R_{DS(ON)}$ break before make switching	300	2.0	1500	1000	−14 to +14	IH6108	IH6208		
		600	2.0	1500	1000	−14 to +14			IH6116	IH6216
IH9108	High Voltage Multiplexer/ Demultiplexer with latches for μP based systems	120	2.5	2000	1000	−50 to +50	IH9108			

Future Products:

DG5_ _A Series		400	10	1500	1000	−15 to +15	DG508A	DG509A		
		400	10	1500	1000	−15 to +15			DG506A	DG507A
DG52_ Series	Multiplexer/Demultiplexer with latches for μP based systems	400	10	1500	1000	−15 to +15	DG528	DG529		
		400	10	1500	1000	−15 to +15			DG526	DG527

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Content:

General Purpose Analog Switches
Drivers for FET Switches
Low Cost, Virtual Ground Switch Family
RF/Video Switch Family
Multiplexers

General Purpose Analog Switches

Intersil offers two general-purpose switch lines, each with various switch configurations. The first consists of bipolar drivers controlling an associated set of field-effect switching transistors in a multi-chip structure that provides a wide choice of parameters at low cost. The second is a monolithic CMOS structure capable of improved performance and greater reliability. All have break-before-make switch action.

All switches are available in commercial and military temperature ranges. Package options include Plastic DIP, CERDIP, Flat Pack, Metal Can, and 16-lead S.O.I.C. (not all options are available for all device types).

General Purpose Analog Switches

Switch Family	Special Features	Switch Type	Switch Parameters				
			$R_{DS(ON)}$ (Ω Max)	$I_{D(OFF)}$ (nA Max)	t_{ON} (ns Max)	t_{OFF} (ns Max)	Analog Voltage Range (V_{SUPPLY} = ±15V)
Multichip							
DG123-125	Inverting/non-inverting logic inputs	PMOS	600	4	300	1000	—
DG126-145	Dual Channel/ Single Channel	N-JFET	10 15 30 50 80	10 10 1 1 1	1000 1000 600 600 600	2500 2500 1600 1600 1600	—
DG180-191	Mature, Industry-standard switch, JAN38510 Approved	N-JFET	10 30 75	10 1 1	300 150 250	250 130 130	−7.5 to +15 −7.5 to +15 −10 to +15
Monolithic							
DGM181-191	Monolithic replacement for DG180 family	CMOS	50 75	2.0 0.5	250 450	200 250	−15 to +15 −15 to +15
DG200/201	Industry-standard low cost	CMOS	70/80	2.0	1000	500	−15 to +15
DG201A DG202	Inverting Non-inverting	CMOS CMOS	175 175	1.0 1.0	600 600	450 450	−15 to +15 −15 to +15
DG211 DG212	Inverting Non-Inverting	CMOS	175	5.0	1000	500	−15 to +15
DG300A-303A	TTL compatible, low power	CMOS	50	1.0	300	250	−15 to +15
DG308A DG309	Normally-Closed Normally-Open	CMOS CMOS	100 100	1 1	200 200	150 150	−15 to +15 −15 to +15
IH5040-47 IH5052-53	Low quiescent current Low $R_{DS(ON)}$	CMOS	75 75	1.0 1.0	750 500	350 250	−10 to +10 −11 to +11
IH5140-45	High speed, low power, low leakage	CMOS	50	0.5	100	75	−11 to +11
IH5148-51	Low $R_{DS(ON)}$, high speed, low power	CMOS	25	0.5	250 350 500	200 250 250	−14 to +14
Separate Driver/Switch Combinations							
IH6201	TTL level translator/driver	N-JFET	30	0.5	50 (Typ)	150 (Typ)	15 p-p (Min)
IH401/A	Low charge injection switch		30/50	0.5	50 (Typ)	150 (Typ)	20 p-p (Min)

Drivers for FET Switches

Monolithic bipolar drivers convert low-level positive logic to high-level positive and negative voltages necessary to drive FET switches.

For other Harris Semiconductor Products, see pages 2715 thru 2775.

Type	Number of Channels	Output Swing		t_{ON} ns Max	t_{OFF} ns Max
		Positive (V Max)	Negative (V Max)		
IH6201	2 TTL	+14.0	−14.0	200	300

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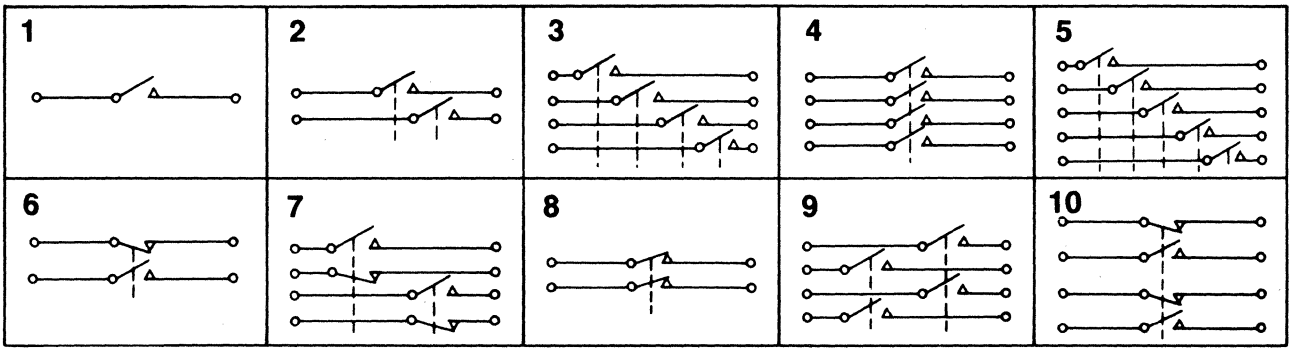
Switch Configurations



Switch Configuration (Diagram)									
SPST (1)	**Dual SPST (2)**	**Quad SPST (3)**	**4PST (4)**	**Five SPST (5)**	**SPDT (6)**	**Dual SPDT (7)**	**DPST (8)**	**Dual DPST (9)**	**DPDT (10)**
				DG123 DG125					
	DG141 DG133 DG134				DG146 DG144 DG143			DG140 DG129 DG126	DG145 DG139 DG142
	DG180 DG181 DG182				DG186 DG187 DG188	DG189 DG190 DG191		DG183 DG184 DG185	
	DGM182					DGM190 DGM191		DGM184 DGM185	
	DG200	DG201 DG201A DG202							
		DG211 DG212							
DG301A	DG300A					DG303A		DG302A	
IH5040	IH5041	IH5052/53	IH5047		IH5042	IH5043	IH5044	IH5045	IH5046
IH5140	IH5141				IH5142	IH5143	IH5144	IH5145	
	IH5148				IH5150	IH5151		IH5149	
		IH401/A							

GE/RCA Solid State

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Operational Amplifiers: Special Purpose

Low/Ultra-low Input Offset Voltage

Type	Description	V_{OS} (μV Max)	$\Delta V_{OS}/\Delta T$ (μV/°C) (Max)	$\Delta V_{OS}/\Delta t$ (nV/month) (Typ)	I_{BIAS} (pA Max)	GBW (MHz)	V_{SUPPLY} (V Max)	Temperature Range (°C)
SINGLES								
ICL7650C	CMOS, Chopper-stabilized	±8	±0.02	100	20	2.0	±9	0 to +70 &
ICL7650I	CMOS, Chopper-stabilized	±10	±0.02	100	50	2.0	±9	−25 to +85 &
ICL7650M	CMOS, Chopper-stabilized	±20	±0.03	100	500	2.0	±9	−55 to +125 &
ICL7652C	Low-noise 7650C	±7	±0.01	100	30	0.5	±9	0 to 70 &
ICL7652I	Low-noise 7650I	±10	±0.02	100	30	0.5	±9	−25 to +85 &
ICL7652M	Low-noise 7650M	±50	±0.1	100	500	0.5	±9	−55 to +125 &
ICL420	High Voltage Chopper	±5	±0.05	100	30	0.5	±16.5	0 to +70 &
ICL421	High Voltage Chopper	±5	±0.05	100	30	0.5	±16.5	−40 to +85 &
ICL422	High Voltage, Low Power	±5	±0.05	100	30	0.4	±16.5	−55 to +125
ICL423	High Voltage, Low Power	±5	±0.05	100	30	0.4	±16.5	

Low Input Bias Current

Type	Description	I_{BIAS} (pA Max)	I_{OS} (pA Typ)	V_{OS} (mV Max)	GBW (MHz)	Compen-sation	V_{SUPPLY} (V Max)	Temperature Range (°C)
SINGLES								
ICL7611	CMOS, Selectable I_Q	50	0.5	2, 5, 15	1.4	INT	±9	0 to +70 &
ICL7612	CMOS, Extended CMVR	50	0.5	2, 5, 15	1.4	INT	±9	−55 to +125
ICL7712	BiMos, Low Offset	40	2	0.25, 0.5	0.6	INT	±8	−40 to +85 &
ICL7713	BiMos, Low Power	40	2	0.25, 0.5	0.1	INT	±8	−55 to +125
ICL8007M	JFET Input Op-Amp	20	0.5	20	1.0	INT	±18	−55 to +125
ICL8007AM	JFET Input, Low Bias	4.0	0.2	30	1.0	INT	±18	−55 to +125
ICL8007C	JFET Input Op-Amp	50	0.5	50	1.0	INT	±18	0 to +70
ICL8007AC	JFET Input, Low Bias	4.0	0.2	30	1.0	INT	±18	0 to +70
ICH8500	PMOS Input	0.1	—	50	0.7	INT	±18	−25 to +85
ICH8500A	PMOS Input, Low Bias	0.01	—	50	0.7	INT	±18	−25 to +85
DUALS								
ICL7621	CMOS, Fixed I_Q	50	0.5	2, 5, 15	0.48	INT	±9	0 to +70 & −55 to +125
ICL8043M	JFET Input Op-Amp	20	0.5	20	1.0	INT	±18	−55 to +125
ICL8043C	JFET Input Op-Amp	50	0.5	50	1.0	INT	±18	0 to +70
TRIPLES								
ICL7631	CMOS, Selectable I_Q	50	0.5	5, 10, 20	1.4	INT	±9	0 to +70 & −55 to +125
QUADS								
ICL7641	CMOS, Fixed I_Q	50	0.5	5, 10, 20	1.4	INT	±9	0 to +70 &
ICL7642	CMOS, Fixed I_Q	50	0.5	5, 10, 20	0.044	INT	±9	−55 to +125

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Special Purpose Amplifiers

ICL420/421
±15V Chopper Stabilized Operational Amplifier

These chopper-stabilized CMOS operational amplifiers are designed for signal conditioning, precision and instrumentation type applications. They offer a wide input and operating supply range, allowing virtual plug-in replacements for conventional lower-performance amplifiers, requiring only two additional external capacitors.

The ICL420 (8-pin) and ICL421 (14-pin) devices draw a maximum supply current of 2 mA and are available in all temperature ranges.

ICL7605/7606
Commutating Auto-Zero (CAZ) Instrumentation Amplifier, CMOS

The ICL7605/ICL7606 CMOS commutating auto-zero (CAZ) instrumentation amplifiers are intended for low-frequency operation in applications such as strain gauge amplifiers which require voltage gains from 1 to 1000 and bandwidths from DC to 10Hz. Since the CAZ amp automatically corrects itself for internal errors, the only periodic adjustment required is that of gain, which is established by two external resistors. This, combined with extremely low offset and temperature coefficient figures, makes the CAZ instrumentation amplifier very desirable for operation in severe environments (temperature, humidity, toxicity, radiation, etc.) where equipment service is difficult.

Available in three temperature ranges.

ICL7712/ICL7713
Low Power Precision BIMOS Operational Amplifiers

The ICL7712/13 are monolithic single operational amplifiers which use Intersil's new BIMOS process. They offer precision performance and low power consumption, with quiescent currents of 150μA for the ICL7712 and 15μA for the ICL7713. These op amps have an input offset voltage of less than 250μV, an input offset current below 10pA, and an open-loop gain of 115dB.

The ICL7712/13 will operate at supply voltages ranging from ±2V to ±8V. The wide common mode voltage range, which includes the negative supply, allows for amplification of signals including ground in a single supply application.

The ICL7712/13 are available in commercial, industrial, and military temperature ranges. The high performance and low power consumption make the ICL7712/13 ideal for military applications.

ICL8048/ICL8049
Log/Antilog Amplifier

The 8048 is a monolithic logarithmic amplifier capable of handling six decades of current input, or three decades of voltage input. It is fully temperature compensated and is nominally designed to provide 1 volt of output for each decade change of input. For increased flexibility, the scale factor, reference current and offset voltage are externally adjustable.

The 8049 is the antilogarithmic counterpart of the 8048; it nominally generates one decade of output voltage for each 1 volt change in the input.

For other Harris Semiconductor Products, see pages 2715 thru 2775.

Content:

Special Purpose Amplifiers
- Instrumentation Amplifiers
- Log/Antilog Amplifiers
- Drive Amplifier for Power Transistors

Operational Amplifiers
- General Purpose
- Low Power
- Low Input Offset Voltage
- Low Input Bias Current

Features:

- **Input Offset Voltage — 2μV**
- **Input Offset Voltage Drift — 0.2μV/Year**
- **Common Mode Input Voltage Range — 0.3V Above Supply Rail**
- **Common Mode Rejection Ration — 100 dB**
- **Operates at Supply Voltages As Low As ±2V**
- **Short Circuit Protection On Outputs**
- **Compensated (ICL7605) or Uncompensated (ICL7606) Versions**

Features:

- **Low Power: 150μA (7712), 15μA (7713)**
- **Low Offset Voltage: 250μV (A Grade)**
  500μV (B Grade)
- **Wide Operating Voltage Range: 4V to 16V**
- **Low Input Bias Current**
- **Common Mode Range Includes the Negative Rail**
- **Output Voltage Swing to ±100mV of Supplies**
- **High Input Impedance: $10^{12}\Omega$**
- **High Gain, CMRR, and PSRR**

Features:

- **½% Full Scale Accuracy**
- **Temperature Compensated for 0°C to +70°C**
- **Scale Factor 1V/Decade, Adjustable**
- **120dB Dynamic Current Range (8048)**
- **60dB Dynamic Voltage Range (8048 & 8049)**
- **Dual JFET-Input Op-Amps**

GE/RCA Solid State

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Operational Amplifiers

Intersil offers a range of single and multiple monolithic operational amplifiers suitable for a number of specific applications categories. Included are bipolar Super-Beta and Chopper-Stabilized CMOS devices for very low input offset requirement, a selection of PMOS and JFET-input devices for very low bias currents, as well as general-purpose and low-power amplifiers for a broad range of applications.

All monolithic operational amplifiers are available in a variety of packages and in die form.

Operational Amplifiers: General Purpose

Type	Description	V_{OS} (mV Max)	I_{BIAS} (pA Max)	Slew Rate (V/μs)	GBW (MHz)	Compensation	V_{SUPPLY} (V Max)	Temperature Range (°C)
SINGLES								
ICL7611	CMOS, Selectable I_Q	2, 5, 15	50	1.6	1.4	INT	±9	0 to 70 −55 to +125
ICL7712	BiMos, Low Offset	0.25, 0.5	40	0.45	0.6	INT	±8	−40 to +85 −55 to +125
ICL8007M	JFET Input Op-Amp	20	20	6	1.0	INT	±18	−55 to +125
ICL8007C	JFET Input Op-Amp	50	50	6	1.0	INT	±18	0 to +70
DUALS								
ICL7621	CMOS, Fixed I_Q	2, 5, 15	50	0.16	0.48	INT	±9	0 to +70 −55 to +125
ICL8043M	JFET Input Op-Amp	20	20	6	1.0	INT	±18	−55 to +125
ICL8043C	JFET Input Op-Amp	50	50	6	1.0	INT	±18	0 to +70
TRIPLES								
ICL7631	CMOS, Selectable I_Q	5, 10, 20	50	1.6	1.4	INT	±9	0 to +70 −55 to +125
QUADS								
ICL7641	CMOS, Fixed I_Q	5, 10, 20	50	1.6	1.4	INT	±9	0 to +70 −55 to +125

GE/RCA Solid State

Low Power

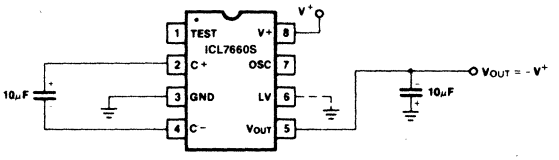
Type	Description	$I_{QUIESCENT}$ (Per Amplifier) (μA Typ)	V_{SUPPLY} (V Max)	V_{OS} (mV Max)	I_{BIAS} (nA Max)	GBW (MHz)	Compensation	Temperature Range (°C)
SINGLES								
ICL7611	CMOS, Selectable I_Q	10	±9	2, 5, 15	0.05	0.044	INT	0 to 70 &
ICL7612	CMOS, Extended CMVR	10	±9	2, 5, 15	0.05	0.044	INT	−55 to +125
ICL7713	BiMos, Low Offset	30	±8	0.25, 0.5	0.04	0.1	INT	−40 to +85 & −55 to +125
ICL8021M	Bipolar, Selectable I_Q	30	±18	3	20	0.27	INT	−55 to +125
ICL8021C	Bipolar, Selectable I_Q	30	±18	6	30	0.27	INT	0 to +70
TRIPLES								
ICL7631	CMOS, Selectable I_Q	10	±9	5, 10, 20	0.05	0.044	INT	0 to +70 &
ICL8023M	Triple 8021M	30	±18	3	20	0.27	INT	−55 to +125
ICL8023C	Triple 8021C	30	±18	6	30	0.27	INT	0 to +70
QUADS								
ICL7642	CMOS, Fixed I_Q	10	±9	5, 10, 20	0.05	0.044	INT	0 to +70 & −55 to +125

For other Harris Semiconductor Products, see pages 2715 thru 2775.

ICL7660S/ICL7662S
Voltage Converters

These voltage converters transform a positive (+) input voltage from a power supply to a corresponding negative (−) output, resulting in complementary output voltages of −1.5V to −12.0V for the ICL7660, and −4.5V to −20V for the ICL7662. Only two non-critical external capacitors are needed to perform the conversions. The converters can also be connected as voltage doublers and will generate output voltages of +18.6V and 22.6V, respectively.

Available in two temperature ranges, 0°C to 70°C and −55°C to +125°C, and three packages, TO-99, 8-pin MiniDIP (ICL7660S only) and SOIC.



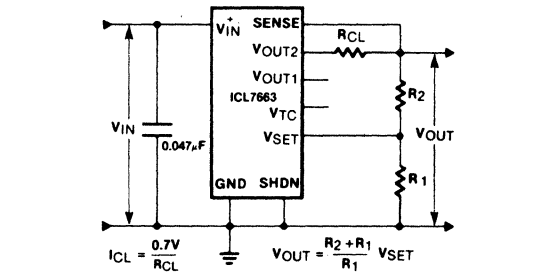
Simple Negative Converter Configuration

ICL7663S
Programmable Micropower Voltage Regulators

The ICL7663 (positive) series regulators are low-power, high-efficiency devices which accept inputs from 1.6V to 16V and provide adjustable outputs over the same range at currents up to 40mA. Operating current is typically less than 4μA, regardless of load.

Output current sensing and remote shutdown are available, thereby providing protection for the regulators and the circuits they power.

The ICL7663 is available in 8-pin plastic, TO-99 metal can, CERDIP, and SOIC packages, in two temperature ranges — 0°C to +70°C and −25°C to +85°C.

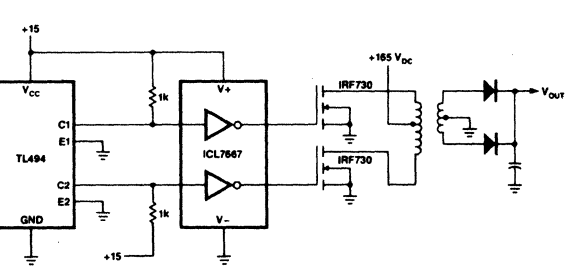


Basic Applications of ICL7663 as Positive Regulator with Current Limit

ICL7667
Dual Power MOSFET Driver

The ICL7667 is a dual monolithic high-speed driver designed to convert TTL level signals into high current outputs at voltages up to 15V. Its high speed and peak current output enable it to drive large capacitive loads with high slew rates and low propagation delays. With an output voltage swing only millivolts less than the supply voltage and a maximum supply voltage of 15V, the ICL7667 is well suited for driving power MOSFETs in high frequency switched-mode power converters.

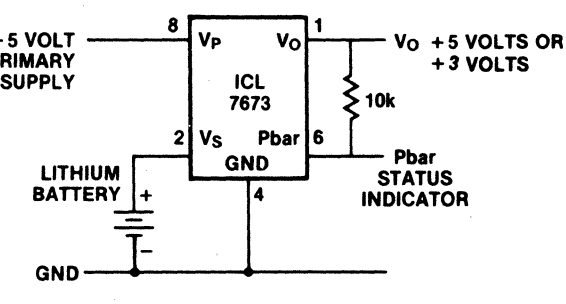
Available in commercial and military temperature ranges, and in 8-pin plastic DIP, SOIC, CERDIP and TO-99 metal packages.



Direct Drive of MOSFET Gates

ICL7673
Automatic Battery Back-Up Switch

The ICL7673 automatically switches from the main power supply to a battery back-up supply in the event of power loss, and back again when power is restored. Ideal for on-board battery back-up for real-time clocks, timers, volatile RAMs, or portable instruments. Available in 8-pin MiniDIP and TO-99 packages.



ICL7673 Battery Backup Circuit

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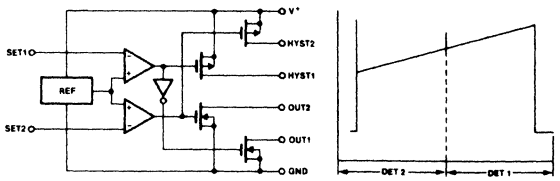
ICL7665
Micropower Under/Over Voltage Detector

The ICL7665 contains two individually programmable voltage detectors on a single chip. Requiring only 3μA, typical, for operation, the device is intended for battery-operated systems and instruments which require high or low voltage warnings, settable trip points, or fault monitoring and corrections.

Available in 8-lead CERDIP, MiniDIP, TO-99 metal can and SOIC packages with a temperature range from 0°C to 70°C.



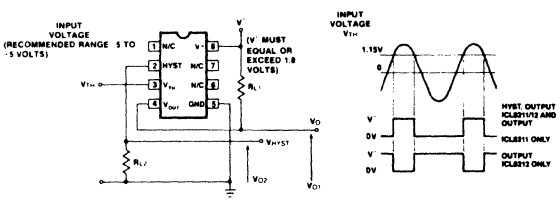
ICL7665 Functional Diagram and Transfer Characteristics of Simple Threshold Detector

ICL8211/ICL8212
Programmable Voltage Detector

These circuits consist of an accurate voltage reference, a comparator and a pair of output buffer/drivers.

The ICL8211 provides a 7mA current limited output sink when the voltage applied to the 'THRESHOLD' terminals is less than 1.15 volts (the internal reference). The ICL8212 requires a voltage in excess of 1.15 volts to switch its output on (no current limit). Both devices have a low current output (HYSTERESIS) which is switched on for input voltages in excess of 1.15V. The HYSTERESIS output may be used to provide positive and noise free output switching using a simple feedback network.

Available in 8-lead MiniDip, TO-99 metal can and SOIC packages, in commercial and military temperature ranges.



Voltage Level Detection with ICL8211/8212

ICL8069
Low Voltage Reference

ICL8069 is a 1.2V temperature compensated voltage reference. It uses the band-gap principal to achieve excellent stability and low noise at reverse currents down to 50μA. Applications include analog-to-digital converters, threshold detectors, and voltage regulators. Its low power consumption makes it especially suitable for battery operated equipment.

Available in TO-92 plastic and TO-52 metal packages with 0°C to 70°C and −55°C to +125°C temperature ranges (metal only) and with temperature coefficients of 0.005 and 0.01/°C.

ICL7675/ICL7676
Switched-Mode Power Supply Controller Set

The ICL7675/7676 two-chip set provides the necessary control circuitry for regulation of an isolated flyback type switching power supply. Specifically designed to operate in this type of configuration, the Intersil controller chip-set is trimmed to provide a regulated 5V output. The isolated flyback converter is the most widely used configuration for switched-mode power supplies in 50W to 150W range because of its simplicity. The chip-set features soft-start and power switch over-current protection.

ICL7677
Power Fail Detector

ICL7677 is a Power Fail Detector which can be incorporated either into the primary or the secondary side of a power supply to give the fastest possible power-fail indication. On the primary side, it can simultaneously monitor AC line voltage, the reservoir capacitor voltage, primary side current and ambient temperature. On the secondary side, it can simultaneously monitor up to two DC voltages, one load current and the ambient temperature. The circuit has an on-chip bandgap-voltage reference to conveniently program the detection thresholds.

ICL7680
5V to ±15V Voltage Converter

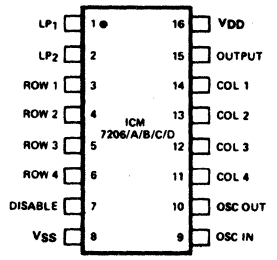
The ICL7680 is a simple boost-type switched-mode converter/inverter chip using minimal external components to convert +5V to ±15V regulated outputs. An internal oscillator is user programmable to optimize efficiency for various load conditions. The device features current limiting protection together with external shut-down.

For other Harris Semiconductor Products, see pages 2715 thru 2775.

ICM7206
Touch-Tone Encoder

The ICM7206 is a 2-of-8 sinewave DTMF generator for use in telephone dialing systems. Requires a 3.58 MHz crystal and will operate with both 3x4 and 4x4 keypads. This low-cost circuit has a high current bipolar output driver providing low harmonic distortion. Supply voltage range is 3 to 6 volts with power dissipation of less than 5.5mW at 5.5 volts. Single and dual tone capability.

Available in 16-pin plastic DIP with a temperature range from −40°C to +85°C.

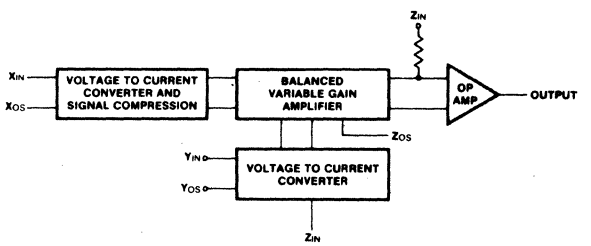


Pin Configuration

ICL8013
Four Quadrant Analog Multiplier

The ICL8013 is a bipolar, four-quadrant analog multiplier whose output is proportional to the algebraic product of two input signals. Feedback around an internal op-amp provides level shifting and can be used to generate division and square root functions. A simple arrangement of potentiometers may be used to time gain accuracy, offset voltage and feedthrough performance.

Available in 10-pin TO-100 metal package in both commercial and military temperature ranges.

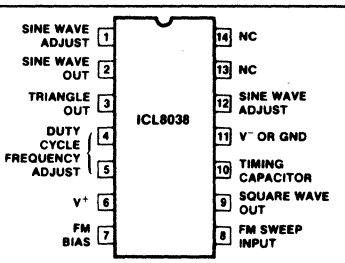


ICL8013 Functional Diagram

ICL8038
Precision Waveform Generator/Voltage Controlled Oscillator

The ICL8038 Waveform Generator is capable of producing high accuracy sine, square, triangular, sawtooth and pulse waveforms with a minimum of external components. The frequency (or repetition rate) can be selected externally from .001Hz to more than 300KHz using either resistors or capacitors, and frequency modulation, and sweeping can be accomplished with an external voltage.

The 14-pin CERDIP package is available with 0°C to +70°C, and −55°C to +125°C temperature ranges.



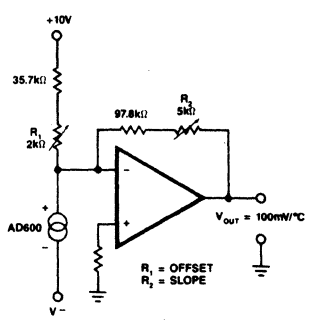
Pin Configuration

AD590
2-Wire, Current-Output Temperature Transducer

The AD590 is a 2-wire integrated-circuit temperature transducer which produces an output current proportional to absolute temperature. The device acts as a high impedance constant current regulator, passing 1μA/°K for supply voltages between +4V and +30V. Laser trimming of the chip's thin-film resistors is used to calibrate the device to 298.2 μA output at 298.2°K (+25°C).

The AD590 could be used in any temperature-sensing application between −55°C and +150°C in which conventional electrical temperature sensors are currently employed.

Plastic (TO-92) packaged device covers temperature ranges from 0°C to +70C; Metal packaged device (TO-52) covers −55°C to +150°C range. With slope and offset trimming circuit it is possible to adjust devices to give less than 0.1% error over the temperature range from 0°C to 90°C.



AD590 Slope and Offset Trimming Circuit

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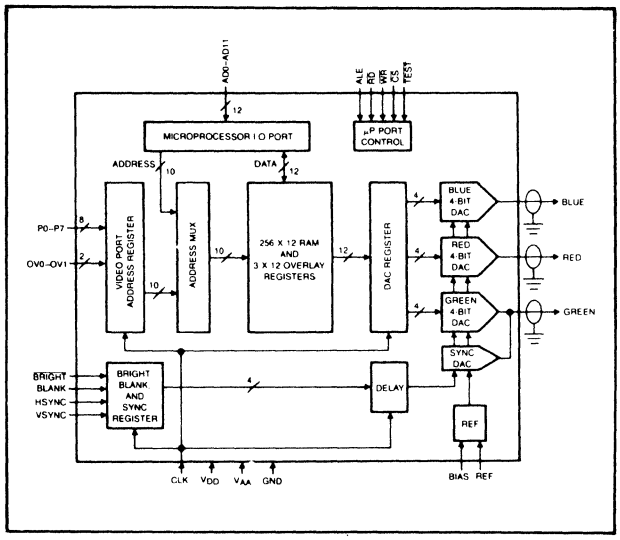
IM2110
256 x 12 Color Lookup Table and DAC

The IM2110 is designed specifically for color graphics, and integrates a 256 x 12 color lookup table, three 4-bit DACs, and a microprocessor interface.

The color lookup table is stored in a RAM and may be written asynchronously by an 8- or 16-bit microprocessor. Three overlay registers are provided for overlaying cursors, grids, text, etc. The chip is capable of simultaneously displaying 256 out of 4096 colors at a 25 MHz rate, for a 640 x 480 non-interlaced display.

The IM2110 generates RS-343-A compatible red, green and blue analog signals, and is capable of driving doubly-terminated 75 Ω coaxial cables directly.

The circuit is available in a 40-pin plastic package and operates over a temperature range of 0°C to +70°C.



CA3338

The CA3338 is a CMOS/SOS high-speed segmented R-2R for low "glitch" energy voltage output DAC operating from a single 5V supply at video-speeds. The first settling of 20ns (typ) to ½ LSB makes it ideal for high-speed oscilloscope displays, digital waveform generators, TV/video displays and feed-forward A/D systems.

For other Harris Semiconductor Products, see pages 2715 thru 2775.

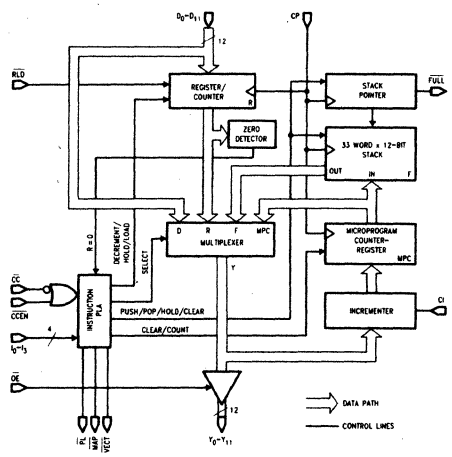
ISP9110
12-Bit Microprogram Sequencer

The ISP9110 is a 12-bit microprogram sequencer/controller used for high speed execution of microprogram instructions stored in external memory. The ISP9110 is typically used in conjunction with bit slice processor systems and DSP building blocks to control the sequence of execution of instructions stored in microprogram memory, but can also be used in digital systems as a stand-alone control element.

The ISP9110 is implemented in Intersil's CMOS 1.5 micron AVLSI technology and is a pin-for-pin compatible replacement for other industry standard microprogram sequencers such as the AM2910. In addition, the nine word stack has been increased to 33 words.

By providing additional internal registers and a multiplexed output, the ISP9110 allows non-sequential program flow (looping, direct jumps, subroutines). In a typical configuration, the address of the next instruction is available at the output within one clock cycle based on a 4-bit instruction code.

The ISP9110 is available in 40-pin DIP and 44-pin PLCC packages.



Functional Diagram

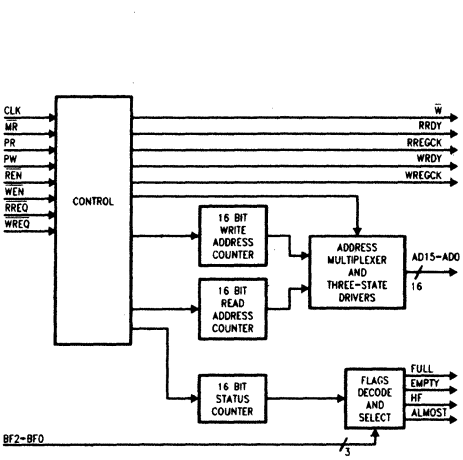
ISP9119
FIFO RAM Controller

The ISP9119 FIFO RAM Controller (FRC), together with a static RAM array, forms a First-In-First-Out (FIFO) buffer. The ISP9119 FRC, implemented in Intersil's 1.5 micron AVLSI CMOS technology, is pin-for-pin compatible with 57/674219. This process allows the ISP9119 to operate at twice the speed, but one tenth the power dissipation of its bipolar counterpart.

The ISP9119 offers high-speed operation with no fall-through time, 16-bit static RAM addressing, arbitration for read and write, control signals that include write enable and read/write handshaking signals and strobes for latching external data, status flag (Full, Half-Full, Empty, Almost) and three-state output buffers for a RAM array which can range from 512 to 64K (65,536) static RAM words.

The ISP9119 allows single-port static RAMs to resolve read and write request conflicts according to priority rules selected via the Priority-on-Read (PR) and Priority-on-Write (PW) inputs. If priority is given to either port, or if only one port is used, the maximum data rate through that port is 15MHz.

The ISP9119 is available in 40-pin DIP and 44-pin PLCC packages.

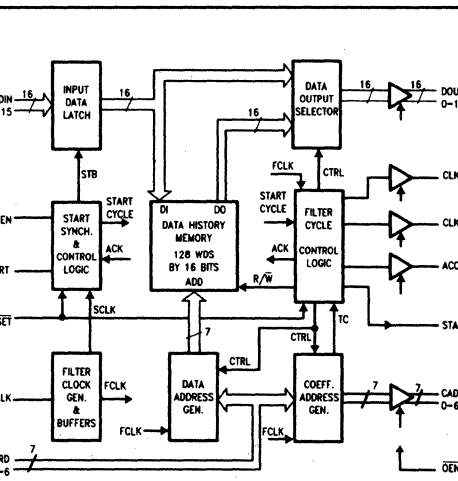


Functional Diagram

ISP9128
Finite Impulse Response Filter Controller

The 16-bit FIR Filter Controller (FFC) provides all the data history, storage, and programmable filter cycle control logic required to implement FIR filters of up to 128 filter points. When used in conjunction with an external filter coefficient memory, of up to 128 words by 16 bits, and an industry standard 16-bit Multiplier-Accumulator (MAC), the FFC provides the system designer with the ability to implement a powerful FIR filter with only three ICs. The FFC provides MAC and coefficient memory three-statable signals, allowing multiplexed usage of these resources. The FFC's asynchronous interface enables easy integration of the FIR filter in any system environment. It incorporates a 16-bit data I/O path, a 128-word by 16-bit RAM memory, and programmable filter control logic capable of handling filter order lengths of up to 128 points.

The ISP9128 is available in 64-pin DIP, 68-pin PLCC, and 68-pin PGA packages.



Functional Diagram

For other Harris Semiconductor Products, see pages 2715 thru 2775.

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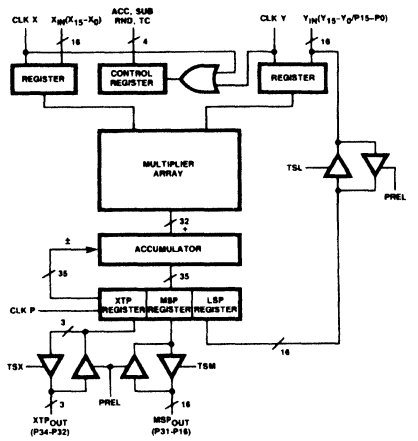
ISP9210
16×16-Bit Multiplier/Accumulator

The ISP9210 is a 16×16-bit parallel multiplier/accumulator, manufactured in Intersil's 1.5 micron CMOS AVLSI technology. The two input registers X and Y, accept 16-bit twos complement or unsigned magnitude operands and produce a 32-bit product, with accumulation up to 35 bits.

To simplify bus interfacing and maximize system throughput, product outputs, X-inputs, and Y-inputs are individually and independently clocked. The Least Significant Product (LSP) is multiplexed with the Y-inputs. Most Significant Product (MSP), and Extended Product (XTP) are independently three-statable.

Individual three-state output ports for the XTP and the MSP are provided. Preloading during three-state is accomplished through the three-stated output pins for the MSP and the XTP, and through the Y-input pins for the LSP. Operation of the accumulator is controlled by the signals ACC (Accumulate), SUB (Subtract), and PREL (Preload).

The ISP9210 is pin and function compatible with the industry standard TDC1010 and is available in 64-pin DIP and 68-pin PLCC packages.



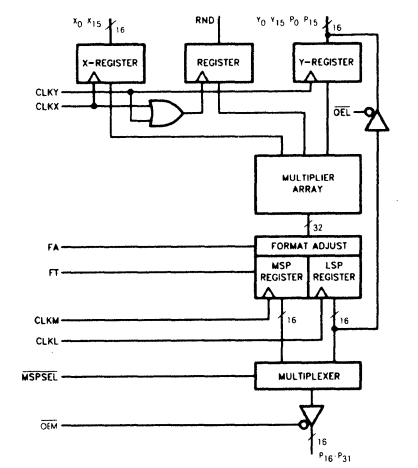
Functional Diagram

ISP9216
16×16-Bit Multiplier

The ISP9216 is a 16×16-bit multiplier, pin and function compatible with industry standard 29516. The X-input, Y-input, and most significant and least significant product outputs are independently clocked into separate registers by the rising edge of the CLKX, CLKY, CLKM, and CLKL signals, respectively. The Least Significant Product (LSP) is multiplexed with the Most Significant Product (MSP) through the MSP outputs (e.g., for use with a 16-bit data bus) by utilizing the $\overline{\text{M BSEL}}$ signal.

The output registers can be made transparent by the Feed Through (FT) signal, although the fully clocked implementation will be capable of higher throughput. The format adjust, FA, causes a right shift of the MSP and deletes the MSP of the LSP, i.e., the sign bit of the LSP.

The ISP9216 is available in 64-pin DIP and 68-pin PLCC packages.



Functional Diagram

For other Harris Semiconductor Products, see pages 2715 thru 2775.

ISP9224
24×24-Bit Multiplier/Accumulator

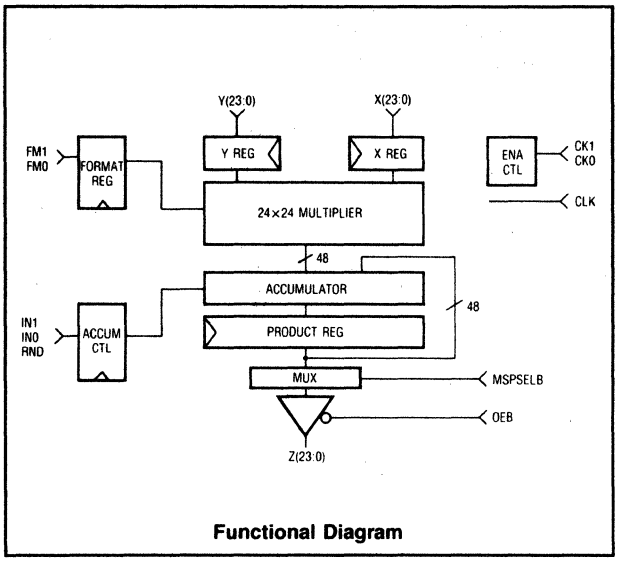
The ISP9224 is a high-speed low power 24-bit fixed-point multiplier/accumulator fabricated with Intersil's 1.5 micron AVLSI CMOS process. It performs multiplication and simultaneous product accumulation of two 24-bit operands in a single 100ns cycle.

The ISP9224 features a 3-bus 24-bit architecture, with two 24-bit input buses (X,Y) and one 24-bit output bus (Z). This configuration provides high I/O bandwidth, and a high degree of flexibility in system design. All buses and control inputs are fully registered with data or control transferred on the rising edge of the master clock (CLK). Independent register clocking is facilitated by two clock control inputs, CK0 and CK1. The upper 24-bit and lower 24-bit accumulated product results (MSP and LSP) are routed through the output port via a multiplexer. The MSPSELB signal multiplexes the LSP of the 48-bit accumulated product to the outputs when it is high, and multiplexes the MSP to the outputs when it is low.

The X and Y inputs can be in unsigned magnitude, two's complement, or mixed mode format through the use of two control inputs, FM0 and FM1. Accumulation control inputs IN0 and IN1 enable the ISP9224 to perform the add nothing, add accumulator to product, subtract accumulator from product, and add sign extension (accumulator X 2^{-24}) to product operations.

The rounding control input (RND) causes rounding to occur when it is high. The IEEE round-to-nearest technique has been implemented to minimize numerical inaccuracies. Three-state control of the output buffers are accomplished through the use of the OEB input.

The ISP9224 is available in 84-pin PLCC and 84-pin PGA packages.



Functional Diagram

ISP9326
32-Bit Floating Point Processor

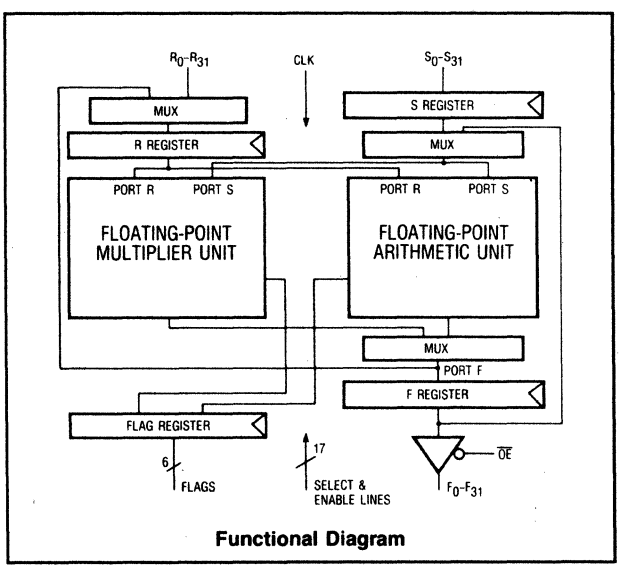
The ISP9326 is a high-speed floating point procesor unit. It performs 32-bit single precision floating point addition, subtraction, and multiplication operations in a single CMOS VLSI integrated circuit using the format specified by the IEEE floating point standard 754. The DEC single-precision floating point format is also supported. Conversion between IEEE and DEC formats are provided as are 32-bit integer format to floating point formats. All operations can be performed in a single clock cycle.

Six flags monitor the status of operations: Invalid, Not-a-Number (NaN), Inexact, Zero, Overflow, and Underflow.

Three bus configurations are user selectable. A 3-bus, 32-bit architecture with two 32-bit inputs, and a single 32-bit output provides high I/O bandwidth and access to all buses. All buses are registered with each register provided with an enable control pin. Alternatively, the ISP9326 can be configured as a 16-bit 3-bus, or a 32-bit 2-bus architecture, easing interface to a wide variety of systems.

Internal 32-bit data paths and registers support single cycle Multiply and Accumulate operations, effectively doubling the throughput when compared to devices that support only one floating point operation per cycle.

Fabricated with Intersil's 1.5 micron AVLSI CMOS technology, the ISP9326 is powered from a single 5-volt supply and is available in 144-pin PGA package.



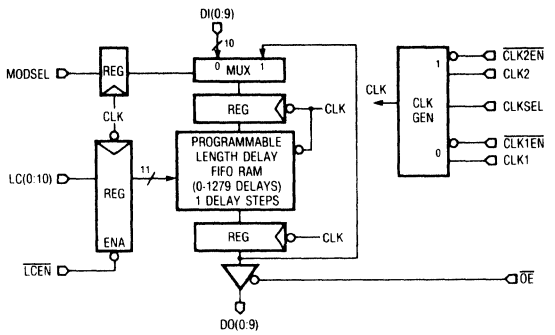
Functional Diagram

For other Harris Semiconductor Products, see pages 2715 thru 2775.

ISP9500
Programmable Length Delay Line/FIFO

The ISP9500 is a programmable length, 10-bit wide, first-in-first-out (FIFO) data buffer designed for use in high-speed digital systems. The ISP9500 can be programmed to operate in a delay mode or a data recirculate mode. In the delay mode data will appear on the outputs N-1 clock cycles after is entered on the inputs, where N is a decimal integer between 2 and 1281, which represents the programmed length of the data buffer. In the data recirculate mode, the data outputs are internally routed back to the data inputs so that N words of data are continuously recirculated. The ISP9500 is recommended for digital video processing applications, or in general, any application requiring a programmable delay or recurring data words.

The ISP9500 is available in 44-pin PLCC and 48-pin DIP packages.



Functional Diagram

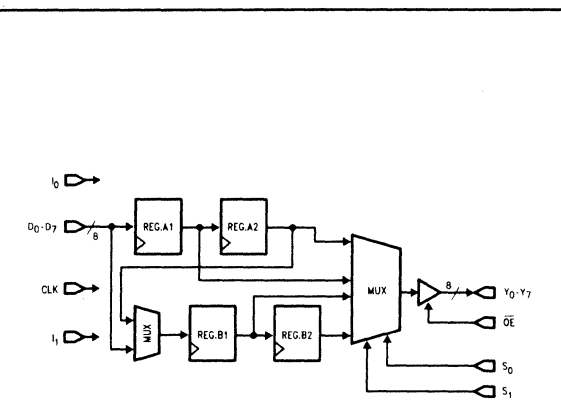
ISP9520/ISP9521
Multilevel Pipeline Register

The ISP9520 and ISP9521 are multilevel pipeline registers implemented using Intersil's 1.5 micron AVLSI CMOS technology. The ISP9520/21 operate at bipolar speeds with one tenth the power dissipation of their bipolar counterparts. The ISP9520 and ISP9521 are pin-for-pin compatible replacements for industry standard multilevel pipeline registers such as the bipolar AM29520 and AM29521.

The ISP9520 and ISP9521 consist of four addressable registers which are dual ported. They can be configured as a single four-level pipeline or two dual pipelines. The configuration is determined by the instruction code input to I0 and I1 pins.

The contents of any of the four registers are selectable at the multiplexed outputs through the use of S0 and S1 control inputs. The output is 8 bits wide and is enabled by the $\overline{EO}$ input.

The ISP9520 and ISP9521 differ only in the way data is loaded into and between the registers in dual 2-level operation. Both parts are available in 24-pin 300-mil (skinny) DIP packages.



Functional Diagram

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HARRIS SEMICONDUCTOR
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INTERSIL Products

Available with and without on-board display drivers, Intersil's broad range of Timer/Counters circuits serves a wide variety of control functions. For separate Display Driver circuits, see separate section.

Timer/Counters With Display Drivers

TYPE	DISPLAY: LED: Common Anode, Non-MUX	DISPLAY: LED: Common Cathode, MUX	DISPLAY: LED: Common Anode, MUX	DISPLAY: LCD: Direct Drive, Non-MUX	DISPLAY: VF: Non-MUX	FUNCTIONS: UNIT COUNT: Up/Down	FUNCTIONS: UNIT COUNT: Up Only	FUNCTIONS: UNIT COUNT: Decade	FUNCTIONS: UNIT COUNT: Modulo 60 (Hr/Min/Sec)	FUNCTIONS: UNIVERSAL COUNTERS: Frequency	FUNCTIONS: UNIVERSAL COUNTERS: Period	FUNCTIONS: UNIVERSAL COUNTERS: Frequency Ratio	FUNCTIONS: UNIVERSAL COUNTERS: Time Interval	FUNCTIONS: MUX BCD Outputs	FUNCTIONS: Display Latch	FUNCTIONS: Display Blanking	FUNCTIONS: Count Enable	FUNCTIONS: Leading Zero Blanking	FUNCTIONS: Preset Count	FUNCTIONS: Comparison Register	FUNCTIONS: Equal and Zero Output	MAX COUNT SPEED (MHz)	Evaluation Kit Available	TYPICAL APPLICATIONS AND COMMENTS
4 DIGIT																								
ICM7217			●			●		●		■				●	●	●		●	●	●	●	2		Industrial control: preset/predetermining counters, sequencers, on/off delay timers, batch counters. Presets and loads compare register from thumbwheel switches.
ICM7217A		●				●		●		■				●	●	●		●	●	●	●	2		
ICM7217B			●			●			●					●	●	●		●	●	●	●	2		
ICM7217C		●				●			●					●	●	●		●	●	●	●	2		
ICM7227			●			●		●						●	●	●		●	●	●	●	2		Microprocessor compatible interface. Industrial control; preset/predetermining counters, sequencers, on/off delay timers, batch counters. Presets and loads compare register from a microprocessor.
ICM7227A		●				●		●						●	●	●		●	●	●	●	2		
ICM7227B			●			●			●					●	●	●		●	●	●	●	2		
ICM7227C		●				●			●					●	●	●		●	●	●	●	2		
4½ DIGIT																								
ICM7224				●			●	●		■					●		●	●				15	●	10 μA operating current. Can be cascaded for more digits.
ICM7224A				●			●		●						●		●	●				15		
ICM7225	●						●	●		■					●	●	●	●				15	●	Has brightness adjustment, 10 μA current with display blanked, cascadable.
ICM7225A	●						●		●						●	●	●	●				15		
5½ DIGIT																								
ICM7249				●			●	●					●						●					Event timer/counter, hour meter. 14 programmable modes. Selectable input filtering.
6 DIGIT																								
ICM7215		●					●		●				●			●	●							4 functions: start/stop/reset, split, taylor, time out. 1/100's seconds and low battery.
7 DIGIT																								
ICM7208		●					●	●		■					●	●	●	●				2.5		Use with ICM7207/A for a 7-digit frequency counter.
8 DIGIT																								
ICM7216A			●				●	●		●	●	●	●		●	●		●				10		Universal frequency counter with display drivers. 4 internal gate times, auto decimal point, leading zero blanking, overflow indication. Display off, hold, and reset inputs.
ICM7216B		●					●	●		●	●	●	●		●	●		●				10		
ICM7216C			●				●	●		●					●	●		●				10		
ICM7216D		●					●	●		●					●	●		●				10		
ICM7226A			●				●	●		●	●	●	●	●	●	●	●	●				10	●	Same as ICM7216 plus period and time interval averaging, BDC outputs, μP PIA compatible.
ICM7226B		●					●	●		●	●	●	●	●	●	●	●	●				10		

■ These counters will measure frequency when used with the ICM7207 (0.01 and 0.1 second timebase) or the ICM7207A (0.1 and 1.0 second timebase)

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Timers/Counters Without Display Drivers

Type	Special Features	Description
ICM7555		Low power CMOS equivalent of industry standard 555 timer — only 80 μA supply current. ICM7555 does not have the large supply current transients of the bipolar 555 and does not require the large bypassing capacitors needed by the 555. Low leakage threshold and trigger inputs allow use of higher impedance RC timing components for extra long time delays.
ICM7556		An ICM7556 is a dual ICM7555, a CMOS, low power equivalent of the Bipolar 556 Timer.
ICM7240 ICM7250	Binary 0–225 BCD 0–99	Programmable CMOS counter timer. Uses on-board RC oscillator or an external clock. The count is programmed by wire-AND connection of the outputs. Excellent for ON/OFF delay timers, ÷ N counters, and long period delays.
ICM7242	Fixed 128/255	RC oscillator + 8-bit counter, similar to ICM7240 but with fixed 256 count. Used for extremely long time delays. Cascadable.

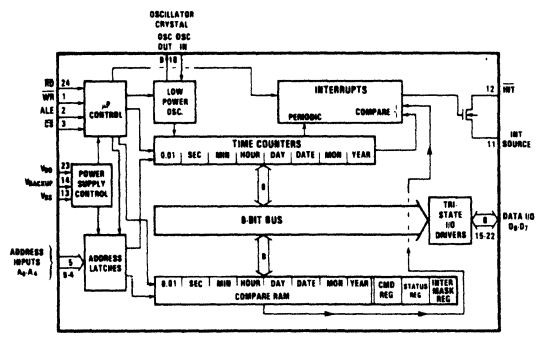
Oscillator/Divider Selector Guide

Type	Output Frequency	Supply Voltage (V)	Typical Current (μA)	Pulse Width (ms)	Crystal Frequency	Other Outputs/Comments
ICM7213	1 Pulse/Min	2–4	100	125, 1000	4.19 MHz	1 Pulse/Sec., 2048, 1024, 34.133, 16 Hz
	1 Hz	2–4	100	7.8	4.19 MHz	1 Pulse/Min., 2048, 1024, 34.133, 16 Hz
	16 Hz	2–4	100	Sq. Wave	4.19 MHz	1 Pulse/Min., 2048, 1024, 34.133, 1 Hz
	1000 Hz 1024 Hz	2–4 2–4	100 100	Sq. Wave Sq. Wave	4.096 MHz 4.19 MHz	2000, 2000 Pulses/Min. 1 Pulse/Min., 2048, 34.133, 16, 1 Hz
	2048 Hz	2–4	100	Sq. Wave	4.19 MHz	1 Pulse/Min., 1024, 34.133, 16, 1 Hz
ICM7209	250 kHz–10 MHz	4.5–5.5	11,000	Sq. Wave	1–10 MHz	Two buffered outputs — Crystal Frequency and ÷ 8 output. Drives up to 5 TTL loads.

ICM7170
μP-Compatible
Real-Time Clock, CMOS

This real-time clock circuit is set or read by accessing eight internal separately addressable and programmable counters from 1/100 seconds to 99 years. An 8-bit bidirectional bus is used for the data I/O circuitry. Access time of 300 ns eliminates the need for mpu wait states or software overhead. An Address Latch Enable input is provided to permit both multiplexed and direct addressing. These features allow easy interface with any available microprocessor. Other features include full calendar with automatic leap-year correction, on-chip battery backup switch over circuit and on-chip alarm comparator and RAM. Available in 24-pin plastic DIP and CERDIP package with temperature range from −40°C to +85°C.

Full Mil temperature range devices are available. Including an 883B Rev. C device. Devices are also screened for <5μA standby current at 32KHz clock.



Functional Diagram

For other Harris Semiconductor Products, see pages 2715 thru 2775.

DISPLAY DRIVERS

HARRIS SEMICONDUCTOR
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INTERSIL Products

Intersil's complete complement of monolithic Display Driver circuits provides a suitable interface for virtually any display application.

- Choice of Displays:
  LED, LCD, Vacuum Fluorescent
- Choice of Characters or Digits:
  4, 8 or 10 7-Segment Digits
  14, 16 or 18-Segment Characters
- Choice of Font:
  Hexadecimal, Code B, ASCII
- Choice of Interface:
  Multiplexed or Direct Drive; BCD, Random Access, Serial or Parallel

All Intersil Drivers are fabricated with CMOS technology for low power dissipation, and most are available in CERDIP and Plastic Dual In-line packages, as well as in die form. All are completely self-contained, requiring few, if any, external components to accomplish their intended basic functions.

The following table offers a quick-glance overview of available functions for a first-order selection.

TYPE	# OF CHARACTERS OR DIGITS						DISPLAY TYPE						FONT			INTERFACE					FEATURES AND COMMENTS
	# of 7-Segment Digits	# of Decimal Points or Annunciators	# of Alphanumeric 14 Segments + D.P.	# of Alphanumeric 16 Segments + D.P.	# of Alphanumeric 18 Segments	# of Dot Matrix	LED, Common Anode Non-MUX	LED, Common Cathode MUX	LED, Common Anode MUX	LCD, Direct Drive	LCD, # of Ways MUX'D	Vacuum Fluorescent	Hexadecimal (0–9, A–F)	Code B (0–9, H, E, L, P, -, and Blank)	ASCII	MUX BCD (BCD + Digit Select Strobes)	Random Access (Data + Address + WR)	Bit Parallel, Digit Serial	Bit Serial	Cycle Time (ns)	
ICM7211	4									●			●			●				1000	Drives Conventional LCD Displays. Includes RC Oscillator, Divider Chain, Latches, Interface and LCD Drivers. Evaluation Kit Available.
ICM7211A	4									●				●		●				1000	
ICM7211M	4									●			●				●			200	
ICM7211AM	4									●				●			●			200	
ICM7212	4						●						●			●				1000	Drives Common Anode LED Displays. 28 Current Controlled Outputs. Includes Latches, Interface and Brightness Control. Evaluation Kit Available.
ICM7212A	4						●							●		●				1000	
ICM7212M	4						●						●				●			200	
ICM7212AM	4						●							●			●			200	
ICM7218A	8	8							●				●	●				●		550	3 Decode Formats Drives UP to 64 Independent LED's. Includes 8 × 8 Memory, Multiplexed LED Drivers, Decoders, Interface and control. Applications Include Bar Graphs.
ICM7218B	8	8						●					●	●				●		550	
ICM7218C	8	8							●				●	●			●			500	
ICM7218D	8	8						●					●	●			●			500	
ICM7218E	8	8							●				●	●			●			500	
ICM7228A	8	8							●				●	●				●		550	
ICM7228B	8	8						●					●	●				●		550	
ICM7228C	8	8							●				●	●			●			500	
ICM7228D	8	8						●					●	●			●			500	
ICM7231A	8	16									3		●				●			500	8 Digits, 16 Annunciators on COM, Hexadecimal
ICM7231B	8	16									3			●			●			500	8 Digits, 16 Annunciators on COM 3, Code B
ICM7231C	8	16									3			●			●			500	8 Digits, 16 Annunciators on COM 1 + 3, Code B
ICM7232A	10	20									3		●						●	350	10 Digits, 20 Annunciators on COM 3, Hexadecimal
ICM7232B	10	20									3			●					●	350	10 Digits, 20 Annunciators on COM 3, Code B
ICM7232C	10	20									3			●					●	350	10 Digits, 20 Annunciators on COM 1 + 3, Code B
ICM7233A					4						3				●		●			500	4 Alphanumeric Characters. Evaluation Kit Available
ICM7233B					4						3				●		●			500	4 Alphanumeric Characters. Full-Width Numbers
ICM7243A				8				●							●		●			250	8 Alphanumeric Characters + Decimal Pt. can be Daisy Chained or Cascaded. Evaluation Kit Avail.
ICM7243B			8					●							●		●			250	

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INTERSIL Products

MIL-STD-883B Rev. C Compliant Devices

Data Acquisition Products 883B Rev. C

AD7520SD/883B
AD7520TD/883B
AD7520UD/883B
AD7521SD/883B
AD7521TD/883B
AD7521UD/883B
AD7533SD/883B
AD7533TD/883B
AD7533UD/883B
AD7541SD/883B
AD7541TD/883B
ICL7134UJMJI/883B
ICL7134UKMJI/883B
ICL7134ULMJI/883B
ICL7109MDL/883B

Digital/Micro Peripheral 883B Rev. C

ICM7170AMDG/883B
ICM7170MDG/883B
ICM7228AMJI/883B
ICM7228BMJI/883B
ICM7228CMJI/883B
ICM7228DMJI/883B
IM64021MJL/883B
IM6402AMJL/883B
IM6402MJL/883B
IM66531MJG/883B
IM6653AMJG/883B
IM66541MJG/883B
IM6654AMJG/883B

Linear Products 883B Rev. C

ICL232MJE/883B
ICL7660MTV/883B
ICL7660SMTV/883B
ICL7662MTV/883B
ICL7667MJA/883B
ICL7667MTV/883B
ICL8021MTY/883B
ICL8023MJE/883B
ICL8038AMJD/883B
ICL8038BMJD/883B
ICL8069CMSQ/883B
ICL8069DMSQ/883B
ICL8211MTY/883B
ICL8212MTY/883B
ICM7555MTV/883B
ICM7556MJD/883B
LM4250H/883B

Analog Switch Products 883B Rev. C

D123AK/883B
D123AL/883B
D125AK/883B
D125AL/883B
D129AK/883B
D129AL/883B
DG123AL/883B
DG123AP/883B
DG125AL/883B
DG125AP/883B
DG126AK/883B
DG126AL/883B
DG126AP/883B
DG129AK/883B
DG129AL/883B
DG129AP/883B
DG133AK/883B
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DG151AK/883B
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DG153AL/883B
DG153AP/883B
DG154AK/883B
DG154AL/883B
DG161AL/883B
DG161AP/883B
DG162AK/883B
DG162AL/883B
DG163AL/883B
DG163AP/883B
DG164AK/883B
DG164AL/883B
DG180AA/883B
DG180AK/883B
DG180AP/883B
DG180AL/883B

Analog Switch Products 883B Rev. C (cont.)

DG180AP/883B
DG181AA/883B
DG181AK/883B
DG181AP/883B
DG181AL/883B
DG181AP/883B
DG182AA/883B
DG182AK/883B
DG182AL/883B
DG182AP/883B
DG183AL/883B
DG183AP/883B
DG184AK/883B
DG184AL/883B
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DG200AA/883B
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DG201AK/883B
DG202AK/883B
DG300AAA/883B
DG300AAK/883B
DG301AAA/883B
DG301AAK/883B
DG302AAK/883B
DG303AAK/883B
DG308AAK/883B
DG309AK/883B
DGM181AA/883B
DGM181AK/883B
DGM182AA/883B
DGM182AK/883B
DGM184AK/883B
DGM185AK/883B
DGM190AK/883B
DGM191AK/883B
IH5009MDD/883B
IH5009MJD/883B
IH5010MDD/883B
IH5010MJD/883B
IH5011MDE/883B
IH5011MJE/883B

Analog Switch Products 883B Rev. C (cont.)

IH5012MDE/883B
IH5012MJE/883B
IH5013MDD/883B
IH5013MJD/883B
IH5014MDD/883B
IH5014MJD/883B
IH5015MDE/883B
IH5015MJE/883B
IH5016MDE/883B
IH5016MJE/883B
IH5017MDD/883B
IH5017MJD/883B
IH5018MDD/883B
IH5018MJD/883B
IH5019MDE/883B
IH5019MJE/883B
IH5020MDE/883B
IH5020MJE/883B
IH5021MDD/883B
IH5021MJD/883B
IH5022MDD/883B
IH5022MJD/883B
IH5023MDE/883B
IH5023MJE/883B
IH5024MDE/883B
IH5024MJE/883B
IH5040MJE/883B
IH5041MJE/883B
IH5042MJE/883B
IH5043MJE/883B
IH5044MJE/883B
IH5045MJE/883B
IH5046MJE/883B
IH5047MJE/883B
IH5052MDE/883B
IH5052MJE/883B
IH5053MDE/883B
IH5053MJE/883B
IH5108MJE/883B
IH5116MJI/883B
IH5140MJE/883B
IH5141MJE/883B
IH5142MJE/883B
IH5143MJE/883B
IH5144MJE/883B
IH5145MJE/883B
IH5148MJE/883B
IH5149MJE/883B
IH5150MJE/883B
IH5151MJE/883B
IH5208MJE/883B
IH5216MJI/883B
IH5341MTW/883B
IH5352MJE/883B
IH6108MJE/883B
IH6116MJI/883B
IH6201MJE/883B
IH6208MJE/883B
IH6216MJI/883B

For other Harris Semiconductor Products, see pages 2715 thru 2775.

QPL/Hi-Rel Devices

INTERSIL Products

Data Acquisition Products
JM38510

JM38510/12702BEA	JAN AD7520
JM38510/12703BVA	JAN AD7521
JM38510/12704BVA	JAN AD7541
JM38510/12704BVC	JAN AD7541

Digital/Micro Peripheral
Standard Military Drawings

5962-8765301JA	ICM7170MDG
5962-8765301JC	ICM7170MDG

Linear
Standard Military Drawings

5962-8766001GA	ICL7667MTV
5962-8766001PA	ICL7667MJA
7703901GA	LM4250H
7703901PA	LM4250J

Analog Switch Products
JM38510

JM38510/10501BEA	JAN IH5040MDE
JM38510/10501BEC	JAN IH5040MDE
JM38510/10502BEA	JAN IH5041MDE
JM38510/10502BEC	JAN IH5041MDE
JM38510/10503BEA	JAN IH5042MDE
JM38510/10503BEC	JAN IH5042MDE
JM38510/10504BEA	JAN IH5043MDE
JM38510/10504BEC	JAN IH5043MDE
JM38510/10505BEA	JAN IH5044MDE
JM38510/10505BEC	JAN IH5044MDE
JM38510/10506BEA	JAN IH5045MDE
JM38510/10506BEC	JAN IH5045MDE
JM38510/11101BAC	JAN DG181AL
JM38510/11101BCA	JAN DG181AP
JM38510/11101BCC	JAN DG181AP
JM38510/11101BIA	JAN DG181AA
JM38510/11101BIC	JAN DG181AA
JM38510/11102BAC	JAN DG182AL
JM38510/11102BCA	JAN DG182AP
JM38510/11102BCC	JAN DG182AP
JM38510/11102BIA	JAN DG182AA
JM38510/11102BIC	JAN DG182AA
JM38510/11103BAC	JAN DG184AL
JM38510/11103BEA	JAN DG184AP
JM38510/11103BEC	JAN DG184AP
JM38510/11104BAC	JAN DG185AL
JM38510/11104BEA	JAN DG185AP
JM38510/11104BEC	JAN DG185AP
JM38510/11105BAC	JAN DG187AL
JM38510/11105BCA	JAN DG187AP
JM38510/11105BCC	JAN DG187AP
JM38510/11105BIA	JAN DG187AA
JM38510/11105BIC	JAN DG187AA
JM38510/11106BAC	JAN DG188AL
JM38510/11106BCA	JAN DG188AP
JM38510/11106BCC	JAN DG188AP
JM38510/11106BIA	JAN DG188AA

Analog Switch Products
JM38510 (cont.)

JM38510/11106BIC	JAN DG188AA
JM38510/11107BAC	JAN DG190AL
JM38510/11107BEA	JAN DG190AP
JM38510/11107BEC	JAN DG190AP
JM38510/11108BAC	JAN DG191AL
JM38510/11108BEA	JAN DG191AP
JM38510/11108BEC	JAN DG191AP
JM38510/11601BCA	JAN DG300AAP
JM38510/11601BCC	JAN DG300AAP
JM38510/11602BCA	JAN DG301AAP
JM38510/11602BCC	JAN DG301AAP
JM38510/11603BCA	JAN DG302AAP
JM38510/11603BCC	JAN DG302AAP
JM38510/11604BCA	JAN DG303AAP
JM38510/11604BCC	JAN DG303AAP
JM38510/12302BEA	JAN DG201AP
JM38510/12302BEC	JAN DG201AP
JM38510/19007BEA	JAN IH6108MDE
JM38510/19007BEC	JAN IH6108MDE
JM38510/19008BEA	JAN IH6208MDE
JM38510/19008BEC	JAN IH6208MDE

Analog Switch Products
Standard Military Drawings

5862-8513106EA	IH5208MJE
5962-8513104XA	IH5116MJI
5962-8513105XA	IH5216MJI
5962-876730CA	DG180AP
5962-876730IA	DG180AA
7705201EA	IH6108MJE
7705203EA	IH5108MJE
7705301EA	DG201AK
7801401CA	DG129AK
7801401CC	DG129AP
8100601EA	IH5040MJE
8100602EA	IH5041MJE
8100603EA	IH5042MJE
8100604EA	IH5043MJE
8100605EA	IH5044MJE
8100606EA	IH5045MJE
8100607EA	IH5046MJE
8100608EA	IH5047MJE
8100609EA	IH5140MJE
8100610EA	IH5141MJE
8100611EA	IH5142MJE
8100612EA	IH5143MJE
8100613EA	IH5144MJE
8100614EA	IH5145MJE
8100615EA	IH5046MJE
8100616EA	IH5047MJE
8100619EA	IH5148MJE
8100620EA	IH5149MJE
8100621EA	IH5150MJE
8100622EA	IH5151MJE

Mil-S-19500
Discrete JFETS

2N4091JAN	2N4859JTX
2N4091JTX	2N4860JAN
2N4092JAN	2N4860JTX
2N4092JTX	2N4861JAN
2N4093JAN	2N4861JTX
2N4093JTX	2N5114JAN
2N4856JAN	2N5114JTX
2N4856JTX	2N5114JAN
2N4857JAN	2N5115JAN
2N4857JTX	2N5115JTX
2N4858JAN	2N5116JAN
2N4858JTX	2N5116JTX
2N4859JAN	

For other Harris Semiconductor Products, see pages 2715 thru 2775.

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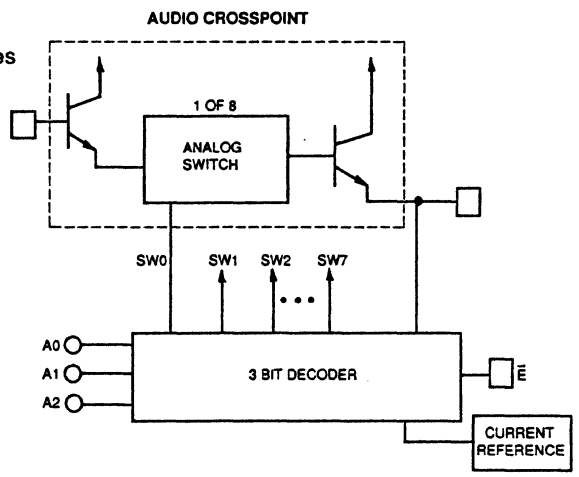
ADVANCE INFORMATION

8 x 1 AUDIO SWITCHES - GX818

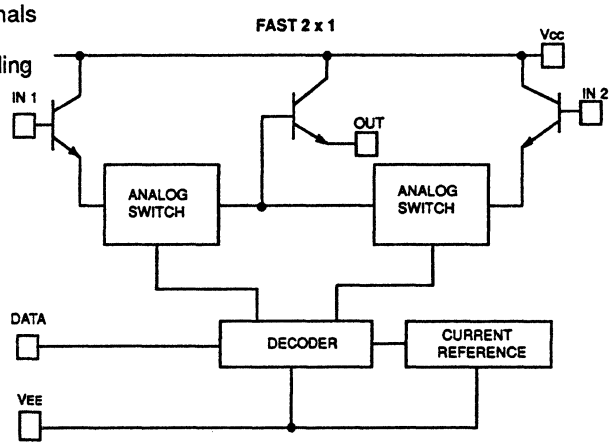
- for applications in production and routing matrices
- 8 inputs, 1 output
- signal level 40V peak to peak
- signal to noise 100dB
- noise level 100dB below 8dBm
- distortion 0.001%
- crosstalk -90dB at 20kHz
- CMOS and TTL logic compatible
- supply voltage 22V



ADVANCE INFORMATION

FAST 2 x 1 VIDEO SWITCHES - GX402

- for sub - pixel switching (toggling) of video signals
- applications in special effects and video sampling
- bandwidth 100MHz
- differential gain 0.05%
- differential phase 0.05°
- switching speed less than 25ns
- crosstalk - 80dB @ 10MHz
- CMOS and TTL logic compatible
- supply voltage ± 5V to ± 12V



Complete data and applications information is available. Call us toll-free 1-800-263-9353.

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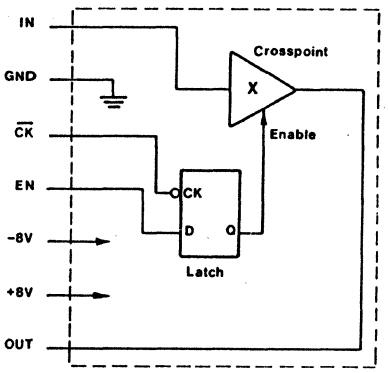
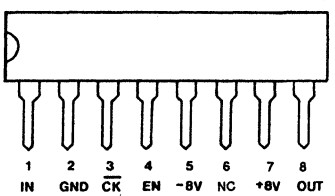
MONOLITHIC 1 x 1 VIDEO CROSSPOINT SWITCH - GX401

- 30MHz bandwidth (±1.0 dB)
- insertion loss 0.05dB at 100KHz
- frequency response DC to 10MHz I.L.±0.05dB
- differential gain @ 3.58MHz 0.04% (max)
- differential phase @ 3.58MHz 0.02o (max)
- TTL and 5V CMOS compatible logic inputs
  compatible with all popular video standards
- 8-pin single-in-line package
- built-in enable latch allows synchronous selection



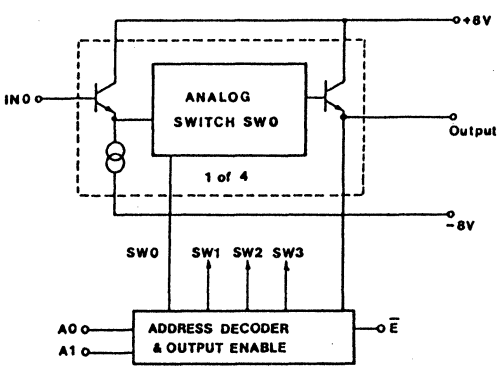
Simplified Block Diagram



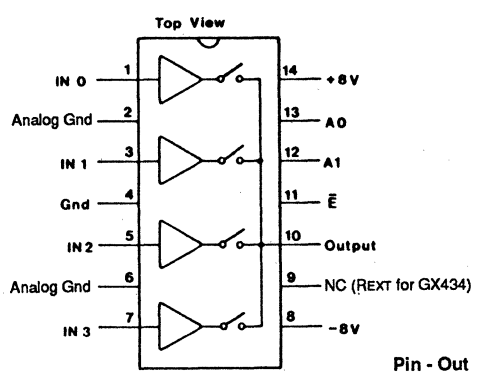
Pin - Out

4 x 1 VIDEO SWITCHES - GX414, GX414A, GX424, GX434

- 40 MHz bandwidth (± 1.0 dB) (50MHz for GX414A)
- insertion loss 0.155 dB (max)
- frequency response DC to 5 MHz ± 0.05 dB
- low all hostile crosstalk -86dB (typ) at 3.58 MHz
- differential gain at 3.58 MHz 0.05% (max)
- differential phase at 3.58 MHz 0.05° (max)
- TTL and CMOS compatible logic inputs
- up to five parts can be paralleled for 20
  inputs and a common output
- low cost 14 pin molded DIP packages
- for NTSC, PAL, SECAM applications
- make before break switching



Functional Schematic



Pin - Out

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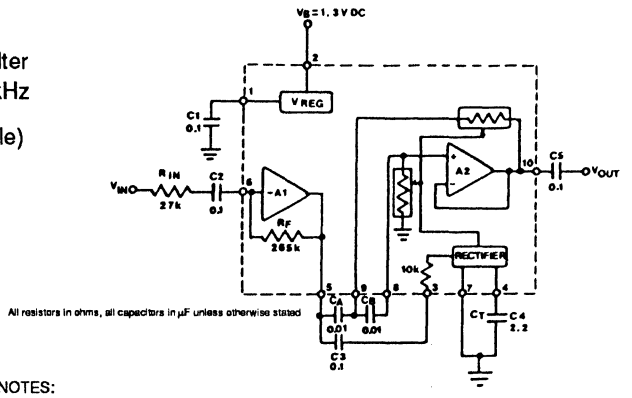
ADAPTIVE HIGHPASS FILTER WITH INDEPENDENT GAIN BLOCK-LS581

- unity gain 12 dB/oct. highpass Butterworth filter
- adaptive frequency range from 200 Hz to 2 kHz
  (Limits are adjustable, but remain one decade apart)
- rectifier threshold set to 82 dBSPL (adjustable) see note 2
- low noise, typically 3 μV
- current drain typically 300 μA
- operates from 1.1 to 2 VDC
- preamplifier with 45 dB open loop gain



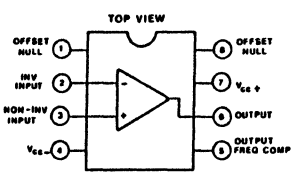
NOTES:
1. To change corner frequency limits, the values of CA and CB are increased or decreased.
2. Using a microphone with a sensitivity of -60dB / μB @ 1kHz

Block Diagram for LS581

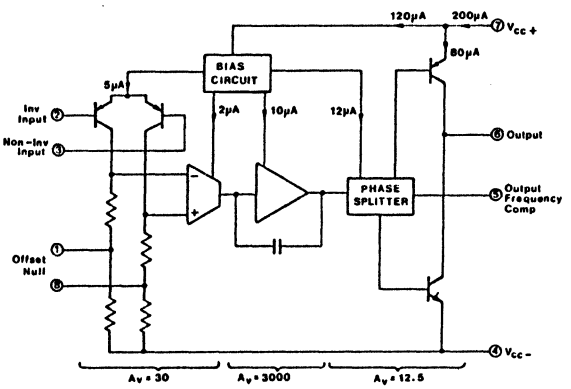
ALSO AVAILABLE WITHOUT GAIN BLOCK AS LF581

LOW VOLTAGE, LOW POWER OPERATIONAL AMPLIFIER – LC810

- low voltage design — operates down to 1.0 V total supply voltage
- low power consumption — 200μA typical quiescent supply current
- single or dual supply operation
- class AB output stage swings virtually rail-to-rail



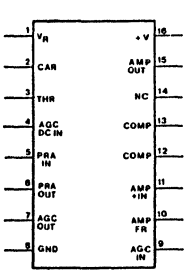
Pin - Out



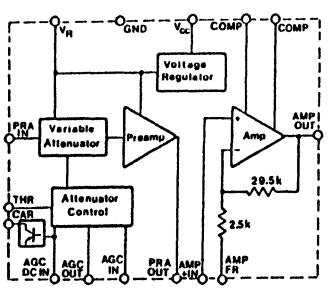
Functional Schematic

LOW DISTORTION AGC AMPLIFIER – LC403

- high stability of output level
- 34 dB AGC operating range
- adjustable AGC threshold
- adjustable attack and release time
- levels adjustable with external components
- can be operated as a voltage controlled gain amplifier
- two gain blocks may be used separately
- maximum frequency 100 kHz
- low carrier (threshold) detector
- operates from standard 5V power supply



Pin - Out



Functional Block Diagram

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RESONANT MODE POWER SUPPLY CONTROLLERS LD405 - GP605

The objective of power supply designers is to achieve ever higher power densities, while lowering the cost per watt and without sacrificing reliability. The resonant mode approach best fulfils this objective.

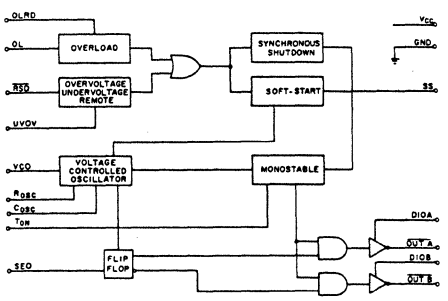
Instead of pulse width modulation (PWM), the LD405 and the GP605 use frequency modulation. The pulse width is constant while the frequency is varied in response to load changes. Some significant advantages include:

- greatly reduced power supply size, weight and cost
- reduced switching losses and EMI
- reduced component stresses from zero current switching

Part No.	Package	Temperature Range
LD405D	16 Pin DIP	0°C to 70°C
LD405K	16 Pin SOIC	0°C to 70°C
GP605CD	16 Pin Plastic DIP	0°C to 70°C
GP605CK	16 Pin SOIC	
GP605ID	16 Pin Plastic DIP	-25°C to +85°C
GP605IK	16 Pin SOIC	
GP605M	TBD	-55°C to +125°C

LD405

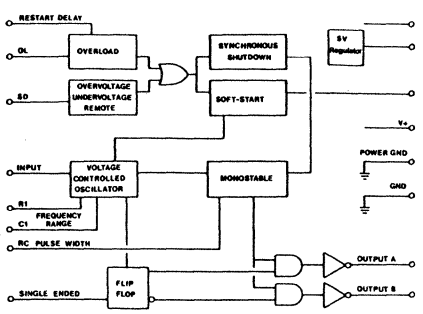
- frequency range of 10kHz to 1MHz
- operating frequency range (min. and max.) set by a resistor and capacitor
- synchronous overload shutdown with delayed restart
- synchronous overvoltage, undervoltage and remote shutdown
- soft start
- single ended or complementary outputs
- drives power MOSFETs directly
- low cost 16 pin DIP or SOIC



Functional Block Diagram

GP605

- frequency range of 1 kHz to 1.2 MHz
- operating frequency range set by resistor and capacitor.
- pulse width set by a resistor and capacitor.
- synchronous overload shutdown with delayed restart
- Synchronous overvoltage, undervoltage and remote shutdown.
- soft start.
- single ended or complementary outputs.
- drives power MOSFETS directly.
- low cost 16 pin DIP package or 16 pin SOIC.
- available in the commercial, industrial and military temperature ranges



GP605 Functional Block Diagram

Complete data and applications information is available. Call us toll-free 1-800-263-9353.

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GBL GigaBit Logic

GaAs IC Product Line

FEATURES

- Industry's broadest family of GaAs ICs
- DC to 3 GHz clock and data rates
- 150 ps output transition times
- Moderate power comparable to ECL 100K logic
- Extended Mil. temp. range for some products
- Demonstrated high reliability stemming from a higher activation energy (1.4 eV) than silicon ICs
- Radiation hardness approaching 10^8 rads
- ECL/GaAs compatible I/O levels and inherent TTL compatible outputs

10G PICOLOGIC™ FAMILY

	PART NO.	SPEED	PACKAGES*	EXT. TEMP
ARITHMETIC OPERATORS				
Dual 9-Bit Parity Generator/Checker and 8-Bit Equivalence Checker	10G045	850 ps	C,L,X	
High Speed 4-Bit Adder	10G100	1200 ps	C,L,X	
Carry Lookahead Generator	10G101	675 ps	C,L,X	
32-bit DDS Phase Accumulator	10G102	1 GHz	C1,X	
COUNTERS/PRESCALERS				
2-Stage Ripple Counter/Divider	10G060	3.0 GHz	F,L36,X	-40°C to +100°C
4-Bit Synchronous Programmable Counter	10G061	1.3 GHz	C,L,X	-40°C to +100°C
7-Stage Ripple Counter/Divider	10G065	3.0 GHz	F,L36,X	-40°C to +100°C
Variable Modulus Divider	10G070	2.0 GHz	F,L36,X	-40°C to +100°C
CROSSPOINT SWITCHES				
8X8X1 Expandable Crosspoint Switch	10G050	2 Gb/s	C1,X	
16X16X1 Crosspoint Switch	10G051	2.6 Gb/s	C1,X	
DRIVERS/RECEIVERS/COMPARATORS				
Dual 2:1 Multiplexed Fanout Buffer	10G010	1.5 GHz	C,L,X	-55°C to +125°C
Dual 1:4 Fanout Buffer	10G011B	1.6 GHz	C,L,X	-55°C to +125°C
Dual Complementary Driver/Comparator	10G012B/10G013	1.75 GHz	C,L,X	
FLIP FLOPS				
Dual Precision D Flip Flop	10G021A	2.7 GHz	C,L,X	
Quad D Flip Flop With 2:1 Muxed Inputs	10G023	1.9 GHz	C,L,X	
Quad D Flip Flop With XOR Inputs	10G024	1.9 GHz	C,L,X	
GATES				
Quad 3 Input NOR	10G000A	320 ps	C,L,X	
Quad 2 Input NOR	10G001	320 ps	C,L,X	
Quad 2-input XOR/XNOR and Line Receiver	10G002	1.8 GHz	C,L,X	-55°C to +125°C
Dual AO/AOI 4-Wide 5,4,3,2 / 2-Wide 3,2	10G003	800 ps	C,L,X	-55°C to +125°C
MULTIPLEXERS/DEMULTIPLEXERS				
Quad 2:1 MUX	10G004	1.8 GHz	C,L,X	
8:1 Time Division MUX	10G040A	1.45 Gb/s	C,L,X	
1:8 Time Division DEMUX	10G041A	1.45 Gb/s	C,L,X	
3:8 or Dual 2:4 Decoder/DEMUX	10G044	650 ps	C,L,X	
Quad 4:1 or Dual 8:1 MUX	10G046	600 ps	C,L,X	
REGISTERS				
Octal Register/Shift Register/PN Code Generator	10G022	1.5 GHz	C,L,X	

16G ANALOG, ATE, AND FIBERCOM PRODUCTS FAMLY

Customizable 15 mA Schottky Diode Array	16G010		F,L36,X	
Customizable 100 mA Schottky Diode Array	16G011		F,L36,X	
Customizable Single Gate MESFET Array	16G020	f_t = 22 GHz	F,L36,X	
Customizable Dual Gate MESFET Array	16G021	f_t = 22 GHz	F,L36,X	
Clock and Data Recovery Circuit	16G040	2.0 Gb/s	C,L,X	
16G040 Demo Board	90GCDR	800 Mb/s	Board	
16G040 Demo Board w/10G041A DEMUX	90GCDR-DX	800 Mb/s	Board	
Phase/Frequency Comparator	16G044	1.0 GHz	C,L,X	
Time Delay Generator / 1 ps resolution	16G060	20 ns Prog. Delay	C,L,X	
Dual 5V Pin Driver	16G061	1.5 GHz	C,L,X	

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Gigabit Logic

GBL GigaBit Logic

12G NANORAM™ & 14G NANOROM™ MEMORY

NanoRam™ Features
- 256 X 4 & 1024 X4-bit organization
- Equal read and write cycle times
- Internally generated write pulse (self-timed)
- ECL/GaAs I/O compatible
- Wire-OR output capability

NanoRom™ Features
- 512 X 8-bit organization
- 500 ps typical OE access time
- ECL compatible power supplies
- ECL/GaAs compatible I/O levels
- Wire-OR output capability

DEVICE DESCRIPTION	PART NO.	SPEED	PACKAGES*
256 X 4-bit Registered Self-Timed RAM	12G014-2	2.5 ns R/W cycle time	C,L,X
256 X 4-bit Registered Self-Timed RAM	12G014-3	3.5 ns R/W cycle time	C,L,X
1024 X 4-bit Latched, Selft-Timed Static RAM	12G044-2	3.5 ns R/W cycle=access time	C,L,X
512 X 8-bit Mask Programmable ROM	14GM048-2	1.5 ns address access	C,L,X
512 X 8-bit Mask Programmable ROM w/on-chip decoder	14GD048-2	1.5 ns address access	C,L,X

90G PROTOTYPING AND SUPPORT PRODUCTS

PROTOTYPE DEVELOPMENT KIT

- Complete kit for prototyping and testing all GigaBit GaAs ICs
- Low cost, quick turnaround solution to initial device performance testing and evaluation needs
- Kit components available separately for expanded applications
- 90GUPB Universal Printed Circuit Board accepts up to eight GigaBit Logic GaAs surface mount ICs and up to eight 300 or 400 mil wide DIP ICs. 90GUPB68 accepts 36, 40, and 68 pin packages.
- Supports signals with 100 ps rise/fall times and up to 3 GHZ clock rate

	PART #	DESCRIPTION
PROTOTYPE DEVELOPMENT KIT	90GKIT-40	Contains 1 90GUPB, 1 90G102, 1 10GBPS, 2 90G101. Board standoffs and power supply connectors included.
KIT ACCESSORIES	90GUPB	Universal Prototyping Board for 36 and 40 pin packages only.
	90GUPB68	As above but with provision for two 68 pin "C1" packages.
	90GPPS	Power Supply Board.
	90G101	Package of 5 right angle SMA connectors for 90GUPB mounting.
	90G102	Components package for 90GUPB (20 ea. chip resistors, capacitors, 2.5' coax).
	90GSKT-40L	Package of 5 high speed sockets for 40 I/O "L" package. Mounts on 90GUPB.
	90GHS40A/B	Heatsinks for 40 I/O "L" and "C" package.
	90GHS36A	Heatsink for 36 I/O "F" and "L36" package.

Gigabit Logic

APPLICATION NOTES

- AB-1 Application and Performance of GigaBit's 40 I/O Chip Carrier
- AB-2 Minimizing Clock Skew Through Use of the 10G010 &10G011B
- AB-3 Decoupling and Termination Recommendations for PicoLogic™ and NanoRAM™ GaAs ICs
- AB-4 Design & Performance of the GigaBit C1 68 Pin LCC Package
- AN-2 Guidelines for the Use of Digital GaAs ICs
- AN-3 Thermal Management of PicoLogic™ and NanoRam™ GaAs Digital IC Families
- AN-4 Interfacing PicoLogic™ & NanoRam™ ICs to Other Logic Families
- AN-5 Guidelines for the Use of the 12G014 400 MHz Registered RAM
- AN-6 Applying the 10G061 as a Universal Programmable Counter
- AN-7 Application of the 16G040 Clock and Data Recovery Circuit

PART NUMBER DESCRIPTION

XXG XXX A B - Y C

Product Family
10G = PicoLogic™
12G = NanoRAM™
14G = NanoROM™
16G = Analog/ATE/Fibercom
80G = ASIC Products
90G = Prototyping/Support

† Absence of character indicates nominal

Device Number

Product Revision Level

Temperature Range identifier†
K = -40°C to +100°C
M = -55°C to +125°C

Speed identifier†

Package indentifier

*AVAILABLE PACKAGES

- C1 = 68 I/O Leaded Chip Carrier
- C = 40 I/O C-Leaded Chip Carrier
- L = 40 I/O Leadless Chip Carrier
- F = 36 I/O Flat Package
- L36* = 36 I/O Leadless Chip Carrier
- X = Unpackaged Dice

*Note: Character "36" not marked on package

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Call your nearest sales representative or sales office for a copy of GigaBit's GaAs IC Data Book and Designer's Guide

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☐ Z80 FAMILY

• Z80® CPU/Central Processing Unit

Part Number	FEATURE
Z8400	• 158 instructions, 8080A software compatibility • 8 MHz, 6 MHz, 4MHz and 2.5 MHz clocks for the Z80H, Z80B, Z80A and Z80 • The extensive instruction set includes string, bit, byte, and word operations. Block searches and block transfers together with indexed and relative addressing. • The Z80 microprocessors and associated family of peripheral controllers are linked by a vectored interrupt system to be daisy-chained. • Duplicate sets of both general-purpose and flag registers, two 16-bit index registers. • On-chip dynamic memory refresh counter.

• Z80® PIO/Parallel Input/Output Controller

Part Number	FEATURE
Z8420	• A direct interface between Z80 microcomputer systems and peripheral devices. • Both ports have interrupt-driven handshake for fast response. • 4 programmable operating modes: byte input, byte output, byte Input/output (Port A only), and bit input/output. • Programmable interrupts on peripheral status conditions. • Standard Z80 Family bus-request and prioritized interrupt-request daisy chains implemented without external logic. • Port B outputs can drive Darlington transistors (1.5 mA 1.5V)

• Z80® CTC/Counter/Time Circuit

Part Number	FEATURE
Z8430	• Four independently programmable counter/timer channels • Zero Count/Timeout outputs capable of driving Darlington transistors. • Selectable positive or negative trigger initiates timer operation. • Standard Z80 Family daisy-chain interrupt structure. • Interfaces directly to the Z80 CPU or for buad rate generation to the Z80 SIO

• Z80® SIO/Serial Input/Output Controller

Part Number	FEATURE
Z8440	• 2 independent full-duplex channels, with separate control and status lines for modems or other devices. • Data rates of 0 to 800K bits/second in the ×1 clock mode. • Synchronous protocols and Asynchronous protocols. • Receiver data registers quadruply buffered transmitter registers doubly buffered. • Highly sophisticated and flexible daisy chain interrupt vector

Note: These Products are available within ASIA and Western Europe.

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□ RAMs, ROMs

• Static RAM

Process	Organization	Part Number	Access Time	Power Supply Current		Power Supply	Package Type
				Operating	Standby		
CMOS	2,048X8	GM76C28-10	100ns	60mA(Max.)	50μA(Max.)	5V ± 10%	24DIP 24SOP
		GM76C28-12	120ns	50mA(Max.)	50μA(Max.)		
	8,192X8	GM76C88-70	70ns	110mA(Max.)	2mA(Max.)		28DIP 28SOP
		GM76C88-85	85ns				
		GM76C88-10	100ns				
	65,536X1	GM76C64-45	45ns	70mA(Max.)	5mA(Max.)		22DIP
		GM76C64-55	55ns				
		GM76C64-70	70ns				
	*32,768X8	GM76C256-85	85ns	80mA(Max.)	200μA(Max.)		28DIP 28SOP
		GM76C256-10	100ns				
		GM76C256-12	120ns				
		GM76C256-15	150ns				

• Dynamic RAM

Process	Organization	Part Number	Access Time	Power Supply Current		Feature (mode)	Package Type
				Operating	Standby		
NMOS	262,144X1	GM71256-10	100ns	70mA(Max.)	4.5mA(Max.)	PAGE	16DIP
		GM71256-12	120ns				
		GM71256-15	150ns				
CMOS	*262,144X1	GM71C256-85	85ns	70mA(Max.)	2mA(Max.)	FAST PAGE	16DIP
		GM71C256-10	100ns				
		GM71C256-12	120ns				
	**1,048,576X1	GM71C1000-85	85ns	75mA(Max.)	3mA(Max.)	FAST PAGE	18DIP
		GM71C1000-10	100ns				
		GM71C1000-12	120ns				
	*262,144X4	GM71C4256-85	85ns	75mA(Max.)	3mA(Max.)	FAST PAGE	20DIP
		GM71C4256-10	100ns				
		GM71C4256-12	120ns				

• ROM

Process	Organization	Part Number	Access Time	Power Supply Current		Power Supply	Package Type
				Operating	Standby		
NMOS	65,536X8	GM23512-10	100ns	100mA(Max.)	20mA(Max.)	5V ± 10%	28DIP
		GM23512-15	150ns				
		GM23512-20	200ns				
	131,072X8	GM231000	250ns	100mA(Max.)	20mA(Max.)		
	131,072X8	GM231000-30A	250ns	100mA(Max.)	20mA(Max.)		
		GM231000-31A	250ns				
		GM231000-32A	250ns				

* : under development
** : to be scheduled

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GM71256

262,144 x 1BIT DYNAMIC RAM

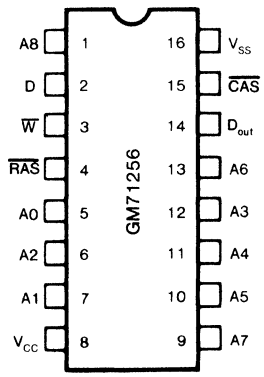
Description

The GM71256 is high speed, high performance dynamic RAM, organized 262,144 and manufactured using advanced NMOS silicon-gate technology. The design is optimised for both high speed and low power dissipation.

The GM71256 features multiplexed addressing, and all input signals, include clocks, are TTL-compatible, input and output signals are the same polarity, and the 3-state output buffer is $\overline{CAS}$ controlled. The Hi-C single transistor memory cell is used to enhance signal margin and reduce the α particle included soft error. This device offers page mode operation which allows high speed random access memory cells within the same row.

The GM71256 features single power supply of 5V±10% tolerance and is available a 16 pin plastic DIP or cerdip

Pin Configuration



Features

- **262,144 words × 1-bit organization**
- **100/120/150 ns access time from $\overline{RAS}$**
- **50/60/75 ns access time from $\overline{CAS}$**
- **385/360/330 mW active power, Page Mode,**
- **25 mW standby power**
- **Multiplexed address inputs**
- **±10% power supply tolerance**
- **Read-Modify-Write capabilities**
- **$\overline{RAS}$ Only Refresh/Hidden Refresh**
- **Latched or high impedance output during refresh**
- **256 refresh cycles**
- **Page Mode operation**

Pin Description

V_{CC}	+5V Supply
D	Data In
D_{out}	Data Out
A_0-A_8	Address Input (0-8)
$\overline{W}$	Write Enable
$\overline{RAS}$	Row Enable
$\overline{CAS}$	Column Enable
V_{SS}	Ground
NC	No Connect

Absolute Maximum Ratings*

PARAMETER	SYMBOL	VALUE	UNIT
Voltage Range on V_{CC} Relative to V_{SS}	V_{CC}	−1.0 to +7.0	V
Power Dissipation	PD	1.0	W
Case Operating Temperature Range	T_C	0 to 85	°C
Ambient Operating Temperature Range	T_A	0 to 70	°C
Storage Temperature Range**	T_{stg}		
Ceramic Package		−65 to +160	°C
Plastic Package		−55 to +120	°C
Short Circuit Output Current	I_{OS}	50	mA

* Maximum Ratings are defined as the limiting conditions that the user can apply to the device under all variations of circuit and environmental conditions. If any rating is exceeded, permanent damage to the device may result. Extended operation at any of these conditions may result in reduced reliability.

** Bonding or soldering of the external pins of these devices can be performed safely at temperatures up to 300°C.

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Electrical Characteristics: (V_{CC}=5V ±10%, V_{SS}=0V, T_A=0 to 70°C)

PARAMETER	SYMBOL	GM71256-10		GM71256-12		GM71256-15		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
Output Voltages								
Low Level (I_{OL}=4.2mA)	V_{OL}	—	0.4	—	0.4	—	0.4	V
High Level (I_{OH}=−5.0mA)	V_{OH}	2.4	—	2.4	—	2.4	—	V
Power Supply Currents								
Operating Current								
(Average Operating Current $\overline{RAS}$ & $\overline{CAS}$ Cycling, t_{RC}=minimum)								
Page Mode	I_{CC1}	—	70*	—	65*	—	60*	mA
Standby Current								
($\overline{RAS}$=V_{IH}, Q=High Impedance)	I_{CC2}	—	4.5	—	4.5	—	4.5	mA
Refresh Current								
(Average Operating Current, Refresh Mode Operation)								
$\overline{RAS}$ Cycling, $\overline{CAS}$=V_{IH}, t_{RC}=min.	I_{CC3}	—	55*	—	50*	—	45*	mA
Page Mode Current								
(Average Operating Current, Page Mode Operation, $\overline{RAS}$=V_{IL}, $\overline{CAS}$ Cycling, t_{PC}=minimum)	I_{CC4}	—	50*	—	45*	—	40*	mA
Input Leakage Current								
(V_{CC}=5.5 V, V_I=0 to 6.5 V, All other leads at 0 V)	I_I	−10	10	−10	10	−10	10	μA
Output Leakage Current								
(Q=High Impedance, V_Q=0 to V_{CC})	I_O	−10	10	−10	10	−10	10	μA
Input Capacitance (A0-A8)**	C_{11}	—	5	—	5	—	5	pF
Input Capacitance (D, $\overline{W}$ Leads)**	C_{12}	—	5	—	5	—	5	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$ Leads)**	C_{13}	—	10	—	10	—	10	pF
Output Capacitance (Q Lead)**	C_O	—	7	—	7	—	7	pF

* Maximum occurs at T_A=0°C, I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} are specified with output open-circuited.
** Parameter periodically sampled and not 100% tested.

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GM71256

Timing Characteristics: (V_{CC}=5V ±10%, V_{SS}=0V, T_A=0 to 70°C) (Notes 1, 2, and 3)

DESCRIPTION	SYMBOL	JEDEC SYMBOL	GM71256-10		GM71256-12		GM71256-15		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
Random Read/Write Cycle Time	t_{RC}	t_{RELREL}	200	—	220	—	260	—	ns
Access Time from $\overline{RAS}$ (Notes 4 & 5)	t_{RAC}	t_{RELQV}	—	100	—	120	—	150	ns
Access Time from $\overline{CAS}$ (Notes 5 & 6)	t_{CAC}	t_{CELQV}	—	50	—	60	—	75	ns
Output Buffer Time Off Delay (Note 7)	t_{OFF}	t_{CEHQZ}	0	20	0	30	0	30	ns
Transition Time	t_T	t_T	2	50	2	50	2	50	ns
$\overline{RAS}$ Precharge Time	t_{RP}	t_{REHREL}	90	—	90	—	100	—	ns
$\overline{RAS}$ Pulse Width	t_{RAS}	t_{RELREH}	100	10000	120	10000	150	10000	ns
$\overline{RAS}$ Hold Time	t_{RSH}	t_{CELREH}	50	—	60	—	75	—	ns
$\overline{CAS}$ Pulse Width (Note 8)	t_{CAS}	t_{CELCEH}	50	10000	60	10000	75	10000	ns
$\overline{CAS}$ Hold Time	t_{CSH}	t_{RELCEH}	100	—	120	—	150	—	ns
$\overline{RAS}$ to $\overline{CAS}$ Delay (Note 4)	t_{RCD}	t_{RELCEL}	25	50	25	60	25	75	ns
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	t_{CEHREL}	0	—	0	—	0	—	ns
Row Address Setup Time	t_{ASR}	t_{RAVREL}	0	—	0	—	0	—	ns
Row Address Hold Time	t_{RAH}	t_{RELRAX}	15	—	15	—	15	—	ns
Column Address Setup Time	t_{ASC}	t_{CAVCEL}	0	—	0	—	0	—	ns
Column Address Hold Time	t_{CAH}	t_{CELCAX}	20	—	25	—	30	—	ns
Column Address Hold Time Ref. to $\overline{RAS}$	t_{AR}	t_{RELCAX}	75	—	90	—	105	—	ns
Read Command Hold Time Ref. to $\overline{RAS}$	t_{RRH}	t_{REHWX}	10	—	10	—	10	—	ns
Read Command Setup Time	t_{RCS}	t_{WHCEL}	0	—	0	—	0	—	ns
Read Command Hold Time Ref. to $\overline{CAS}$	t_{RCH}	t_{CEHWX}	0	—	0	—	0	—	ns
Write Command Hold Time	t_{WCH}	t_{CELWX}	15	—	20	—	25	—	ns
Write Command Hold Time Ref. to $\overline{RAS}$	t_{WCR}	t_{RELWX}	85	—	100	—	120	—	ns
Write Command Pulse Width	t_{WP}	t_{WLWH}	15	—	20	—	25	—	ns
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	t_{WLREH}	30	—	35	—	45	—	ns
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	t_{WLCEH}	20	—	30	—	40	—	ns
Data In Setup Time	t_{DS}	t_{DVCEL}	0	—	0	—	0	—	ns
Data In Hold Time	t_{DH}	t_{CELDX}	15	—	20	—	25	—	ns
Data In Hold Time Ref. to $\overline{RAS}$	t_{DHR}	t_{RELDX}	85	—	100	—	120	—	ns
Write Command Setup Time (Note 9)	t_{WCS}	t_{WLCEL}	0	—	0	—	0	—	ns
$\overline{CAS}$ to $\overline{W}$ Delay (Read-Modify-Write)	t_{CWD}	t_{CELWL}	25	—	30	—	35	—	ns
$\overline{RAS}$ to $\overline{W}$ Delay (Read-Modify-Write) (Note 6)	t_{RWD}	t_{RELWL}	75	—	100	—	125	—	ns
Data In Hold Time (Read-Modify-Write) (Note 6)	t_{DH}	t_{WLDX}	20	—	20	—	20	—	ns
Data In Setup Time (Read-Modify-Write)	t_{DS}	t_{DVWL}	0	—	0	—	0	—	ns
Refresh Period	t_{REF}	t_R	—	4.0	—	4.0	—	4.0	ms
Cycle Time (Read-Modify-Write)	t_{RMW}	$t_{WRELREL}$	245	—	260	—	310	—	ns
PAGE MODE OPTION									
Page Mode Cycle Time	t_{PC}	t_{CELCEL}	**120**	—	**130**	—	**145**	—	**ns**
$\overline{CAS}$ Precharge Time	t_{CP}	t_{CEHCEL}	**45**	—	**50**	—	**60**	—	**ns**

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GM76C28

CMOS 16K-BIT STATIC RAM

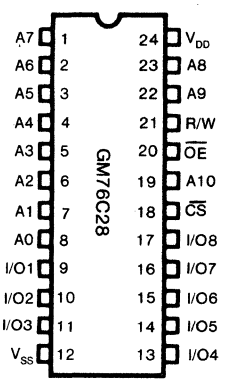
Description

The GM76C28$_{10/12}$ is a 2,048 words × 8 bits asynchronous, static, random access memory on a monolithic CMOS chip. Its very low standby power requirement makes it ideal for applications requiring non-volatile storage with back-up batteries. The asynchronous and static nature of the memory requires no external clock or refreshing circuit. Both the input and output ports are TTL compatible and the 3-state output allows easy expansion of memory capacity.

Features

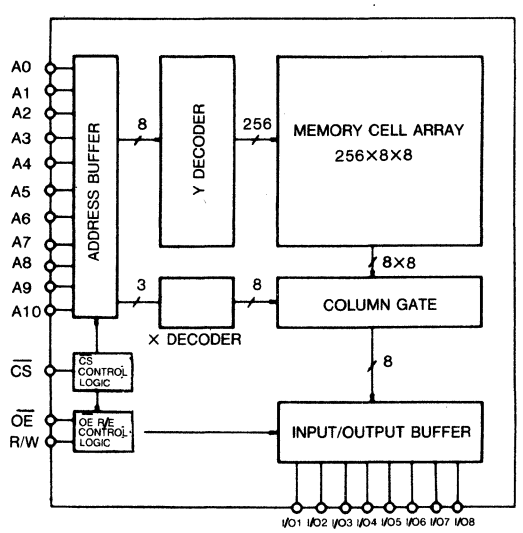
- **Access time ..... GM76C28-10 100ns(Max)**
  GM76C28-12 120ns(Max)
- **Low supply current ..... standby : 1μA(Typ)**
  operation: GM76C28-10 30mA(Typ)
  GM76C28-12 25mA(Typ)
- **Complete static operation**
- **Single power supply ..... 5V±10%**
- **TTL compatible inputs and outputs**
- **3-state output with wired-OR capability**
- **Non-volatile storage with back-up batteries**
- **Standard 24 DIP (600mil)/24 SOP (330mil)**

Pin Configuration



A0 to A10	Address Input
R/W	Read/Write
$\overline{OE}$	Output Enable
$\overline{CS}$	Chip Select
I/O1 to 8	Data Input/Output
V_{DD}	Power Supply(+5V)
V_{SS}	Power Supply(0V)

Schematic Diagram



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GM76C28

Absolute Maximum Ratings

Voltage on Any Pin with respect to GND	V_{DD}	−0.5 to 7.0V
Storage Temperature	T_{STG}	−65°C to +150°C
Operating Temperature	T_{OPR}	0°C to +70°C
Power dissipation	P_D	1.0W

Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

T_A=0°C to +70°C

V_{DD} Supply Voltage	4.5 to 5.5V
V_{IH} Input High Voltage	2.2 to 6.0V
V_{IL} Input Low Voltage	−0.5 to 0.8V

All voltages are referenced to GND pin=0V

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields, however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

Electrical Characteristics

DC Electrical Characteristics (V_{DD}=5V±10%, V_{SS}=0V, T_a=0 to 70°C)

SYMBOL	PARAMETER	CONDITIONS	GM76C28-10			GM76C28-12			UNIT
			MIN.	TYP.*	MAX.	MIN.	TYP.*	MAX.	
I_{LI}	Input leakage current	V_{DD}=5.5V, V_I=0 to V_{DD}	−1		1	−1		1	μA
I_{LO}	Output leakage current	$\overline{CS}$=V_{IH}, or $\overline{OE}$=V_{IH}, $V_{I/O}$=0 to V_{DD}	−1		1	−1		1	μA
I_{DDO}	Operating supply current	$\overline{CS}$=V_{IL}, $I_{I/O}$=0mA		30	60		25	50	mA
I_{DDO1}		V_{IH}=3.5V, V_{IL}=0.6V, $I_{I/O}$=0mA		16			16		mA
I_{DDA}	Average operating current	Min. cycle, duty=100%, $I_{I/O}$=0mA		30	60		25	50	mA
I_{DDS}	Standby supply current	$\overline{CS}$=V_{IH}		1.5	3.0		1.5	3.0	mA
I_{DDS1}		$\overline{CS}$=V_{DD}−0.2V		1	50		1	50	μA
V_{OL}	Output voltage	I_{OL}=4.0mA			0.4			0.4	V
V_{OH}		I_{OH}=−1.0mA	2.4			2.4			V

* Typical values are for reference, with V_{DD}=5V and Ta=25°C assumed

Terminal Capacitance (f=1MHz, Ta=25°C)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
C_I	Input capacitance	V_I=0V		4	6	pF
$C_{I/O}$	I/O capacitance	$V_{I/O}$=0V		6	8	pF

AC Electrical Characteristics:

Read Cycle (V_{DD}=5V±10%, V_{SS}=0V, Ta=0 to 70°C)

SYMBOL	PARAMETER	CONDITIONS	GM76C28-10		GM76C28-12		UNIT
			MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read cycle time	*1	100		120		ns
t_{ACC}	Address access time			100		120	ns
t_{ACS}	$\overline{CS}$ access time			100		120	ns
t_{CLZ}	$\overline{CS}$ output setup time	*2	10		10		ns
t_{OE}	$\overline{OE}$ access time	*1		55		60	ns
t_{OLZ}	$\overline{OE}$ output setup time	*2	5		10		ns
t_{CHZ}	$\overline{CS}$ output floating		0	40	0	40	ns
t_{OHZ}	$\overline{OE}$ output floating		0	40	0	40	ns
t_{OH}	Output hold time	*1	10		10		ns

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Write Cycle: (V_{DD}=5V±10%, V_{SS}=0V, Ta=0 to 70°C)

SYMBOL	PARAMETER	CONDITIONS	GM76C28-10		GM76C28-12		UNIT
			MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write cycle time	*1	100	—	120	—	ns
t_{CW}	Chip select time ($\overline{CS}$)		80	—	85	—	ns
t_{AW}	Address enable time		80	—	85	—	ns
t_{AS}	Address setup time		0	—	0	—	ns
t_{WP}	Write pulse width		65	—	70	—	ns
t_{OHZ}	$\overline{OE}$ output floating	*2	0	40	0	40	ns
t_{WHZ}	R/W output floating	*3	0	45	0	50	ns
t_{DW}	Input data setup time	*1	45	—	50	—	ns
t_{WR}	Address hold time		5	—	5	—	ns
t_{DH}	Input data hold time		0	—	0	—	ns
t_{OW}	R/W output setup time	*3	5	—	10	—	ns

Functions

Truth Table

$\overline{CS}$	$\overline{OE}$	R/W	A0 to A10	DATA I/O	MODE	I_{DD}
H	—	—	—	Hi-Z	Unselected	I_{DDS}, I_{DDSI}
L	L	H	Stable	Output data	Read	I_{DDO}
L	H	L	Stable	Input data	Write	I_{DDO}
L	L	L	Stable	Input data	Write	I_{DDO}

X: "H" or "L",—: "H", "L" or "Hi-Z"

Data Retention Characteristics with Low Voltage Power Supply (Ta=0 to 70°C)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDR}	Data retentions supply voltage	$\overline{CS}\geq V_{DDR}$-0.2V	2.0	—	5.5	V
I_{DDR}	Data retention current	V_{DD}=3.0V, $\overline{CS}\geq$2.8V	—	—	25	μA
t_{CDR}	Chip select data hold time	Refer to the figure below	0	—	—	ns
t_R	Operation recovery time		t_{RC}*	—	—	ns

* t_{RC}: read cycle time

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GM76C88

8,192 × 8 BIT STATIC RAM

Description

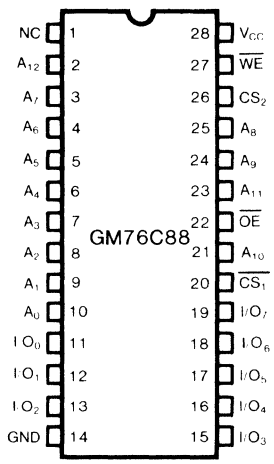
The GM76C88 is 65,536 bit staic random access memory organized as 8,192 words by 8 bits using CMOS technology, and operated from a single 5V supply. Advanced circuit techniques provide both high speed and low power features with a maximum operating current of 80mA and minimum cycle time of 70/85/100ns. The combination of speed-optimized circuitry results in a very high-speed memory device. Thus the GM76C88 is suitable for use in various microprocessor application systems where high speed are required. The GM76C88 is offered in 28 pin DIP

Features

- **8,192 × 8 organization**
- **High Speed:**
  Fast Access and Cycle Time 70/85/100ns (max.)
- **Low Power Standby and Low Power Operation**
- **Completely Static RAM: No Clock or Timing Strobe Required**
- **Common I/O (Three-State Output)**
- **Directly TTL Compatible: All Inputs and Outputs**
- **Single + 5V Operation (±10%)**
- **Standard 28 DIP (600 mil)/28 SOP (330 mil)**

Pin Configuration

(Top View)



Pin Name

$A_0 \sim A_{12}$	:	Address Input
$\overline{WE}$	:	Write Enable Input
$\overline{OE}$	:	Output Enable Input
$\overline{CS1}$, CS2	:	Chip Select Input
$I/O_0 \sim I/O_7$	:	Data Input/Output
V_{CC}	:	Power Supply, +5V
GND	:	Ground

Absolute Maximum Ratings

Voltage on Any Pin with respect to GND	V_{CC}	−2.0 to 7.0V
Storage Temperature	T_{STG}	−55°C to +150°C
Operating Temperature	T_{OPR}	0°C to +70°C
Power dissipation	P_D	1.0W

Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions:

T_A=0°C to +70°C

V_{CC}	Supply Voltage	4.5 to 5.5V
V_{IH}	Input High Voltage	2.2 to 6.0V
V_{IL}	Input Low Voltage	−0.5 to 0.8V

All voltages are referenced to GND pin=0V.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

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GM76C88

Truth Table

$\overline{WE}$	$\overline{CS_1}$	CS_2	$\overline{OE}$	Mode	I/O PIN	V_{CC} CURRENT	NOTE
X	H	X	X	Not Selected (Power Down)	High Z	I_{SB}, I_{SB1}	
X	X	L	X		High Z	I_{SB}, I_{SB2}	
H	L	H	H	Output Disabled	High Z	I_{CC}, I_{CC1}	
H	L	H	L	Read	Dout	I_{CC}, I_{CC1}	
L	L	H	H	Write	Din	I_{CC}, I_{CC1}	Write Cycle (1)
L	L	H	L		Din	I_{CC}, I_{CC1}	Write Cycle (2)

X: Don't Care

DC Electrical Characteristics: (V_{CC}=5V±10%, T_A=0°~70°C)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP*	MAX	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{IN}=GND to V_{CC}	−5	—	+5	μA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CS1}$=V_{IH} or CS2=V_{IL} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL}, $V_{I/O}$=GND to V_{CC}	−10	—	+10	μA
I_{CC}	Operating Power Supply Current	$\overline{CS1}$=V_{IL}, CS2=V_{IH}, $I_{I/O}$=0mA	—	40	80	mA
I_{CC1}	Average Operating Current	Min. cycle, duty=100%, $I_{I/O}$=0mA	—	60	110	mA
I_{SB}	Standby Power Supply Current	$\overline{CS1}$=V_{IH} or CS2=V_{IL}	—	1	3	mA
I_{SB1}**		$\overline{CS1}$≥V_{CC}−0.2V, CS2≥V_{CC}−0.2V or CS2≤0.2V	—	0.02	2	mA
I_{SB2}**		CS2≤0.2V	—	0.02	2	mA
V_{OL}	Output Voltage	I_{OL}=2.1mA	—	—	0.4	V
V_{OH}		I_{OH}=−1.0mA	2.4	—	—	V

* Typical limits are at V_{CC}=5.0V, T_A=25°C and specified loading.
** V_{IL} min=−0.3V

Capacitance: (T_A=25°C, f=1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MIN	MAX	UNIT
C_{IN}	Input Capacitance	V_I=0V		6	pF
C_{OUT}	Output Capacitance	V_O=0V		8	

Note: This parameter is sampled and not 100% tested.

AC Test Conditions

Input Pulse Levels ..... GND to 3.0V
Input Rise and Fall Times 10ns
Input and Output Timing References 1.5V
Output Load ..... 1 TTL Gate and C_L=100 pF (including scope and jig.)

Figure 1 Output Load

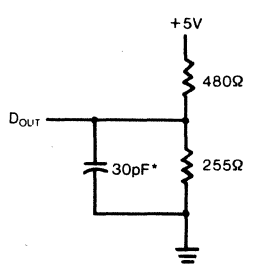
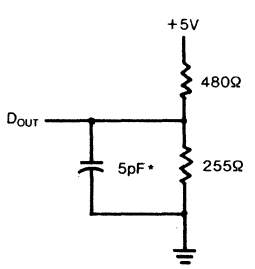


Figure 2 Output Load
(for t_{LZ1}, t_{LZ2}, t_{WHZ}, t_{OW})



* Including scope and jig

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GM71C4256
262,144 WORDS × 4 BIT CMOS DYNAMIC RAM

Description

The GM71C4256 is the new generation dynamic RAM organized 262,144×4 Bit. The GM71C4256 utilizes GoldStar's silicon Gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. Multiplexed address inputs permit the GM71C4256 to be packaged in a standard 20 pin DIP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V±10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL.

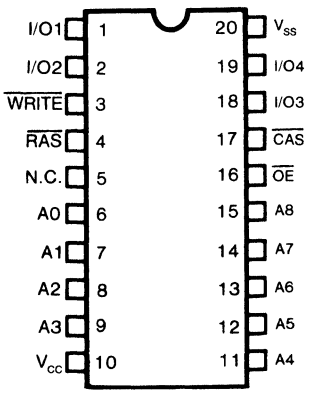
Features

- **262,144 × 4 Bit organization**
- **Fast access time and cycle time: 85/100/120(Max)**

PARAMETER		GM71C4256(ns)		
		-85	-10	-12
t_{RAC}	$\overline{RAS}$ Access Time	85	100	120
t_{AA}	Column Adress Access Time	45	50	60
t_{CAC}	$\overline{CAS}$ Access Time	30	30	35
t_{RC}	Cycle Time	165	190	220
t_{PC}	Fast Page Mode Cycle Time	50	55	70

- **Single Power Supply of 5V±10% with a built-in V_{BB} generator**
- **Low Power**
  - **330mW MAX. Operating (GM71C4256-85)**
  - **274mW MAX. Operating (GM71C4256-12)**
  - **16.5mW MAX. Standby**
- **Output unlatched at cycle end allows two-dimensional chip selection**
- **Read-Modify-Write, $\overline{RAS}$-only refresh, and Fast Page Mode Capability**
- **All input and output TTL compatible**
- **512 refresh cycles/8ms**
- **Industry standard 20 pin Plastic DIP**

Pin Configuration



A_0–A_8	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WRITE}$	Read/Write Input
$\overline{OE}$	Output Enable
I/O1~I/O4	Data Input/Output
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

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GM71C4256

Absolute Maximum Ratings

Input Voltage	V_{IN}	−1∼7V
Output Voltage	V_{OUT}	−1∼7V
Power Supply Voltage	V_{CC}	−1∼7V
Operating Temperature	T_{OPR}	0∼70°C
Storage Temperature	T_{STG}	−55∼150°C
Short Circuit Output Current	I_{OUT}	50mA

(Note 1)

Recommended DC Operating Conditions

(T_A=0°C to +70°C)

V_{CC}	Supply Voltage	4.5∼5.5V
V_{IH}	Input High Voltage	2.4∼6.5V
V_{IL}	Input Low Voltage	−1.0∼0.8V

(Note 2)

Functional Block Diagram

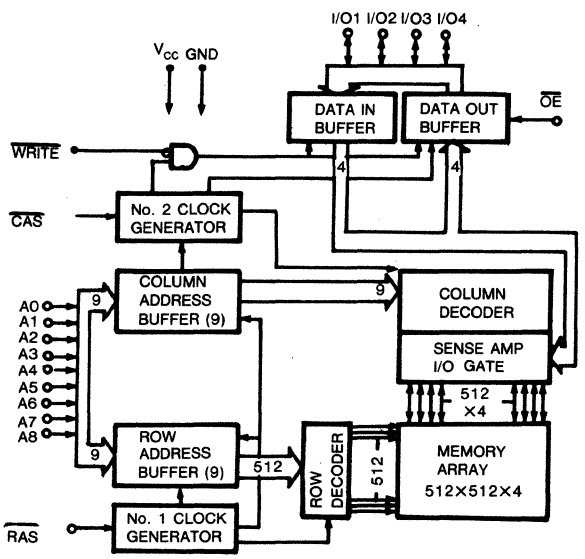

Figure 1

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DC Electrical Characteristics: (V_{CC}=5±10%, T_A=0 ~70°C)

SYMBOL	PARAMETER		MIN	MAX	UNIT	NOTES
V_{OH}	Output Level Output "H" Level Voltage (I_{OUT}=−5mA)		2.4	—	V	
V_{OL}	Output Level Output "L" Level Voltage (I_{OUT}=4.2mA)		—	0.4	V	
I_{CC1}	Operating Current	85	—	70	mA	3,4
	Average Power Supply Operating Current	100	—	65		
	($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC}=t_{RC} MIN)	120	—	55		
I_{CC2}	Standby Current Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{IH})		—	3	mA	
I_{CC3}	$\overline{RAS}$ Only Refresh Current	85	—	75	mA	3
	Average Power Supply Current	100	—	65		
	$\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$=V_{IH}: t_{RC}=t_{RC} MIN)	120	—	55		
I_{CC4}	Fast Page Mode Current	85	—	55	mA	3,4
	Average Power Supply Current	100	—	45		
	Fast Page Mode ($\overline{RAS}$=V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC}=t_{PC} MIN)	120	—	35		
I_{CC5}	Standby Current Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{CC}−0.2V)		—	1	mA	
$I_{I(L)}$	Input Leakage Current Any Input (0V≤V_{IN}≤6.5V, All other Pins Not Under Test = 0V)		−10	10	μA	
$I_{O(L)}$	Output Leakage Current (D_{OUT} is is Disabled, 0V≤V_{OUT}≤V_{CC}		−10	10	μA	

Capacitance (V_{CC}=5V±10%, f=1MHz, T_A=0~70°C)

SYMBOL	PARAMETER	MIN	MAX	UNIT
CI_1	Input Capacitance (A0—A8)	—	5	pF
CI_2	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$, $\overline{OE}$)	—	7	pF
C_O	Output Capacitance (I/O_1–I/O_4)	—	7	pF

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Part No.	Package	Availability
GD74LS00	14 B, J, D	NOW
GD74LS02	14 B, J, D	NOW
GD74LS04	14 B, J, D	NOW
GD74LS05	14 B, J, D	NOW
GD74LS06	14 B, J, D	NOW
GD74LS07	14 B, J, D	NOW
GD74LS08	14 B, J, D	NOW
GD74LS09	14 B, J, D	NOW
GD74LS10	14 B, J, D	NOW
GD74LS11	14 B, J, D	NOW
GD74LS14	14 B, J, D	NOW
GD74LS15	14 B, J, D	
GD74LS16	14 B, J, D	NOW
GD74LS17	14 B, J, D	NOW
GD74LS20	14 B, J, D	NOW
GD74LS21	14 B, J, D	NOW
GD74LS26	14 B, J, D	NOW
GD74LS27	14 B, J, D	NOW
GD74LS30	14 B, J, D	NOW
GD74LS32	14 B, J, D	NOW
GD74LS38	14 B, J, D	
GD74LS42	16 B, J, D	
GD74LS51	14 B, J, D	NOW
GD74LS55	14 B, J, D	
GD74LS73	14 B, J, D	NOW
GD74LS74A	14 B, J, D	NOW
GD74LS75	16 B, J, D	NOW
GD74LS86	14 B, J, D	NOW
GD74LS92	14 B, J, D	
GD74LS93	14 B, J, D	NOW
GD74LS95B	14 B, J, D	
GD74LS107A	16 B, J, D	
GD74LS109A	16 B, J, D	NOW
GD74LS112	16 B, J, D	NOW
GD74LS123	14 B, J, D	NOW
GD74LS125A	14 B, J, D	NOW
GD74LS132	14 B, J, D	
GD74LS138	16 B, J, D	NOW
GD74LS139	16 B, J, D	NOW
GD74LS145	16 B, J, D	
GD74LS148	16 B, J, D	
GD74LS151	16 B, J, D	NOW
GD74LS153	16 B, J, D	NOW

Part No	Package	Availability
GD74LS154	24 B, J, D	NOW
GD74LS155	16 B, J, D	NOW
GD74LS157	16 B, J, D	NOW
GD74LS158	16 B, J, D	NOW
GD74LS161A	16 B, J, D	NOW
GD74LS163A	16 B, J, D	NOW
GD74LS164	14 B, J, D	NOW
GD74LS165	16 B, J, D	NOW
GD74LS166	16 B, J, D	NOW
GD74LS174	16 B, J, D	NOW
GD74LS175	16 B, J, D	NOW
GD74LS191	16 B, J, D	NOW
GD74LS193	16 B, J, D	NOW
GD74LS194A	16 B, J, D	
GD74LS195A	16 B, J, D	
GD74LS240	20 B, J, D	NOW
GD74LS241	20 B, J, D	NOW
GD74LS243	14 B, J, D	
GD74LS244	20 B, J, D	NOW
GD74LS245	20 B, J, D	NOW
GD74LS251	16 B, J, D	
GD74LS257A	16 B, J, D	NOW
GD74LS258	16 B, J, D	NOW
GD74LS273	20 B, J, D	NOW
GD74LS280	14 B, J, D	NOW
GD74LS283	16 B, J, D	
GD74LS299	20 B, J, D	NOW
GD74LS322	20 B, J, D	
GD74LS365A	16 B, J, D	NOW
GD74LS366A	16 B, J, D	NOW
GD74LS367A	16 B, J, D	NOW
GD74LS368A	16 B, J, D	NOW
GD74LS373	20 B, J, D	NOW
GD74LS374	20 B, J, D	NOW
GD74LS377	20 B, J, D	
GD74LS390	16 B, J, D	
GD74LS393	14 B, J, D	NOW
GD74LS395A	16 B, J, D	NOW
GD74LS590	16 B, J, D	
GD74LS612	40 B, J	
GD74LS640	20 B, J, D	
GD74LS646	24 B, J, D	
GD74LS670	16 B, J, D	NOW

Part No.	Package	Availability
GD74S00	14 B, J, D	NOW
GD74S02	14 B, J, D	NOW
GD74S04	14 B, J, D	NOW
GD74S05	14 B, J, D	NOW
GD74S08	14 B, J, D	NOW
GD74S10	14 B, J, D	NOW
GD74S20	14 B, J, D	NOW
GD74S30	14 B, J, D	NOW
GD74S32	14 B, J, D	NOW
GD74S38	14 B, J, D	
GD74S51	14 B, J, D	NOW
GD74S64	14 B, J, D	
GD74S74	14 B, J, D	NOW
GD74S85	16 B, J, D	
GD74S86	14 B, J, D	NOW

Part No	Package	Availability
GD74S112	16 B, J, D	NOW
GD74S133	16 B, J, D	NOW
GD74S138	16 B, J, D	NOW
GD74S139	16 B, J, D	NOW
GD74S151	16 B, J, D	
GD74S153	16 B, J, D	
GD74S157	16 B, J, D	
GD74S163	16 B, J, D	NOW
GD74S174	16 B, J, D	NOW
GD74S175	16 B, J, D	
GD74S251	16 B, J, D	NOW
GD74S257	16 B, J, D	
GD74S280	14 B, J, D	NOW
GD74S299	20 B, J, D	NOW
GD74S374	20 B, J, D	NOW

• Miscellaneous

Part No.	Package	Availability
GD26LS29	16 B, J, D	
GD26LS33	16 B, J, D	
GD75188	14 B, J, D	NOW

Part No	Package	Availability
GD75189	14 B, J, D	NOW
GD75189A	14 B, J, D	NOW

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Note2 : No Mark Codes in Available column are under development.

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• 74HC/HCT/HCU

Part No.	Package	Availability
HC/HCT00	14 B, J, D	NOW
HC/HCT01	14 B, J, D	
HC/HCT02	14 B, J, D	NOW
HC/HCT03	14 B, J, D	NOW
HC/HCT04	14 B, J, D	NOW
HCU04	14 B, J, D	NOW
HC/HCT05	14 B, J, D	NOW
HC/HCT08	14 B, J, D	NOW
HC/HCT09	14 B, J, D	NOW
HC/HCT10	14 B, J, D	NOW
HC/HCT11	14 B, J, D	NOW
HC/HCT14	14 B, J, D	
HC/HCT20	14 B, J, D	NOW
HC/HCT21	14 B, J, D	NOW
HC/HCT27	14 B, J, D	NOW
HC/HCT30	14 B, J, D	NOW
HC/HCT32	14 B, J, D	NOW
HC/HCT34	14 B, J, D	NOW
HC/HCT42	14 B, J, D	NOW
HC/HCT51	14 B, J, D	NOW
HC/HCT58	14 B, J, D	NOW
HC/HCT73	14 B, J, D	
HC/HCT74	14 B, J, D	NOW
HC/HCT75	16 B, J, D	
HC/HCT76	16 B, J, D	
HC/HCT85	16 B, J, D	
HC/HCT86	14 B, J, D	NOW
HC/HCT93	14 B, J, D	
HC/HCT107	14 B, J, D	
HC/HCT109	16 B, J, D	
HC/HCT112	16 B, J, D	
HC/HCT113	14 B, J, D	
HC/HCT123	16 B, J, D	
HC/HCT125	14 B, J, D	NOW
HC/HCT126	14 B, J, D	NOW
HC/HCT132	14 B, J, D	
HC/HCT133	16 B, J, D	
HC/HCT137	16 B, J, D	
HC/HCT138	16 B, J, D	NOW
HC/HCT139	16 B, J, D	NOW
HC/HCT147	16 B, J, D	
HC/HCT148	16 B, J, D	
HC/HCT151	16 B, J, D	NOW
HC/HCT153	16 B, J, D	NOW
HC/HCT154	24 B, J, D	
HC/HCT155	16 B, J, D	NOW
HC/HCT157	16 B, J, D	NOW
HC/HCT158	16 B, J, D	NOW
HC/HCT160	16 B, J, D	NOW
HC/HCT161	16 B, J, D	NOW
HC/HCT162	16 B, J, D	NOW
HC/HCT163	16 B, J, D	NOW
HC/HCT164	14 B, J, D	NOW
HC/HCT165	16 B, J, D	NOW
HC/HCT166	16 B, J, D	

Part No.	Package	Availability
HC/HCT173	16 B, J, D	NOW
HC/HCT174	16 B, J, D	NOW
HC/HCT175	16 B, J, D	NOW
HC/HCT190	16 B, J, D	
HC/HCT191	16 B, J, D	
HC/HCT192	16 B, J, D	
HC/HCT193	16 B, J, D	
HC/HCT194	16 B, J, D	
HC/HCT195	16 B, J, D	
HC/HCT221	16 B, J, D	
HC/HCT237	16 B, J, D	
HC/HCT238	16 B, J, D	
HC/HCT240	20 B, J, D	NOW
HC/HCT241	20 B, J, D	NOW
HC/HCT244	20 B, J, D	NOW
HC/HCT245	20 B, J, D	NOW
HC/HCT251	16 B, J, D	
HC/HCT253	16 B, J, D	
HC/HCT257	16 B, J, D	NOW
HC/HCT258	16 B, J, D	NOW
HC/HCT259	16 B, J, D	
HC/HCT273	20 B, J, D	NOW
HC/HCT280	14 B, J, D	
HC/HCT283	16 B, J, D	
HC/HCT298	16 B, J, D	
HC/HCT299	20 B, J, D	
HC/HCT322	20 B, J, D	
HC/HCT365	16 B, J, D	NOW
HC/HCT366	16 B, J, D	NOW
HC/HCT367	16 B, J, D	NOW
HC/HCT368	16 B, J, D	NOW
HC/HCT373	20 B, J, D	NOW
HC/HCT374	20 B, J, D	NOW
HC/HCT377	20 B, J, D	
HC/HCT386	14 B, J, D	
HC/HCT390	16 B, J, D	
HC/HCT393	14 B, J, D	NOW
HC/HCT423	16 B, J, D	
HC/HCT533	20 B, J, D	NOW
HC/HCT534	20 B, J, D	NOW
HC/HCT540	20 B, J, D	
HC/HCT541	20 B, J, D	
HC/HCT590	16 B, J, D	
HC/HCT610	40 B, J	
HC/HCT612	40 B, J	
HC/HCT620	20 B, J, D	
HC/HCT623	20 B, J, D	
HC/HCT640	20 B, J, D	
HC/HCT643	20 B, J, D	
HC/HCT645	20 B, J, D	
HC/HCT646	24 B, J, D	NOW
HC/HCT648	24 B, J, D	NOW
HC/HCT670	16 B, J, D	
HC/HCT688	20 B, J, D	

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☐ CMOS 4000B Series

Part No.	Package	Availability
GD4001B	14 B, J, D	NOW
GD4002B	14 B, J, D	NOW
GD4006B	14 B, J, D	NOW
GD4007UB	14 B, J, D	NOW
GD4008B	16 B, J, D	NOW
GD4011B	14 B, J, D	NOW
GD4012B	14 B, J, D	NOW
GD4013B	14 B, J, D	NOW
GD4014B	16 B, J, D	NOW
GD4015B	16 B, J, D	NOW
GD4016B	14 B, J, D	NOW
GD4017B	16 B, J, D	NOW
GD4018B	16 B, J, D	NOW
GD4019B	16 B, J, D	NOW
GD4020B	16 B, J, D	NOW
GD4021B	16 B, J, D	NOW
GD4022B	16 B, J, D	NOW
GD4023B	14 B, J, D	NOW
GD4024B	14 B, J, D	NOW
GD4025B	14 B, J, D	NOW
GD4027B	16 B, J, D	NOW
GD4028B	16 B, J, D	NOW
GD4029B	16 B, J, D	NOW
GD4030B	14 B, J, D	NOW
GD4034B	24 B, J, D	
GD4035B	16 B, J, D	NOW
GD4040B	16 B, J, D	NOW
GD4041B	14 B, J, D	NOW
GD4042B	16 B, J, D	NOW
GD4043B	16 B, J, D	NOW
GD4044B	16 B, J, D	NOW
GD4046B	16 B, J, D	
GD4047B	14 B, J, D	NOW
GD4049B	16 B, J, D	NOW
GD4050B	16 B, J, D	NOW
GD4051B	16 B, J, D	NOW
GD4052B	16 B, J, D	NOW
GD4053B	16 B, J, D	NOW
GD4066B	14 B, J, D	NOW
GD4067B	24 B, J, D	NOW
GD4068B	14 B, J, D	NOW
GD4069UB	14 B, J, D	NOW
GD4070B	14 B, J, D	NOW
GD4071B	14 B, J, D	NOW
GD4075B	14 B, J, D	
GD4076B	16 B, J, D	NOW
GD4077B	14 B, J, D	NOW
GD4078B	14 B, J, D	NOW
GD4081B	14 B, J, D	NOW
GD4085B	14 B, J, D	NOW
GD4086B	14 B, J, D	NOW
GD4093B	14 B, J, D	NOW
GD4104B	16 B, J, D	NOW
GD4510B	16 B, J, D	NOW
GD4511B	16 B, J, D	NOW

Part No.	Package	Availability
GD4512B	16 B, J, D	NOW
GD4514B	24 B, J, D	NOW
GD4516B	16 B, J, D	NOW
GD4518B	16 B, J, D	
GD4520B	16 B, J, D	NOW
GD4522B	16 B, J, D	NOW
GD4526B	16 B, J, D	NOW
GD4528B	16 B, J, D	NOW
GD4531B	16 B, J, D	NOW
GD4532B	16 B, J, D	NOW
GD4539B	16 B, J, D	NOW
GD4553B	16 B, J, D	
GD4555B	16 B, J, D	NOW
GD4556B	16 B, J, D	NOW
GD4582B	16 B, J, D	NOW
GD4702B	16 B, J, D	NOW
GD4703B	24 B, J, D	NOW
GD4704B	24 B, J, D	
GD4705B	24 B, J, D	
GD4706B	24 B, J, D	
GD4707B	24 B, J, D	
GD4708B	40 B, J, D	
GD4710B	18 B, J, D	NOW
GD4720B	16 B, J, D	NOW
GD4721B	22 B, J, D	
GD4723B	16 B, J, D	
GD4724B	16 B, J, D	NOW
GD4725B	16 B, J, D	NOW
GD4727B	14 B, J, D	
GD4731B	14 B, J, D	NOW
GD4735B	24 B, J, D	
GD4736B	16 B, J, D	
GD4737B	14 B, J, D	
GD40014B	14 B, J, D	NOW
GD40085B	16 B, J, D	NOW
GD40097B	16 B, J, D	NOW
GD40098B	16 B, J, D	NOW
GD40160B	16 B, J, D	
GD40161B	16 B, J, D	NOW
GD40163B	16 B, J, D	NOW
GD40174B	16 B, J, D	NOW
GD40175B	16 B, J, D	NOW
GD40192B	16 B, J, D	NOW
GD40193B	16 B, J, D	NOW
GD40194B	16 B, J, D	NOW

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.TV

PART NO	PKG	FUNCTION	FEATURES
* GL1130	7 SIP/HS	CTV Vertical Deflection Output Circuit	High Output, On Chip Pump-up Ckt and Low Power Dissipation, Minimum Number of External Parts Required, Max. Def. Out. : 1.5A
* GL1131	7 SIP/HS	CTV Vertical Deflection Output Circuit	High Output, On Chip Pump-up Ckt and Low Power Dissipation Minimum Number of External Parts Required, Max. Def. Out. : 1.5A
GL1150	20 DIP	Sync. Deflection Ckt for CRT Display	Horizontal Display Shift Right/Left, Good Linearity, Duty Setting
GL1151	20 DIP	Sync. Deflection Ckt for CRT Display	Horizontal Display Shift Right/Left, Good Linearity, Duty Setting, Vertical Pull-in range extended to 20Hz
GL3101A	16 DIP	PIF	Direct Coupled SAW-Filter, 920kHz & Cross-Color Reduced, Minimized Ext. Components
GL3120	30 SDIP	PIF + SIF	Peak IF AGC, High Gain VIF Amp, Video Detector B/W Noise Canceller, RF AGC,SIF Limiter, FM Detector, DC Attenuator
GL3201A	14 DIP	SIF Amp	IF Amp, Limiter, FM Detector, Electronic Attenuator, Zener Diode Regulated, High Stability, Low Harmonic Distortion
GL3202	22/24 DIP	Dual SIF Amp	IF Amp, Limiter, FM Detector, Electronic Attenuator, Zener Diode Regulated, High Stability, Low Harmonic Distortion
GL3301	28 DIP	Video, Chroma System	With Automatic Flesh Control
GL3320	30 SDIP	Video, Chroma, Def. Circuit	Small Sized Pkg, Minimum Number of Parts Required, Fewer Adjustment Required, Multi Function
GL3401	20/24 DIP	Deflection Signal Processor	On Chip Blanking Ckt, Horizontal OSC. Freq. Limitter, X-Ray Protection
GL3711	16 DIP	Tuner Controller	2-input 5-output Band Switch Meets CATV Tuner Requirements Small Saturation Voltage
* GL3810	14 DIP	A/V Switch	Video Crosstalk $\geq$ 60dB, Low Video Output Impedance(75Ω), Short-Ckt Protection of In/Outputs
GL3812	22 DIP	A/V Switch	Video/Stereo 4-input Switch Mute Function
GL3813	30 SDIP	Bilingual Signal Processor	Highly Resistant to Vibration/ Impact, Good Characteristics in Weak Electric Field
GL3814	30 SDIP	Korean Bilingual Decoder	Good Characteristics in Weak Electric Field, Good Stereo Separation & Crosstalk in Matrix, LED Drive
* GL3820	8 DIP	Video Switch	Video Crosstalk:50dB Typ., 1 Video Output 75Ω-1V_{PP} No Switched, 1 Switched Video Output 2V_{PP}, Short-Ckt Protection of In/Outputs

.VCR

PART NO	PKG	FUNCTION	FEATURES
* GL3130	20 DIP	PIF + SIF	VIF Amp, Video Detector, Peak IF AGC, B/W Noise Canceller, RF AGC, AFT, Video Mute, SIF Limiter, FM Detector
GL3615	18 DIP	Audio PB/REC	Low Power Consumption, Minimum Number of External Parts Required
GL3667	18 DIP	Fine Slow/Still Motion Control	File Slow, Fine Still, Frame Advance, Head Drum Noise Reduction
* GL3816	8 SIP	A/V Switch	Wide Input Dynamic Range, Good Freq. Characteristics, Low Distortion
* GL8121	9 SIP	Synchronous Signal Detector	Highly Stable V_{CC} & Temp., Highly Stable Signal Separation Ckt Resistant to Noise

* Under Development

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. AUDIO

PART NO	PKG	FUNCTION	FEATURES
GL5808	16 DIP	AM Tuner/FM IF System	FM IF Quad Detector, Operating Voltage 3 to 8V, Independant FM/AM Output Pin, Tuning Indicator
* GL5835	20 DIP	AM Tuner System	Auto Search Stop Signal, Double Balanced MIX, Local OSC Buffer Output, Wide Band AGC
* GL5643	9 SIP	PLL FM Stereo MPX	Excellent Channel Separation, VCO Stop Capability, Suitable for LED Driving
GL5501	14 DIP	Dual EQ Amp with ALC	Good ALC Channel Balance, Low Noise, Direct Motor Drive Obtained through SEPP Output
GL5529	20 DIP	Dual EQ Amp with ALC	Electronic Switching Type MIC and EQ Amp, Built-in Line Amp, Low Noise, Low Distortion
GL5560	8 SIP	Dual EQ Amp	Low Noise, Fewer External Parts
GL5561	8 SIP	Dual EQ Amp	Low Noise, Fewer External Parts, Built-in Voltage Regulator
* GL5526	16 DIP	5-Point Graphic EQ Amp	Operation Voltage 5 to 13V, Low Distortion, Low Noise
GL386	8 DIP	Low Voltage Power Amp	Battery Operation, Variable Voltage Gain 26 to 46dB, Ground Reference Input, Low Distortion
GL1223	9 SIP	5 Dot LED Level Meter	Built-in Rectifying Amp, Logarithmic Indicator, Constant LED Current(7mA Typ.)
GL3230	16 DIP	Dual Volume Balance Tone Control	Wide Volume Control Range, Excellent Cross Talk, Suitable for Temperature Drift, Wide Tone Control Range
GL3630	42 SDIP	CDP Servo Control	Focus Preamp, Tracking Preamp, Disc Drive Amp, HF Edge Detection

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. REMOTE CONTROL

PART NO	PKG	FUNCTION	FEATURES
GM3043	20 SOP	CMOS Remote Control Transmitter	Low Voltage Operation, Low Power Consumption, 32 Function Key, 256 Custom Code, 16Bit Pulse Code
GM3044	20 SOP	CMOS Remote Control Transmitter	Low Voltage Operation, Low Power Consumption, 32 Function Key, Custom Code is Included, 16Bit Pulse Code
GMC4055	28 SOP/DIP	4Bit Microcomputer for Remote Control	CMOS LSI 4Bits Parallel Processing, On Chip Prescaler, Clock Frequency 400 to 500kHz, 10x10 Key Matrix
GL3274	8 SOP/SIP	Remote Control Preamp	Low Power Consumption, Limiter Amp, Direct Connection to a Photo Diode, Open Collector Output

* Under Development

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. TELECOMMUNICATION

PART NO	PKG	FUNCTION	FEATURES
* GL6840	8 DIP	Electronic Two Tone Ringer	Low Current Consumption, Built-in Bridge Zener Diodes, Tone and Switching Frequency Adjustable by External Components
GL6901	16 DIP	Speech Network	Mask Programmable Speech circuit, Low voltage Operation, High Output Swing On Long Lines, Very Short Start-up Time
* GL6981	18 DIP/FIN	Speech Network	Low Voltage Operation Down to 1.3V, Balanced REC Output, AC Voltage Swing Down to 0.4V
GL6801	16 DIP	DTMF Generator	Wide Operating Line Voltage and Current Range, Short Start-up Time, Internal Protection of All Inputs
GM6380	16 DIP	Tone Dialer	Minimum External Parts Count Improved Loop Compensations, Multiple Key Entry, Pin-Selectable to either Single Tone or No Tone
GM6375	18 DIP	10 Number Repertory Tone/Pulse Dialer	LND Privacy, Pacifier Tone and PABX Pause, Stores Ten-16 Digit Numbers, Variable Dialing Rate
* GM6388	22 DIP	15 Number Repertory Tone/Pulse Dialer	Store Ten-16 Digit Number for Emergency Calling and LDC, One-31 Digits for Last Number Redial Memory
* GM6486	40 DIP	Key Phone LED Driver	33 Outputs 15mA Sink Capability, TTL Compatibility, Wide Supply Voltage 4.75 to 13.2V
* GM3054A	16 CERDIP	Serial CODEC/Filter	Complete CODEC and Filtering μ-Law, Exceeds All D3/D4 CCITT Specifications, Automatic Power Down
* GM3057	16 CERDIP	Serial CODEC/Filter	Complete CODEC and Filtering A-Law, Exceeds All D3/D4 CCITT Specifications, Automatic Power Down
GM6155	20 DIP	Time Slot Assignment Circuit	Controls 4 CODEC/Filters, 4.096MHz Max. Clock Rate, 8 Channel Unidirectional Mode.
GM16C450	40 DIP	Asynchronous Communication Element	Easily Interfaces to Most Popular Microprocessors, Independant Receiver Clock Input, False Start Bit Detection
GM82C50	40 DIP	Asynchronous Communication Element	Easily Interfaces to Most Popular Microprocessors, Independant Receiver Clock Input, False Start Bit Detection
GM62093	40 DIP	Multiplexer	12x8 Cross Point Switch with Control Memory, Latch Control, Low On Resistance

. MOTOR DRIVER

PART NO	PKG	FUNCTION	FEATURES
GL7401	10 SIP/HS	Single Bidirectional Motor Driver	Built-in Braking Function, Direct Drivable with TTL, Built-in Diode to Absorb Dash Current
GL7445	10 SIP/HS	Single Bidirectional Motor Driver	Built-in Braking Function, Input Connectable Direct to MOS LSI, Output Voltage Variable by Use of External Zener Diode
GL7438	10 SIP/HS	Dual Bidirectional Motor Driver	Logic Control, Power Driver, Thermal Shutdown

. TIMER

PART NO	PKG	FUNCTION	FEATURES
GLC555	8 DIP	CMOS General Purpose Single Timer	Single CMOS Version Industrial Standard 555 Timer, 2~18V Power Supply, 500kHz
GLC556	14 DIP	CMOS General Purpose Dual Timer	Dual CMOS Version Industrial Standard 556 Timer, 2~18V Power Supply, 500kHz
GL555	8 DIP	Bipolar General Purpose Single Timer	Operate in both Astable and Monostable Modes, Output can Source and Sink 200mA, 4.5~18V Power Supply

* Under Development

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. A/D CONVERTER

PART NO	PKG	FUNCTION	FEATURES
* GM7136	40 DIP	$3^1/_2$ Digit LCD A/D Converter	Low Power (1mW), 7 Segment Decoder, Display Driver, Reference and Clock True Polarity at Zero for Precise Null Detection
* GM0832	8 DIP	8 Bit Serial I/O A/D Converter	TTL/MOS Input/Output Compatible, Remote Operation Serial Digital Data Link, No Zero or Full Scale Adjust Required

. OPERATIONAL AMPLIFIER & COMPARATOR

PART NO	PKG	FUNCTION	V_{IO}max (mV)	$I_B$max (mA)	Band Width (MHz)	Offset Adjustment	Max Supply Voltage
GL358/A	8 DIP	General Dual Type(internal compensation type)	7/3	250	0.8	No	±18 or 36
GL324/A	14 DIP	General Quad Type(internal compensation type)	7/3	250	0.8	No	±18 or 36
GL4558	8 DIP	Low Noise Dual(internal compensation type)	6	500	3	No	±18
* GL4559	14 DIP	Low Noise Quad(internal compensation type)	6	500	3	No	±18
GL348	14 DIP	General Quad Type(internal compensation type)	6	200	1	Yes	±18
GLC9458	8 DIP	CMOS Dual Type(internal compensation type)	5	50pA	0.48	No	±18
* GLC9459	14 DIP	CMOS Quad Type(internal compensation type)	5	50pA	0.48	No	±18
GL393/A	8 DIP	Dual Voltage Comparator(open collector)	5/2	250	-	No	±18 or 36
GL339/A	14 DIP	Quad Voltage Comparator(open collector)	5/2	250	-	No	±18 or 36

. VOLTAGE REGULATOR

GL78XX Series (Positive)

PART NO	PKG	Typical Input Voltage	Output at I_O=500mA	Ripple Rejection at I_O=500mA f=120Hz	
		V_{IN}(V)	V_{OUT}(V)	Typ(dB)	Min(dB)
GL7805	TO-220	10	5	80	62
GL7806		11	6	80	59
GL7808		14	8	80	56
GL7809		15	9	80	56
GL7812		19	12	80	55
GL7815		23	15	70	54
GL7818		27	18	70	52
GL7824		33	24	70	50

GL79XX Series (Negative)

PART NO	PKG	Typical Input Voltage	Output at I_O=500mA	Ripple Rejection at I_O=500mA f=120Hz	
		V_{IN}(V)	V_{OUT}(V)	Typ(dB)	Min(dB)
GL7905	TO-220	-10	-5	60	54
GL7909		-15	-8	60	54
GL7912		-19	-12	60	54
GL7915		-23	-15	60	54
GL7924		-33	-24	58	54

. MISCELLANEOUS ICs

PART NO	PKG	FUNCTION	FEATURES
GL8901/S	9 SIP/HS	SMPS Controller	Low Start-up Current, Direct Control of Switching Transistor, Collector Current Proportional to Base Current Input
GL494	16 DIP	PWM Control Circuit	Switch Mode Pulse Width Modulation Control, Adjustable Dead Time Control, Easy Synchronization
GL317	TO-220	Positive Adjustable Regulator	Guaranted Output Current Capabilbity of 1.5A, Ripple Rejection 80dB Typ.
* GL574	TO- 92	33V Voltage Stabilizer	Low Temperature Coefficient, Low Dynamic Resistance
GL7101	8 DIP	Earth Leakage Current Detector	Low Power Consumption, Few External Parts, Built-in Voltage Regulator, High Gain Differential Amp
GM6845S	40 DIP	CRT Controller	3.7MHz High Speed Display Operation, TTL Compatible, On Screen, Line Bufferless Refreshing, Single 5V Power Supply

* Under Development

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MILITARY PRODUCT REFERENCE GUIDE

Harris Semiconductor has long been a major supporter of the military market. The knowledge and expertise gained from this association is manifested in our latest military efforts: Military Drawing and 883-compliant products. This Military Product Guide gives you a complete overview of our commitment to military support. For more information on these products, please contact Harris Semiconductor or your nearest Harris sales office or representative.

Radiation Hardened Products

Part Number	JAN Part Number	DESC Drawing Number	883 Part Number
HS-6504RH	24503SVC	—	HS-6504RH/883
HS-6514RH	24504SVC	—	HS-6504RH/883
HS-65C262RH	29107SJB	—	HS-65C262RH/883
HS-65T262RH	29108SJB	—	HS-65T262RH/883
HS-508ARH	—	5962R8753701EX	HS-508ARH/883
HS-1840RH	—	5962R8753801XX	HS-1840RH/883

Microprocessor Products

Part Number	JAN Part Number	Military Drawing Number	883 Part Number
MD80C86	—	8405201QA	MD80C86/883
MR80C86	—	84052012C	—
MD80C88	—	—	*MD80C88/883
MR80C88	—	—	*MR80C88/883
MD82C37A	—	*IN DEVELOPMENT	*MD82C37A/883
MR82C37A	—	*IN DEVELOPMENT	—
MD82C50A-5	—	—	*MD82C50A-5/883
MR82C50A-5	—	—	*MR82C50A-5/883
MD82C52	—	8501501XA	MD82C52/883
MR82C52	—	85015013C	—
MD82C54	—	8406501JA	*MD82C54/883
MR82C54	—	84065013C	—
MD82C55A-5	—	8406601QA	—
MR82C55A-5	—	8406601XC	—
MD82C55A	—	8406602QA	*MD82C55A/883
MR82C55A	—	8406602XC	—
MD82C59A-5	—	8501601YA	—
MR82C59A-5	—	85016013C	—
MD82C59A	—	8501602YA	*MD82C59A/883
MR82C59A	—	85016023C	—
MD82C82	—	8406701RA	*MD82C82/883
MR82C82	—	84067012C	—
MD82C83H	—	8406702RA	*MD82C83H/883
MR82C83H	—	84067022C	—
MD82C84A	—	8406801VA	*MD82C84A/883
MR82C84A	—	84068012C	—
MD82C85	—	*IN DEVELOPMENT	*MD82C85/883
MR82C85	—	*IN DEVELOPMENT	—
MD82C86H-5	—	8757701RA	*MD82C86H/883
MR82C86H-5	—	87577012C	—
MD82C87H-5	—	8757702RA	*MD82C87H/883
MR82C87H-5	—	87577022C	—
MD82C88	—	8406901RA	*MD82C88/883
MR82C88	—	84069012C	—
MD82C89	—	8552801RA	*MD82C89/883
MR82C89	—	85528012C	—

*Scheduled for Q1 CY89

MILITARY PRODUCT REFERENCE GUIDE

Microprocessor Products (continued)

Part Number	JAN Part Number	Military Drawing Number	883 Part Number
HD1-4702	—	—	HD1-4702/883
HD1-6402	—	—	HD1-6402/883
HD1-15530	—	7802991JA	HD1-15530/883**
HD4-15530	—	78029913C	—
HD1-15531	—	—	HD1-15531/883*

* Scheduled for Q1 CY89
** Scheduled for Q4 CY88

Data Acquisition Products

Part Number	JAN Part Number	Military Drawing Number	883 Part Number
HA-2420	—	8001601CA	HA-2420/883
HI-506	38510/190-01BXC	—	HI-0506/883
HI-506A	38510/190-02BXC	8513101XA	See HI-546/883
HI-507	38510/190-03BXC	—	HI-0507/883
HI-507A	38510/190-04BXC	8513102XA	See HI-547/883
HI-508	38510/190-07BEC	7705201EC	HI-0508/883
HI-508A	38510/190-05BEC	7705202EA	See HI-548/883
HI-509	38510/190-08BEC	—	HI-0509/883
HI-509A	38510/190-06BEC	85131-03	See HI-549/883
HI-516	—	—	HI-0516/883
HI-518	—	—	HI-0518/883
HI-524	—	—	HI-0524/883
HI-546	—	8513101XA	HI-0546/883
HI-547	—	8513102XA	HI-0547/883
HI-548	—	7705202EA	HI-0548/883
HI-549	—	8513103EA	HI-0549/883
HI-562A	—	—	HI-0562A/883
HI-1818A	—	—	HI-1818/883
HI-1828A	—	—	HI-1828A/883
HA-2420	—	—	HA-2420/883
HI-5320	—	—	—
HI-5330	—	—	HI-5330/883
HI-562A	—	—	HI-562A/883
HI-5687	—	83003-02	HI-5687/883
HI-5697	—	—	HI-5697/883
HI-574ASD	—	—	HI-574ASD/883
HI-574ATD	—	85127-04	HI-574ATD/883
HI-674ASD	—	—	HI-674ATD/883
HI-674ATD	—	85127-06	HI-674ATD/883
HI-565A	—	—	HI-565A/883
HI-774SD	—	—	HI-774SD/883
HI-774TD	—	—	HI-774TD/883

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CMOS Memory Products			
Part Number	**JAN Part Number**	**DESC Drawing Number**	**883 Part Number**
1K CMOS Static RAMs			
HM1-6508	—	—	HM1-6508/883
HM1-6508B	—	—	HM1-6508B/883
HM1-6518	—	—	HM1-6518/883
HM1-6518B	—	—	HM1-6518B/883
HM1-6551	—	—	HM1-6551/883
HM1-6551B	—	—	HM1-6551B/883
HM1-6561	—	—	HM1-6561/883
HM1-6561B	—	—	HM1-6561B/883
4K CMOS Static RAMs			
HM1-6504	—	8102405VA	HM1-6504/883
HM1-6504B	—	8102403VA	HM1-6504B/883
HM1-6504S	24501BVX	8102401VA*	HM1-6504S/883
HM1-6514	—	8102406VA	HM1-6514/883
HM1-6514B	—	8102404VA	HM1-6514B/883
HM1-6514S	24502BVX	8102402VA*	HM1-6514S/883
HM4-6514	—	—	HM4-6514/883
HM4-6514B	—	—	HM4-6514B/883
HM1-6514S	—	—	HM4-6514S/883
16K CMOS Synchronous Static RAMs			
HM1-6516	29102BJX	8403601JA	HM1-6516/883
HM1-6516B	—	8403607JA	HM1-6516B/883
HM4-6516	—	8403601ZC	HM4-6516/883
16K CMOS Asynchronous Static RAMs			
HM1-65162	29104BJX	8403602JA	HM1-65162/883
HM1-65162B	—	8403606JA	HM1-65162B/883
HM1-65162C	—	8403603JA	HM1-65162C/883
HM1-65162S	—	—	—
HM4-65162	—	8403602XC	HM4-65162/883
HM4-65162B	—	8403606XC	HM4-65162B/883
HM4-65162C	—	8403603XC	HM4-65162C/883
HM1-65262	29103BJX	8413201RA	HM1-65262/883
HM1-65262B	—	8413203RA	HM1-65262B/883
HM4-65262	—	8413201YC	HM4-65262/883
HM4-65262B	—	8413203YC	HM4-65262B/883
64K CMOS Static RAMs			
HM1-65642	29201BJX	8552503YA	HM1-65642/883
HM4-65642	—	8552503XC	HM4-65642/883
HM1-65642B	—	—	HM1-65642B/883

*Obsolete - may still be purchased for contracts prior to 10/22/85.

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CMOS Memory Products (continued)			
Part Number	**JAN Part Number**	**DESC Drawing Number**	**883 Part Number**
CMOS Static RAM Modules HM5-6564 HM5-8808 HM5-8808B HM5-8808S HM5-8808A HM5-8808AB HM5-8808AS HM5-8816H HM5-8832B HM5-91M2 HM5-92560 HM5-92570	Harris CMOS static RAM modules are available for military and high-reliability applications processed to our high-rel DASH 8 program flow. This includes burn-in and value-added processing (temperature cycling, SEM inspection, etc.). Please contact your local Harris sales office or representative for details.		
CMOS Fuse Link PROMs			
HM1-6642	—	—	HM1-6642/883
HM4-6642	—	—	HM4-6642/883
HM6-6642	—	—	HM6-6642/883
HM1-6617	—	—	HM1-6617/883
HM4-6617	—	—	HM4-6617/883
HM6-6617	—	—	HM6-6617/883

Linear Products			
Part Number	**JAN Part Number**	**DESC Drawing Number**	**883 Part Number**
HA240X	—	—	HA1-2400/883
	—	—	HA4-2400/883
HA2500	12204BGC	—	HA2-2500/883
	—	—	HA7-2500/883
HA2502	—	—	HA2-2502/883
	—	—	HA4-2502/883
	—	—	HA7-2502/883
HA2510	12205BGC	—	HA2-2510/883
	—	—	HA7-2510/883
HA2512	—	—	HA2-2512/883
	—	—	HA4-2512/883
	—	—	HA7-2512/883
HA2520	12206BGC	—	HA2-2520/883
	—	—	HA7-2520/883
HA2522	—	—	HA2-2522/883
	—	—	HA4-2522/883
	—	—	HA7-2522/883
HA2529	—	—	HA2-2529/883
	—	—	HA4-2529/883
	—	—	HA7-2529/883

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Linear Products (continued)

Part Number	JAN Part Number	DESC Drawing Number	883 Part Number
HA2539	—	—	HA1-2539/883
	—	—	HA4-2539/883
HA2540	—	—	HA1-2540/883
	—	—	HA4-2540/883
HA2541	—	—	HA2-2541/883
	—	—	HA1-2541/883
HA2542	—	—	HA2-2542/883
HA2544	—	—	HA2-2544/883
	—	—	HA4-2544/883
	—	—	HA7-2544/883
HA2600	12202BGC	—	HA2-2600/883
	—	—	HA7-2600/883
HA2602	—	—	HA2-2602/883
	—	—	HA4-2602/883
	—	—	HA7-2602/883
HA2620	12203BGC	—	HA2-2620/883
	—	—	HA7-2620/883
HA2622	—	—	HA2-2622/883
	—	—	HA4-2622/883
	—	—	HA7-2622/883
HA2640	—	7800302GC	HA2-2640/883
	—	—	HA4-2640/883
	—	—	HA7-2640/883
HA4741	—	—	HA1-4741/883
	—	—	HA4-4741/883
HA4900	—	—	—
HA4902	—	—	HA1-4902/883
	—	—	HA4-4902/883
HA5002	—	—	HA2-5002/883
	—	—	HA4-5002/883
	—	—	HA7-5002/883
HA5033	—	—	HA2-5033/883
HA5101	—	—	HA2-5101/883
	—	—	HA4-5101/883
	—	—	HA7-5101/883
HA5102	—	—	HA2-5102/883
	—	—	HA4-5102/883
	—	—	HA7-5102/883
HA5104	—	—	HA1-5104/883
	—	—	HA4-5104/883
HA5111	—	—	HA2-5111/883
	—	—	HA4-5111/883
	—	—	HA7-5111/883
HA5112	—	—	HA2-5112/883
	—	—	HA4-5112/883
	—	—	HA7-5112/883

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Harris Semiconductor

MILITARY PRODUCT REFERENCE GUIDE

Linear Products (continued)

Part Number	JAN Part Number	DESC Drawing Number	883 Part Number
HA5114	—	—	HA1-5114/883
	—	—	HA4-5114/883
HA5127	—	—	HA2-5127/883
	—	—	HA4-5127/883
	—	—	HA7-5127/883
HA5134	—	—	HA1-5134/883
	—	—	HA4-5134/883
HA5135	—	—	HA2-5135/883
	—	—	HA4-5135/883
	—	—	HA7-5135/883
HA5137	—	—	HA2-5137/883
	—	—	HA4-5137/883
	—	—	HA7-5137/883
HA5141	—	—	HA2-5141/883
	—	—	HA4-5141/883
	—	—	HA7-5141/883
HA5142	—	—	HA2-5142/883
	—	—	HA4-5142/883
	—	—	HA7-5142/883
HA5144	—	—	HA1-5144/883
	—	—	HA4-5144/883
HA5147	—	—	HA2-5147/883
	—	—	HA4-5147/883
	—	—	HA7-5147/883
HA5151	—	—	HA2-5151/883
	—	—	HA4-5151/883
	—	—	HA7-5151/883
HA5152	—	—	HA2-5152/883
	—	—	HA4-5152/883
	—	—	HA7-5152/883
HA5154	—	—	HA1-5154/883
	—	—	HA4-5154/883
HA5177	—	—	HA2-5177/883
	—	—	HA4-5177/883
	—	—	HA7-5177/883
HA5190	—	—	HA1-5190/883
HA5190	—	—	HA2-5190/883
	—	—	HA4-5190/883
HI200	—	—	HI1-200/883
	—	—	HI2-200/883
HI201	12302BEA	—	HI1-201/883
	12302BEC	—	—
	—	—	HI4-201/883
HI201HS	—	8671601EA	HI1-201HS/883
	—	86716012A	HI-201HS/883
HI222	—	—	HI1-222/883
	—	—	HI4-222/883

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Linear Products (continued)

Part Number	JAN Part Number	DESC Drawing Number	883 Part Number
HI300	—	86716012C	HI2-300/883
	—	—	HI1-300/883
HI301	—	—	HI2-301/883
	—	—	HI1-301/883
HI302	—	—	HI1-302/883
HI303	—	—	HI1-303/883
HI304	—	—	HI1-304/883
	—	—	HI2-304/883
HI305	—	—	HI1-305/883
	—	—	HI2-305/883
HI306	—	—	HI1-306/883
HI307	—	—	HI1-307/883
HI381	—	—	HI1-381/883
	—	—	HI2-381/883
HI384	—	—	HI1-384/883
HI387	—	—	HI1-387/883
	—	—	HI2-387/883
HI390	—	—	HI1-390/883
HI5040	—	8100609EX	HI1-5040/883
HI5041	—	8100610EX	HI1-5041/883
HI5042	—	8100611EX	HI1-5042/883
HI5043	—	8100612EX	HI1-5043/883
	—	81006122A	HI4-5043/883
HI5044	—	8100613EX	HI1-5044/883
HI5045	—	8100614EX	HI1-5045/883
	—	81006142A	HI4-5045/883
HI5046	—	8100615EA	HI1-5046/883
HI5046A	—	8100621EA	HI1-5046A/883
HI5047	—	8100616EA	HI1-5047/883
HI5047A	—	8100622EA	HI1-5047A/883
HI5048	—	8100617EA	HI1-5048/883
HI5049	—	8100620EA	HI1-5049/883
	—	81006202A	HI4-5049/883
HI5050	—	8100618EA	HI1-5050/883
HI5051	—	8100619EA	HI1-5051/883
	—	81006192A	HI4-5051/883

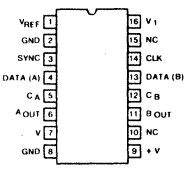
For other Harris Semiconductor products see pages 2637-2688

SPECIALIZED PRODUCTS

ARINC 429 Bus Interface Line Driver Circuit HS-3182

Features

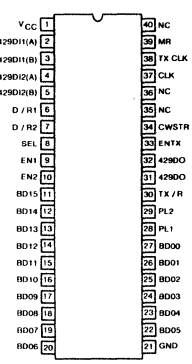
- Inputs TTL and CMOS compatible
- Adjustable rise and fall times via two external capacitors
- Programmable output differential range via voltage reference input (V_{REF})
- Outputs are inhibited (0 V) if data (A) and data (B) inputs are both in the "logic one" state
- Can operate up to a 100-Kbit data rate
- Output short circuit proof and contains overvoltage protection
- Data "A" and Data "B" signals are "AND'D" with clock and sync signals
- Full military temperature range



ARINC 429 Bus Interface Circuit HS-3282

Features

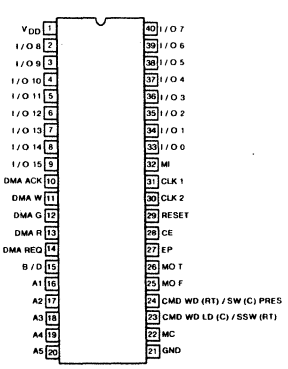
- ARINC specification 429 compatible
- Data rates of 100 Kbits or 12.5 Kbits
- Separate receiver and transmitter section
- Dual and independent receivers, connecting directly to ARINC bus
- Serial to parallel receiver data conversion
- Parallel to serial transmitter data conversion
- Word lengths of 25 or 32 bits
- Parity status of received data
- Generate parity of transmitter data
- Automatic word gap timer
- Single 5 V supply
- Low power dissipation
- Full military temperature range



MIL-STD-1553B Bus Interface Circuit HS-3273

Features

- MIL-STD-1553C compatible
- Up to 5 MHz data rate for non-MIL-STD-1553C applications
- Parallel to serial transmitter data conversion
- 8/16 bits host I/O interface
- Error interception and recognition
- DMA capability
- Single 5 V power supply
- Full military temperature range



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RAD-HARD
CMOS MICROPROCESSOR PRODUCTS

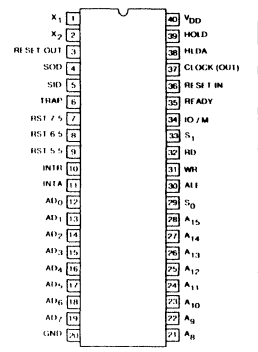
8-Bit Microprocessor
HS-80C85RH

Features

- Specifically designed for radiation hardness
- Low standby power: 2.7 mW max.
- Low operating power: 26 mW/MHz max.
- Multiplexed address/data bus
- 5 Volt operation
- Software and pin compatibility with Intel 8085
- Equivalent to Sandia SA3000
- Full military temperature range

Radiation Effects

- Each lot screened for total dose hardness
- Parametrics guaranteed to 1 x 10^5 RADs (Si)
- Latch-up free > 10^{12} RADs (Si)/sec
- Upset: > 10^8 RADs (Si)/sec



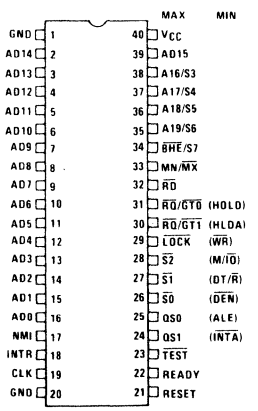
16-Bit Microprocessor
HS-80C86RH

Features

- Specifically designed for radiation hardness
- Pin compatible with Harris 80C86
- Completely static design
  - ▶DC to 5 MHz
- Low-power operation
  - ▶ICCSB = 500 μA maximum
  - ▶ICCOP = 12 mA/MHz max.
- 1 Mbyte of direct memory addressing capability
- 24 operand addressing modes
- Bit, byte, word, and block move operations
- 8 and 16-bit signed/unsigned arithmetic
  - ▶Binary or decimal
  - ▶Multiply and divide
- Single 5V power supply
- Military temperature range

Radiation Effects

- Each lot screened for total dose hardness
- Parametrics guaranteed to 1 x 10^5 RADs (Si)
- Latch-up free
- Upset: > 10^8 RADs (Si)/sec

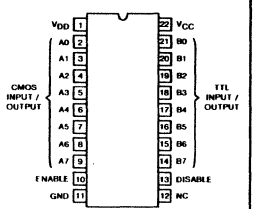


For other Harris Semiconductor products see pages 2637-2688

RAD-HARD
CMOS MICROPROCESSOR PRODUCTS

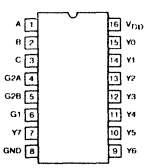
8-Bit Bidirectional CMOS/TTL Level Converter
HS-3374RH

Features	Radiation Effects
• Specifically designed for radiation hardness • Static operation for low power consumption • Non-inverting outputs • Low propagation delay • Full military temperature range • Equivalent to Sandia SA2996	• Each lot screened for total dose hardness • Parametrics guaranteed to 1 x 10^5 RADs (Si) • Latch-up free > 10^{12} RADs (Si)/sec • Upset: > 10^8 RADs (Si)/sec



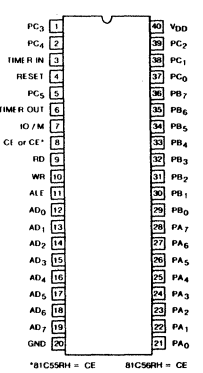
3-Line to 8-Line Decoder/Demultiplexer
HS-54C138RH

Features	Radiation Effects
• Specifically designed for radiation hardness • Static operation for low power consumption • High noise immunity • Active low outputs • 5 Volt operation • Full military temperature range • Equivalent to Sandia SA2995	• Each lot screened for total dose hardness • Parametrics guaranteed to 1 x 10^5 RADs (Si) • Latch-up free > 10^{12} RADs (Si)/sec • Upset: > 10^8 RADs (Si)/sec



2K (256x8) RAM with I/O and Timer
HS-81C55RH, HS-81C56RH

Features	Radiation Effects
• Specifically designed for radiation hardness • Static operation for low power consumption • Pin compatible with Intel 8155/56 • Equivalent to Sandia SA3001 • 5 Volt operation • 3 programmable I/O ports • 14-Bit programmable timer • Multiplexed address and data bus • Full military temperature range	• Each lot screened for total dose hardness • Parametrics guaranteed to 1 x 10^5 RADs (Si) • Latch-up free > 10^{12} RADs (Si)/sec • Upset: > 10^8 RADs (Si)/sec



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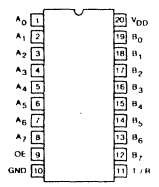
RAD-HARD
CMOS MICROPROCESSOR PRODUCTS

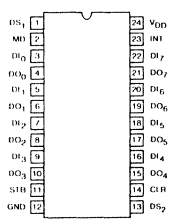
8-Bit Bus Transceiver
HS-82C08RH

Features	Radiation Effects
• Specifically designed for radiation hardness • Static operation for low power consumption • Bidirectional three-state input/outputs • Low propagation delay • 5 Volt operation • Full military temperature range • Equivalent to Sandia SA2997	• Each lot screened for total dose hardness • Parametrics guaranteed to 1 x 10^5 RADs (Si) • Latch-up free > 10^{12} RADs (Si)/sec • Upset: > 10^8 RADs (Si)/sec • Increased tolerance to cosmic radiation



8-Bit Input/Output Port
HS-82C12RH

Features	Radiation Effects
• Specifically designed for radiation hardness • Static operation for low power consumption • Asynchronous register clear • 8-bit data register and buffer • Service request flip-flop • Three-state outputs • Full military temperature range • Equivalent to Sandia SA3026	• Each lot screened for total dose hardness • Parametrics guaranteed to 1 x 10^5 RADs (Si) • Latch-up free > 10^{12} RADs (Si)/sec • Upset: > 10^8 RADs (Si)/sec



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RAD-HARD
CMOS MICROPROCESSOR PRODUCTS

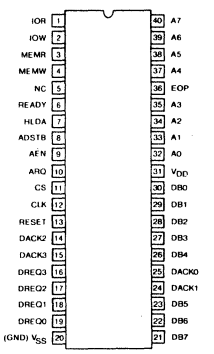
Programmable DMA Controller
HS-82C37ARH

Features

- Specifically designed for radiation hardness
- Pin compatible with Harris 82C37A
- High-speed data transfers up to 2.5 MBPS with 5 MHz clock
- Four independent maskable channels with autoinitialization capability
- Expandable to any number of channels
- Memory-to-memory transfer capability
- Software-accessible internal registers
- Single 5V power supply
- Low power consumption
  >IDDOP = 20 mA/MHz maximum
  >IDDSB = 20 μA maximum
- Full military temperature range

Radiation Effects

- Each lot screened for total dose hardness
- Parametrics guaranteed to 1 x 10^5 RADs (Si)
- Latch-up free
- Upset: > 10^8 RADs (Si)/sec
- Functional after 1 x 10^6 RADs (Si) total dose



Serial Controller Interface
HS-82C52RH

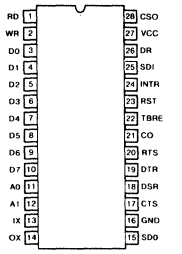
COMING SOON

Features

- Specifically designed for radiation hardness
- Pin compatible with Harris 82C52
- Uses either parallel mode crystal circuit or external frequency source
- DC to 16 MHz operation (DC to 1M Baud rate)
- Microprocessor bus oriented interface
- Modem interface
- Line break generation and detection
- Loopback and echo modes
- Interrupt mode with mask capability
- TTL/CMOS compatible inputs/outputs
- Single 5V supply
- Low power consumption: 1 mA/MHz typical
- Full military temperature range

Radiation Effects

- Each lot screened for total dose hardness
- Parametrics guaranteed to 1 x 10^5 RADs (Si)
- Latch-up free
- Upset: > 10^8 RADs (Si)/sec
- Total dose capabilities above look RADs available; contact factory for details



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RAD-HARD
CMOS MICROPROCESSOR PRODUCTS

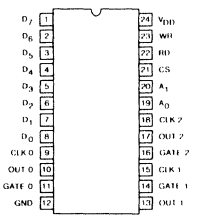
Programmable Interval Timer
HS-82C54RH

Features

- Specifically designed for radiation hardness
- Pin compatible with Harris 82C54A and NMOS 8254A
- High speed, no "wait state" operation with 5MHz HS-80C86RH
- Three independent 16 bit counters
- Six programmable counter modes
- Binary or BCD counting
- Status read back command
- Fully TTL compatible
- Single 5V power supply
- Low power consumption
  >IDDSB = 20 μA
  >IDDOP = 10 mA/MHz
- Full military temperature range

Radiation Effects

- Each lot screened for total dose hardness
- Parametrics guaranteed to 1 x 10^5 RADs (Si)
- Latch-up free
- Upset: > 10^8 RADs (Si)/sec
- Functional after 1 x 10^6 RADs (Si) total dose



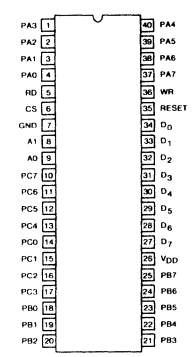
Programmable Peripheral Interface
HS-82C55ARH

Features

- Specifically designed for radiation hardness
- Pin compatible with Harris 82C55A and NMOS 8255A
- High speed, no "wait state" operation with 5 MHz HS-80C86 RH
- Fully TTL compatible
- 24 programmable I/O pins
- Direct bit set/reset capability
- Enhanced control word read capability
- Single 5V power supply
- 2.0 mA drive capability on all I/O port outputs
- Low standby power
  >ICCSB = 10 μA
- Full military temperature range

Radiation Effects

- Each lot screened for total dose hardness
- Parametrics guaranteed to 1 x 10^5 RADs (Si)
- Latch-up free
- Upset: > 10^8 RADs (Si)/sec
- Functional after 1 x 10^6 RADs (Si) total dose



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RAD-HARD
CMOS MICROPROCESSOR PRODUCTS

Programmable Interrupt Controller
HS-82C59ARH

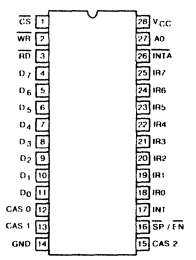
COMING SOON

Features

- Specifically designed for radiation hardness
- Pin compatible with Harris 82C59A and NMOS 8259A
- High speed, no "wait state" operation with 5 MHz HS-80C86RH
- Eight level priority controller
- Expandable to 64 priority levels
- Fully TTL compatible
- Programmable interrupt modes
- HS-80C85RH and HS-80C86RH compatible operation
- Individual request mask capability
- Fully static design
- Single 5V power supply
- Low standby power 20 μA
- Full military temperature range

Radiation Effects

- Each lot screened for total dose hardness
- Parametrics guaranteed to 1 x 10^5 RADs (Si)
- Latch-up free
- Upset: > 10^8 RADs (Si)/sec



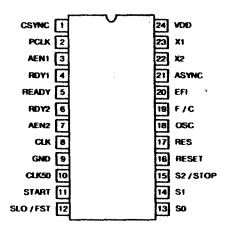
Static Clock Controller/Generator
HS-82C85RH

Features

- Specifically designed for radiation hardness
- Pin compatible with Harris 82C85
- Generates system clocks for microprocessors and peripherals
- Complete control over system clock operation for very low system power
  - ▶Stop-oscillator
  - ▶Stop-clock
  - ▶Low-frequency (slo) mode
  - ▶Full-speed operation
- DC to 15 MHz operation (DC to 5 MHz system clock)
- Uses either parallel mode crystal circuit or external frequency source
- TTL/CMOS compatible inputs/outputs
- Single 5V power supply
- Very low power consumption
- Full military temperature range

Radiation Effects

- Each lot screened for total dose hardness
- Parametrics guaranteed to 1 x 10^5 RADs (Si)
- Latch-up free
- Upset: > 10^8 RADs (Si)/sec
- Functional after 1 x 10^6 RADs



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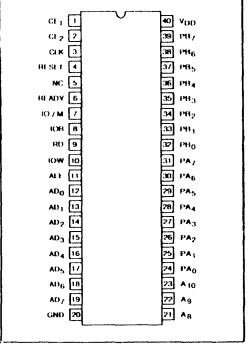
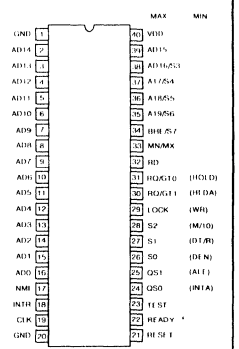
RAD-HARD CMOS MICROPROCESSOR PRODUCTS

16K (2Kx8) ROM with I/O Ports HS-83C55RH

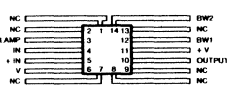
Features	Radiation Effects	
• Specifically designed for radiation hardness • Static operation for low power consumption • Pin compatible with Intel 8355 • Equivalent to Sandia SA3002 • 5 Volt operation • 2 programmable I/O ports • Multiplexed address and data bus • Full military temperature range	• Each lot screened for total dose hardness • Parametrics guaranteed to 1 x 10^5 RADs (Si) • Latch-up free > 10^{12} RADs (Si)/sec • Upset: >10^8 RADs (Si)/sec	

Radiation Hardened CMOS 16 Bit Microprocessor HS-80C86RRH

Features		
• Pin compatible with NMOS 8086 and Harris 80C86 • Radiation hardened (guaranteed) > Latch up free Epi-CMOS > Total dose > 100K Rad(Si) > Transient upset > 10^8 Rad(Si)/sec > Single event upset hardened • Completely static design > DC to 5MHz • Low power operation > ICCSB = 500μA maximum > ICCOP = 12 mA/MHz typical • 1 Mbyte of direct memory addressing capability	• 24 Operand Addressing Modes • Bit, byte, word, and block move operations • 8 and 16 bit signed/unsigned arithmetic > Binary or decimal > Multiply and divide • Bus-hold circuitry eliminates pull-up resistors for CMOS Interfacing • Hardened field, self aligned, Junction Isolated CMOS Process Single 5V power supply • Military temperature range	

RAD-HARD ANALOG OPERATIONAL AMPLIFIERS, COMPARATOR, AND REGULATOR

High Slew Rate/Wide band Operational Amplifier HS-3516RH

Features	Radiation Effects	
• Specifically designed for radiation hardness • High slew rate: — $\geq \pm 22$ V/μs • Fast settling time: — $\leq$ 450 ns • Unity gain bandwidth: — 12 MHz • Low offset voltage @ 25°C: — $\leq \pm 5$ mV • Short circuit protection • Full military temperature range	• Dielectric Isolation technology • Each lot screened for total dose hardness • Parametrics guaranteed to 1 x 10^6 RADs (Si) • Latch-up free • Tolerant to neutron fluence > 5 x 10^{12} n/cm^2 (E $\geq$ 10 KeV) • Tolerant to gamma rate > 1 x 10^9 RADs (Si)/sec	

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RAD-HARD OPERATIONAL AMPLIFIERS, COMPARATOR AND REGULATOR

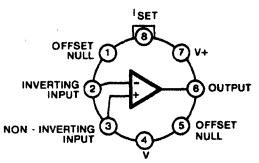
Low-Power/Programmable Operational Amplifier HS-3530RH

Features

- Specifically designed for radiation hardness
- Wide range AC programming:
  - — Slew rate: 0.06 to 3 V/μs
  - — Gain x bandwidth: 100 kHz to 5 MHz
- Wide range DC programming:
  - — Power supply: $\pm$ 1.5 to $\pm$ 18 V
  - — Supply current: 10 μA to 1.2 mA
- Short circuit protection
- Full military temperature range

Radiation Effects

- Dielectric Isolation technology
- Each lot screened for total dose hardness
- Parametrics guaranteed to 1 x 10^6 RADs (Si)
- Latch-up free
- Tolerant to neutron fluence > 5 x 10^{12} n/cm^2 (E $\geq$ 10 KeV)
- Tolerant to gamma rate > 1 x 10^9 RADs (Si)/sec



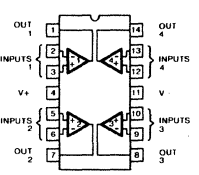
High Performance Quad Operational Amplifier HS-5104RH

Features

- Specifically designed for radiation hardness
- Low offset voltage: $\leq$ 3.0 mV
- High slew rate: $\geq$ 1.0 V/μs
- Unity gain bandwidth 6.5 MHz
- Single 5V supply capability
- Short circuit protection
- Full military temperature range

Radiation Effects

- Dielectric Isolation technology
- Each lot screened for total dose hardness
- Parametrics guaranteed to 1 x 10^5 RADs (Si)
- Latch-up free
- Tolerant to neutron fluence > 5 x 10^{12} n/cm^2 (E $\geq$ 10 KeV)
- Tolerant to gamma rate > 1 x 10^9 RADs (Si)/sec



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RAD-HARD
CMOS ANALOG MULTIPLEXERS

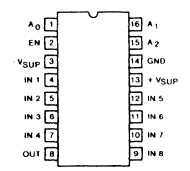
8-Channel Multiplexer — Overvoltage Protection
HS-508ARH

Features

- Specifically designed for radiation hardness
- Analog/digital overvoltage protection
- Fail-safe with power loss (no latch-up)
- Break-before-make switching
- DTL/TTL/CMOS compatible
- Analog signal range: — ± 15 V
- Access time (typical): — 500 ns
- Supply current @ 1 MHz address toggle (typical): — 4 mA
- Standby power (typical): — 7.5 mW
- Full military temperature range

Radiation Effects

- Dielectric Isolation technology
- Each lot screened for total dose hardness
- Parametrics guaranteed to 1 x 10^5 RADs (Si)
- Latch-up free
- Tolerant to neutron fluence > 1 x 10^{13} n/cm^2 (E ≥ 10 KeV)
- Tolerant to gamma rate > 1 x 10^9 RADs (Si)/sec



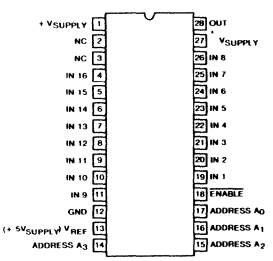
16-Channel Multiplexer-High-Z Analog Input Protection
HS-1840RH

Features

- Analog signal range: -5 V to + 15 V
- Specifically designed for radiation hardness
- High analog input impedance during power loss (open): — 500 MΩ
- Low standby power consumption (typical): — 600 μW
- Access time (typical): — 500 ns
- Excellent in hi-rel redundant systems
- Full military temperature range
- Break-before-make switching

Radiation Effects

- Dielectric Isolation technology
- Each lot screened for total dose hardness
- Parametrics guaranteed to 2 x 10^5 RADs (Si)
- Latch-up free
- Tolerant to neutron fluence > 1 x 10^{13} n/cm^2 (E ≥ 10 KeV)
- Tolerant to gamma rate > 1 x 10^9 RADs (Si)/sec



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RAD-HARD CMOS ANALOG SWITCHES

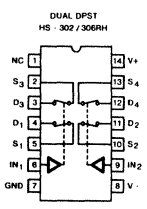
Radiation Hardened CMOS Analog Switches HS-302RH, HS-303RH, HS-306RH, HS-307RH, HS-384RH, HS-390RH

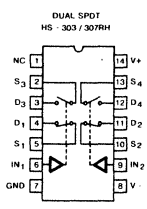
Features

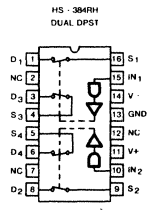
- Pin for pin compatible with Harris HI-3XX series analog switches
- Analog signal range: ± 15 V
- Low leakage (pre RAD typical at 25°C): 90 pA
- Low R_{ON} (pre RAD typical at 25°C): 30Ω
- Break-before-make delay (typical): 65 ns
- Full military temperature range
- Low operating power

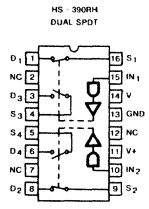
Radiation Effects

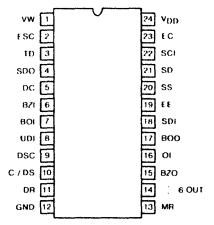
- Dielectric Isolation technology
- Each lot screened for total dose hardness
- Parametrics guaranteed to 1 x 10^5 RADs (Si)
- Latch-up free
- Tolerant to neutron fluence > 5 x 10^{13} n/cm² (E ≥ 10 KeV)
- Tolerant to gamma rate > 1 x 10^9 RADs (Si)/sec











RAD-HARD CMOS COMMUNICATION PRODUCTS

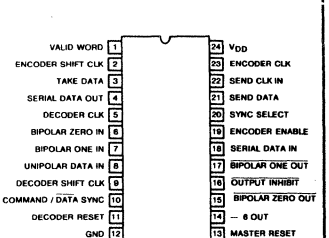
Manchester Encoder/Decoder (MED) HS-15530RH

Features

- Specifically designed for radiation hardness
- Support of MIL-STD-1553
- 1.0 Mbit/sec data rate
- Sync identification and lock-in
- Clock recovery
- Manchester II encode, decode
- Separate encode and decode
- Low operating power: 50 mW @ 5 V
- Full military temperature range

Radiation Effects

- Each lot screened for total dose hardness
- Parametrics guaranteed to 1 x 10^5 RADs (Si)
- Latch-up free
- Upset: > 10^8 RADs (Si)/sec



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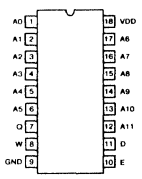
RAD-HARD CMOS STATIC RAMs 1K, 4K

4096 x 1 — 4K
HS-6504RH

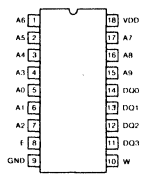
Features	Radiation Effects
• Specifically designed for radiation hardness • Low standby power (max): — 1100 μW • Low operating power (max): — 38.5 mW/MHz • TTL compatible output • Three-state output • On-chip address register • Standard JEDEC pinout • Full military temperature range	• Each lot screened for total dose hardness • Parametrics guaranteed to 1 x 10^5 RADs (Si) • Post rad standby current (max): — 200 μA • Post rad access time (typical): 120 ns (max): 200 ns • Latch-up free> 1 x 10^{12} RADs (Si)/sec • Upset: > 10^8 RADs (Si)/sec • SEU immune option available



RAD-HARD CMOS STATIC RAMs 4K & 16K

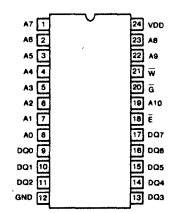
1024 x 4 — 4K
HS-6514RH

Features	Radiation Effects
• Specifically designed for radiation hardness • Low standby power (max): — 1100 μW • Low operating power (max): — 38.5 mW/MHz • TTL compatible output • Three-state output • Common data in/out • Standard JEDEC pinout • Full military temperature range	• Each lot screened for total dose hardness • Parametrics guaranteed to 1 x 10^5 RADs (Si) • Post rad standby current (typ): — 6 μA • Post rad access time: (typical): 120 ns (max): 225 ns • Latch-up free> 1^{12} RADs (Si)/sec • Upset: > 10^8 RADs (Si)/sec • SEU immune option available



(2048 x 8)—16K
HS-65C162RH, HS-65T162RH

Features	Radiation Effects
• Specifically designed for radiation hardness • Asynchronous operation • CMOS or TTL compatible input/output • Low standby power (max): CMOS: 1100 μW • Low operating current (max): 40 mA + 4mA/MHz • Three-state outputs • Full military temperature range	• Each lot screened for radiation hardness • Parametrics guaranteed to 2 x 10^5 RADs (Si) • Functional to 1 x 10^6 RADs (Si) • Access time (max., CMOS): 120 ns • Access time (typ., CMOS): 80 ns • Access time (typ., TTL): 100 ns • Transient upset > 1 x 10^9 RADs (Si)/s • Latch-up free > 1 x 10^{12} RADs (Si)/s • SEU immune option available



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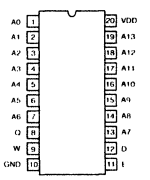
RAD-HARD CMOS STATIC RAMs/RAM MODULES 16K & 64K

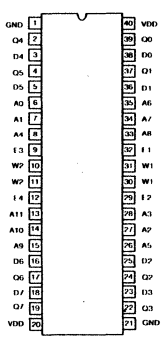
(16384 x 1) 16K
HS-65C262RH, HS-65T262RH

Features	Radiation Effects
• Specifically designed for radiation hardness • Asynchronous • TTL/CMOS compatible input/output • Low standby power (CMOS): 1 mW max. • Low operating power (max): 2.8 mW + 33 mW/MHz • Three-state output • Standard JEDEC pinout • Full military temperature range	• Each lot screened for radiation hardness • Parametrics guaranteed to 2 x 10^5 RADs (Si) • Access time (CMOS input): 150ns max., 80ns (typ) • Access time (TTL inputs): 175ns max., 100ns typ. • Data upset > 5 x 10^8 RADs (Si)/sec • Latch-up free> 1 x 10^{12} RADs (Si)/sec • SEU hardening option available



LCC RAM Module — 16384 x 4 or 8192 x 8 — 64K
HS-6564RH

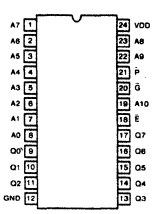
Features	Radiation Effects
• Specifically designed for radiation hardness • Low standby power (max): — 8.8 μW • Low operating power (max): — 308 mW/MHz • TTL compatible input/output • Three-state output • On-chip address register • Full military temperature range	• Each lot screened for total dose hardness • Total dose guaranteed to 1 x 10^5 RADs (Si) • Post rad standby current (typ): — 96 μA • Post rad access time (max): 250ns • Latch-up free> 10^{12} RADs (Si)/sec • Upset > 10^9 RADs (Si)/sec



RAD-HARD CMOS PROM — 16K

(2048 x 8) — 16K
HS-6617RH

Features	Radiation Effects
• Specifically designed for radiation hardness • Low standby power (max): — 550 μW • Low operating power (max): — 37.5 mW/MHz • TTL compatible input/output • Synchronous Operation • On-chip address latches • Three-state output • NiChrome fuse links • Full military temperature range	• Each lot screened for total dose hardness • Total dose guaranteed to 1 x 10^5 RADs (Si) • Access time (max): — 120ns • Latch-up free > 10^{12} RADs (Si)/sec



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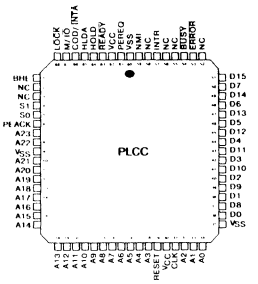
CMOS STATIC MICROPROCESSORS

High Performance Microprocessor With Memory Management and Protection 80C286

Features

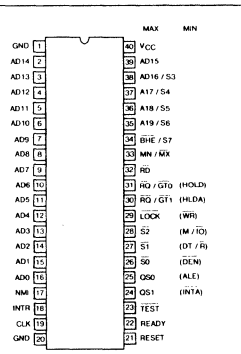
- Compatible with NMOS 80286
- Static CMOS Design for Low Power Operation
  > ICCSB = 5mA Maximum
  > ICCOP = 20mA/MHz Maximum
- High Performance Processor (Up to Fourteen Times the Throughput of the 8086)
- Two 80C86 Upward Compatible Operating Modes:
  > 80C286 Real Address Mode
  > Protected Virtual Address Mode
- Wide Range of Clock Rates:
  > DC to 16MHz (80C286-16)
  > DC to 12.5MHz (80C286-12)
  > DC to 10MHz (80C286-10)
- Available in 68 Pin PGA (Pin Grid Array) and PLCC (plastic leaded chip carrier) packages



16-Bit Microprocessor 80C86

Features

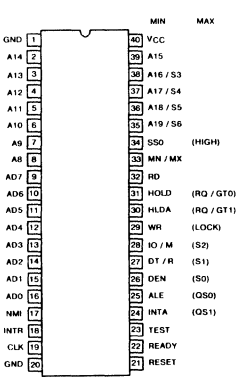
- Compatible with NMOS 8086
- Completely static design
  — DC to 5 MHz (80C86)
  — DC to 8 MHz (80C86-2)
- Low power operation:
  — 10 mA/MHz operating current
  — 500 μA standby current
- 1 MByte of direct memory addressing capability



8-Bit Microprocessor 80C88

Features

- Compatible with NMOS 8088
- Completely static design
  — DC to 5 MHz (80C88)
  — DC to 8 MHz (80C88-2)
- Low power operation:
  — 10 mA/MHz operating current
  — 500 μA standby current
- Software compatible with 80C86/8086/8088
- 1 MByte of direct memory addressing capability



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HARRIS SEMICONDUCTOR

80C286

High Performance Microprocessor With Memory Management and Protection

September 1988

Features

- Compatible with NMOS 80286
- Wide Range of Clock Rates:

Commercial	Industrial
-DC to 20MHz (C80C286-20)	-DC to 12.5MHz (I80C286-12)
-DC to 16MHz (C80C286-16)	-DC to 10MHz (I80C286-10)
-DC to 12.5MHz (C80C286-12)	

- Static CMOS Design for Low Power Operation
  - ICCSB = 5mA Maximum
  - ICCOP = 220mA Maximum (80C286-12)
    260mA Maximum (80C286-16)
    310mA Maximum (80C286-20)
- High Performance Processor (Up to 15 Times the 8086 Throughput)
- Wide Operating Temperature Ranges:
  - C80C286 ..... 0°C to +70°C
  - I80C286 ..... -40°C to +85°C
- Large Address Space:
  - 16 Megabytes Physical/1 Gigabyte Virtual per Task
- Integrated Memory Management, Four-Level Memory Protection and Support for Virtual Memory and Operating Systems
- Two 80C86 Upward Compatible Operating Modes:
  - 80C286 Real Address Mode
  - PVAM
- Compatible with 80287 Numeric Data Co-Processor
- High Bandwidth Bus Interface (20 Megabyte/Sec)
- Available In:
  - 68 Pin PGA (Commercial and Industrial)
  - 68 Pin PLCC (Commercial)

Description

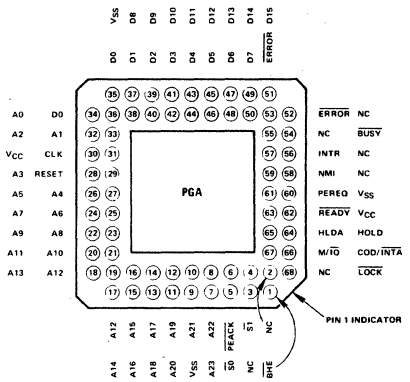
The Harris 80C286 is a static CMOS version of the NMOS 80286 microprocessor. The 80C286 is an advanced, high-performance microprocessor with specially optimized capabilities for multiple user and multi-tasking systems. The 80C286 has built-in memory protection that supports operating system and task isolation as well as program and data privacy within tasks. A 20MHz 80C286 provides up to fifteen times the throughput of a standard 5MHz 8086. The 80C286 includes memory management capabilities that map 2^{30} (one gigabyte) of virtual address space per task into 2^{24} bytes (16 megabytes) of physical memory.

The 80C286 is upwardly compatible with 80C86 and 80C88 sofware (the 80C286 instruction set is a superset of the 80C86/80C88 instruction set). Using the 80C286 real address mode, the 80C286 is object code compatible with existing 80C86 and 80C88 software. In protected virtual address mode, the 80C286 is source code compatible with 80C86 and 80C88 software but may require upgrading to use virtual address as supported by the 80C286's integrated memory management and protection mechanism. Both modes operate at full 80C286 performance and execute a superset of the 80C86 and 80C88 instructions.

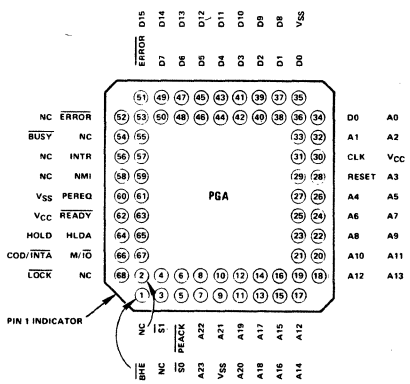
The 80C286 provides special operations to support the efficient implementation and execution of operating systems. For example, one instruction can end execution of one task, save its state, switch to a new task, load its state, and start execution of the new task. The 80C286 also supports virtual memory systems by providing a segment-not-present exception and restartable instructions.

Pin Configurations

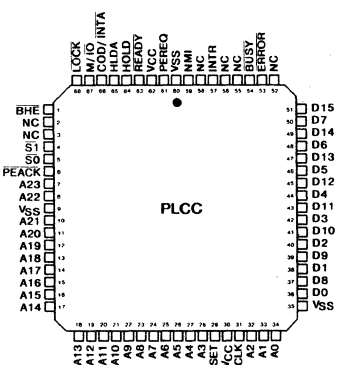
Component Pad View — As viewed from underside of the component when mounted on the board.



P.C. Board View — As viewed from the component side of the P.C. board.



P.C. Board View — As viewed from the component side of the P.C. board.



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CMOS
REAL-TIME MICROCONTROLLER

RTX 2000™

Features

- Fast 100ns Machine Cycle
- Single Cycle Instruction Execution
- Direct Execution of FORTH
  >Eliminates Assembly Language Programming
- Single Cycle 16-bit Multiply
- Fast Division, Square Root
- Single Cycle Subroutine Call/Return
- Three Cycle Interrupt Latency
- Two On-Chip 256 Word Stacks
- On-Chip Interrupt Controller
- Three On-Chip 16-bit Timer/Counters
- ASIC Bus™ for Off-Chip Extension of Architecture
- 1 Megabyte Total Address Space
- Word and Byte Memory Access
- Low Power CMOS . . . . . 5mA/MHz Typical
- Fully Static
- 84-Pin PGA Package
- Available in Harris Standard Cell Library

Description

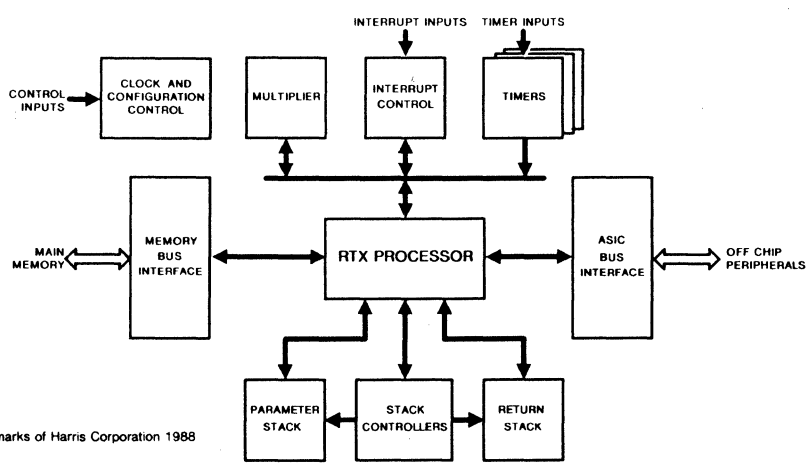
The RTX 2000 is a high performance 16-bit microcontroller with on-chip times, interrupt controller, and multiplier. A unique feature of this processor is the high performance ASIC Bus, which provides for architecture extension using off-chip hardware acceleration logic and application specific I/O devices.

Utilizing a stack oriented, multiple bus architecture and one or two cycle instruction timers, the RTX 2000 allows the efficient implementation of such real-time applications as Digital Signal Processing (DSP), Digital Control Processing, Image Processing, Robotics, Graphics, Simulation, Animation, and many other applications. Because these applications can be supported in high level languages such as FORTH and C on the RTX 2000, the development cycle time to system implementation is drastically reduced.

The RTX 2000 Microprocessor is an exceptionally powerful device with the ability to meet numerous application specific needs. The advantages of the RTX are further enhanced through the use of optional peripherals and by the development system support which Harris provides for the RTX hardware and IBM™ PC-based software.

The RTX 2000 has been designed and fabricated utilizing the Harris Advanced Standard Cell and Compiler Library. As part of the Harris family of compatible cell libraries, the RTX 2000 can be incorporated into customer ASIC designs.

RTX Block Diagram



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RTX 2001™

ADVANCE INFORMATION

September 1988

Real Time Express™ Microcontroller

Features

- **Fast 100ns Machine Cycle**
- **Single Cycle Instruction Execution**
- **Fast Multiply, Divide, Square Root**
- **Direct Execution of FORTH**
  - ▸ **Eliminates Assembly Language Programming**
- **Single Cycle Subroutine Call/Return**
- **Four Cycle Interrupt Latency**
- **On-Chip Interrupt Controller**
- **Three On-Chip 16-Bit Timer/Counters**
- **ASIC Bus™ for Off-Chip Extension of Architecture**
- **1 Megabyte Total Address Space**
- **Word and Byte Memory Access**
- **Low Power CMOS ..... 5mA/MHz Typical**
- **Fully Static ..... Low Standby Power**
- **84-Pin PGA or PLCC Package**
- **Available in the Harris Standard Cell Library**
- **Pin Compatible Subset of the RTX 2000™**
  - ▸ **Two On-Chip 64 Word Stacks**
  - ▸ **Fast Fixed Point, 20 Cycle 16/32-Bit Multiply**
  - ▸ **Refer to the RTX 2000 Data Sheet for Additional Specifications and Functional Descriptions**

RTX™, RTX 2000™, RTX 2001™, Real Time Express™ and ASIC Bus™ are Trademarks of Harris Corporation 1988

Description

The RTX 2001 is a 16-bit microcontroller which is particularly well suited for very high speed control tasks which are less arithmetically intensive than those tasks which require the full capabilities of the RTX 2000. In these application areas, this device offers cost/performance advantages, surpassing competing 8- and 16-bit microcontrollers by up to 50X.

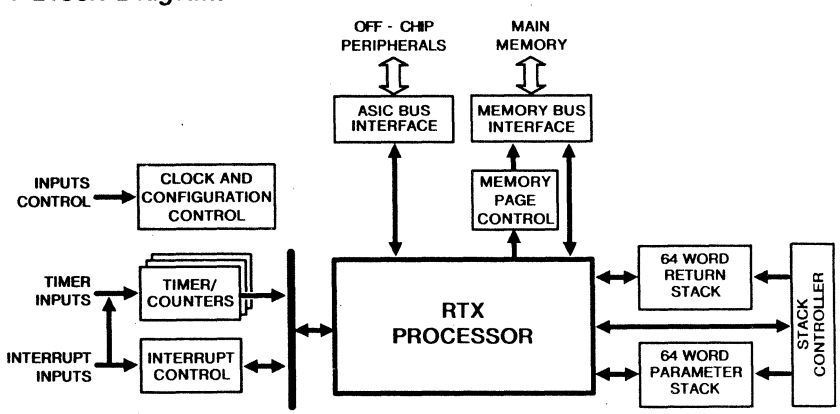
Pin compatible to the RTX 2000, this device incorporates most of the features provided on the RTX 2000, including on-chip timers and an interrupt controller. Instruction times of one or two cycles are achieved by utilizing a stack oriented, multiple bus architecture. The high performance ASIC Bus, which is unique to the RTX™ family of processors, provides for extension of the microprocessor architecture using off-chip hardware acceleration logic and application specific I/O devices. The RTX supports high level languages such as FORTH and C, which can greatly reduce the cycle time of system development to system implementation for a given application.

Combined, these features make the RTX 2001 an extremely powerful device, providing the ability to meet numerous applications in low cost, high performance systems. Logic intensive tasks for which this device is especially well suited include random logic replacement, bus interfaces, serial communications, peripheral device control, data acquisition, DMA controllers, stepper motor control, and even closed loop digital control and filter applications of moderate speed.

The advantages of the RTX are further enhanced through the use of the optional peripherals and development system support which Harris provides for the RTX family.

The RTX 2001 has been designed and fabricated utilizing the Harris Advanced Standard Cell and Compiler Library. As part of the Harris family of compatible cell libraries, the RTX 2001 can be incorporated into customer ASIC designs.

RTX 2001 Block Diagram



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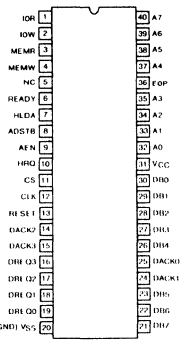
CMOS PERIPHERAL CIRCUITS

DMA Controller 82C37A

COMING SOON

Features

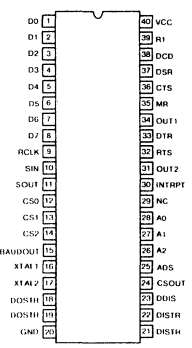
- Compatible with NMOS 8237A
- Provides control for direct memory access operation
- Up to 4 Mb/s transfer rate with 8 MHz clock
- Four independently programmable DMA channels
- Low power operation
- 12.5 MHz operation with 0 wait state DMA transfers
- 16 bit DMA transfer capability



Asynchronous Communication Element 82C50A

Features

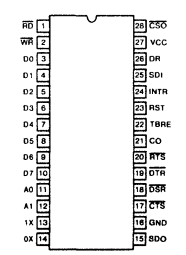
- Complete serial communication interface
  - — UART
  - — Baud rate generator
- 80C86/88 compatible
- DC to 10 MHz operation (DC to 625 Kbaud)
- Modem interface control lines
- Low CMOS power dissipation
- Compatible with NMOS 8250A



Serial Controller Interface 82C52

Features

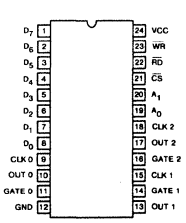
- UART/Baud rate generator in a single 28-pin package
- Operates from DC to 1 Mbaud with an asynchronous 16X clock
- 72 programmable baud rates
- Low power operation:
  - — 1 mA/MHz operating current, typical
- 40-pin version available (HD-6406)



Programmable Interval Timer 82C54

Features

- Compatible with NMOS 8254
- Enhanced version NMOS 8253
- Three independent 16-bit counters
- Six programmable counter modes
- Completely TTL compatible
- 8 MHz count frequency
- Low power operation:
  - >ICCOP: 10 mA @ 8 MHz count frequency
  - >ICCSB: 10 μA maximum



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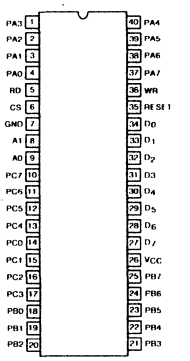
CMOS PERIPHERAL CIRCUITS

Programmable Peripheral Interface 82C55A

Features

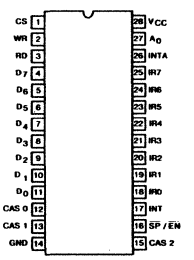
- Three independent programmable 8-bit I/O ports
- High speed, no "wait state" operation with 5 MHz/8 MHz 80C86/88
- Fully TTL compatible
- 2.5 mA drive capability on all I/O port outputs
- Compatible with NMOS 8255A
- 24 programmable I/O pins
- Enhanced control word read capability
- High darlington drive outputs on all ports
- Standby current: 10μA, maximum



Priority Interrupt Controller 82C59A

Features

- Compatible with NMOS 8259A
- Eight maskable interrupt inputs
- Cascade operation allows up to 64 interrupt inputs with no additional circuitry
- Supports both 8080/85 and 80C86/88 formats
- Standby current: 10 μA, maximum
- Fully TTL compatible
- Programmable interrupt modes



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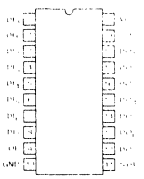
CMOS BUS SUPPORT CIRCUITS

Octal Latching Bus Driver 82C82

Features

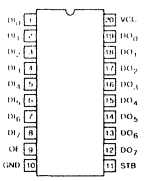
- Bipolar 8282 function compatible
- Propagation delay guaranteed: 35 ns maximum
  - — Full temperature range
  - — 10% power supply tolerances
  - — Load capacitance: 300 pf
- Gated inputs reduce operating power
- ICCSB: 10 μA maximum



Octal Latching Inverting Bus Driver 82C83H

Features

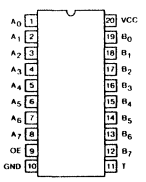
- Bipolar 8283 function compatible
- Full eight-bit latching buffer with inverted data output
- Guaranteed propagation delay of 25 ns Max. @ C_L = 300 pf
- Gated inputs reduce operating power
- ICCSB: 10 μA maximum
- High output sink current: 20 mA



Octal Transceiver 82C86H

Features

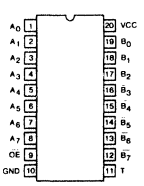
- Bipolar 8286 function compatible
- Eight-bit bidirectional bus transceiver
- Guaranteed propagation delay of 32 ns Max. @ C_L = 300 pf
- Gated inputs reduce operating power
- ICCSB: 10 μA maximum
- High output sink current: 20 mA



Octal Inverting Transceiver 82C87H

Features

- Bipolar 8287 function compatible
- Eight-bit bidirectional bus transceiver with inverting data outputs
- Guaranteed propagation delay of 30 ns Max. @ C_L = 300 pf
- Gated inputs reduce operating power dissipation
- ICCSB: 10 μA maximum
- High output sink current: 20 mA



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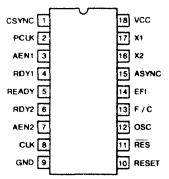
CMOS BUS SUPPORT CIRCUITS

Clock Generator/Driver 82C84A

Features

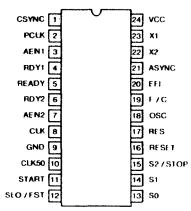
- Compatible with bipolar 8284A
- Output frequencies up to 8 MHz
- Provides Ready synchronization
- Parallel resonant crystal inputs
- ICCOP: 40 mA @ 8 MHz system frequency
- TTL compatible inputs/outputs



Static Clock Controller/Generator 82C85

Features

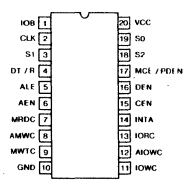
- Provides complete static clock control for 80C86 and 80C88 systems
- Supports stop-clock, stop-oscillator and low-frequency operation
- 80C86/88 status line interface allows software control
- DC to 8 MHz system clock
- Low CMOS power dissipation
- 24 pin slimline package



Bus Controller 82C88

Features

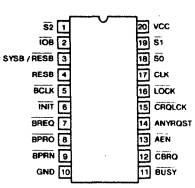
- Pin compatible with bipolar 8288
- Generates system control signals for maximum mode 80C86/88, 8086/88
- Bipolar drive capability
- Low power operation:
  - — ICC standby: 10 μA maximum
  - — ICC operating: 1 mA/MHz maximum



Bus Arbiter 82C89

Features

- Pin compatible with bipolar 8289
- Provides bus control arbitration in multi-master processor systems
- Low power operation:
  - — ICCSB: 10 μA maximum
  - — ICCOP: 1 mA/MHz maximum
- Bipolar drive capability



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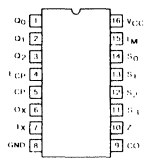
CMOS DATA COMMUNICATION

Bit Rate Generator (BRG) HD-4702

Features

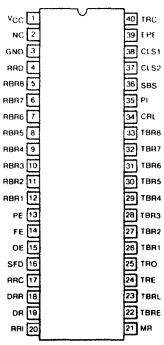
- Low power dissipation
- Programmable bit rate selection
- 13 commonly used bit rates
- Uses standard 2.4575 MHz crystal
- Conforms to EIA RS-404
- On-chip input pull-up circuits



Universal Asynchronous Receiver/Transmitter (UART) HD-6402R, HD-6402B

Features

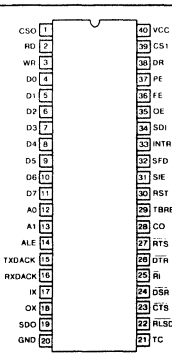
- Operates from DC to 8 MHz (DC to 500 Kbaud)
- Programmable word length, stop bits and parity
- Industry standard pinout
- Single +5 V power supply
- Fully TTL compatible
- Automatic data formatting and status generation



Programmable Asynchronous Communications Interface HD-6406

Features

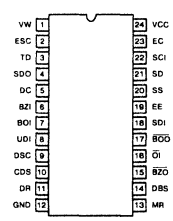
- UART/Baud rate generator in a single 40-pin package
- Data rates from DC to 1 Mbaud with an asynchronous 16X clock
- 72 programmable baud rates
- Complete modem interface signals
- DMA handshaking operation
- Low power operation:
  — 1 mA/MHz, typical
- 28-pin version available (82C52)



Asynchronous Serial Manchester Adapter (ASMA) HD-6408

Features

- 1 Mb/s data rate
- Sync identification and lock-in
- Clock recovery
- Manchester II encode and decode
- Low bit error rate
- Industrial temperature range
  -40°C to +85°C



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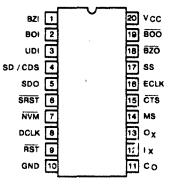
CMOS DATA COMMUNICATION

Manchester Encoder/Decoder (MED) HD-6409

Features

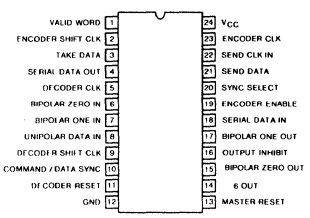
- 1 Mb/s data rate
- Digital PLL clock recovery
- On chip oscillator
- Independent Manchester II encode and decode
- Wide temperature ranges available
  -40°C to +85°C
  -55°C to +125°C



Manchester Encoder/Decoder (MED) HD-15530

Features

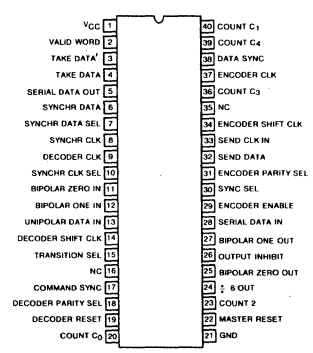
- Support of MIL-STD-1553
- 1.25 Mb/s data rate
- Sync identification and lock-in
- Clock recovery
- Separate encode and decode
- Low operating power: 50 mW @ 5 Volts
- Full temperature range: -55°C to +125°C



Manchester Encoder/Decoder (MED) HD-15531

Features

- Support of MIL-STD-1553
- 1.25 Mb/s data rate
- 2.5 Mb/s option (HD-15531B)
- Sync identification and lock-in
- Clock recovery
- Variable frame length to 32 bits
- Separate encode and decode
- Low operating power: 50 mW @ 5 Volts
- Full temperature range: -55°C to +125°C



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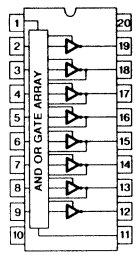
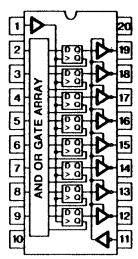
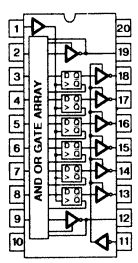
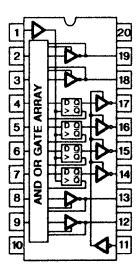
CMOS PROGRAMMABLE LOGIC

Part Number	Description	Maximum Pwr. Supply Current	Maximum I/O Propagation Delay	
HPL-16LC8	CMOS 16L8 10 inputs 6 bidirectionals 2 outputs Programmable output polarity Security fuse for pattern protection	ICCSB: 150 μA ICCOP: 6 mA/MHz	125 ns	

Part Number	Description	Maximum Pwr. Supply Current	Maximum I/O Propagation Delay	
HPL-16RC8	CMOS 16R8 8 inputs 8 registered outputs Programmable output polarity Security fuse for pattern protection	ICCSB: 150 μA ICCOP: 7 mA/MHz	125 ns	

Part Number	Description	Maximum Pwr. Supply Current	Maximum I/O Propagation Delay	
HPL-16RC6	CMOS 16R6 8 inputs 6 registered outputs 2 bidirectionals Programmable output polarity Security fuse for pattern protection	ICCSB: 150 μA ICCOP: 7 mA/MHz	125 ns	

Part Number	Description	Maximum Pwr. Supply Current	Maximum I/O Propagation Delay	
HPL-16RC4	CMOS 16R4 8 inputs 4 registered outputs 4 bidirectionals Programmable output polarity Security fuse for pattern protection	ICCSB: 150 μA ICCOP: 7 mA/MHz	125 ns	

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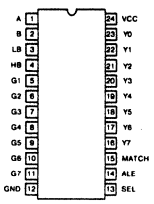
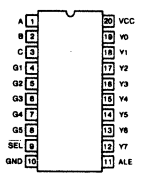
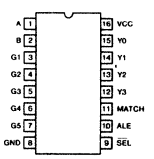
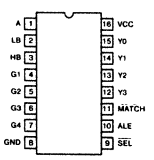
CMOS PROGRAMMABLE LOGIC

Part Number	Description	Maximum Pwr. Supply Current	Maximum Propagation Delay	
HPL-82C339	• 24-pin Programmable Chip Select Decoder (PCSD™) • Nine programmable inputs • Superset of 74138/74139	ICCSB: 50 μA ICCOP: 2 mA/MHz	50 ns	

Part Number	Description	Maximum Pwr. Supply Current	Maximum Propagation Delay	
HPL-82C338	• 20-pin Programmable Chip Select Decoder (PCSD™) • Five programmable inputs • Superset of 74138	ICCSB: 50 μA ICCOP: 2 mA/MHz	50 ns	

Part Number	Description	Maximum Pwr. Supply Current	Maximum Propagation Delay	
HPL-82C138	• 16-pin Programmable Chip Select Decoder (PCSD™) • Five programmable inputs • Similar to 74138	ICCSB: 50 μA ICCOP: 2 mA/MHz	50 ns	

Part Number	Description	Maximum Pwr. Supply Current	Maximum Propagation Delay	
HPL-82C139	• 16-pin Programmable Chip Select Decoder (PCSD™) • Six programmable inputs • Similar to 74139	ICCSB: 50 μA ICCOP: 2 mA/MHz	50 ns	

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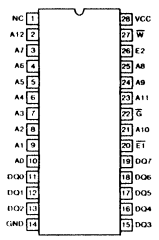
CMOS STATIC RAMs 64K

8192 x 8 — 64K Asynchronous

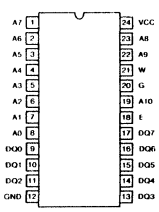
Part Number	Access Time	Power Supply Current		Replaces Pin for Pin
		Operating	Standby	
HM-65642	150 ns	20 mA	250 μA	AM99C88 NMC6164 MB8464 CDM6264
HM-65642B	150 ns	20 mA	100 μA	



CMOS STATIC RAMs — 16K

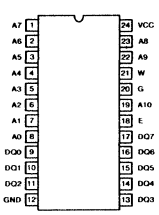
2048 x 8 — 16K Synchronous

Part Number	Access Time	Power Supply Current		Similar To
		Operating	Standby	
HM-6516B	120 ns	10 mA/MHz	50 μA	Hitachi 6116 Toshiba 5517 National 6516
HM-6516	200 ns	10 mA/MHz	100 μA	



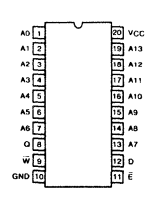
2048 x 8 — 16K Asynchronous

Part Number	Access Time	Power Supply Current		Replaces Pin for Pin
		Operating	Standby	
HM-65162S	55 ns	70 mA	100 μA	Fujitsu 8416 Hitachi 6116 NEC 446 Toshiba 5517 National 6116 IDT 6116
HM-65162B	70 ns	70 mA	50 μA	
HM-65162	90 ns	70 mA	100 μA	
HM-65162C	90 ns	70 mA	900 μA	



16384 x 1 — 16K Asynchronous

Part Number	Access Time	Power Supply Current		Replaces Pin for Pin
		Operating	Standby	
HM-65262S	55 ns	50 mA	50 μA	Hitachi 6167 IDT 6167
HM-65262B	70 ns	50 mA	50 μA	
HM-65262	85 ns	50 mA	50 μA	



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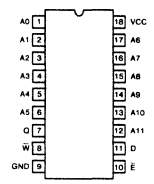
CMOS STATIC RAMs — 4K & 1K

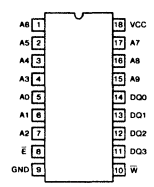
4096 x 1 — 4K Synchronous

Part Number	Access Time	Power Supply Current		Replaces Pin for Pin
		Operating	Standby	
HM-6504S	120 ns	7 mA/MHz	25 μA	Fujitsu 8404
HM-6504B	200 ns	7 mA/MHz	25 μA	Oki 5104
HM-6504	300 ns	7 mA/MHz	25 μA	National 6504



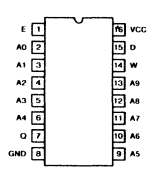
1024 x 4 — 4K Synchronous

Part Number	Access Time	Power Supply Current		Replaces Pin for Pin
		Operating	Standby	
HM-6514S	120 ns	7 mA/MHz	25 μA	Fujitsu 6514 Hitachi 4334 Nec 444
HM-6514B	200 ns	7 mA/MHz	25 μA	RCA 5114 Toshiba 5514
HM-6514	300 ns	7 mA/MHz	25 μA	National 6514



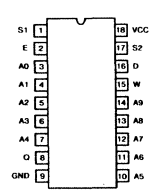
1024 x 1 — 1K Synchronous

Part Number	Access Time	Power Supply Current		Replaces Pin for Pin
		Operating	Standby	
HM-6508B	180 ns	4 mA/MHz	10 μA	National 74C929 Intersil 6508
HM-6508	250 ns	4 mA/MHz	10 μA	AMI 56508



1024 x 1 — 1K Synchronous

Part Number	Access Time	Power Supply Current		Replaces Pin for Pin
		Operating	Standby	
HM-6518B	180 ns	4 mA/MHz	10 μA	National 74C930 Intersil 6518
HM-6518	250 ns	4 mA/MHz	10 μA	



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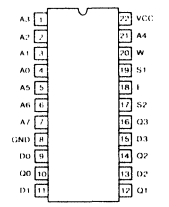
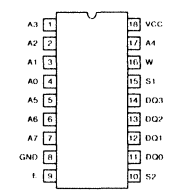
CMOS STATIC RAMS — 1K

256 x 4 — 1K Synchronous					
Part Number	**Access Time**	**Power Supply Current**		**Replaces Pin for Pin**	
		Operating	**Standby**		
HM-6551B	220 ns	4 mA/MHz	10 μA	Intersil 6551	
HM-6551	300 ns	4 mA/MHz	10 μA		

256 x 4 — 1K Synchronous					
Part Number	**Access Time**	**Power Supply Current**		**Replaces Pin for Pin**	
		Operating	**Standby**		
HM-6561B	220 ns	4 mA/MHz	10 μA	Intersil 6561	
HM-6561	300 ns	4 mA/MHz	10 μA		

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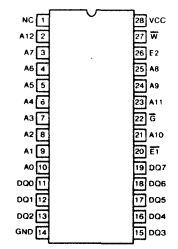
CMOS STATIC RAM MODULES

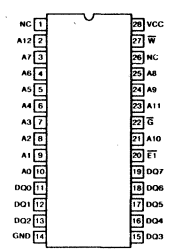
LCC RAM Module — 8K x 8 — 64K Asynchronous

Part Number	Access Time	Power Supply Current		Replaces Pin for Pin
		Operating	Standby	
HM-8808AS	100 ns	70 mA	250 μA	EDH8808A
HM-8808AB	120 ns	70 mA	250 μA	IDT7M864
HM-8808A	150 ns	70 mA	900 μA	HM6264



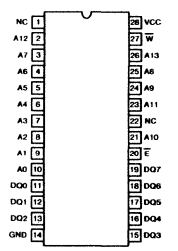
LCC RAM Module — 8K x 8 — 64K Asynchronous

Part Number	Access Time	Power Supply Current		Replaces Pin for Pin
		Operating	Standby	
HM-8808S	100 ns	70 mA	250 μA	EDH8808
HM-8808B	120 ns	70 mA	250 μA	IDT8M864
HM-8808A	150 ns	70 mA	900 μA	



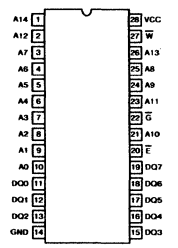
LCC RAM Module — 16K x 8 — 128K Asynchronous

Part Number	Access Time	Power Supply Current		Replaces Pin for Pin
		Operating	Standby	
HM-8816H	85 ns	400 mA	800 μA	—
HM-8816HB	70 ns	400 mA	800 μA	—



LCC RAM Module — 32768 x 8 — 256K Asynchronous

Part Number	Access Time	Power Supply Current		Replaces Pin for Pin
		Operating	Standby	
HM-8832	180 ns	20 mA	900 μA	EDH8832 IDT7M856 HM62256 MSM5256 μPD43256 TC55256



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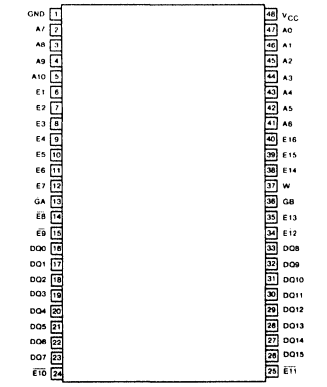
CMOS STATIC RAM MODULES

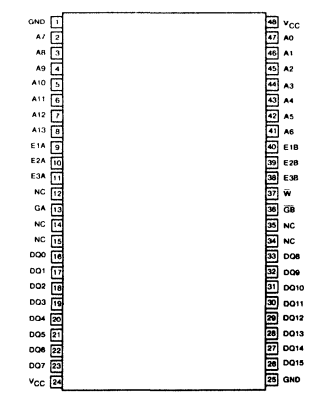
LCC RAM Module — 16384 x 16 / 32768 x 8 — 256K Synchronous

Part Number	Access Time	Power Supply Current		Replaces Pin for Pin
		Operating	Standby	
HM-92560	150 ns	30/15 mA	500 μA	—
HM-92560-5	250 ns	35/20 mA	3.5 mA	—



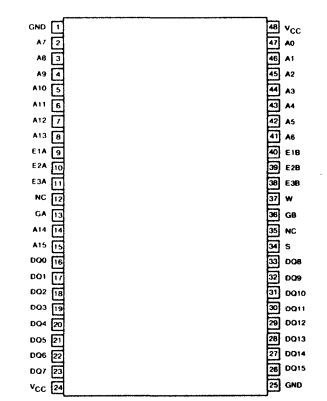
LCC Buffered Ram Module — 16384 x 16 / 32768 x 8 — 256K Synchronous

Part Number	Access Time	Power Supply Current		Replaces Pin for Pin
		Operating	Standby	
HM-92570	250 ns 300 ns	30/15 mA 35/20 mA	600 μA 3.5 mA	EDH892570



LCC Buffered Ram Module — 65536 x 16 / 131072 x 8 — 1M Asynchronous

Part Number	Access Time	Power Supply Current		Replaces Pin for Pin
		Operating	Standby	
HM-91M2	180 ns	20 mA	750 mA	EDH891M2



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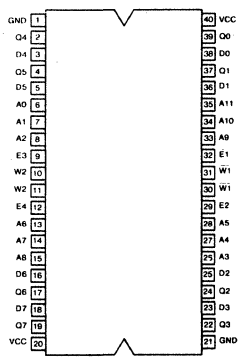
CMOS STATIC RAM MODULES

LCC RAM Module — 16384 x 4 / 8192 x 8 — 64K Synchronous

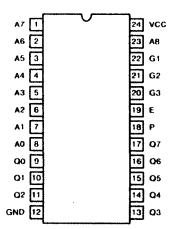
Part Number	Access Time	Power Supply Current		Replaces Pin for Pin
		Operating	Standby	
HM5-6564	350 ns	56/28 mA	800 μA	—
HM5-6564-5	450 ns	60/30 mA	5.6 mA	—



CMOS PROMs — 4K & 16K

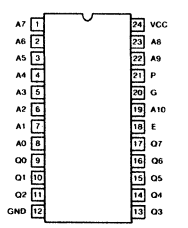
512 x 8 — 4K Synchronous

Part Number	Fuse Element	Access Time	Power Supply Current		Replaces Pin for Pin
			Operating	Standby	Harris 6641
HM-6642B	NiCr	120 ns	20 mA/MHz	100 μA	Similar to: Harris 7641
HM-6642	NiCr	200 ns	20 mA/MHz	100 μA	Signetics 82S141



2048 x 8 — 16K Synchronous

Part Number	Fuse Element	Access Time	Power Supply Current		Replaces Pin for Pin
			Operating	Standby	Harris 6616
HM-6617B	NiCr	90 ns	20 mA/MHz	100 μA	Similar to: NMOS 2716
HM-6617	NiCr	120 ns	20 mA/MHz	100 μA	National 27C16 National 6716 Intersil 6716 Harris 6616



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HARRIS SEMICONDUCTOR

HI-546/547

Single 16/Differential 8 Channel CMOS Analog Multiplexers with Active Overvoltage Protection

Features

- **Analog Overvoltage Protection ..... $70V_{p-p}$**
- **No Channel Interaction During Overvoltage**
- **ESD Resistant ..... >4,000V**
- **Guaranteed R_{ON} Matching**
- **44V Maximum Power Supply**
- **Break-Before-Make Switching**
- **Analog Signal Range ..... ±15V**
- **Access Time (Typical) 500ns**
- **Standby Power (Typical) 7.5mW**

Applications

- **Data Acquisition**
- **Industrial Controls**
- **Telemetry**

Description

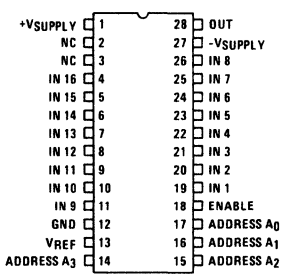
The HI-546 and HI-547 are analog multiplexers with Active Overvoltage Protection and guaranteed R_{ON} matching. Analog input levels may greatly exceed either power supply without damaging the device or disturbing the signal path of other channels. Active protection circuitry assures that signal fidelity is maintained even under fault conditions that would destroy other multiplexers. Analog inputs can withstand constant 70 volt peak-to-peak levels and typically survive static discharges beyond 4,000 volts. Digital inputs will also sustain continuous faults up to 4 volts greater than either supply. In addition, signal sources are protected from short circuiting should multiplexer supply loss occur; each input presents 1kΩ of resistance under this condition. These features make the HI-546 and HI-547 ideal for use in systems where the analog inputs originate from external equipment or separately powered circuitry. Both devices are fabricated with 44 volt dielectrically isolated CMOS technology. The HI-546 is a 16 channel device and the HI-547 is a 8 channel differential version. If input overvoltage protection is not needed, the HI-506 and HI-507 multiplexers are recommended. For further information see Application Notes 520 and 521.

The HI-546/547 are offered in both commercial and military grades. Additional Hi-Rel screening to MIL-STD-883 is available when specified by the "/883" suffix. For details, request the HI-546/883 or HI-547/883 data sheets.

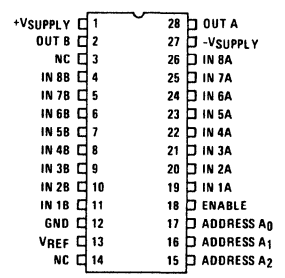
Each device is available in a 28 pin Plastic or Ceramic DIP, and a 28 pin Plastic Leaded Chip Carrier (PLCC).

Pinouts

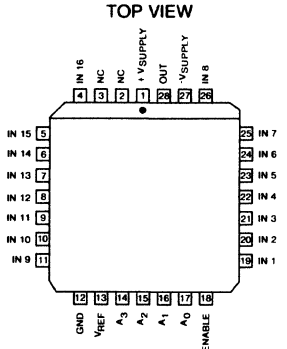
HI1-546 (CERAMIC DIP)
HI3-546 (PLASTIC DIP)
TOP VIEW



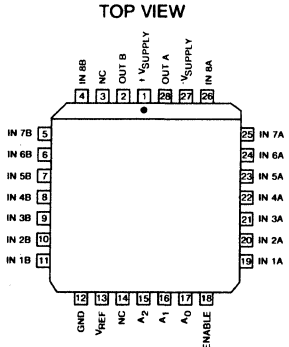
HI1-547 (CERAMIC DIP)
HI3-547 (PLASTIC DIP)
TOP VIEW



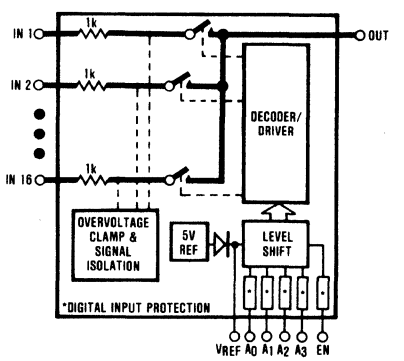
HI4P546 (PLCC)
TOP VIEW



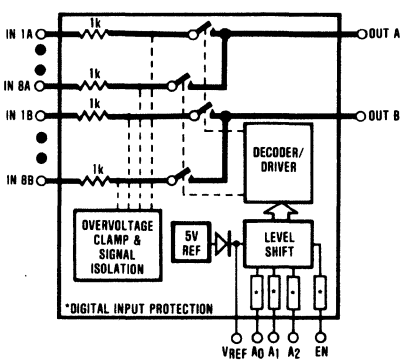
HI4P547 (PLCC)
TOP VIEW



Functional Diagrams



HI-546



HI-547

CAUTION: These devices are sensitive to electrostatic discharge. Proper IC handling procedures should be followed.

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HARRIS SEMICONDUCTOR

HI-548/549

Single 8/Differential 4 Channel CMOS Analog Multiplexers with Active Overvoltage Protection

Features

- Analog Overvoltage Protection ..... $70V_{p-p}$
- No Channel Interaction During Overvoltage
- ESD Resistant ..... >4,000V
- Guaranteed RON Matching
- 44V Maximum Power Supply
- Break-Before-Make Switching
- Analog Signal Range ..... ±15V
- Access Time (Typical) 500ns
- Standby Power (Typical) 7.5mW

Applications

- Data Acquisition
- Industrial Controls
- Telemetry

Description

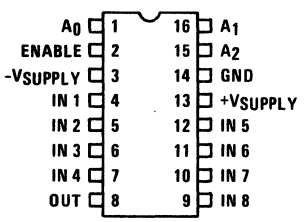
The HI-548 and 549 are analog multiplexers with Active Overvoltage Protection and guaranteed R_{ON} matching. Analog input levels may greatly exceed either power supply without damaging the device or disturbing the signal path of other channels. Active protection circuitry assures that signal fidelity is maintained even under fault conditions that would destroy other multiplexers. Analog inputs can withstand constant 70 volt peak-to-peak levels and typically survive static discharges beyond 4,000 volts. Digital inputs will also sustain continous faults up to 4 volts greater than either supply. In addition, signal sources are protected from short circuiting should multiplexer supply loss occur; each input presents 1kΩ of resistance under this condition. These features make the HI-548 and HI-549 ideal for use in systems where the analog inputs originate from external equipment or separately powered circuitry. Both devices are fabricated with 44 volt dielectrically isolated CMOS technology. The HI-548 is an 8 channel device and the HI-549 is a 4 channel differential version. If input overvoltage protection is not needed, the HI-508 and HI-509 multiplexers are recommended. For further information see Application Notes 520 and 521.

The HI-548/549 are offered in both commercial and military grades. Additional Hi-Rel screening to MIL-STD-883 is available, when specified by the "/883" suffix. For details, request the HI-548/883 or HI-549/883 data sheets.

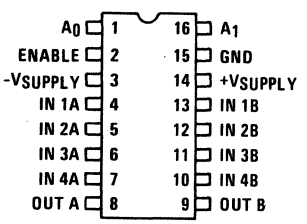
Each device is available in a 16 pin Plastic or Ceramic DIP, and a 20 pin Plastic Leaded Chip Carrier (PLCC).

Pinouts

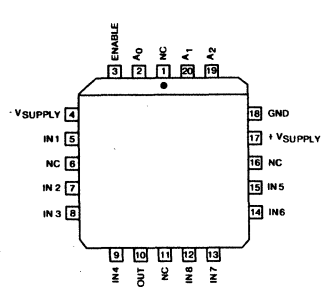
HI1-548 (CERAMIC DIP)
HI3-548 (PLASTIC DIP)
TOP VIEW



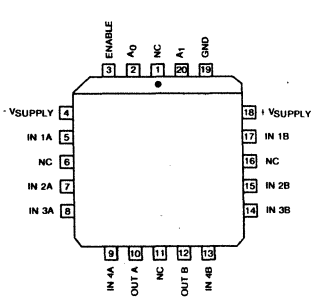
HI1-549 (CERAMIC DIP)
HI3-549 (PLASTIC DIP)
TOP VIEW



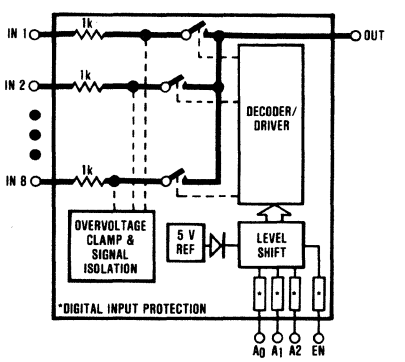
HI4P548 (PLCC)
TOP VIEW



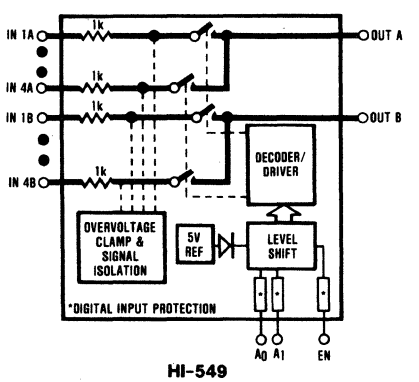
HI4P549 (PLCC)
TOP VIEW



Functional Diagrams



HI-548



HI-549

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HARRIS SEMICONDUCTOR

HI-5690V/95V/97V

High Speed, 12-Bit Low Cost Monolithic Digital-to-Analog Converter

Features

- **Voltage Output with Fast Settling 750ns**
  High Slew Rate 50V/μs
- **Industry Standard Pinout - AD-DAC 80 & HI-5680 Compatible**
- **Two-Supply Operation ..... 11.4V to 16.5V**
  -11.4V to -16.5V
- **Low Noise Voltage Reference**
  1/f (0.1Hz to 10Hz) ..... 15μV_{p-p}
- **Guaranteed Monotonic Over Full Temperature Range**
- **Application Resistors On-Chip**
- **Complementary Binary Input Code**
- **Voltage Output**
- **Complete Family of Temperature Grades**

Applications

- **High Speed A/D Converters**
- **Precision Instrumentation**
- **CRT Display Generation**

Description

The HI-5690V series of complete 12 bit digital to analog converters includes a low noise, low temperature coefficient buried zener reference and a fast settling output amplifier. The series consists of the HI-5690V, -5695V and -5697V, for the commercial, industrial and military temperature ranges. Monolithic construction along with several design innovations make these converters an optimum choice for high speed, high reliability applications.

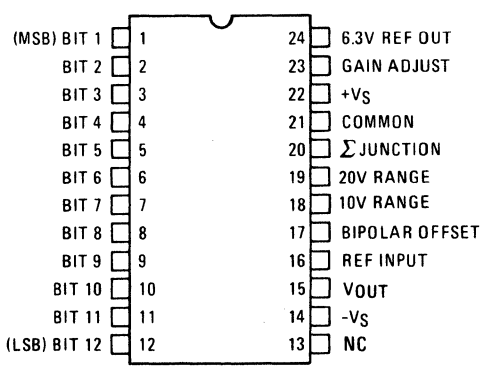
The Harris unique Dielectric Isolation (DI) processing reduces internal parasitics, resulting in fast switching times and minimum glitch. Wafer-level laser trimming of span resistors and bit current cells ensures high accuracy and exceptional tracking over temperature.

Internally, the HI-5690V series eliminates code dependent ground currents by routing current from the positive supply to the internal ground node, as determined by an auxiliary R-2R ladder. This results in a cancellation of code dependent ground currents, allowing virtually zero variation in current through the package common, thus minimizing analog ground noise seen by the converter.

The HI-5690V series operates from two supplies $\pm V_S$ in the range of ±11.4 Volts to ±16.5 volts. It is pin compatible with the AD-DAC 80 series and HI-5680 series, and since Pin 13 is not internally connected (Logic supply on standard 5680's) this device is compatible in applications with or without +5 Volts applied to Pin 13. The converter performance is guaranteed over the full power supply operating range, but not all output ranges are available with low supply voltages. The package is a 24 pin Ceramic Sidebrazed DIP. For Mil-Std-883 compliant parts, request the HI-5697V/883 data sheet.

Pinouts

DIP
TOP VIEW



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HARRIS SEMICONDUCTOR

HI-574A

Fast, Complete 12-Bit A/D Converter with Microprocessor Interface

Features

- Complete 12-Bit A/D Converter with Reference and Clock
- Full 8-, 12- or 16-Bit Microprocessor Bus Interface
- 150ns Bus Access Time
- No Missing Codes Over Temperature
- Minimal Set-up Time for Control Signals
- 25μs Maximum Conversion Time
- Low Noise, via Current-Mode Signal Transmission Between Chips
- Byte Enable/Short Cycle (A_0 Input)
  - Guaranteed Break-Before-Make Action, Eliminating Bus Contention During Read Operation. Latched by the Start Convert Input (To Set the Conversion Length)
- Improved Second Source for AD574A and HS574
- $\pm$12V to $\pm$15V Operation

Applications

- Military and Industrial Data Acquisition Systems
- Electronic Test and Scientific Instrumentation
- Process Control Systems

Description

The HI-574A is a complete 12-bit Analog-to-Digital Converter, including a +10V reference, clock, three-state outputs and a digital interface for microprocessor control. Successive approximation conversion is performed by two monolithic dice housed in a 28 pin package. The bipolar analog die features the Harris Dielectric Isolation process, which provides enhanced AC performance and freedom from latch-up.

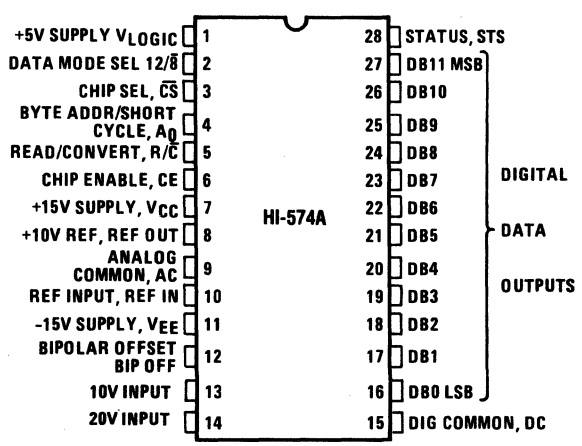
Custom design of each IC (bipolar analog and CMOS digital) has yielded improved performance over existing versions of this converter. The voltage comparator features high PSRR plus a high speed current-mode latch, and provides precise decisions down to 0.1 LSB of input overdrive. More than 2X reduction in noise has been achieved by using current instead of voltage for transmission of all signals between the analog and digital IC's. Also, the clock oscillator is current-controlled for excellent stability over temperature. The oscillator is trimmed for a nominal conversion time of 20 $\pm$ 1μs.

The HI-574A offers standard unipolar and bipolar input ranges, laser trimmed for specified linearity, gain and offset accuracy. The buried zener reference circuit is trimmed for minimum temperature coefficient.

Power requirements are +5V and $\pm$12V to $\pm$15V, with typical dissipation of 385mW at $\pm$12V. All models are available in a 28 pin Sidebrazed DIP. For additional Hi-Rel screening including 160 hour burn-in, specify the "-8" suffix. For MIL-STD-883 compliant parts, request the HI-574A/883 data sheet.

Pinouts

SIDEBRAZE DIP
TOP VIEW



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HARRIS SEMICONDUCTOR

HI-674A

12μs, Complete 12-Bit A/D Converter with Microprocessor Interface

Features

- Complete 12-Bit A/D Converter with Reference and Clock
- Full 8-, 12- or 16-Bit Microprocessor Bus Interface
- 150ns Bus Access Time
- No Missing Codes Over Temperature
- Minimal Set-up Time for Control Signals
- 15μs Maximum Conversion Time
- Low Noise, via Current-Mode Signal Transmission Between Chips
- Byte Enable/Short Cycle (A_0 Input)
  - ▸ Guaranteed Break-Before-Make Action, Eliminating Bus Contention During Read Operation. Latched by the Start Convert Input (To Set the Conversion Length)
- Faster Version of the HI-574A
- Same Pinout as the HI-574A
- ±12V to ±15V Operation

Applications

- Military and Industrial Data Acquisition Systems
- Electronic Test and Scientific Instrumentation
- Process Control Systems

Description

The HI-674A is a complete 12-bit Analog-to-Digital Converter, including a +10V reference, clock, three-state outputs and a digital interface for microprocessor control. Successive approximation conversion is performed by two monolithic dice housed in a 28 pin package. The bipolar analog die features the Harris Dielectric Isolation process, which provides enhanced AC performance and freedom from latch-up.

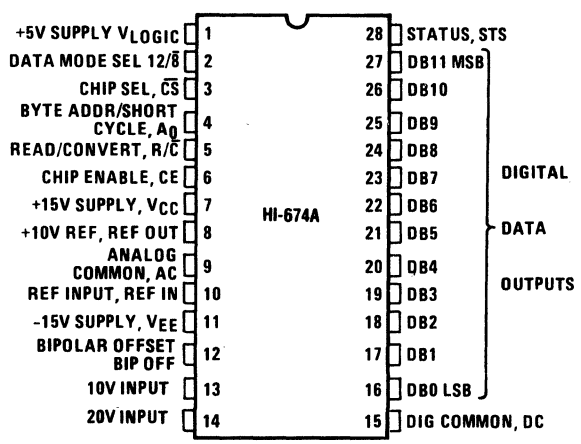
Custom design of each IC (bipolar analog and CMOS digital) has yielded improved performance over existing versions of this converter. The voltage comparator features high PSRR plus a high speed current-mode latch, and provides precise decisions down to 0.1 LSB of input overdrive. More than 2X reduction in noise has been achieved by using current instead of voltage for transmission of all signals between the analog and digital IC's. Also, the clock oscillator is current-controlled for excellent stability over temperature. The oscillator is trimmed for a nominal conversion time of 12 ± 1μs.

The HI-674A offers standard unipolar and bipolar input ranges, laser trimmed for specified linearity, gain and offset accuracy. The buried zener reference circuit is trimmed for minimum temperature coefficient.

Power requirements are +5V and ±12V to ±15V, with typical dissipation of 385mW at ±12V. All models are available in a 28 pin Sidebrazed DIP. For additional Hi-Rel screening including 160 hour burn-in specify the "-8" suffix. For MIL-STD-883 compliant parts, request the HI-674A/883 data sheet.

Pinout

CERAMIC DIP
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Proper IC handling procedures should be followed.

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HARRIS SEMICONDUCTOR

HI-774

ADVANCED

8μs, Complete 12-Bit A/D Converter With Microprocessor Interface

Features

- **Complete 12 Bit A/D Converter With Reference and Clock**
- **Digital Error Correction**
- **Full 8-, 12-, or 16-Bit Microprocessor Bus Interface**
- **150 nS Buss Access Time**
- **No Missing Codes Over Temperature**
- **Minimal Setup Time For Control Signals**
- **8μs Maximum Conversion Time Over Temperature**
- **Low Noise, Via Current-mode signal transmission between chips**
- **Byte enable/short cycle (Ao Input)**
- ▸ **Guarantees break-before-make action, eliminating bus contention during read operation. Latched by the Start Convert Input (To Set the Conversion Length)**
- **Faster Version of the HI-574A and HI-674A**
- **Same Pin-Out as HI-574A and HI-674A**
- **±12V to ±15V Operation**

Applications

- **Military and Industrial Data Acquisition Systems**
- **Electronics Test and Scientific Instrumentation**
- **Process Control Systems**

Description

The HI-774 is a complete 12 bit Analog-to-Digital Converter, including a +10V reference, clock, three-state outputs and a digital interface for microprocessor control. Successive approximation conversion is performed by two monolithic dice housed in a 28-pin package. The bipolar analog die features the Harris Dielectric Isolation process, whch provides enhanced AC performance and freedom from latch-up. The digital die features the smart SAR (SSAR™), which includes a digital error correction circuit.

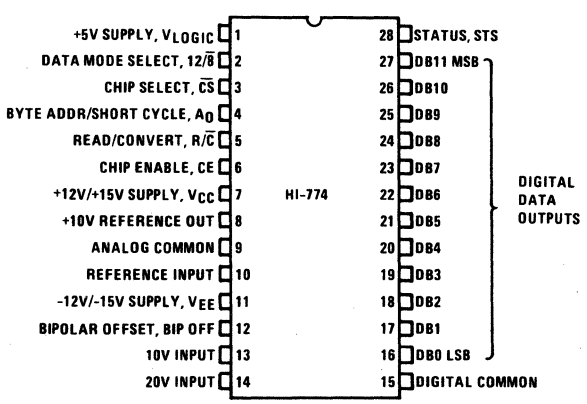
Custom design of each IC (bipolar and CMOS digital) has yielded improved performance over existing versions of this converter. The voltage comparator features high PSRR plus a high speed current-mode latch, and provides precise decisions down to 0.1 LSB of input overdrive. More than 2X reduction in noise has been achieved by using current instead of voltage for transmission of all signals between the analog and digital IC's. Also, the clock oscillator is current controlled for excellent stability over temperature. The oscillator is trimmed for a guaranteed conversion time of 7 ± 1μs over temperature.

The HI-774 offers standard unipolar and bipolar input ranges, laser trimmed for specified linearity gain and offset accuracy. The low noise buried zener reference circuit is trimmed for minimum temperature coefficient.

Power requirements are +5V and ±12V to ±15V, with typical dissipation of 390mW at ±12V. Three electrical grades each are offered for the commercial and military temperature ranges. All models are packaged in a 28 pin side-brazed, ceramic DIP. For information on MIL-STD-883 compliant device's request the HI-774/883 data sheet.

Pinout

TOP VIEW



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HARRIS SEMICONDUCTOR

HA-2420/25

Fast Sample and Hold

Features

- Maximum Acquisition Time (10V Step to 0.1%) ... 4μs (10V Step to 0.01%) 6μs
- Low Droop Rate (C_H = 1000pF) ..... 5μV/ms (Typ.)
- Gain Bandwidth Product ..... 2.5MHz (Typ.)
- Low Effective Aperture Delay Time ..... 30ns (Typ.)
- TTL Compatible Control Input
- ±12V to ±15V Operation

Applications

- 12-Bit Data Acquisition
- Digital to Analog Deglitcher
- Auto Zero Systems
- Peak Detector
- Gated Operational Amplifier

Description

The HA-2420/2425 is a monolithic circuit consisting of a high performance operational amplifier with its output in series with an ultra-low leakage analog switch and MOSFET input unity gain amplifier.

With an external holding capacitor connected to the switch output, a versatile, high performance sample-and-hold or track-and-hold circuit is formed. When the switch is closed, the device behaves as an operational amplifier, and any of the standard op amp feedback networks may be connected around the device to control gain, frequency response, etc. When the switch is opened the output will remain at its last level.

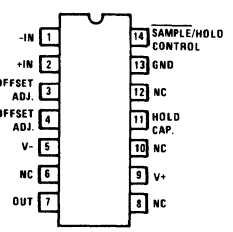
Performance as a sample-and-hold compares very favorably with other monolithic, hybrid, modular, and discrete circuits. Accuracy to better than 0.01% is achievable over the temperature range. Fast acquisition is coupled with superior droop characteristics, even at high temperatures. High slew rate, wide bandwidth, and low acquisition time produce excellent dynamic characteristics. The ability to operate at gains greater than 1 frequently eliminates the need for external scaling amplifiers.

The device may also be used as a versatile operational amplifier with a gated output for applications such as analog switches, peak holding circuits, etc. For more information, please see Application Note 517.

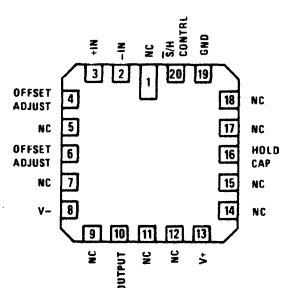
The HA-2420/25 is offered in a 14 pin Ceramic or Plastic DIP and a 20 pad Ceramic LCC or 20 pad PLCC. The MIL-STD-883 data sheet for this device is available on request.

Pinouts

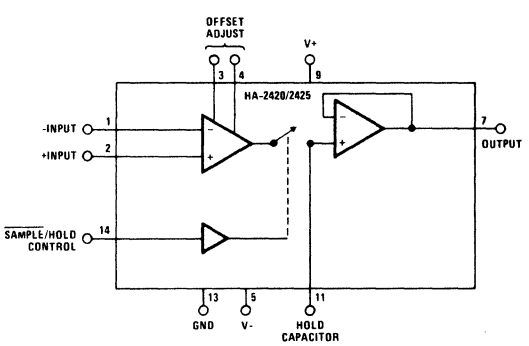
14 PIN CERAMIC/PLASTIC DIP
TOP VIEW



20 PAD LCC/PLCC
TOP VIEW



Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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HARRIS SEMICONDUCTOR

HA-2539

Very High Slew Rate Wideband Operational Amplifier

Features

- Very High Slew Rate 600V/μs
- Open Loop Gain 30kV/V
- Wide Gain-Bandwidth ($A_V \geq 10$) 600MHz
- Power Bandwidth 9.5MHz
- Low Offset Voltage 8mV
- Input Voltage Noise ..... 6nV/$\sqrt{Hz}$
- Output Voltage Swing ..... $\pm$10V
- Monolithic Bipolar Dielectric Isolation Construction

Applications

- Pulse and Video Amplifiers
- Wideband Amplifiers
- High Speed Sample-Hold Circuits
- RF Oscillators

Description

The Harris HA-2539 represents the ultimate in high slew rate, wideband, monolithic operational amplifiers. It has been designed and constructed with the Harris High Frequency Bipolar Dielectric Isolation process and features dynamic parameters never before available from a truly differential device.

With a 600V/μs slew rate and a 600MHz gain bandwidth product, the HA-2539 is ideally suited for use in video and RF amplifier designs, in closed loop gains of 10 or greater. Full $\pm$10V swing coupled with outstanding A.C. parameters and complemented by high open loop gain makes the devices useful in high speed data acquisition systems.

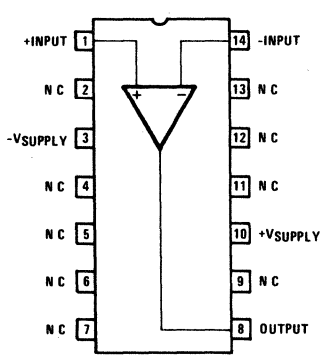
The HA-2539 is available in 14 pin ceramic and plastic DIP. The HA-2539-2 operates over -55°C to +125°C temperature range while the HA-2539-5 and HA-2539C-5 operates over the 0°C to +75°C range.

For further design assistance please refer to Application Note 541 (Using The HA-2539 Very High Slew Rate Wideband Operational Amplifiers) and Application Note 556 (Thermal Safe-Operating-Areas For High Current Operational Amplifiers).

For military grade product information, the HA-2539/883 data sheet is available upon request.

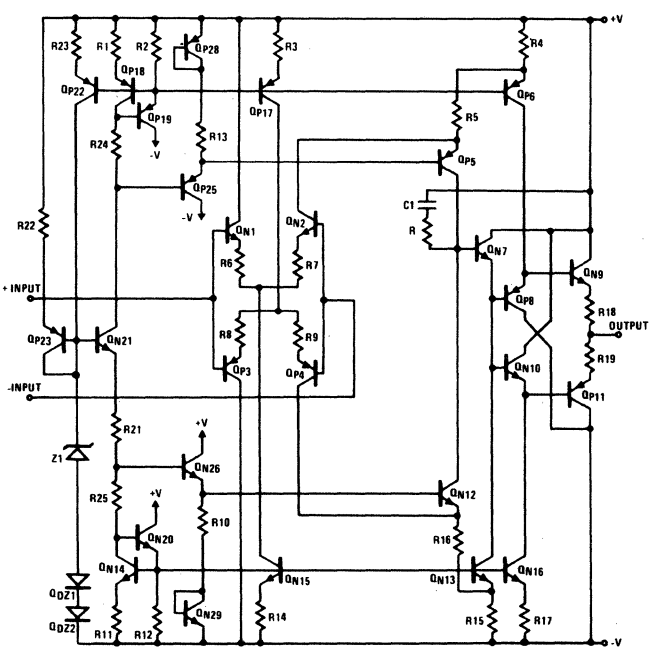
Pinout

HA1-2539/2539C (CERAMIC DIP)
HA3-2539/2539C (PLASTIC DIP)
TOP VIEW



(N C) No Connection pins may be tied to a ground plane for better isolation and heat dissipation.

Schematic



CAUTION: These devices are sensitive to electostatic discharge. Proper IC handling procedures should be followed.

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HARRIS SEMICONDUCTOR

HA-2540

Wideband, Fast Settling Operational Amplifier

Features

- Very High Slew Rate 400V/μs
- Fast Settling Time 200ns
- Wide Gain-Bandwidth (Av $\geq$ 10) 400MHz
- Power Bandwidth 6MHz
- Low Offset Voltage 8mV
- Input Voltage Noise ..... 6nV/$\sqrt{Hz}$
- Output Voltage Swing ..... $\pm$10V
- Monolithic Bipolar Construction

Applications

- Pulse and Video Amplifiers
- Wideband Amplifiers
- High Speed Sample-Hold Circuits
- Fast, Precise D/A Converters

Description

The Harris HA-2540 is a wideband, very high slew rate, monolithic operational amplifier featuring superior speed and bandwidth characteristics. Bipolar construction coupled with dielectric isolation allows this truly differential device to deliver outstanding performance in circuits where closed loop gain is 10 or greater. Additionally, the HA-2540 has a drive capability of $\pm$10V into a 1KΩ load. Other desirable characteristics include low input voltage noise, low offset voltage, and fast settling time.

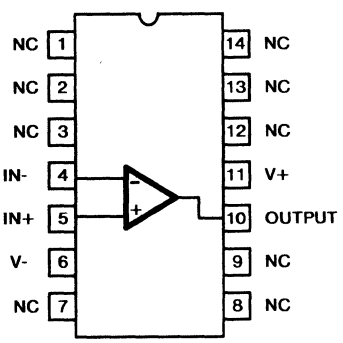
A 400/μs slew rate ensures high performance in video and pulse amplification circuits, while the 400MHz gain-bandwidth-product is ideally suited for wideband signal amplification. A settling time of 200ns also makes the HA-2540 an excellent selection for high speed Data Acquisition Systems.

The HA-2540-2 is specified over the -55°C to +125°C range while the HA-2540-5 and HA-2540C-5 is specified from 0°C to +75°C. The HA-2540 and HA-2540C are available in the 14 pin Ceramic and Epoxy DIP packages.

Refer to Application Note 541 and Application Note 556 for more information on High Speed Op-Amp applications. MIL-STD-883 data sheet is available on request.

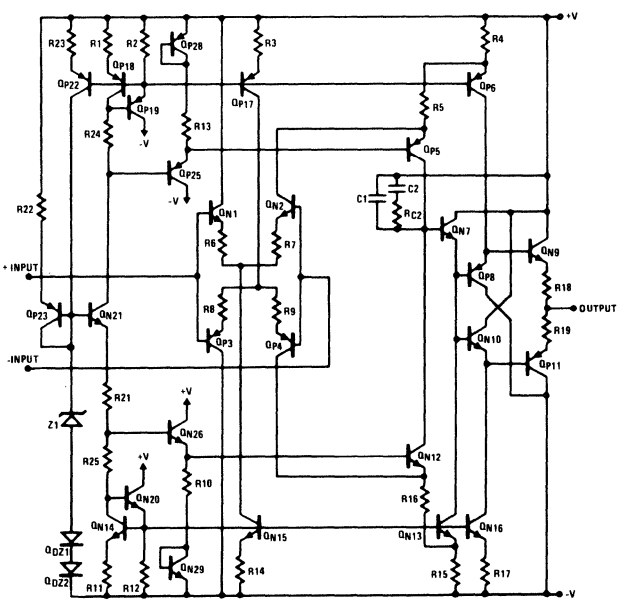
Pinout

HA1-2540/2540C (CERAMIC DIP)
HA3-2540/2540C (PLASTIC DIP)
TOP VIEW



NC - No Connection. These pins may be tied to a ground plane for added isolation and heat dissipation

Schematic



CAUTION: Electronic devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

For other Harris Semiconductor products see pages 2637-2688

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HARRIS SEMICONDUCTOR

HA-2541

Wideband, Fast Settling, Unity Gain Stable, Operational Amplifier

Features

- Unity Gain Bandwidth 40MHz
- High Slew Rate 250V/μs
- Low Offset Voltage 0.8mV
- Fast Settling Time (0.1%) 90ns
- Power Bandwidth 4MHz
- Output Voltage Swing (Min) ..... $\pm$10V
- Unity Gain Stability
- Monolithic Bipolar Dielectric Isolation Construction

Applications

- Pulse and Video Amplifiers
- Wideband Amplifiers
- High Speed Sample-Hold Circuits
- Fast, Precise D/A Converters
- High Speed A/D Input Buffer

Description

The HA-2541 is the first unity gain stable monolithic operational amplifier to achieve 40MHz unity gain bandwidth. A major addition to the Harris series of high speed, wideband op amps, the HA-2541 is designed for video and pulse applications requiring stable amplifier response at low closed loop gains.

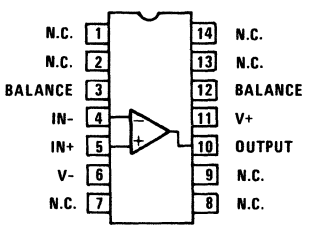
The uniqueness of the HA-2541 is that its slew rate and bandwidth characteristics are specified at unity gain. Historically, high slew rate, wide bandwidth and unity gain stability have been incompatible features for a monolithic operational amplifier. But features such as 250V/μs slew rate and 40MHz unity gain bandwidth clearly show that this is not the case for the HA-2541. These features, along with 90ns settling time to 0.1%, make this product an excellent choice for high speed data acquisition systems.

Packaged in a metal can (TO-8) or 14 pin ceramic DIP, the HA-2541 is pin compatible with the HA-2540 and HA-5190 op amps. The HA-2541-2 is specified over the temperature range of -55°C to +125°C. The HA-2541-5 is specified over the temperature range of 0°C to +75°C. For the military grade product, refer to the HA-2541 military data sheet.

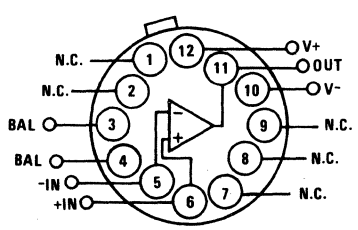
For further application suggestions on the HA-2541, please refer to Applicaton Note 550 (Using the HA-2541), and Application Note 556 (Thermal Safe-Operating-Areas For High Current Operational Amplifiers). Also see 'Applications' in this data sheet.

Pinouts

HA1-2541 (CERAMIC DIP)
TOP VIEW

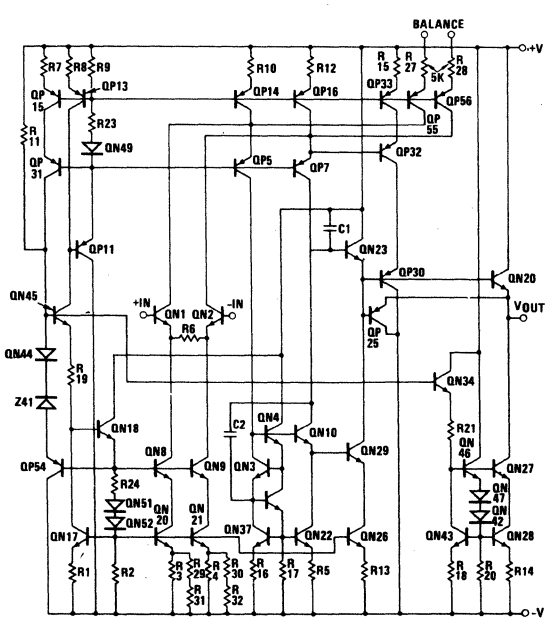


HA2-2541 (TO-8 METAL CAN)
TOP VIEW



V_{CASE} = V-

Schematic



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Harris Semiconductor

HARRIS SEMICONDUCTOR

HA-2542

Wideband, High Slew Rate, High Output Current Operational Amplifier

Features

- Stable at Gains of 2 or Greater
- Gain Bandwidth.....70MHz
- High Slew Rate (Min.).....300V/μs
- High Output Current (Min.).....100mA
- Power Bandwidth (Typ.).....5.5MHz
- Output Voltage Swing (Min.).....$\pm$10V
- Monolithic Bipolar Dielectric Isolation Construction

Applications

- Pulse and Video Amplifiers
- Wideband Amplifiers
- Coaxial Cable Drivers
- Fast Sample-Hold Circuits
- High Frequency Signal Conditioning Circuits

Description

The HA-2542 is a wideband, high slew rate, monolithic operational amplifier featuring an outstanding combination of speed, bandwidth, and output drive capability.

Utilizing the advantages of the Harris D. I. technology this amplifier offers 350V/μs slew rate, 70MHz gain bandwidth, and $\pm$100mA output current. Application of this device is further enhanced through stable operation down to closed loop gains of 2.

For additional flexibility, offset null and frequency compensation controls are included in the HA-2542 pinout.

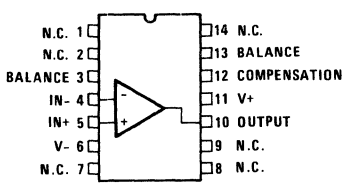
The capabilities of the HA-2542 are ideally suited for high speed coaxial cable driver circuits where low gain and high output drive requirements are necessary. With 5.5MHz full power bandwidth, this amplifier is most suitable for high frequency signal conditioning circuits and pulse video amplifiers. Other applications utilizing the HA-2542 advantages include wideband amplifiers and fast sample-hold circuits.

The HA-2542 is available in ceramic or plastic 14 lead DIP packages, or a 12 lead metal can (TO-8) which is pin compatible with the HA-2541, HA-5190, LH0032 and HOS-050C. The HA-2542-2 is specified over the -55°C to +125°C temperature range and is also offered as a military part. The HA-2542-5 is specified over the commercial temperature range of 0°C to 75°C.

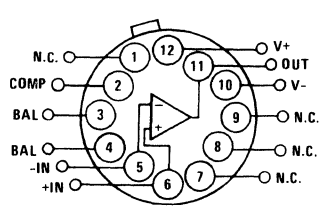
For more information on the HA-2542, please refer to Application Note 552 (Using The HA-2542), or Application Note 556 (Thermal Safe-Operating-Areas For High Current Op Amps).

Pinouts

HA1-2542 (CERAMIC DIP)
HA3-2542 (PLASTIC DIP)
TOP VIEW

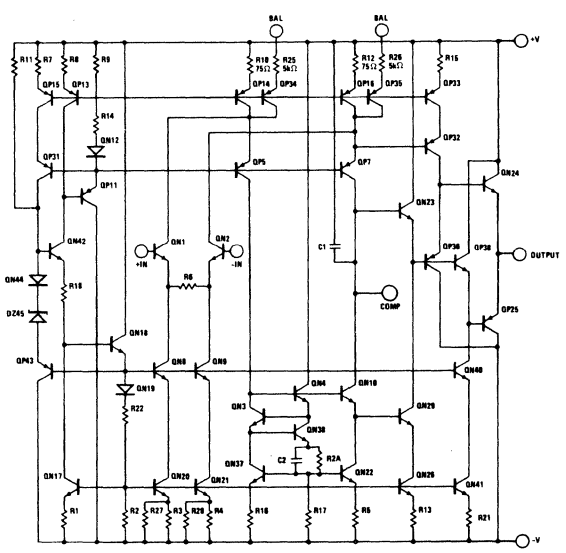


HA2-2542 (TO-8 METAL CAN)
TOP VIEW



V_{CASE} = V-

Schematic



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HARRIS SEMICONDUCTOR

HA-2544

Video Operational Amplifier

Features

- Gain Bandwidth 50MHz
- High Slew Rate 150V/µs
- Low Supply Current 10mA
- Differential Gain Error ..... <0.05dB
- Differential Phase Error ..... <0.1 degree
- Gain Tolerance at 5MHz ..... <0.15dB

Applications

- Video Systems
- Video Test Equipment
- Radar Displays
- Imaging Systems
- Pulse Amplifiers
- Signal Conditioning Circuits
- Data Acquisition Systems

Description

The HA-2544 is a fast, unity gain stable, monolithic op amp designed to meet the needs required for accurate reproduction of video or high speed signals. It offers high voltage gain (6kV/V) and high phase margin (65 degrees) while maintaining tight gain tolerance over the video bandwidth. Built from high quality Dielectric Isolation, the HA-2544 is another addition to the Harris series of high speed, wideband op-amps, and offers true video performance combined with the versatility of an op-amp.

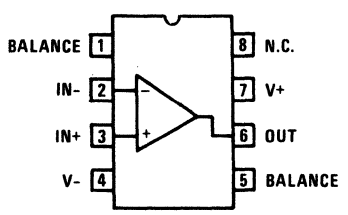
The primary features of the HA-2544 include 50MHz Gain Bandwidth, 150V/µs slew rate, < 0.05dB differential gain error and gain tolerance of just 0.15dB at 5MHz. High performance and low power requirements are met with a supply current of only 10mA.

Uses of the HA-2544 range from video test equipment guidance systems, radar displays and other precise imaging systems where stringent gain and phase requirements have previously been met with costly hybrids and discrete circuitry. The HA-2544 will also be used in non-video systems requiring high speed signal conditioning such as data acquisition systems, medical electronics, specialized instrumentation and communication systems.

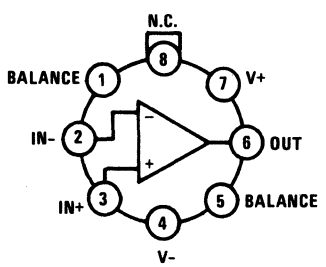
The HA-2544-2 is guaranteed over the military temperature range (-55°C to +125°C); the HA-2544-5 and the HA-2544C-5 over the commercial temperature range (0°C to +75°C). The HA-2544 is available in TO-99 Metal Can, and both Plastic and Ceramic Mini-DIP packages. Military (/883) product and data sheets are available upon request.

Pinouts

HA7-2544 (CERAMIC MINI-DIP)
HA3-2544/2544C (PLASTIC MINI-DIP)
TOP VIEW

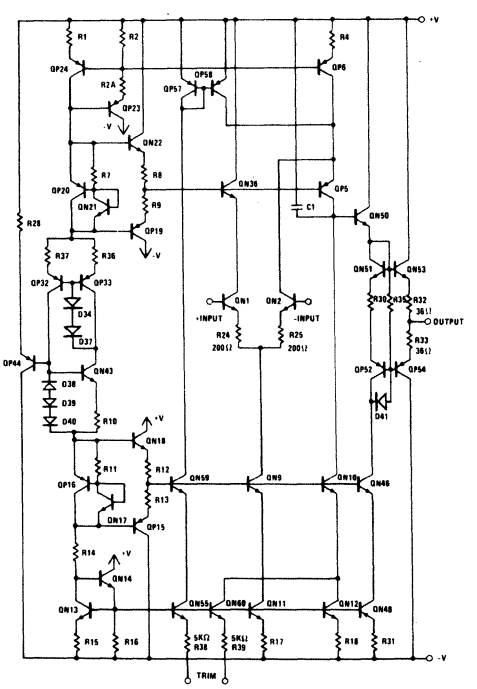


HA2-2544 (TO-99 METAL CAN)
TOP VIEW



NOTE: V_{CASE} = V-

Schematic



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HARRIS SEMICONDUCTOR

HA-5002

Monolithic, Wideband, High Slew Rate, High Output Current Buffer

Features

- Voltage Gain 0.995
- High Input Impedance 3000kΩ
- Low Output Impedance 3Ω
- Very High Slew Rate 1300V/μsec
- Very Wide Bandwidth 110MHz
- High Output Current ..... ±200mA
- Pulsed Output Current 400mA
- Monolithic Construction

Applications

- Line Driver
- Data Acquisition
- 110MHz Buffer
- High Power Current Booster
- High Power Current Source
- Sample and Holds
- Radar Cable Driver
- Video Products

Description

The HA-5002 is a monolithic, wideband, high slew rate, high output current, buffer amplifier.

Utilizing the advantages of the Harris D.I. technologies, the HA-5002 current buffer offers 1300V/μsec slew rate with 110MHz of bandwidth. The ±200mA output current capability is enhanced by a 3 ohm output impedance.

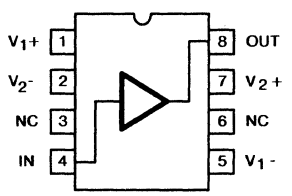
The monolithic HA-5002 will replace the hybrid LH0002 with corresponding performance increases. These characteristics range from the 3000K ohm input impedance to the increased output voltage swing. Monolithic design technologies have allowed a more precise buffer to be developed with more than an order of magnitude smaller gain error.

The HA-5002 will provide many present hybrid users with a higher degree of reliability and at the same time increase overall circuit performance.

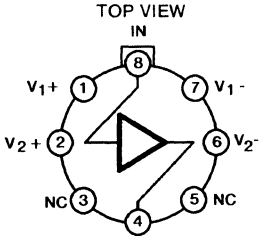
The HA-5002 is available in an 8 pin Metal Can, and 8 pin Ceramic and Plastic Mini-DIPs. For the military grade product, refer to the HA-5002/883 Data Sheet.

Pinouts

HA7-5002 (CERAMIC MINI-DIP)
HA3-5002 (PLASTIC MINI-DIP)
TOP VIEW

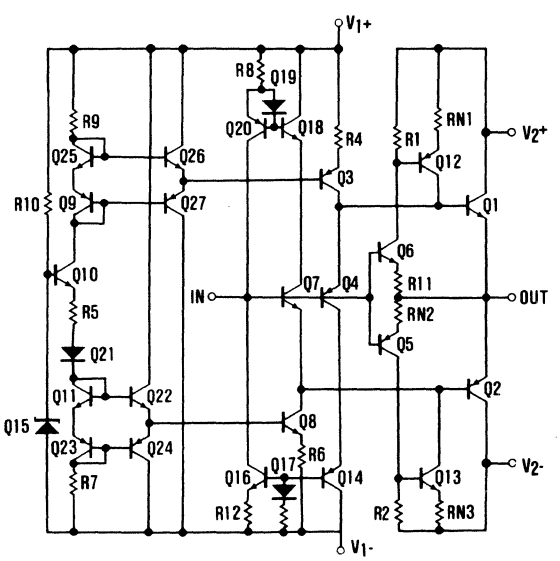


HA2-5002 (TO-99 METAL CAN)
TOP VIEW



LCC Package Available
for HA-5002/883.
See HA-5002/883 Data Sheet

Schematic



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HARRIS SEMICONDUCTOR

HA-5033

Video Buffer

Features

- **Differential Phase Error .....0.1 Degree**
- **Differential Gain Error 0.1%**
- **High Slew Rate 1300V/μs**
- **Wide Bandwidth (Small Signal) 250MHz**
- **Wide Power Bandwidth .....DC to 65MHz**
- **Fast Rise Time 3ns**
- **High Output Drive ..... ±8V With 100Ω Load**
- **Wide Power Supply Range ..... ±5V to ±16V**
- **Replace Costly Hybrids**

Applications

- Video Buffer
- High Frequency Buffer
- Isolation Buffer
- High Speed Line Driver
- Impedance Matching
- Current Boosters
- High Speed A/D Input Buffers
- For Further Application Ideas, See App. Note 548

Description

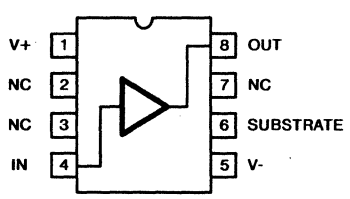
The HA-5033 is a unity gain monolithic I.C. designed for any application requiring a fast, wideband buffer. Featuring a bandwidth of 250MHz and outsanding differential phase/gain characteristics, this high performance voltage follower is an excellent choice for video circuit design. Other features, which include a minimum slew rate of 1000V/μs and high output drive capability, make the HA-5033 applicable for line driver and high speed data conversion circuits.

The high performance of this product is a result of the Harris Dielectric Isolation process. A major feature of this process is that it produces both PNP and NPN high frequency transistors which makes wide bandwidth designs, such as the HA-5033, practical. Alternative process methods typically produce a lower AC performance.

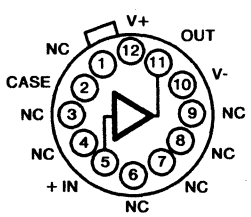
The HA-5033 is available in a 12 pin (TO-8) Metal Can or an 8 pin Plastic Mini-DIP.

Pinouts

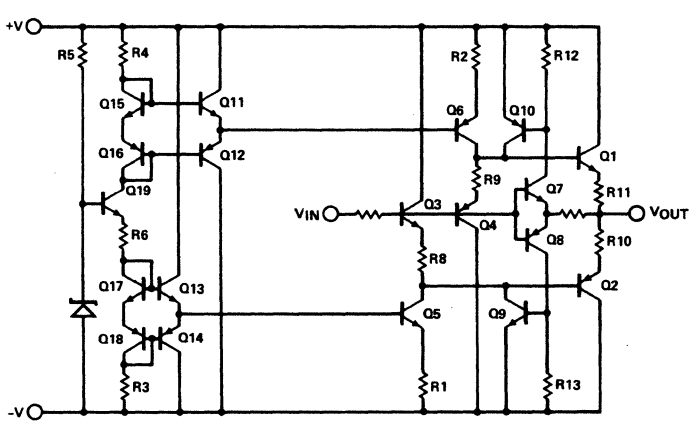
HA3-5033 (PLASTIC MINI-DIP)
TOP VIEW



HA2-5033 (TO-8 METAL CAN)
TOP VIEW



Schematic



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HARRIS SEMICONDUCTOR

HA-5101/5111

Low Noise, High Performance Operational Amplifiers

Features

- Low Noise ..... 3.3nV/$\sqrt{Hz}$ at 1kHz
- Wide Bandwidth ..... 10MHz (Compensated)
  100MHz (Uncompensated)
- High Slew Rate ..... 10V/μs (Compensated)
  50V/μs (Uncompensated)
- Low Offset Voltage Drift ..... 3μV/°C
- High Gain ..... 1 x 10^6V/V
- High CMRR/PSRR 100dB
- High Output Drive Capability 30mA

Applications

- High Quality Audio Preamplifiers
- High Q Active Filters
- Low Noise Function Generators
- Low Distortion Oscillators
- Low Noise Comparators
- For Further Design Ideas, See App. Note 554

Description

The HA-5101/5111 are dielectrically isolated operational amplifiers featuring low noise and high performance. Both amplifiers have an excellent noise voltage density of 3.5nV/$\sqrt{Hz}$ at 1kHz. The uncompensated HA-5111 is stable at a minimum gain of 10 and has the same DC specifications as the unity gain stable HA-5101. The difference in compensation yields a 100MHz gain-bandwidth product and a 50V/μs slew rate for the HA-5111 versus a 10MHz unity gain bandwidth and a 10V/μs slew rate for the HA-5101.

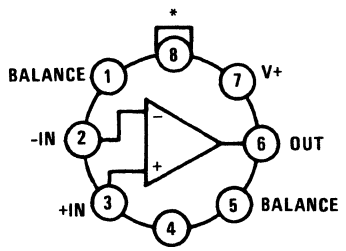
DC characteristics of the HA-5101/5111 assure accurate performance. The 1mV offset voltage is externally adjustable and offset voltage drift is just 3μV/°C. An offset current of only 30nA reduces input current errors and an open loop voltage gain of 1 x 10^6V/V increases loop gain for low distortion amplification.

The HA-5101/5111 are ideal for audio applications, especially low-level signal amplifiers such as microphone, tape head and phono cartridge preamplifiers. Additionally, it is well suited for low distortion oscillators, low noise function generators and high Q filters.

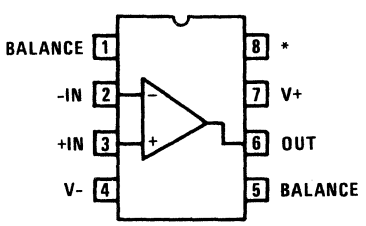
The HA-5101/5111-2 has guaranteed operation from -55°C to +125°C and can be ordered as a military grade part. The HA-5101/5111-5 has guaranteed operation from 0°C to +75°C. All devices are available in Ceramic Mini-DIP and TO-99 Can packages. Additionally, the HA-5101/5111-5 is available in a Plastic Mini-DIP package.

Pinouts

HA2-5101/5111 (TO-99 METAL CAN)
TOP VIEW



HA3-5101/5111 (PLASTIC MINI-DIP)
HA7-5101/5111 (CERAMIC MINI-DIP)
TOP VIEW



*HA-5101 No Connect
HA-5111 Compensation

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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HARRIS SEMICONDUCTOR

HA-5134

Precision Quad Operational Amplifier

Features

- Low Offset Voltage.....Max 200μV
- Low Offset Voltage Drift.....Max 2μV/^{o}C
- Offset Voltage Match (5134A)...Full Temp. Max 250μV
- High Channel Separation.....120dB
- Low Noise.....7nV/$\sqrt{Hz}$
- Wide Unity Gain Bandwidth.....4MHz
- High CMRR/PSRR (Typ).....120dB
- Dielectric Isolation

Applications

- Instrumentation Amplifiers
- State-Variable Filters
- Precision Integrators
- Threshold Detectors
- Precision Data Acquisition Systems
- Low-Level Transducer Amplifiers

Description

The HA-5134 is a precision quad operational amplifier that is pin compatible with the OP-400, LT1014, OP11, RM4156, and LM148 as well as the HA-4741. Each amplifier features guaranteed maximum values for offset voltage of 200μV, offset voltage drift of 2μV/^{o}C, and offset current of 75nA over the full military temperature range while CMRR/PSRR is guaranteed greater than 94dB and A_{VOL} is guaranteed above 750kV/V from -55^{o}C to +125^{o}C.

Precision performance of the HA-5134 is enhanced by a noise voltage density of 7nV/$\sqrt{Hz}$ at 1kHz, noise current density of 2pA/$\sqrt{Hz}$ at 1kHz and channel separation of 120dB. Each unity-gain stable quad amplifier is fabricated using the dielectric isolation process to assure performance in the most demanding applications.

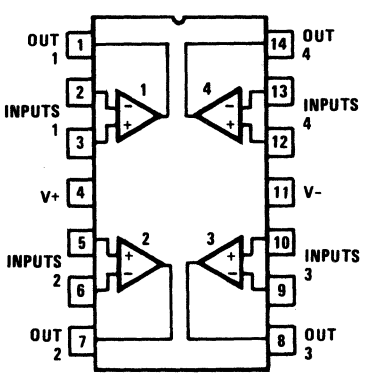
The HA-5134 is ideal for compact circuits such as instrumentation amplifiers, state-variable filters, and low-level transducer amplifiers. Other applications include precision data acquisition, precision integrators, and accurate threshold detectors in designs where board space is a limitation.

The HA-5134-2 has guaranteed operation from -55^{o}C to +125^{o}C and can be ordered as a military grade part. The HA-5134-5 is guaranteed from 0^{o}C to +75^{o}C and all devices are available in ceramic dual-in-line packages. For military grade product, refer to the HA-5134/883 Data Sheet.

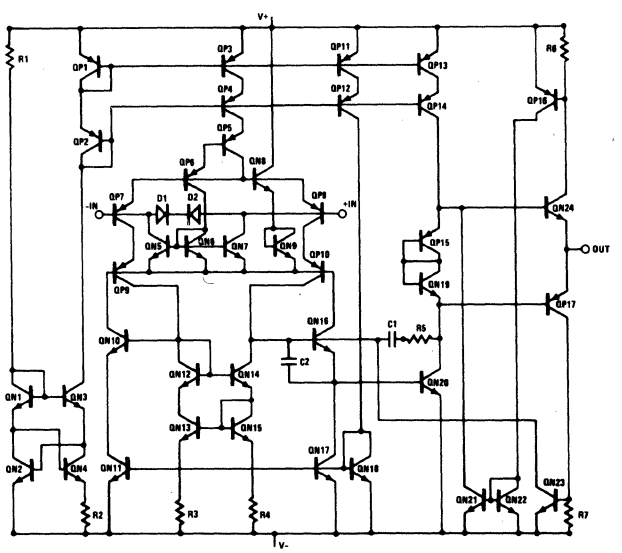
Pinout

HA1-5134 (CERAMIC DIP)

TOP VIEW



Schematic (Each Amplifier)



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HARRIS SEMICONDUCTOR

HA-5141/42/44

Single/Dual/Quad Ultra-Low Power Operational Amplifiers

Features

- Low Supply Current 45μA/Amp
- Wide Supply Voltage Range ..... Single 3V to 30V or Dual ±1.5V to ±15V
- High Slew Rate 1.5V/μs
- High Gain 100kV/V
- Unity Gain Stable
- Available in Singles, Duals and Quads

Applications

- Portable Instruments
- Meter Amplifiers
- Telephone Headsets
- Microphone Amplifiers
- Instrumentation
- For Further Design Ideas See App. Note 544

Description

The HA-5141/42/44 ultra-low power operational amplifiers provided AC and DC performance characteristics similar to or better than most general purpose amplifiers while only drawing 1/30 of the supply current of most general purpose amplifiers. In applications which require low power dissipation and good A.C. electrical characteristics, this family offers the industry's best speed/power ratio.

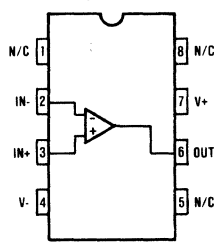
The HA-5141/42/44 provides accurate signal processing by virtue of their low input offset voltage (0.5mV), low input bias current (45nA), high open loop gain (100kV/V) and low noise, for low power operational amplifiers (20nV/$\sqrt{Hz}$). These characteristics coupled with a 1.5/μs slew rate and a 400kHz bandwidth make the HA-5141/42/44 ideal for use in low power instrumentation, audio amplifier and active filter designs. The wide range of supply voltages (3V to 30V) also allow these amplifiers to be very useful in low voltage battery powered equipment. These parts are also tested and guaranteed at both ±15V and single ended +5V supplies.

These amplifiers are available in singles (HA-5141, Can or Mini-DIP), duals (HA-5142, Can, Mini-DIP or 20 pin LCC) or quads (HA-5144, 14 pin DIP or 20 pin LCC) with industry standards pinouts which allow the HA-5141/5142/5144's to be interchangeable with most other operational amplifiers. For military grade product refer to the 5141, 5142, 5144/883 data sheet.

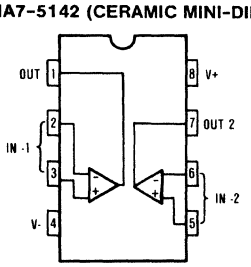
Pinouts

TOP VIEWS

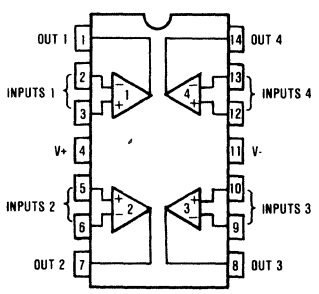
HA1-5141 (CERAMIC MINI-DIP)
HA3-5141 (PLASTIC MINI-DIP)



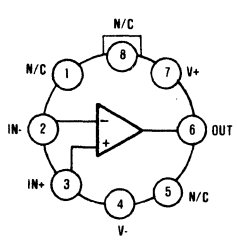
HA3-5142 (PLASTIC MINI-DIP)
HA7-5142 (CERAMIC MINI-DIP)



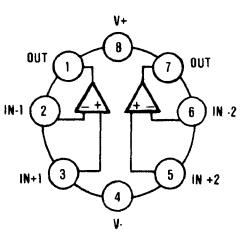
HA1-5144 (CERAMIC DIP)
HA3-5144 (PLASTIC DIP)



HA2-5141 (TO-99 METAL CAN)



HA2-5142 (TO-99 METAL CAN)



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HA-5147

Ultra-Low Noise Precision High Slew Rate Wideband Operational Amplifier

Features

- High Speed 35V/μs
- Wide Gain Bandwidth ($A_V \geq 10$)..... 120 MHz
- Low Noise ..... 3 nV/$\sqrt{Hz}$ at 1 KHz
- Low V_{OS} 10μV
- High CMRR ..... 126 dB
- High Gain 1800V/mV

Applications

- High Speed Signal Conditioners
- Wide Bandwidth Instrumentation Amplifiers
- Low Level Transducer Amplifiers
- Fast, Low Level Voltage Comparators
- Highest Quality Audio Preamplifiers
- Pulse/RF Amplifiers

Description

The HA-5147 monolithic operational amplifier features an unparalleled combination of precision DC and wideband high speed characteristics. Utilizing the Harris D. I. technology and advanced processing techniques, this unique design unites low noise (3 nV/$\sqrt{Hz}$) precision instrumentation performance with high speed (35V/μs) wideband capability.

This amplifier's impressive list of features include low V_{OS} (10 μV), wide gain-bandwidth (120 MHz), high open loop gain (1800V/mV), and high CMRR (126 dB). Additionally, this flexible device operates over a wide supply range (±5V to ±20V) while consuming only 140 mW of power.

Using the HA-5147 allows designers to minimize errors while maximizing speed and bandwidth in applications requiring gains greater than ten.

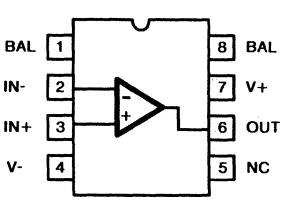
This device is ideally suited for low level transducer signal amplifier circuits. Other applications which can utilize the HA-5147's qualities include instrumentation amplifiers, pulse or RF amplifiers, audio preamplifiers, and signal conditioning circuits. Further application ideas are given in Application Note 553.

This device can easily be used as a design enhancement by directly replacing the 725, OP25, OP06, OP07, OP27 and OP37 where gains are greater than ten. The HA-5147 is available in TO-99 Metal Can and Ceramic 8 pin Mini-DIPs. For military grade product, refer to the HA-5147/883 data sheet.

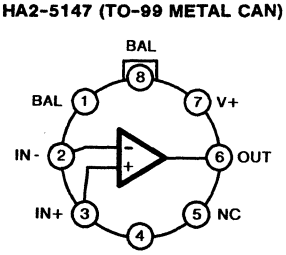
Pinouts

TOP VIEWS

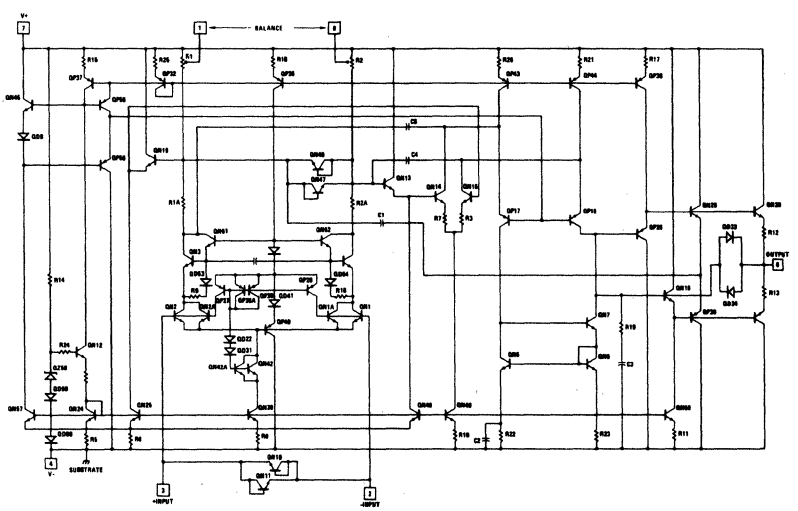
HA7-5147 (CERAMIC MINI-DIP)



HA2-5147 (TO-99 METAL CAN)



Schematic



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HARRIS SEMICONDUCTOR

HA-5151/52/54

Single/Dual/Quad Low Power Operational Amplifiers

Features

- Low Supply Current ..... < 200μA/Amplifier
- Dual Supply Voltage Range ..... ±1.5V to ±15V
- Single Supply Voltage Range ..... 3V to 30V
- High Slew Rate 6V/μs
- Low V_{OS} Drift ..... 3μV/°C
- Low Noise ..... 15nV/$\sqrt{Hz}$
- Dielectric Isolation

Applications

- Portable Instruments
- Meter Amplifiers
- Telephone Headsets
- Microphone Amplifiers
- Remote Sensor/Transmitter
- Battery Powered Equipment
- For Further Design Ideas See App. Note 544.

Description

The HA-5151/52/54 series is a group of dielectrically isolated bipolar amplifiers designed to provide excellent AC performance while drawing less than 200μA of supply current per amplifier. These unity gain stable amplifiers are especially well suited for portable and lightweight equipment where available power is limited.

The HA-5151/52/54 series combines superior low power AC performance with DC precision not usually found in general purpose amplifiers. The DC performance is centered around low input offset voltage (0.5mV), low offset voltage drift (3μV/°C), and low input bias current (70nA). This is combined with a very low input noise voltage of 15nV/$\sqrt{Hz}$ at 1kHz.

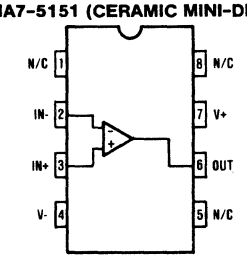
The AC performance of the HA-5151/52/54 series surpasses that of typical low power amplifiers with 6V/μs slew rate and a full power bandwidth of 95kHZ. This makes the HA-5151/52/54 series an excellent choice for virtually all audio processing applications as well as remote sensor/transmitter designs requiring both low power and high speed. The suitability of the HA-5151/52/54 series for remote and low power operation is further enchaced by the wide range of supply voltages (±1.5V to ±15V) as well as single supply operation (3V to 30V). These parts are also tested and guaranteed at both ±15 and single ended +5V supplies.

These amplifiers are available in singles (HA-5151, Can or Mini-DIP), duals (HA-5152, Can or Mini-DIP) or quads (HA-5154, 14 pin DIP), as well as over both the commercial (0°C to +75°C) and military (-55°C to +125°C) temperature ranges. These amplifiers also carry industry standard pinouts which allow the HA-5151/52/54's to be interchangeable with most other operational amplifiers. For military grade product refer to the HA-5151, 5152, 5154/883 data sheets.

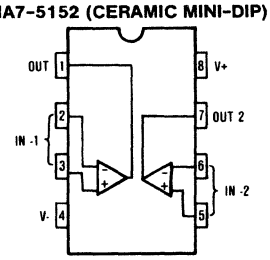
Pinouts

TOP VIEWS

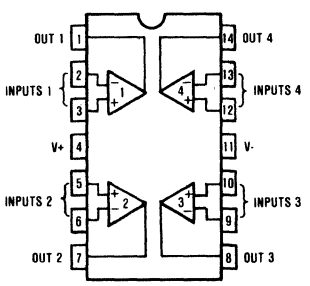
HA3-5151 (PLASTIC MINI-DIP)
HA7-5151 (CERAMIC MINI-DIP)



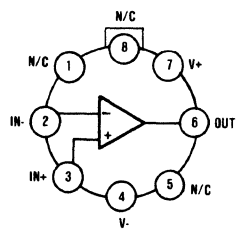
HA3-5152 (PLASTIC MINI-DIP)
HA7-5152 (CERAMIC MINI-DIP)



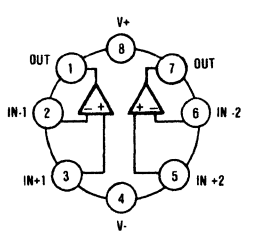
HA1-5154 (CERAMIC DIP)
HA3-5154 (PLASTIC DIP)



HA2-5151 (TO-99 METAL CAN)



HA2-5152 (TO-99 METAL CAN)



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HA-5330

Very High Speed Precision Monolithic Sample and Hold

Features

- Very Fast Acquisition.....350ns (0.1%)
  500ns (0.01%)
- Low Droop Rate 0.01μV/μs
- Very Low Offset.....0.2mV
- High Slew Rate 90V/μs
- Wide Supply Range..... ±11V to ±18V
- Internal Hold Capacitor
- Fully Differential Input
- TTL/CMOS Compatible

Applications

- Precision Data Acquisition Systems
- D/A Converter Deglitching
- Auto-Zero Circuits
- Peak Detectors

Description

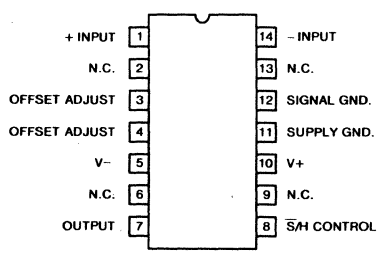
The HA-5330 is a very fast sample and hold amplifier designed primarily for use with high speed A/D converters. It utilizes the Harris Dielectric Isolation process to achieve a 500ns acquisition time to 12-bit accuracy and a droop rate of 0.01μV/μs. The circuit consists of an input transconductance amplifier capable of producting large amounts of charging current, a low leakage analog switch, and an integrating output stage which includes a 90pF hold capacitor.

The analog switch operates into a virtual ground, so charge injection on the hold capacitor is constant and independent of V_{IN}. Charge injection is held to a low value by compensation circuits and, if necessary, the resulting 0.5mV hold step error can be adjusted to zero via the Offset Adjust terminals. Compensation is also used to minimize leakage currents which cause voltage droop in the Hold mode.

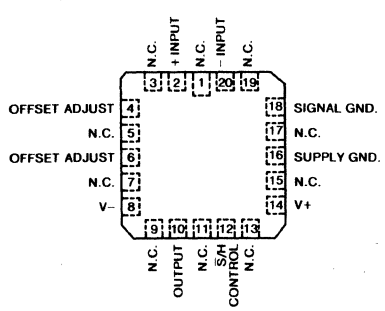
The HA-5330 will operate at reduced supply voltages (to ±11V) with a reduced signal range. This monolithic device is available in a 14 pin Ceramic DIP and a 20 pad LCC package. The MIL-STD-883 data sheet for this device is available on request.

Pinouts

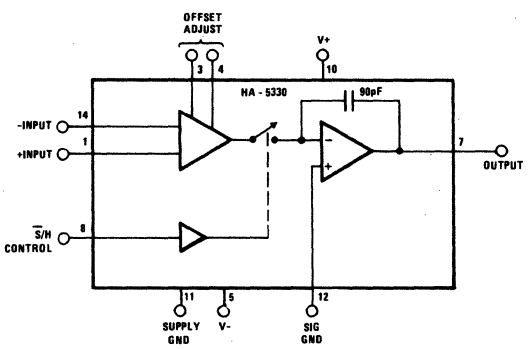
14 PIN CERAMIC DIP
TOP VIEW



20 PAD (LCC)
TOP VIEW



Functional Diagram



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Harris Semiconductor

GaAs FET PRODUCTS

Products And Services	GaAs FET Products
Gallium Arsenide-based standard and custom products are available from Harris Microwave Semiconductor (HMS), located in Milpitas, CA. Standard products include: 1. GaAs Field Effect Transistors (GaAs FETs) for RF and microwave applications. 2. GaAs Monolithic Microwave Integrated Circuits (MMICs) for broadband amplification of RF and microwave signals in receive, transmit, and IF stage applications. Custom design and fabrication services are available whereby customers can design or specify specialized MMIC or FET products for manufacture at HMS. Analysis, testing, packaging, and screening options are available for all standard and custom products.	Microwave GaAs FETs from Harris Microwave Semiconductor have been designed and built for performance, reliability and consistency. To achieve these objectives, Harris employs extremely low defect gallium arsenide substrates of its own manufacture, ion implantation, a Ti/Pt/Au metallization system, large cross-section "T" gate structure and integral dielectric scratch and short circuit protection. Each wafer undergoes an extensive reliability and performance qualification procedure exceeding the element evaluation requirements of MIL-STD-883C, Method 5008, Class B. Each die is DC tested and visually inspected prior to packaging and shipment. To accommodate specialized requirements, Harris can provide selections tailored to meet these needs. High-reliability screening and qualification testing are available on all Harris GaAs FET Products.

HIGH GAIN FET PRODUCTS

P/N HMF-	MAG* (dB)		P_{MAG} (dBm)	G_{1dB} (dB)	P_{1dB}* (dBm)		FREQ (GHz)	BIAS V_{DS}.I_{DS}	APPLICATION/ DESCRIPTION
	MIN	TYP			MIN	TYP			
03100-100	6.0	7.5	11	4.5	13	15	18	4 V, 20 mA	2-20 GHz Low Noise
03100-200	6.0	7.5	13.5	4.5	18	19	18	6 V, 50% I_{DSS}	2.20 GHz Gain/Drive
03100-300	6.0	7.5	14.5	4.5	20	21	18	6 V, 50% I_{DSS}	2-20 GHz Drive
0330	—	7.5	13.5	5.0	—	14	18	4 V, 20 mA	2-20 GHz Low Noise, Low Current
0610	5.0	6.0	19.5	4.0	21.5	23.5	18	6 V, 50% I_{DSS}	2-20 GHz Power
0620	—	10	17	7.0	—	20	12	4 V, 50% I_{DSS}	2-14 GHz High Transconductance
1210	—	6.0	22	4.0	—	25	18	6 V, 50% I_{DSS}	2-20 GHz Power

For other Harris Semiconductor products see pages 2637-2688

HIGH POWER FET PRODUCTS

P/N HMF-	G_{1dB} (dB)	P_{1dB}* (dBm)		η (%)	FREQ (GHz)	MAG* (dB)		P_{MAG} (dBm)	FREQ (GHz)	BIAS V_{DS}, I_{DS}	APPLICATION/ DESCRIPTION
		MIN	TYP			MIN	TYP				
0300	8.5	—	21.5	35	8	—	12	18	8	8 V, 50% I_{DSS}	2-18 GHz, 125 mW
0600	8	—	24.5	35	8	—	10	22	8	8 V, 50% I_{DSS}	2-18 GHz, 250 mW
12000-100	7.5	25.5	27	30	8	9	10	25.0	8	8 V, 50% I_{DSS}	2-16 GHz, 500 mW
12000-200	7.5	27.5	28.5	35	8	8	9	25.5	8	8 V, 50% I_{DSS}	2-16 GHz, 650 mW
24000-100	5.0	28.5	29.5	25	8	6.0	8.0	27.0	8	8 V, 50% I_{DSS}	2-14 GHz, 800 mW
24000-200	5.0	30.0	31.0	30	8	6.0	8.0	28.5	8	8 V, 50% I_{DSS}	2-14 GHz, 1.2 mW

*Compliance with microwave performance limits for MAG and P1dB is confirmed by qualifying wafers on sample evaluation basis.

GaAs MMIC STANDARD PRODUCTS

HMM Series

Our half-micron (gate length) family of fully integrated MMIC amplifiers is intended for broadband applications where noise figure, gain or output power are key specifications in a system design.

HMM Product Family — Electrical Specifictions

Model No.	Frequency Band (GHz)	Small Signal Gain (dB)		Gain Flatness (Over full BW) (dB) Max	1dB Gain Compression Output Power (dBm) Typ	Noise Figure (dB) Typ	VSWR	
		Min	Typ					Max
HMM-10610 HMM-10620	2 — 6 2 — 6 (Low Current)	10	12 11.5	± .5	+ 19 + 13	6 5.5	Input Output	2:1 1.75:1 1.75:1
HMM-11810 HMM-11820	6 — 18 6 — 18 (Low Current)	4.5	5 5	± .75	+ 16.5 + 12	6.5 5.5	Input Output	2:1 2:1 2:1

V_{DD} = 5V, I_{DD} = 120 mA (typical/HMM-10610)/ 100 mA (typical/HMM-11810)

HMR Series

For lower frequency application, specify the Harris HMR one-micron (gate length) MMIC family. Distributed as gain blocks throughout your system, they often permit relaxing the specifications of other cost-critical components.

HMR Product Family — Electrical Specifictions

Model No.	Frequency Band (GHz)	Small Signal Gain (dB) Typ	Gain Flatness (Over full BW) (dB) Max	1dB Gain Compression Output Power (dBm) Typ	Noise Figure (dB) Typ	VSWR Typ	VSWR Max
HMR-10502	0.5 — 5	9.5	± .75	+ 10	7	1.7:1	2:1
HMR-10503	1 — 5	9.5	± .75	+ 10	7	1.7:1	2:1

V_{DD} = 10V, I_{DD} = 100 mA

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GaAs Custom MMIC Programs

Custom and Fabrication Services

KEY FEATURES

- Fully Documented Design Rule Book Includes Microwave and Physical Layout Rules
- 0.5 Micron Plated "T"-Gate Technology Based Upon Our Line of Discrete FETs (HMF-0310, -0610, etc.)
- Reliable Ti/Pt/Au Metallization
- Ion Implantation Processing for Uniformity, Consistency
- Circuit Elements
  - "n+" Type (Low Sheet RHO) Resistors
  - "n" Type (High Sheet RHO) Resistors
  - Diodes
  - FETs
  - Dual Gate FETs
  - Transmission Lines
  - Inductors
  - Capacitors
  - Through Substrate Via Holes

MMIC PROGRAM OPTIONS

- Gain, Power or Low Current FET Models and Processing
- Circuit Design from Customer Specs
- "Layout" from Customer-Supplied Design
- Computer Simulation of Design
- Generation of Digitized Data From Customer Drawing
- RF Screening of Selected Parts *(i.e., #/Wafer)*
- Special Packaging/Assembly
- Specialized DC Testing
- Volume Quotations on Qualified Wafers
- High Reliability Screening
- Supplementary Consultation/Training

TABLE 2. PROCESSES FOR CUSTOM MMICs

PROCESS TYPE (GATE LENGTH)	PRATICAL OPERATING FREQUENCIES	f_t	f_{max}	PROCESS OPTIONS
0.5 Micron	0.5 to 20 GHz	18 GHz	40 GHz	High Gain, Low Current High Power
1.0 Micron	0.1 to 12 GHz	12 GHz	26 GHz	High Gain

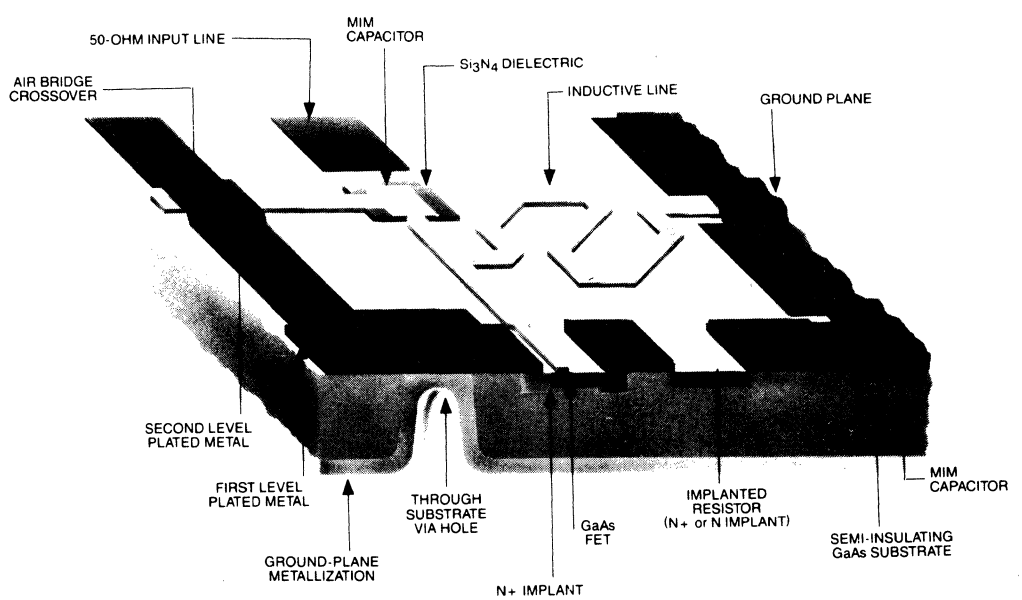

FIGURE 2. FEATURES OF A TYPICAL MMIC CHIP

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Harris Semiconductor

HOLT INC.
INTEGRATED CIRCUITS

STANDARD PRODUCTS

HI-8010/8020

HIGH VOLTAGE DISPLAY DRIVER

- The HI-8010/8020 devices are 35 volt High Voltage dichroic display drivers with internally generated backplane drive. These devices allow easy interface to 5 volt logic systems. The chip can drive 30-38 LCD segments and requires minimal display-to-data source interfacing. Data is loaded serially and held in internal latches until new data is received. The backplane is controlled either by an external RC network or by an external squarewave. The devices are easily cascadable and run at 2 MHz. Holt offers a large selection of packages for both military and industrial applications. The HI-8020 is pin-for-pin compatible with the AMI 4520 series display drivers.

HI-8182/8282

ARINC 429 BUS INTERFACE RECEIVER/TRANSMITTER

- The HI-8182 is a CMOS device compatible with the ARINC specification 429, 32 bit word, digital data protocol. The low power device consists of two data receivers and one data transmitter with on-chip line driver circuitry. Operating at 100 Kbits/sec. or 12.5 Kbits/sec., each independent, double buffered, receiver section can perform serial to parallel data conversion in conjunction with parallel to serial data conversion in its FIFO transmitter section. The HI-8282 device is similar to the HI-8182 with the exception of the elimination of the on-chip transmitter line driver, which makes the device pin compatible with the Harris 3282 device. Both the HI-8182 and the HI-8282 are available in ceramic and plastic packages as well as operation over commercial and military temperature ranges.

Holt Integrated Circuits

HI-8504

QUAD INVERTING HIGH VOLTAGE UP/DOWN LEVEL SHIFTER

- The HI-8504 is a low power CMOS device capable of converting from one voltage swing to another (higher or lower) while accommodating high absolute voltages up to 35 volts. A typical application is the conversion from 5 volt logic (TTL) to ±15 volts or vise versa. The translation and direction is easily controlled by the application of the appropriate reference levels to the device. The HI-8504 is available in 14 pin packages and over both commercial and military temperature ranges.

HI-8573/8574/8575

GENERAL PURPOSE OP AMP/COMPARATOR

- The HI-8573/8574/8575 series devices are pin-for-pin compatible with the Motorola MC14573/MC14574/MC14575 op amp/comparator chips. These devices provide selectable bias currents for trading off power consumption against slew rate. The CMOS technology enables extremely high input resistance and picoamp range input bias currents. These devices are internally compensated.

FOUNDRY SERVICES

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HOLT INTEGRATED CIRCUITS
9351 Jeronimo Road, Irvine, CA 92718
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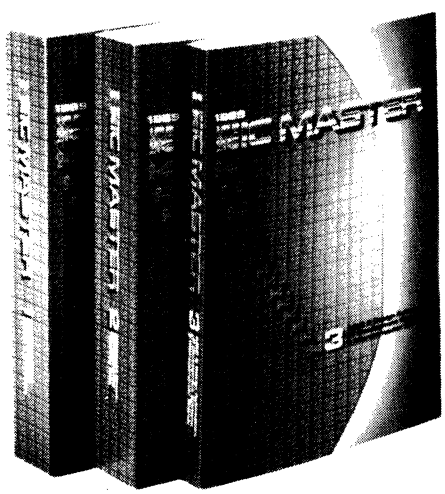
Can an engineer find out who makes a 256K dynamic RAM with an access time of 120 nanoseconds or faster in less than 30 seconds? He can if he turns to the Memory section of IC MASTER and looks for the 256K organization (words and bits per word) that he needs. Because each device is listed in order of access time, he can easily determine the devices that satisfy his speed requirements.



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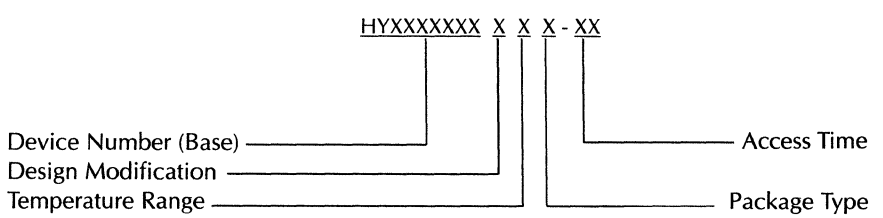
HYUNDAI SEMICONDUCTOR

PRODUCT SELECTION GUIDE

DEVICE	PART NUMBER	DESCRIPTION	PACKAGE TYPE				ACCESS TIME
			S	P	F	J	
DRAM	HY51C64X-10/12/15	64K X 1 CMOS	•				100/120/150
	HY51C64LX-10/12/15	64K X 1 CMOS, LOW POWER	•				100/120/150
	HY5164X-10/12/15	64K X 1	•				100/120/150
	HY51C256X-10/12/15/20	256K X 1 CMOS	•				100/120/150/200
	HY51C256LX-10/12/15/20	256K X 1 CMOS, LOW POWER	•				100/120/150/200
	HY51256X-10/12/15/20	256K X 1	•				100/120/150/200
	HY53C256X-70/80/10/12	256K X 1 CMOS	•		•		70/80/100/120
	HY53C256LX-70/80/10/12	256K X 1 CMOS, LOW POWER	•		•		70/80/100/120
	HY53C464X-70/80/10/12	64K X 4 CMOS	•		•		70/80/100/120
	HY53C464LX-70/80/10/12	64K X 4 CMOS, LOW POWER	•		•		70/80/100/120
	HY51C1000X-70/80/10/12	1M X 1 CMOS	•				80/100/120/150
	HY51C1000LX-70/80/10/12	1M X 1 CMOS, LOW POWER	•				80/100/120/150
	HY51C1002X-70/80/10/12	1M X 1 CMOS	•				80/100/120/150
	HY51C1002LX-70/80/10/12	1M X 1 CMOS, LOW POWER	•				80/100/120/150
	HY51C4256X-80/10/12/15	256K X 4 CMOS	•				80/100/120/150
	HY51C4256LX-80/10/12/15	256K X 4 CMOS, LOW POWER	•				80/100/120/150
	HY51C4258X-80/10/12/15	256K X 4 CMOS	•				80/100/120/150
	HY51C4258LX-80/10/12/15	256K X 4 CMOS, LOW POWER	•				80/100/120/150
SRAM	HY6116AX-10/12/15	2K X 8		•			85/100/120/150
	HY6116ALX-10/12/15	2K X 8, LOW POWER		•			85/100/120/150
	HY6264X-85/10/12/15	8K X 8		•		•	85/100/120/150
	HY6264LX-85/10/12/15	8K X 8, LOW POWER		•		•	85/100/120/150
	HY62C256X-80/10/12/15	32K X 8 CMOS		•		•	80/100/120/150
	HY62C256LX-80/10/12/15	32K X 8 CMOS, LOW POWER		•		•	80/100/120/150
	HY63C256X-35/45/55	32K X 8 CMOS, HI SPEED		•			35/45/55
	HY63C256LX-35/45/55	32K X 8 CMOS, HI SPEED, LOW POWER		•			35/45/55
EEPROM	HY93C46X	64 X 16 CMOS (SERIAL ACCESS)		•		•	
EEPLD	HY18CV8	20 PIN PLD REPLACEMENT		•			

NOTES:

1. 'X' is the package type
2. If you want any package type other than listed above, contact our sales office or representative nearest you.



TEMP RANGE-OPERATION

NO MARK: 0° C TO +70° C, STD PWR
L 0° C TO +70° C, LOW PWR
E: −40° C TO +85° C, STD PWR

PACKAGE TYPE

PLASTIC DIP 300 MIL : S
600 MIL : P
LCC J-FORM : F
SOIC : J

DESIGN MODIFICATION

NO MARK : NONE
A : FIRST
B : SECOND
C : THIRD

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IMS C004 programmable link switch

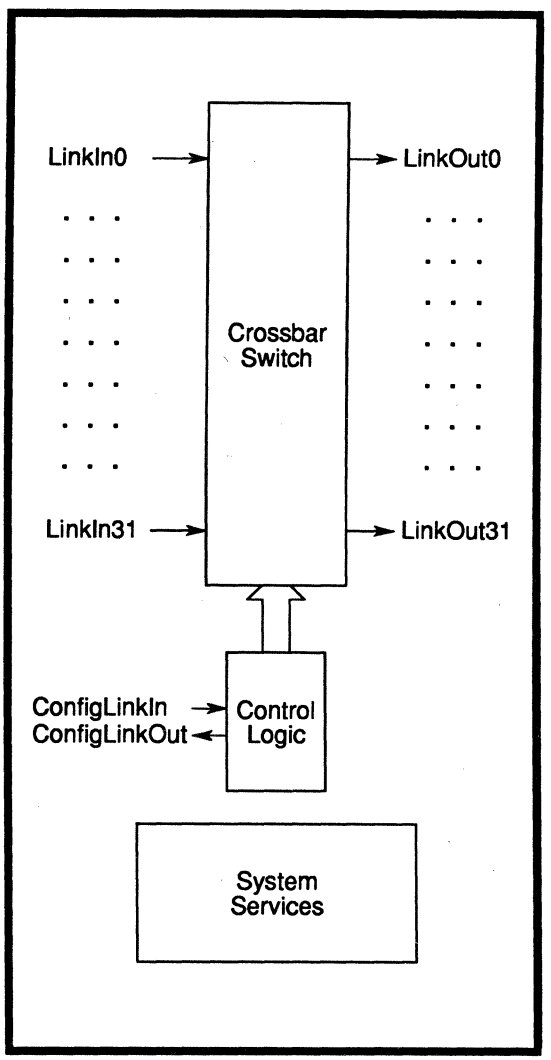
Engineering Data

FEATURES

Standard INMOS serial links
32 way crossbar switch
Regenerates input signal
Cascadable to any depth
No loss of signal integrity
10 or 20 Mbits/sec operating speed
Separate INMOS configuration link
Single +5V ±5% power supply
TTL and CMOS compatibility
1W power dissipation
Standard 84 pin ceramic PGA
MIL-STD-883C device will be available

APPLICATIONS

Programmable crossbar switch
Component of larger switch
Reconfigurable supercomputers
Message routing system
High speed multiprocessor systems
Telecommunications
Robotics
Fault tolerant systems
Additional links for transputers



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IMSC011 link adaptor

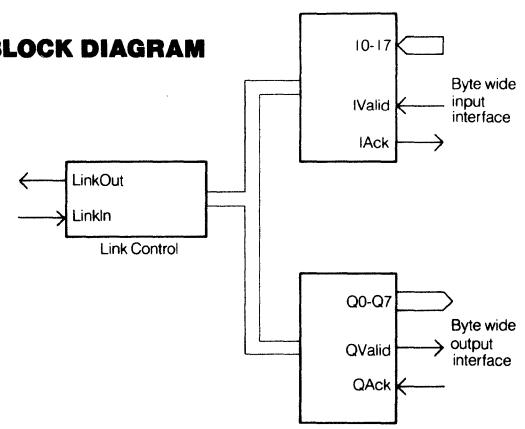
FEATURES

- High performance system interconnect
- Bi-directional handshaken byte-wide interface
- INMOS serial link
- 10 or 20 Mbits/sec data rate
- Interrupt control for microprocessor buses
- Two configuration options
- Advanced 1.5 micron CMOS technology
- Standard 600 mil 28 pin DIP

APPLICATIONS

- Programmable I/O pins for a transputer
- Link between transputers running at different clock frequencies
- Interface between transputers and industry standard peripherals
- High performance handshaken link between standard microprocessor buses

BLOCK DIAGRAM



IMSC012 link adaptor

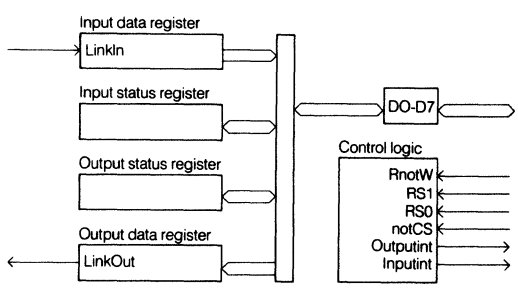
FEATURES

- High performance system interconnect
- Bi-directional handshaken byte-wide interface
- INMOS serial link
- 10 or 20 Mbits/sec data rate
- Interrupt control for microprocessor buses
- Advanced 1.5 micron CMOS technology
- Standard 300 mil 24 pin DIP

APPLICATIONS

- Interface between transputers and industry standard peripherals
- High performance handshaken link between standard microprocessor buses

BLOCK DIAGRAM



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IMS T222
transputer

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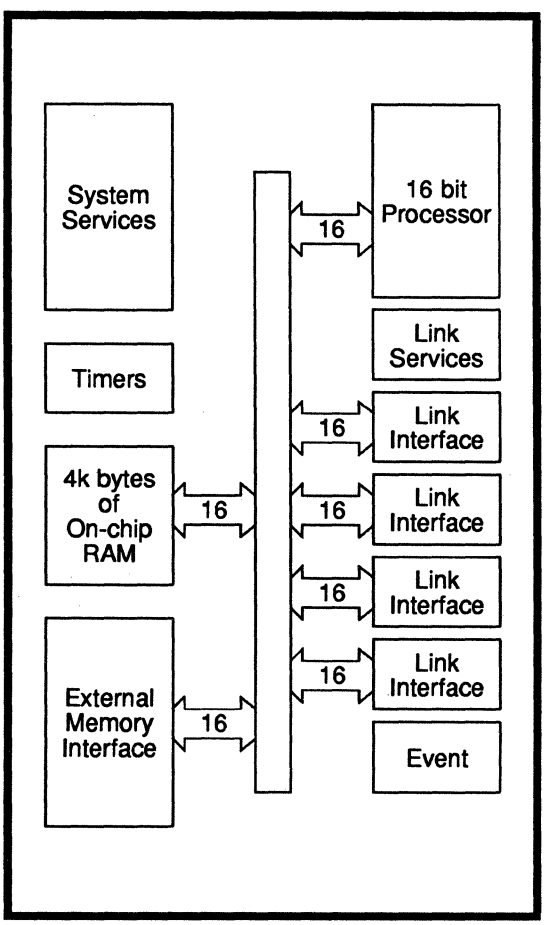
Engineering Data

FEATURES

16 bit architecture
50 ns internal cycle time
20 MIPS (peak) instruction rate
Pin compatible with IMS T212
4 Kbytes on-chip static RAM
80 Mbytes/sec sustained data rate to internal memory
64 Kbytes directly addressable external memory
20 Mbytes/sec sustained data rate to external memory
950 ns response to interrupts
Four INMOS serial links 5/10/20 Mbits/sec
Bi-directional data rate of 2.4 Mbytes/sec per link
Internal timers of 1 μs and 64 μs
Boot from ROM or communication links
Single 5 MHz clock input
Single +5V ±5% power supply
MIL-STD-883C processing will be available

APPLICATIONS

Real time processing
Microprocessor applications
High speed multi processor systems
Industrial control
Robotics
System simulation
Digital signal processing
Telecommunications
Fault tolerant systems
Medical instrumentation



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IMS T425
transputer

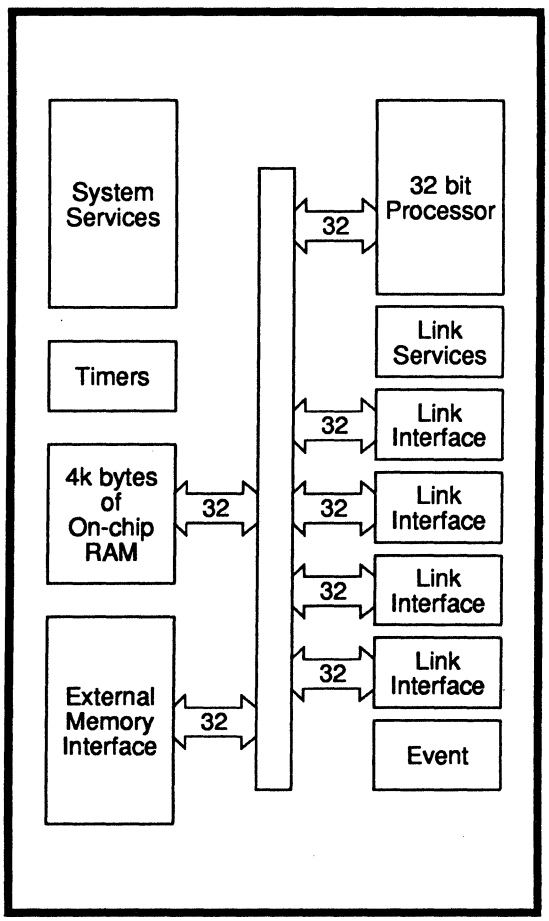
Advance Data

FEATURES

32 bit architecture
33 ns internal cycle time
30 MIPS (peak) instruction rate
Pin compatible with IMS T800 and IMS T425
4 Kbytes on-chip static RAM
120 Mbytes/sec sustained data rate to internal memory
4 Gbytes directly addressable external memory
40 Mbytes/sec sustained data rate to external memory
630 ns response to interrupts
Four INMOS serial links 5/10/20 Mbits/sec
High performance graphics support with block move instructions
Boot from ROM or communication links
Single 5 MHz clock input
Single +5V ±5% power supply
MIL-STD-883C processing will be available

APPLICATIONS

High speed multi processor systems
High performance graphics processing
Supercomputers
Workstations and workstation clusters
Digital signal processing
Accelerator processors
Distributed databases
System simulation
Telecommunications
Robotics
Fault tolerant systems
Image processing
Pattern recognition
Artificial intelligence



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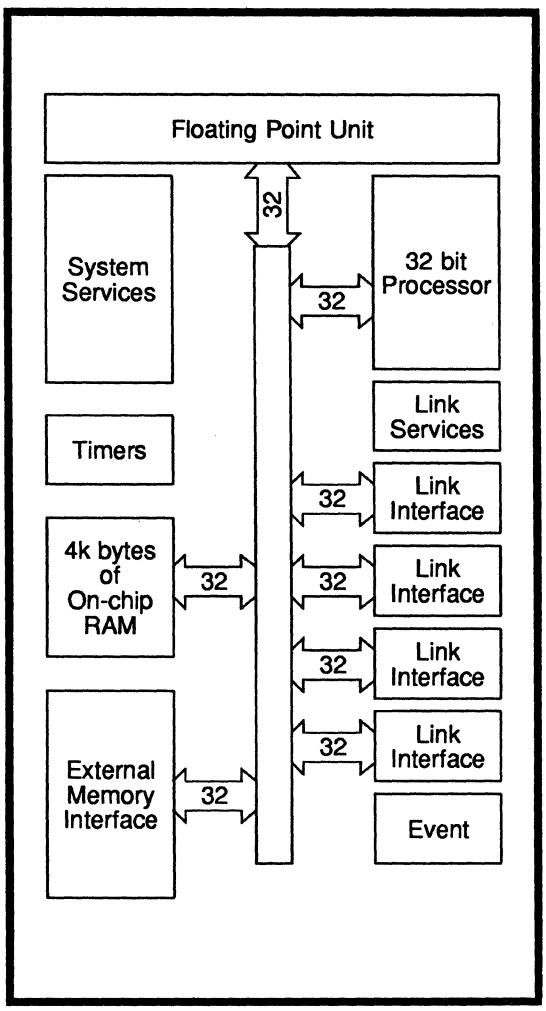
IMS T800
transputer

inmos®

Engineering Data

FEATURES

32 bit architecture
33 ns internal cycle time
30 MIPS (peak) instruction rate
4.3 Mflops (peak) instruction rate
64 bit on-chip floating point unit which conforms to IEEE 754
4 Kbytes on-chip static RAM
120 Mbytes/sec sustained data rate to internal memory
4 Gbytes directly addressable external memory
40 Mbytes/sec sustained data rate to external memory
630 ns response to interrupts
Four INMOS serial links 5/10/20 Mbits/sec
Bi-directional data rate of 2.4 Mbytes/sec per link
High performance graphics support with block move instructions
Boot from ROM or communication links
Single 5 MHz clock input
Single +5V ±5% power supply
MIL-STD-883C processing will be available



APPLICATIONS

Scientific and mathematical applications
High speed multi processor systems
High performance graphics processing
Supercomputers
Workstations and workstation clusters
Digital signal processing
Accelerator processors
Distributed databases
System simulation
Telecommunications
Robotics
Fault tolerant systems
Image processing
Pattern recognition
Artificial intelligence

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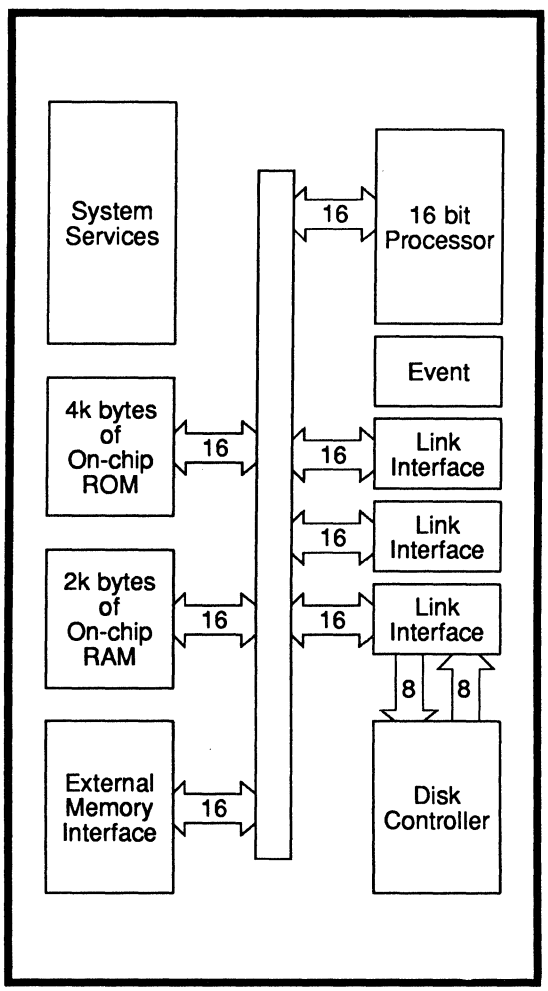
IMS M212 disk processor

Product Preview

FEATURES

ST506/ST412, SA400/450 compatible interface
Full disk interface logic on chip
Minimum of external components required
On-chip 16 bit processor
2 Kbytes on-chip RAM
4 Kbytes on-chip ROM disk control software
External memory interface
Hardware CRC/ECC generator
Two bi-directional 8 bit data ports
Two 10/20 Mbits/sec INMOS serial links
External event interrupt
Variable wait states for slow memory
Internal timers
Support for run-time error diagnostics
Bootstraps from ROM, link or disk
Single 5 MHz processor clock input
Power dissipation less than 1 Watt



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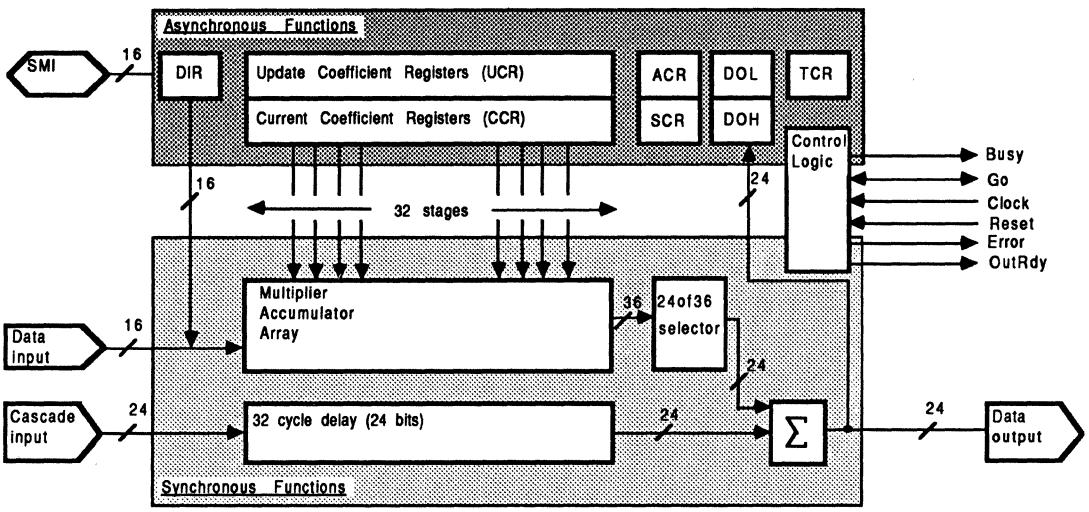
IMS A100
Cascadable signal processor

Advance information



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FEATURES

- Full 16 bit, 32 stage, multiply accumulator.
- Fully cascadable with no speed degradation or reduction in dynamic range.
- Coefficients selectable as 4, 8, 12, or 16 bits wide
- Data throughput to 10 MHz
- High speed microprocessor compatible interface.
- Data input and output through dedicated ports or via the microprocessor interface
- Fully static high speed CMOS implementation
- TTL compatible
- Single +5V ±10 % power supply
- Power dissipation < 1.5 Watts
- Standard 84-pin chip carrier

APPLICATIONS

- Digital FIR filtering up to 10 MHz sample rates
- High speed adaptive filtering
- Correlation and Convolution
- Discrete Fourier Transform
- Speech processing using Linear Predictive Coding
- Image processing
- Waveform synthesis
- Adaptive and fixed equalizers and echo cancellers
- Spread spectrum communication
- Beamforming and beamscanning in sonar and radar
- Pulse compression
- High speed fixed point matrix multiplication

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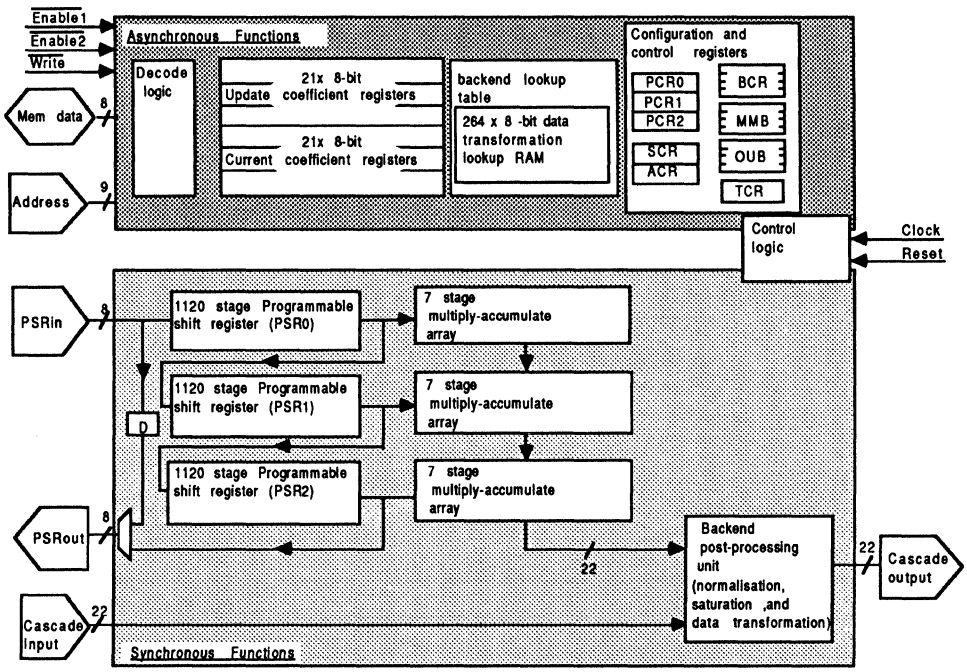
IMS A110

Image and signal processing sub-system

Advance information



FEATURES

- 1-D/2-D software configurable convolver/filter
- On-chip programmable line delays (0 – 1120 stages)
- 8-bit data and 8-bit coefficient slice
- 21 multiply-and-accumulate stages
- 1-D (21) or 2-D (3x7) convolution window
- On-chip post processor for data transformation
- Fully cascadable in window size and accuracy
- 20-MHz data throughput (420 MOPs)
- Microprocessor interface
- Fully static high speed CMOS implementation
- TTL compatible
- Single +5V ±10% Supply
- Power dissipation < 2.0 Watts
- 100-pin ceramic PGA

APPLICATIONS

- 1-D and 2-D digital convolution and correlation
- Real time image processing and enhancement
- Edge and feature detection
- Data transformation and histogram equalisation
- Computer vision and robotics
- Template matching
- Pulse compression
- 1-D or 2-D interpolation

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Inmos

IMS1203

CMOS High Performance 4K x 1 Static RAM

MIL-STD-883C Versions Available

inmos®

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FEATURES

- INMOS Very High Speed CMOS
- Advanced Process - 1.6 Micron Design Rules
- 4K x 1 Bit Organization
- 20, 25, 35 and 45 nsec Address Access Times
- 20, 25, 35 and 45 nsec Chip Enable Access Times
- Fully TTL Compatible
- Separate Data Input & Output
- Three-state Output
- 18-Pin, 300-mil DIP
- Single +5V ± 10% Operation
- Power Down Function

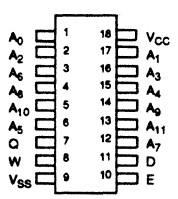
DESCRIPTION

The INMOS IMS1203 is a high performance 4K x 1 CMOS static RAM. The IMS1203 allows speed enhancements to existing 4K X 1 applications with the additional benefit of reduced power consumption.

The IMS1203 features fully static operation requiring no external clocks or timing strobes, and equal address access and cycle times. The IMS1203 provides a Chip Enable (/E) function that can be used to place the device into a low-power standby mode.

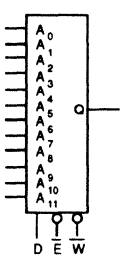
The IMS1203M is a MIL-STD-883 version intended for military applications that demand superior reliability and performance.

PIN CONFIGURATION

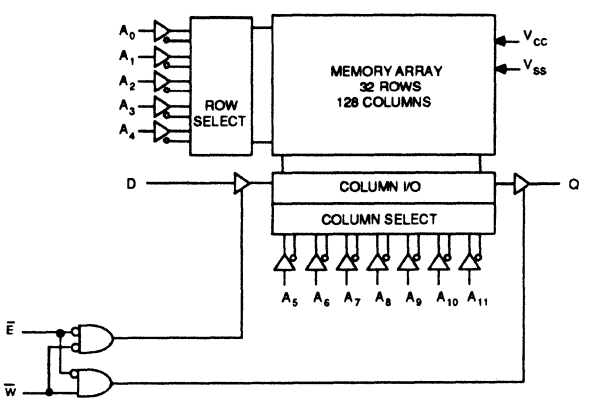


DIP

LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

$A_0 - A_{11}$	ADDRESS INPUTS	V_{CC}	POWER (+5V)
$\overline{W}$	WRITE ENABLE	V_{SS}	GROUND
D	DATA IN		
$\overline{E}$	CHIP ENABLE		
Q	DATA OUTPUT		

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INMOS Limited, 1000 Aztec West, Almondsbury, Bristol BS12 4SQ, England, (0454) 616616, TLX 851-444723

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IMS1223

CMOS High Performance 1K x 4 Static RAM

MIL-STD-883C Versions Available

FEATURES

- INMOS Very High Speed CMOS
- Advanced Process - 1.6 Micron Design Rules
- 1K x 4 Bit Organization
- 20, 25, 35 and 45 nsec Address Access Times
- 20, 25, 35 and 45 nsec Chip Enable Access Times
- Fully TTL Compatible
- Common Data Input & Output
- Three-state Output
- 18-Pin, 300-mil DIP
- Single +5V ± 10% Operation
- Power Down Function

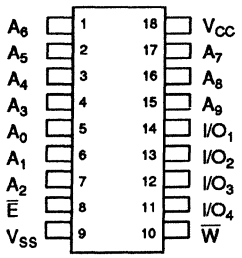
DESCRIPTION

The INMOS IMS1223 is a high performance 1K x 4 CMOS static RAM. The IMS1223 allows speed enhancements to existing 1K X 4 applications with the additional benefit of reduced power consumption.

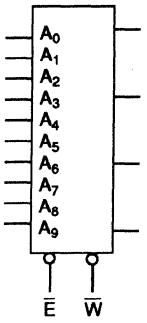
The IMS1223 features fully static operation requiring no external clocks or timing strobes, and equal address access and cycle times. The IMS1223 provides a Chip Enable (/E) function that can be used to place the device into a low-power standby mode.

The IMS1223M is a MIL-STD-883 version intended for military applications that demand superior reliability and performance.

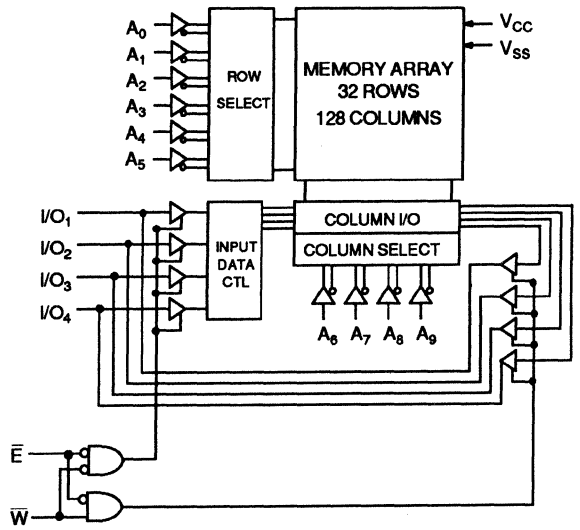
PIN CONFIGURATION



LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

A_0 - A_9	ADDRESS INPUTS	V_{CC}	POWER
$\overline{W}$	WRITE ENABLE	V_{SS}	GROUND
$\overline{E}$	CHIP ENABLE		
I/O	DATA IN/OUT		

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IMS1403
IMS1403L
CMOS
High Performance
16K x 1 Static RAM

MIL-STD-883C Versions Available

FEATURES

- INMOS Very High Speed CMOS
- Advanced Process - 1.6 Micron Design Rules
- 16K x 1 Bit Organization
- 25, 35, 45 and 55 nsec Access Times
- Fully TTL Compatible
- Separate Data Input & Output
- Three-state Output
- 20-Pin, 300-mil DIP (JEDEC Std.)
- 20-Pin Ceramic LCC (JEDEC Std.)
- Single +5V ± 10% Operation
- Power Down Function
- Pin Compatible with IMS1400
- Battery Backup Operation - 2V Data Retention (L version only)

DESCRIPTION

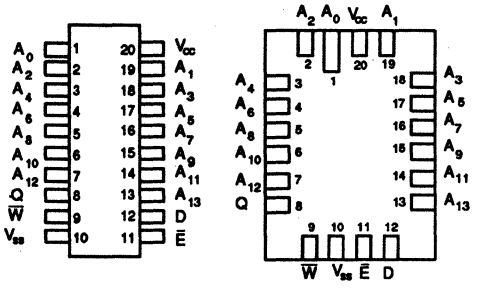
The INMOS IMS1403 is a high performance 16K x 1 CMOS static RAM. The IMS1403 provides maximum density and speed enhancements with the additional CMOS benefits of lower power and superior reliability.

The IMS1403 features fully static operation requiring no external clocks or timing strobes, and equal address access and cycle times. Additionally, the IMS1403 provides a Chip Enable (/E) function that can be used to place the device into a low-power standby mode.

The IMS1403L is a low power version offering battery backup data retention operating from a 2 volt supply.

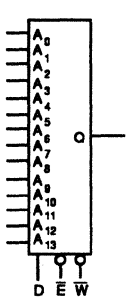
The IMS1403M and IMS1403LM are extended temperature versions for military applications.

PIN CONFIGURATION

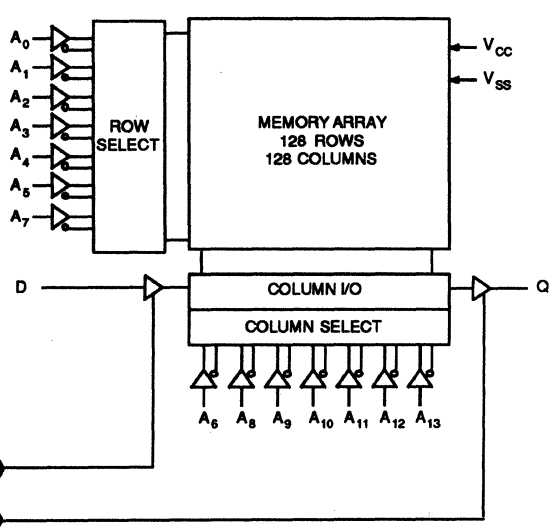


DIP CHIP CARRIER

LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

A_0 - A_{13}	ADDRESS INPUTS	Q	DATA OUTPUT
$\overline{W}$	WRITE ENABLE	V_{CC}	POWER
$\overline{E}$	CHIP ENABLE	V_{SS}	GROUND
D	DATA INPUT		

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IMS1423
CMOS
High Performance
4K x 4 Static RAM

MIL-STD-883C Versions Available

FEATURES

- INMOS' Very High Speed CMOS
- Advanced Process - 1.6 Micron Design Rules
- 4K x 4 Bit Organization
- 25, 35, 45 and 55 nsec Access Times
- Fully TTL Compatible
- Common Data Input & Output
- Three-state Output
- 20-Pin, 300-mil DIP (JEDEC Std.)
- 20-Pin Ceramic LCC (JEDEC Std.)
- Single +5V ± 10% Operation
- Power Down Function for Low Standby Power
- Pin Compatible with IMS1420

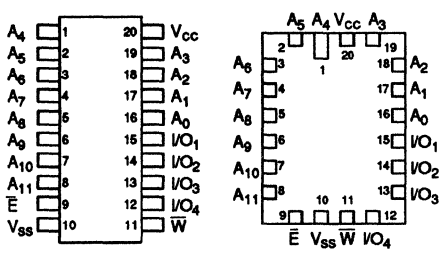
DESCRIPTION

The INMOS IMS1423 is a high performance 4K x 4 CMOS static RAM. The IMS1423 provides maximum density and speed enhancements with the additional CMOS benefits of lower power and superior reliability.

The IMS1423 features fully static operation requiring no external clocks or timing strobes, and equal address access and cycle times. Additionally, the IMS1423 provides a Chip Enable (/E) function that can be used to place the device into a low-power standby mode.

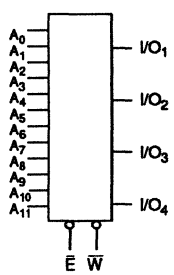
The IMS1423M is a MIL-STD-883 version intended for military applications that demand superior performance and reliability.

PIN CONFIGURATION

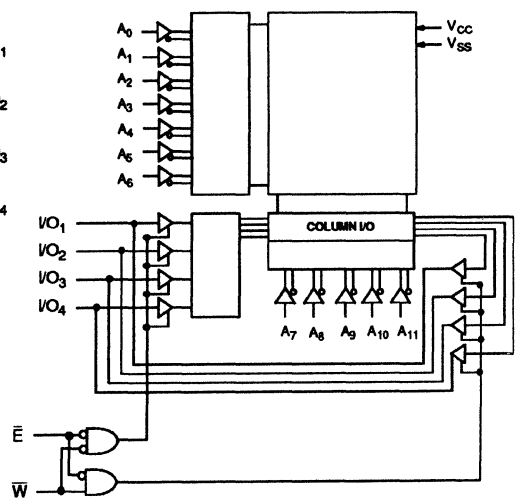


DIP CHIP CARRIER

LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

A_0 - A_{11}	ADDRESS INPUTS	V_{CC}	POWER
$\overline{W}$	WRITE ENABLE	V_{SS}	GROUND
$\overline{E}$	CHIP ENABLE		
I/O	DATA IN/OUT		

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IMS1600

High Performance 64K x 1 CMOS Static RAM

inmos®

MIL-STD-883C Versions Available

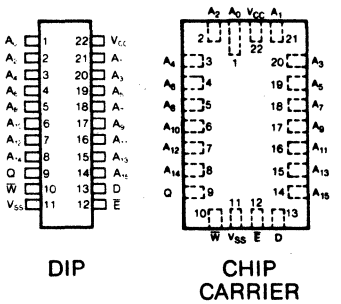
FEATURES

- INMOS Very High Speed CMOS Advanced Process—1.6 Micron Design Rules
- 64K x 1 Bit Organization
- 35, 45, 55 and 70nsec Address Access Times
- 35, 45, 55 and 70nsec Chip Enable Access Times
- Fully TTL Compatible
- Separate Data Input and Output
- Three-state Output
- 22-Pin, 300-mil DIP (JEDEC Standard Pinout)
- Single +5V ± 10% Operation
- Power Down Function

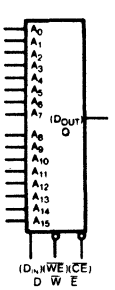
DESCRIPTION

The IMS1600 features fully static operation requiring no external clocks or timing strobes, and equal address access and cycle times. Additionally, the IMS1600 provides a Chip Enable ($\overline{E}$) function that can be used to place the device into a low-power standby mode, thus reducing power. By using stable CMOS levels, the standby power may be reduced to an even lower level.

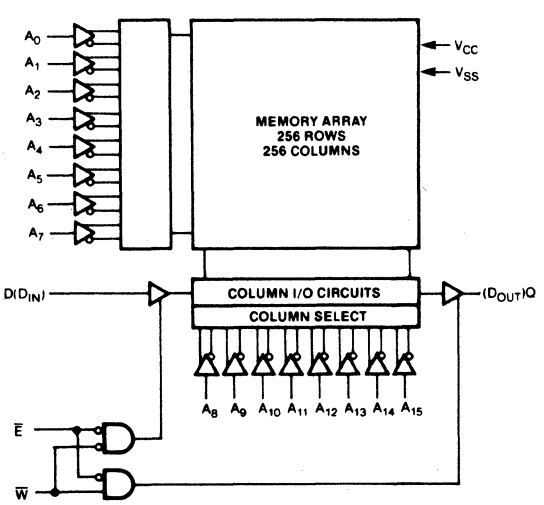
PIN CONFIGURATION



LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

A_0 - A_{15} ADDRESS INPUTS	V_{CC} POWER (+5V)
$\overline{W}$ WRITE ENABLE	
$\overline{E}$ CHIP ENABLE	
D DATA INPUT	
Q DATA OUTPUT	

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IMS1601L
CMOS Commercial Battery Backed 64K x 1 Static RAM

inmos®

MIL-STD-883C Versions Available

FEATURES

- INMOS Very High Speed CMOS
- Advanced Process—1.6 Micron Design Rules
- 64K x 1 Bit Organization
- 35, 45, 55 and 70nsec Address Access Times
- 35, 45, 55 and 70nsec Chip Enable Access Times
- Fully TTL Compatible
- Separate Data Input and Output
- Three-state Output
- 22 Pin, 300-mil DIP (JEDEC Standard Pinout)
- 22 Pin LCC (JEDEC Standard Pinout)
- Single +5V ± 10% Operation
- Power Down Function
- Data Retention to 2 volts

DESCRIPTION

The IMS1601L is a high performance 64K x 1 CMOS static RAM.

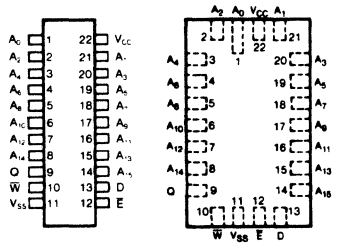
The IMS1601L features fully static operation requiring no external clocks or timing strobes, and equal address access and cycle times. Additionally, the IMS1601L provides a Chip Enable ($\overline{E}$) function that can be used to place the device into a low-power standby mode.

The IMS1601L also provides battery backup capability offering data retention from a 2 volt supply.

The IMS1601L extended temperature version is available for military applications.

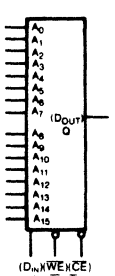
Inmos

PIN CONFIGURATION

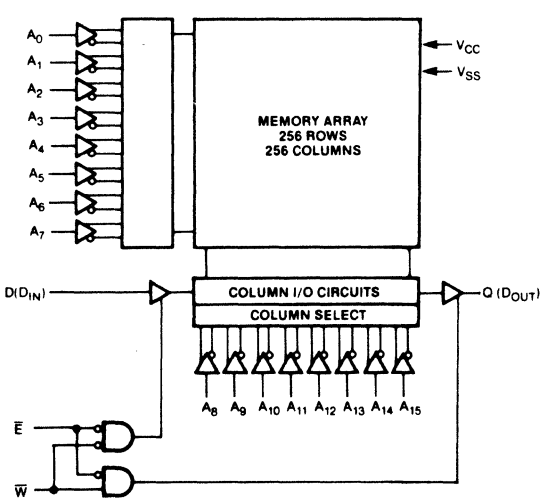


DIP CHIP CARRIER

LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

A_0 - A_{15}	ADDRESS INPUTS
$\overline{W}$	WRITE ENABLE
$\overline{E}$	CHIP ENABLE
D	DATA INPUT
Q	DATA OUTPUT
V_{CC}	POWER (+5V)

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IMS1620
IMS1620L
IMS1620A
CMOS
High Performance
16K x 4 Static RAM

MIL-STD-883C Versions Available

FEATURES

- INMOS Very High Speed CMOS
  - 1620A -1.2 Micron Design Rules
  - 1620/20L - 1.6 Micron Design Rules
- 16K x 4 Bit Organization
- 25, 35, 45, 55 and 70 nsec Access Times
- Fully TTL Compatible
- Common Data Inputs & Outputs
- Single +5V ± 10% Operation
- Power Down Function
- 22-Pin, 300-mil DIP
- 22 Pin LCC
- Battery Backup Operation 2V Data Retention (L Version Only)

DESCRIPTION

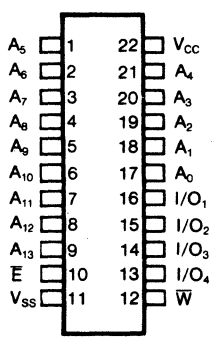
The IMS1620 is a high speed CMOS 16K x 4 Static RAM having access times of 25, 35, 45, 55 and 70ns. These characteristics are made possible by the combination of innovative circuit design and INMOS' proprietary CMOS technology.

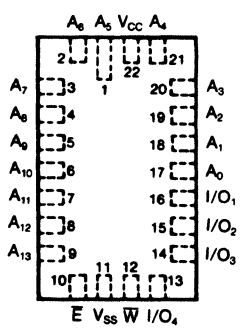
The IMS1620 features fully static operation requiring no external clocks or timing strobes. The IMS1620 is optimized for high speed system operation as well as providing increased reliability due to the CMOS process.

The low power version (IMS1620L) offers a battery backup data retention capability operating from a 2 volt battery.

The IMS1620 is available in JEDEC Standard 22-pin Plastic and Ceramic 300-mil DIP, and a JEDEC Standard 22-pin Ceramic Leadless Chip Carrier. INMOS also provides a Military version, the IMS1620M, as well as a 16K x 4 Static RAM with an Output Enable function $\overline{G}$, the IMS1624 and IMS1624M.

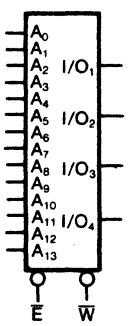
PIN CONFIGURATION





CHIP CARRIER

LOGIC SYMBOL



PIN NAMES

A_0-A_{13}	ADDRESS INPUTS	V_{CC}	POWER (+5V)
$\overline{W}$	WRITE ENABLE	V_{SS}	GROUND
I/O	DATA IN/OUT		
$\overline{E}$	CHIP ENABLE		

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IMS1624
IMS1624L
IMS1624A
CMOS
High Performance
16K x 4 Static RAM

MIL- STD-883 Versions Available

FEATURES

- INMOS Very High Speed CMOS
  - 1620A - 1.2 Micron Design Rules
  - 1620/1620L - 1.6 Micron Design Rules
- 16K x 4 Bit Organization
- 25, 35, 45, 55 and 70nsec Access Times
- Fully TTL Compatible
- Common Data Input & Output
- Single +5V ± 10% Operation
- Power Down Function
- 24-Pin, 300-mil DIP
- 28- Pin LCC
- Output Enable to Control Bus Contention
- Battery Backup Operation 2V Data Retention (L Version Only)

DESCRIPTION

The IMS1624 is a high performance 16K x 4 CMOS static RAM.

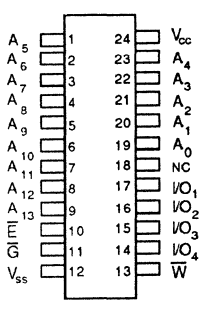
The IMS1624 features fully static operation requiring no external clocks or timing strobes, and equal address access and cycle times. The IMS1624 provides a Chip Enable ($\overline{E}$) function that can be used to place the device into a low-power standby mode. The IMS1624 also includes an Output Enable ($\overline{G}$) function to improve system performance and to control bus contention. The IMS1624 is functionally equivalent to the IMS1620, with the addition of the $\overline{G}$ control function.

The IMS1624 is available in a 24 Pin Ceramic and Plastic DIP and a 28 Pin Ceramic Leadless Chip Carrier.

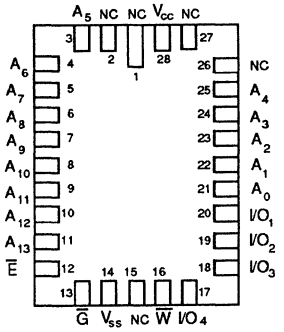
The IMS1624L is a low power version offering battery backup data retention operating from a 2 volt supply.

The IMS1624M and IMS1624LM are MIL-STD-883 versions intended for military applications that demand superior performance and reliability.

PIN CONFIGURATION

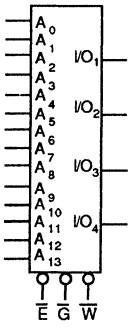


DIP



CHIP CARRIER

LOGIC SYMBOL



PIN NAMES

A_0–A_{13}	ADDRESS INPUTS	V_{CC}	POWER (+5V)
$\overline{W}$	WRITE ENABLE	V_{SS}	GROUND
I/O	DATA IN/OUT		
$\overline{E}$	CHIP ENABLE		
$\overline{G}$	OUTPUT ENABLE		

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IMS1630
IMS1630L
CMOS
High Performance
8K x 8 Static RAM

inmos®

MIL-STD-883C Versions Available

Inmos

FEATURES

- INMOS Very High Speed CMOS
- Advanced Process - 1.6 Micron Design Rules
- 8K x 8 Bit Organization
- 45, 55 and 70 nsec Address Access Times
- 45, 55 and 70 nsec Chip Enable Access Times
- Fully TTL Compatible
- Common Data Inputs and Outputs
- Single +5V ± 10% Operation
- 28 Pin, 600-mil DIP (JEDEC Standard)
- Fast Write Cycle when Outputs Disabled
- Battery Backup Operation - 2V data retention (L version only)

DESCRIPTION

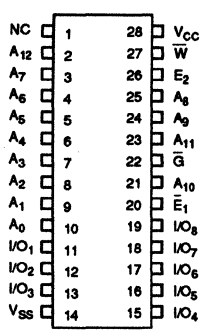
The IMS1630 is a high speed CMOS 8K x 8 Static RAM having access times of 45, 55 and 70ns.

The IMS1630 features fully static operation requiring no external clocks or timing strobes, and equal address access and cycle times. The IMS1630 provides two Chip Enable functions (/E1, E2) to place the circuit in a reduced power standby mode.

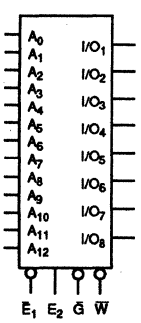
The IMS1630L is a low power version offering battery backup data retention operating from a 2 volt supply.

The IMS1630M and IMS1630LM are available in extended temperature versions for military operating applications.

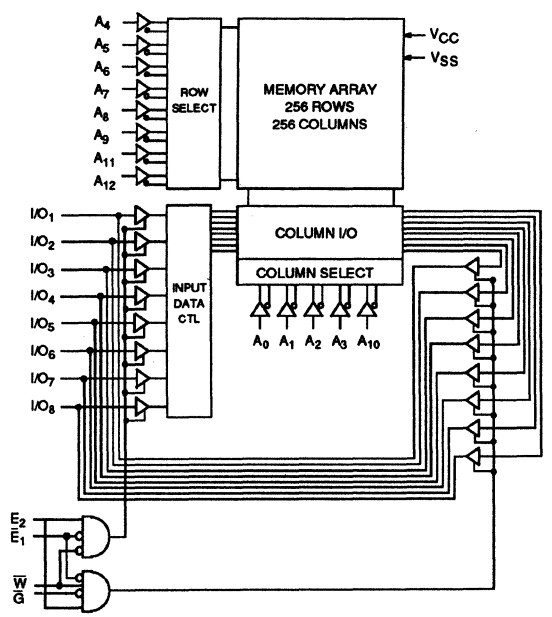
PIN CONFIGURATION



LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

A_0-A_{12}	ADDRESS INPUTS	V_{CC}	POWER (+5V)
$\overline{W}$	WRITE ENABLE	V_{SS}	GROUND
I/O_1-I/O_8	DATA IN/OUT		
E_1, E_2	CHIP ENABLE		
$\overline{G}$	OUTPUT ENABLE		

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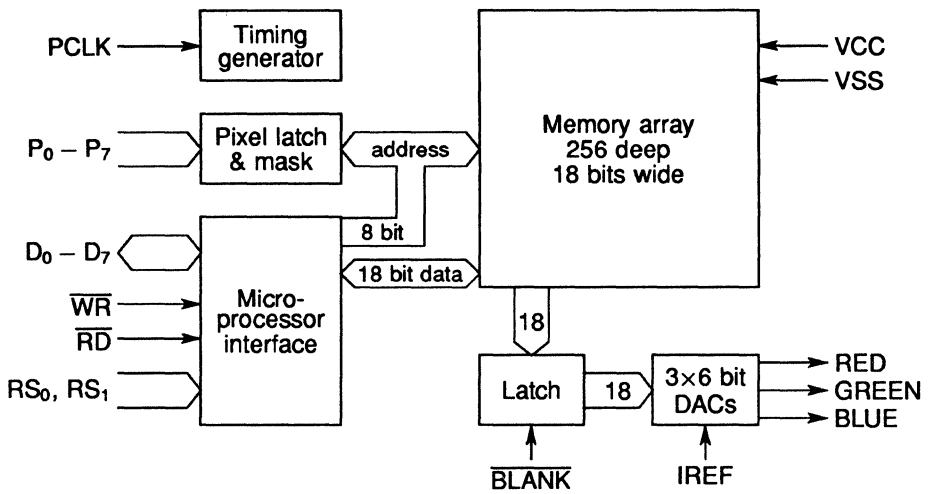
IMS G171
High performance CMOS colour look-up table

Designed to be compatible with
IBM PS/2[1], VGA graphics systems



Inmos

FEATURES

- Compatible with the RS170 video standard.
- Pixel rates up to 50MHz.
- 256K possible colours.
- Single monolithic, high performance CMOS.
- Up to 8 bits per pixel.
- Pixel word mask.
- RGB analogue output, 6 bit DAC per gun, composite blank.
- Low DAC glitch energy.
- Video signal output into 37.5Ω.
- TTL compatible inputs.
- Microprocessor compatible interface.
- Single +5V ±10% power supply.
- Low power dissipation, 880mW max. at maximum pixel rate.
- Standard 600 mil 28 pin DIL package.

DESCRIPTION

The IMS G171 integrates the functions of a colour look-up table (or colour palette), digital to analogue converters (designed to drive into a doubly terminated 75Ω line) and bi-directional microprocessor interface into a single 28 pin package.

Capable of displaying 256 colours from a total of 262,144 colours, the IMS G171 replaces TTL/ECL systems, giving reduced component cost, board area and power consumption.

The pixel word mask allows displayed colours to be changed in a single write cycle rather than by modifying the look-up table.

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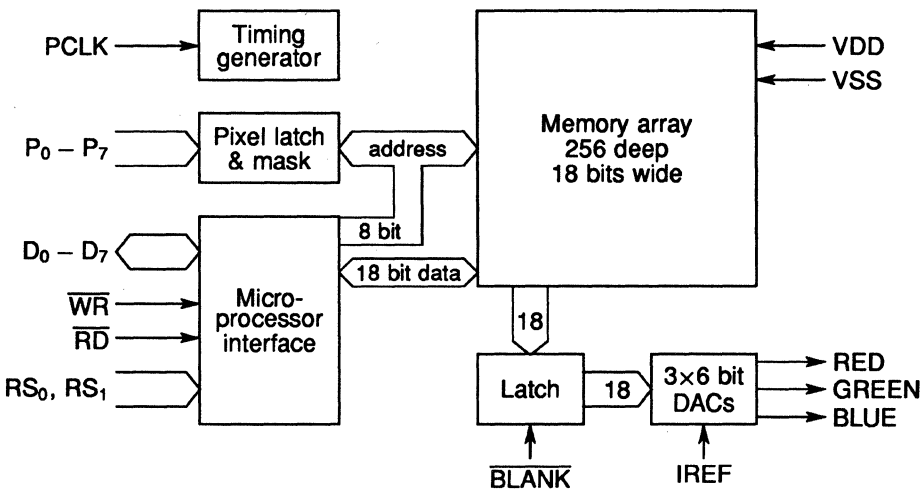
IMS G176
High performance CMOS colour look-up table

Designed to be compatible with IBM PS/2[1], VGA graphics systems



Inmos

FEATURES

- Compatible with the RS170 video standard.
- Pixel rates up to 65MHz.
- 256K possible colours.
- Single monolithic, high performance CMOS.
- Pixel word mask.
- RGB analogue output, 6 bit DAC per gun.
- Composite blank on all three channels.
- Low DAC glitch energy.
- Video signal output into 37.5Ω.
- Up to 8 bits per pixel.
- TTL compatible inputs.
- Microprocessor compatible interface.
- Single +5V ±10% power supply.
- Low power dissipation, 950mW max. at maximum pixel rate.
- Standard 600 mil 28 pin DIL or 32 pin Plastic LCC.
- Pin compatible with IMS G171.

DESCRIPTION

The IMS G176 integrates the functions of a colour look-up table (or colour palette), digital to analogue converters and bi-directional microprocessor interface into a single 28 pin DIL or 32 pin PLCC package.

The device is capable of driving a doubly-terminated 75Ω line with no external buffering, and composite blank signals can be generated on all three outputs.

Capable of displaying 256 colours from a total of 262,144 colours, the IMS G176 replaces TTL/ECL systems, giving reduced component cost, board area and power consumption.

The pixel word mask allows displayed colours to be changed in a single write cycle rather than by modifying the look-up table.

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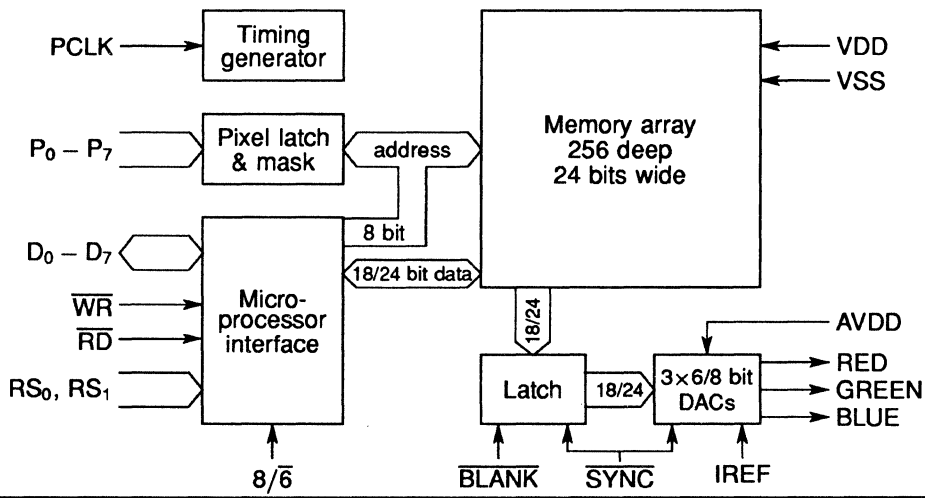
IMS G178

High performance CMOS colour look-up table

Designed to be compatible with
IBM PS/2[1], VGA graphics systems

Preliminary Data



FEATURES

- Compatible with the RS170 video standard.
- RGB analogue output, configurable to 6 or 8 bit DAC operation
- 256K or 16M possible colours.
- Composite sync and blank on all three channels
- Pixel rates up to 80MHz.
- Low DAC glitch energy.
- Video signal output into 37.5Ω.
- TTL compatible inputs.
- Microprocessor compatible interface.
- Asynchronous access to all internal registers.
- Single monolithic, high performance CMOS.
- Up to 8 bits per pixel.
- Pixel word mask.
- Single +5V ±10% power supply.
- Low power dissipation, typically 1W at maximum pixel rate.
- 32 pin Plastic LCC package.
- Backward compatible with other members of IMS G17x look-up table family.

DESCRIPTION

The IMS G178 integrates the functions of a colour look-up table (or colour palette), digital to analogue converters and bi-directional microprocessor interface into a single 32 pin PLCC package.

The device is switchable between 6 or 8 bit DAC operation, so is capable of displaying 256 colours from a total of 262,144 colours in 6 bit mode, or from over 16 million colours in 8 bit mode.

The device is capable of driving a doubly-terminated 75Ω line with no external buffering, and composite sync and blank signals can be generated on all three outputs.

The pixel word mask allows displayed colours to be changed in a single write cycle rather than by modifying the look-up table.

The IMS G178 is software-compatible with the IMS G171 and both software and pin-compatible with the IMS G176 products in 6 bit mode. It replaces TTL/ECL systems and thus gives reduced component cost, board area and power consumption.

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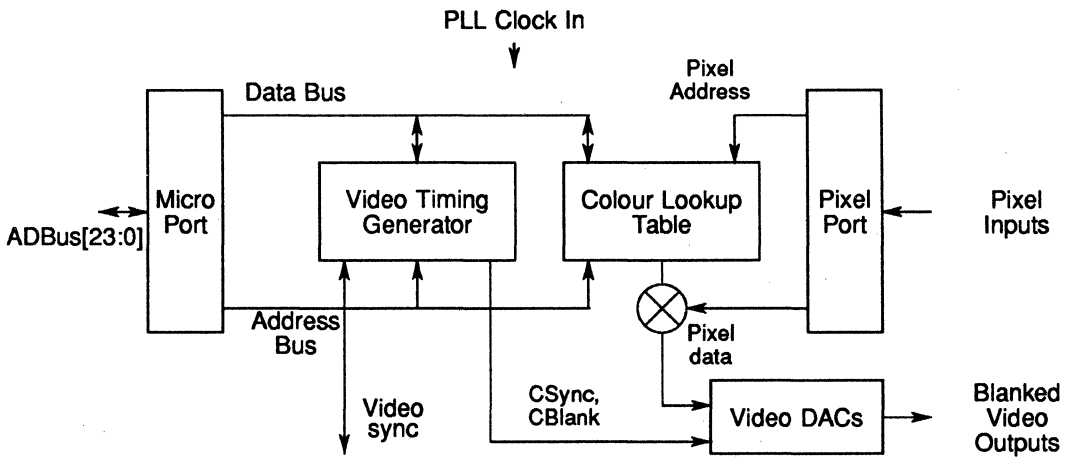
IMS G300
colour video controller

Preliminary Data



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FEATURES

Video rates up to 120MHz
Software configurable video timing generator
Interlaced or non-interlaced video
Generates Studio broadcast standard Sync signals
Supplies blanked analogue video outputs
Internal or external Sync options
Single or synchronous multiple operation

4 into 1 multiplexed Pixel input
On chip 256 location x 24 bits colour palette
Triple high speed 8 bit video DACs
RS 170a and EIA 343-A compatible
Indirect 8 planes per pixel mode via palette, or:
24 planes per pixel mode direct to DACs

General purpose Video RAM support
Synchronous VRAM DataTransfer strobing
Video RAM Row address auto-increment
Screen line length independent of VRAM architecture
On-chip phase-locked loop (PLL)
All external signals and clocks at 1/4 video rate

APPLICATIONS

General purpose raster scan control
CRT Screen control
Colour plotters and printers
Plane-based workstations
Portable personal computers

Three dimensional modelling
Real time animation systems
Computer visualisation
Multiple processor systems
Frame swapping systems
Scene insertion into live camera data

Distributed computing environments

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IMS B401 TRAM (TRAnsputer Module)

FEATURES

- Choice of Transputer (IMS T414 or IMS T800)
- 32 Kbytes of no–wait–state SRAM (150 ns memory cycle time)
- Communicates via 4 INMOS serial links (Selectable between 10 or 20 Mbits/s)
- Stackability allows other TRAMs to be "piggy-backed"
- Package has only 16 active pins.
- Designed to a published specification (*INMOS Technical Note 29*).

GENERAL DESCRIPTION

A low cost, high performance, 16 pin transputer, ideal for applications where 2 Kbytes or 4 Kbytes of on-chip RAM is not quite enough. The 32 Kbytes of off chip RAM is ideal for systolic processing, signal processing, feature extraction etc. The IMS B008, fitted with ten IMS B401-3s, offers 40 MWhetstones/s in a single slot of an IBM PC, XT, AT, PS2 model 30, or clone. In the INMOS ITEM, 160 IMS B401-2s offer 1.6 GIPS (1600 MIPS) and 5 Mbytes.

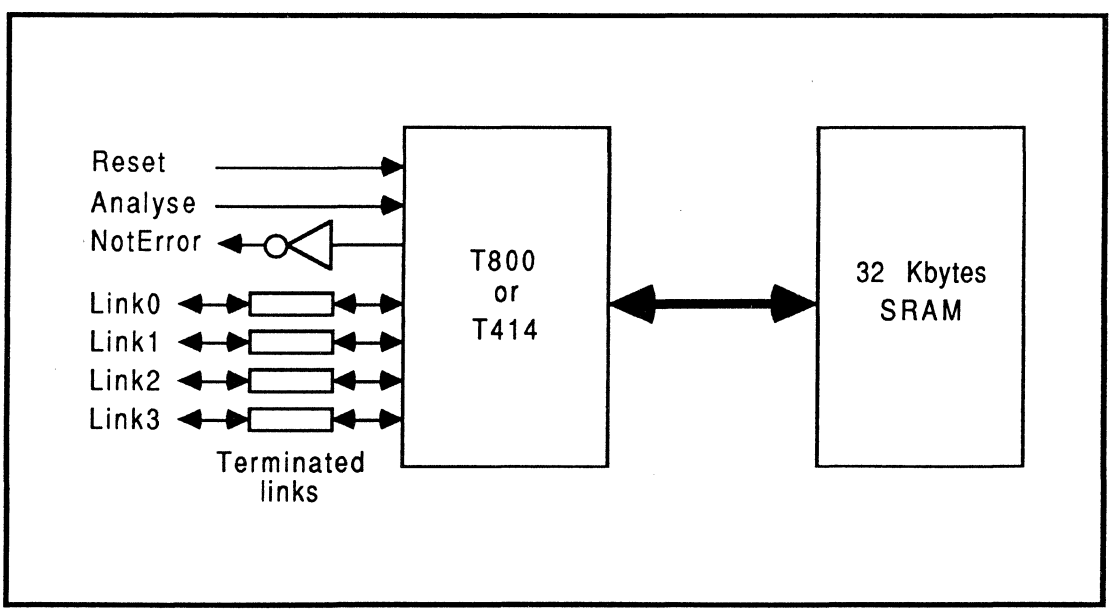

Figure 1: IMS B401 block diagram

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IMS B402 TRAM (TRAnsputer Module)

FEATURES

- IMS T212 Transputer
- 8 Kbytes of no–wait–state SRAM (100 ns memory cycle time)
- Communicates via 4 INMOS serial links (Selectable between 10 or 20 Mbits/s)
- Stackability allows other TRAMs to be "piggy-backed"
- Package has only 16 active pins.
- Designed to a published specification (*INMOS Technical Note 29*).

GENERAL DESCRIPTION

The faster multiplication of the 16 bit transputer and the faster external memory interface on the IMS B402 give it a higher performance than the IMS B401, for fixed point signal processing and feature extraction. Even with programmed floating point, the IMS B402 delivers 127 KWhetstones/s, ten times the speed of the 68000. And Occam makes it easy to program 64 bit integers on this 16 bit processor, for high precision arithmetic and operations on sets. The IMS B402 is also ideal for message switching, intelligent control of IMS C004 link switches, and for protocol conversion.

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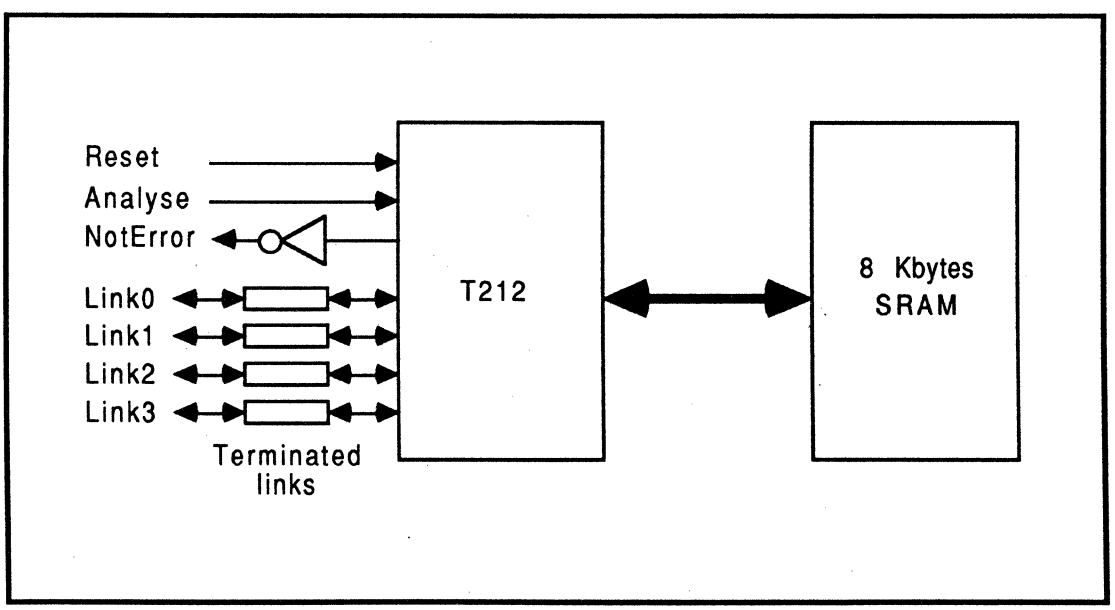

Figure 1: IMS B402 block diagram

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IMS B403 TRAM (TRAnsputer Module)

FEATURES

- Choice of Transputer (IMS T414-20 or IMS T800-20)
- 1 Mbyte of no–wait–state DRAM (150 ns memory cycle time)
- Subsystem controller circuitry
- Communicates via 4 INMOS serial links (Selectable between 10 or 20 Mbits/s)
- Stackability allows other TRAMs to be "piggy-backed"
- Package has only 16 active pins
- Designed to a published specification

GENERAL DESCRIPTION

The IMS B403 obtains the ultimate performance from a full Mbyte of RAM; with an IMS T800-20 it offers 4 MWhetstones/s. Rather than use expensive 256K SRAMs, which would take up much more board area, the IMS B403 uses 60 ns access time DRAMs, designed by INMOS. Using IMS B403s, a fully packed INMOS ITEM will hold 40 transputers, just as it would with IMS B003s, but the IMS B403s offer 4 times the memory (40 Mbytes total), higher speed (3 cycle instead of 5 cycle memory) and fully flexible network configurations.

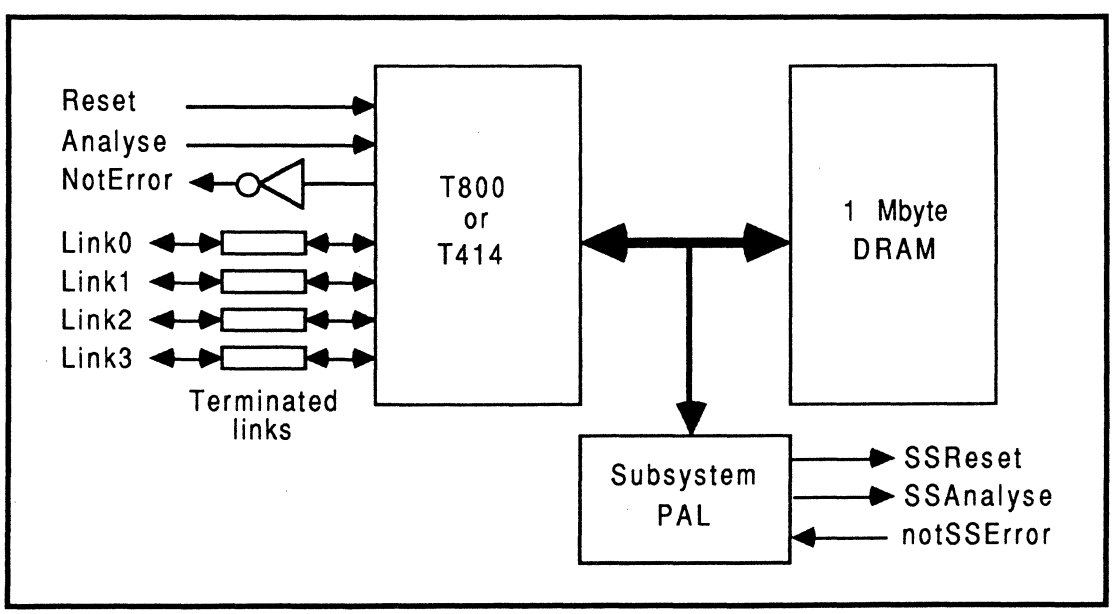

Figure 1: IMS B403 block diagram

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IMS B404 TRAM (TRAnsputer Module)

FEATURES

- IMS T800 Transputer
- 128 Kbytes of zero wait-state SRAM
- 2 Mbytes of single wait-state DRAM
- Subsystem controller circuitry
- Communicates via 4 INMOS serial links (Selectable between 10 or 20 Mbits/s)
- Package has only 16 active pins
- Designed to a published specification (*INMOS Technical Note 29*)

GENERAL DESCRIPTION

The IMS B404 runs the occam Compiler in the Transputer Development System fully twice as fast as the IMS B004. It does this by using the IMS T800-20, by using 1Mbit DRAMs, but principally by extending the principle of fast on chip RAM to include 128 Kbytes of static RAM which cycles as fast as possible. So any technique which puts most frequently accessed memory locations near the bottom of memory will speed up the processing. The IMS B404, of all INMOS board level products, has the highest packing density of silicon; 11 cm^2 on a board the size of a credit card. Four IMS B404s fit onto the IMS B008 in a single slot of the IBM PC. Fifty IMS B404s fit into an ITEM, to give 100 Mbytes, 500 MIPS, 200 MWhetstones, with space to spare for other modules.

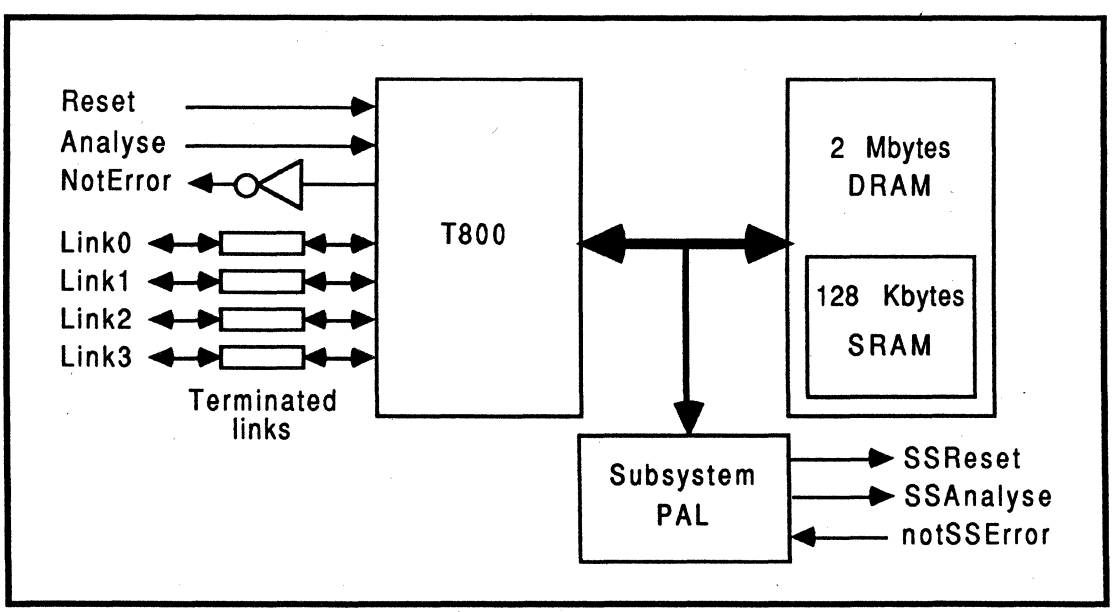

Figure 1: IMS B404 block diagram

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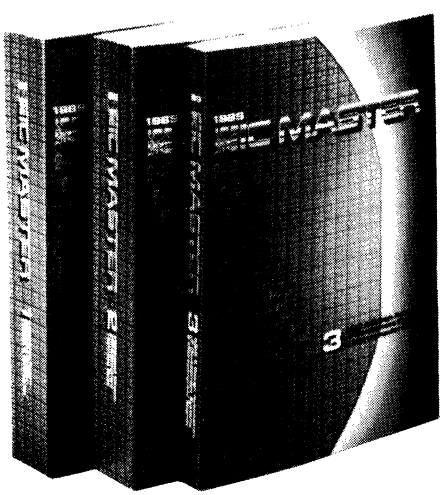

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128K x 8 Static RAM

Parameter	Unit	S128K8-70C	S128K8-85M,I S128K8-85C	S128K8-100M,I S128K8-100C	S128K8-120M,I
Access Time	ns	70	85	100	120
Cycle Time	ns	70	85	100	120
Operating Current at 125°C	mA		120	120	120

Features

- **Fully static 128Kx8 SRAM**
- **Advanced 4-T CMOS technology**
- **32 pin JEDEC standard pinout**
- **Fully monolithic**
- **Military, industrial and commercial temperature ranges**
- **Processed to standards set forth in MIL-STD-883C**
- **Ceramic dip package**

General Description

The Inova S128K8 is a high performance 1-megabit Static Random Access Memory (SRAM), organized as 128K 8-bit bytes. This device is constructed by employing Inroute™, Inova's routing technology, an advance that turns VLSI devices into ULSI macrocircuits. Higher density means lower weight and higher reliability as compared to multiple lower density devices.

The Inova S128K8 is manufactured using a high reliability 4-transistor cell CMOS process, which has low active and standby power characteristics. All inputs and outputs are fully TTL compatible. Operation is fully static; there is no need for extra control logic to generate clocks and timing strobes.

The package outline and pinout are JEDEC standard.

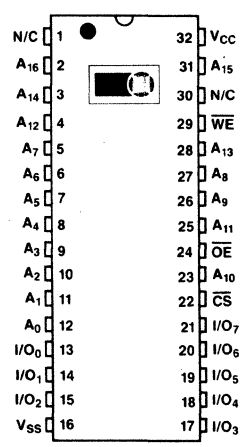
Every military grade device is screened to conditions set forth in MIL-STD-883C, Paragraph 1.2.2.

Inova offers a true packaging alternative to the larger capacity hybrid solutions by offering a monolithic device in a JEDEC standard pinout.

Pin Names

A_0–A_{16}	Address Inputs
I/O_0–I/O_7	Data Input/Output
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
V_{CC}	+5V Power
V_{SS}	Ground

Pinout



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64K x 16 Static RAM

Parameter	Unit	S64K16-70C	S64K16-85M,I S64K16-85C	S64K16-100M,I S64K16-100C	S64K16-120M,I S64K16-120C
Access Time	ns	70	85	100	120
Cycle Time	ns	70	85	100	120
Operating Current	mA	70	70	70	70
CMOS Standby Current (C)	mA	0.5	0.5	0.5	0.5

Features

- **Monolithic 64Kx16 SRAM**
- **Advanced 4-T CMOS technology**
- **40 pin JEDEC standard pinout**
- **Ceramic dip package**
- **Military, industrial and commercial temperature ranges**
- **Processed to standards set forth in MIL-STD-883C**
- **2-volt data retention**

General Description

The Inova S64K16 is a high performance 1-megabit Static Random Access Memory (SRAM), organized as 64K 16-bit words. This device is constructed by employing Inroute,™ Inova's routing technology, an advance that turns VLSI devices into ULSI macrocircuits. Higher density means lower weight and higher reliability as compared to multiple lower density devices.

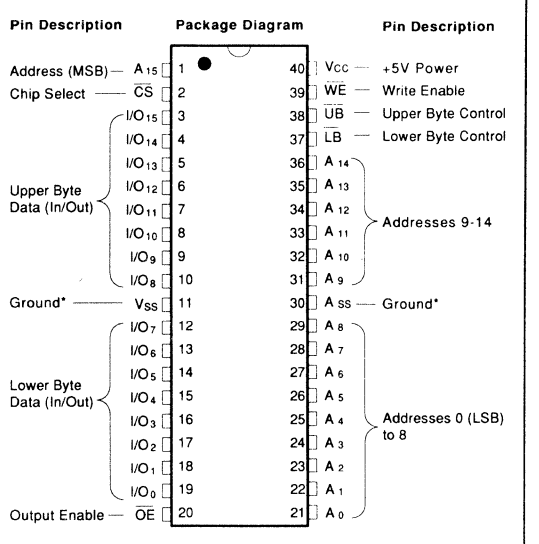
The Inova S64K16 is manufactured using a high reliability 4-transistor cell CMOS process, which has low active and standby power characteristics. All inputs and outputs are fully TTL compatible. Operation is fully static; there is no need for extra control logic to generate clocks and timing strobes.

The package outline and pinout are JEDEC standard.

Every military grade device is screened to conditions set forth in MIL-STD-883C, Paragraph 1.2.2.

Inova offers a true packaging alternative to the larger capacity hybrid solutions by offering a monolithic device in a JEDEC standard pinout.

Pinout



NOTE: To assure proper operation both grounds must be connected.

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32K x 8 Static RAM

Parameter	Unit	S32K8-55C	S32K8-70M,I S32K8-70C	S32K8-85M,I S32K8-85C	S32K8-100M,I
Access Time	ns	55	70	85	100
Cycle Time	ns	55	70	85	100
Operating Current	mA	110	100	100	100
CMOS Standby Current (C)	mA	2	2	2	

Features

- **Fully static 32Kx8 SRAM**
- **Advanced 4-T CMOS technology**
- **28 pin JEDEC standard pinout**
- **Fully monolithic**
- **Military, industrial and commercial temperature ranges**
- **Processed in conformance to MIL-STD-883C**
- **Ceramic dip package**

General Description

The Inova S32K8 is a high performance 256K Static Random Access Memory (SRAM), organized as 32K 8-bit bytes. This device is constructed by employing Inroute™, Inova's routing technology, an advance that turns VLSI devices into ULSI macrocircuits. Higher density means lower weight and higher reliability as compared to multiple lower density devices.

The Inova S32K8 is manufactured using a high reliability 4-transistor cell CMOS process, which has low active and standby power characteristics. All inputs and outputs are fully TTL compatible. Operation is fully static; there is no need for extra control logic to generate clocks and timing strobes.

The package outline and pinout are JEDEC standard.

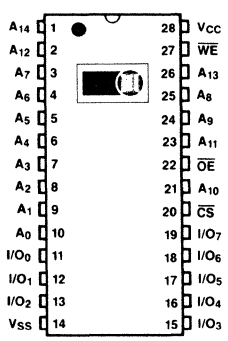
Every military grade device is processed and screened to the demanding requirements of MIL-STD-883C.

Inova offers a true packaging alternative to the larger capacity hybrid solutions by offering a monolithic device in a JEDEC standard pinout.

Pin Names

A_0–A_{14}	Address Inputs
I/O_0–I/O_7	Data Input/Output
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
V_{CC}	+5V Power
V_{SS}	Ground

Pinout



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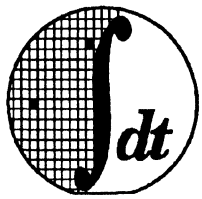

IDT — LEADING THE CMOS FUTURE

A major revolution is taking place in the semiconductor industry today. A new technology is rapidly displacing older NMOS and bipolar technologies as the workhorse of the '80s and beyond. That technology is high-speed CMOS. Integrated Device Technology, a company totally predicated on and dedicated to implementing high-performance CMOS products, is on the leading edge of this dramatic change.

Beginning with the introduction of the industry's fastest CMOS 2K x 8 static RAM, IDT has grown into a company with multiple divisions producing a wide range of high-speed CMOS circuits that are, in almost every case, the fastest available. These advanced products are produced with IDT's proprietary CEMOS™ technology, a twin-well dry-etched, stepper-aligned process utilizing progressively smaller dimensions.

From inception, our product strategy has been to apply the advantages of our extremely fast CEMOS technology to produce the integrated circuit elements required to implement high-performance digital systems. IDT's goal is to provide the circuits necessary to create systems which are far superior to previous generations in performance, reliability, cost, weight and size. Many of our innovative product designs offer higher levels of integration, advanced architectures, higher density packaging and systems enhancement features that are establishing tomorrow's industry standards. The company is committed to providing its customers with an ever-expanding series of these high-speed, lower-power IC solutions to system design needs.

IDT's commitment, however, extends beyond state-of-the-art technology and advanced products to providing the highest level of customer service and satisfaction in the industry. Producing products to exacting quality standards that provide excellent, long-term reliability is given the same level of importance and priority as device performance. IDT is also dedicated to delivering these high-quality advanced products on time. The company would like to be known not only for its technological capabilities, but also for providing its customers with quick, responsive and courteous service.

IDT's product families are available in both commercial and military grades. As a bonus, commercial customers obtain the benefits of military processing disciplines, established to meet or exceed the stringent criteria of the applicable military specifications.

IDT is the leading U.S. supplier of high-speed CMOS circuits. The company's high-performance static RAMs, logic, DSP, MICROSLICE™ bit-slice microprocessor products, RISC, data conversion devices, ECL I/O devices and modular subsystem assemblies complement each other to provide high-speed CMOS solutions to a wide range of applications and systems.

Dedicated to maintaining its leadership position as a state-of-the-art IC manufacturer, IDT will continue to focus on maintaining its technology edge as well as developing a broader range of innovative products. New products and speed enhancements are continuously being added to each of the existing products families and additional product lines will be introduced. Contact your IDT field representative of factory marketing a 1-800-IDT-CMOS to determine the latest product offerings. If you're building state-of-the-art equipment, IDT may be able to solve some of your design problems.

Integrated Device Technology

Integrated Device Technology, Inc.

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IDT High-Speed CMOS Products Common Features

- Fabricated with IDT's advanced CEMOS™ dual-well, oxide-isolated, ion-implanted technology with feature sizes down to submicron.
- Proprietary ESD protection circuitry is designed into all inputs and outputs to ensure that they withstand repeated applications of ESD stress and do not exhibit the degradation found in many other MOS or bipolar products.
- IDT products are designed, manufactured and tested to the highest standards of quality and reliability
  — they begin with stringent design rules derived for use in high-reliability programs
  — they are manufactured with a dedicated commitment to reliable workmanship
  — rigid controls are employed throughout wafer fab, device assembly and test
- All military grade products are manufactured in compliance with the latest revision of MIL-STD-883, Class B.
- Military module assemblies are constructed using screened IDT monolithic products and receive additional burn-in and electrical test screening to assure package integrity and mechanical reliability.
- Monolithic products are available in ceramic and plastic packages. The various packages available are DIPs, Pin Grid Arrays, LCCs, SOICs and Flatpacks.
- All products operate from a single 5V power supply.
- Inputs and outputs, depending on the product, are directly TTL, CMOS or ECL-compatible.
- Alpha-particle induced soft error protection for static RAMs.
- Latch-up protection circuitry.

High-Speed CMOS Radiation Hardened Products

- Radiation Enhanced ('RE) or Radiation Tolerant ('RT) versions of IDT products available. Parameters/Speed options of IDT's military product data sheets are applicable for most 'RT & 'RE devices (consult factory).
- IDT has purchased/installed equipment for Total Dose testing. The IDT Total Dose Test plan exposes a sample of die on a wafer to a particular Total Dose level. Only wafers with sampled die that pass Total Dose level tests are assembled and used for order (consult factory for more details on Total Dose sample testing).
- Memory devices processed on the Radiation Enhanced process on Epi wafers are qualified by IDT's Total Dose test plan sample die testing of 10K to 30K Rads Total Dose [RADs(Si)], 'RE non-memory devices are are qualified by IDT's Total Dose test plan sample die testing of 30K to 100K Rads Total Dose [RADs(Si)].
- Radiation Tolerant devices are qualified by IDT's Total Dose test plan sample die testing of 10K Rads Total Dose [RADs(Si)].
- Manufactured in compliance with the latest revision of MIL-STD-883, Class B or Class S.

Key

Shaded area indicates new product.

Boldface indicates an improved IDT feature.

The availability column shows the date when limited production quantities will be available.

CALL in the data book page column means that the data sheet has not been included in the 1988 data book; A copy, when available, may be obtained from IDT or from its sales offices.

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FAST is a trademark of Fairchild Semiconductor Company
UNIX is a trademark of AT&T

High-Speed CMOS RISC Microprocessors

- Highest performance CMOS RISC processors available
- Efficient pipelining assists in obtaining an execution rate of one instruction per cycle
- Optimizing compilers for C, Pascal, FORTRAN, Ada, PL/1 and Cobol
- Unix™ System V.3 and Berkely 4.3 versions supported
- Tightly coupled co-processor interface between CPU and Floating-Point Accelerator
- Floating-Point Accelerator conforms with IEEE 754-1985 standard
- Write buffers enhance CPU performance by allowing memory writes during run cycles

Part Number	Description	Typical Power (mW)	Avail.	Data Book Page
IDT79R3000	RISC CPU Processor, 20 mips @ 25MHz On-chip Cache Control, Memory Management Unit, 64-entry Translation Lookaside Buffer, Thirty two 32-bit General Purpose Registers	1500	Q4'88	CALL
IDT79R3010	RISC Floating-Point Accelerator, 25MHz 7 MFLOPS single precision LINPACK 4 MFLOPS double precision LINPACK	1500	Q4'88	CALL
IDT79R3020	RISC CPU Write Buffer, 25MHz	200	Q4'88	CALL
IDT79R2000	RISC CPU Processor, 10 mips @ 16.7MHz On-chip Cache Control, Memory Management Unit, 64-entry Translation Lookaside Buffer, Thirty two 32-bit General Purpose Registers	1500	Q4'88	9-1
IDT79R2010	RISC Floating-Point Accelerator, 16.7MHz 4 MFLOPS single precision LINPACK 2 MFLOPS double precision LINPACK	1500	Q4'88	9-10
IDT79R2020	RISC CPU Write Buffer, 16.7MHz	200	Q4'88	9-15

Integrated RISC Solutions

In November, 1987, Integrated Device Technology, Inc. entered into a 10 year technology partnership agreement with MIPS Computer Systems of Sunnyvale, California to market and manufacture the MIPS family of 32-bit RISC processors. IDT is licensed to manufacture the R2000 and R3000 families of 32-bit RISC processors, and all future generations of MIPS RISC processors. IDT is marketing system software support, including innovative optimizing compilers and the UNIX operating system, run on the MIPS RISC processors. The M series of supermicrocomputers are available for microprocessor software development from IDT.

To place this agreement into perspective, a brief history of the microprocessor is due. Since its invention as a 4-bit entity in 1971, the microprocessor market has grown to a $1 billion market. Advances in MOS semiconductor technology allowed for higher levels of functional integration, microprocessors grew in data path width (8-bit, 16-bit and now 32-bit) and in complexity to gain greater system speed. This trend lead to Complex Instruction Set Computing (CISC) technology.

A major technology shift is occuring in the microprocessor market in the form of Reduced Instruction Set Computing (RISC) technology. Various studies of computer programs indicate that 20% of the instructions are executed 80% of the time. RISC technology takes advantage of this fact by reducing the instruction set and by optimizing the architecture to execute these instructions very quickly. RISC differs from CISC in that the instruction set is simplified and can therefore be executed more quickly. Thus, RISC represents a dramatic increase in system performance at much lower costs.

The key to a successful microprocessor is an integration of hardware and software solutions. The MIPS RISC architecture is a unique approach from other RISC architectures in that the software and hardware were developed concurrently. Innovative optimizing compiler technology determines the hardware architecture, as opposed to the software being written around the existing hardware. This approach yields a highly integrated processor and a tight coupling of software and hardware.

The MIPS architecture is an approved Applications Binary Interface (ABI) standard for AT&T UNIX System V. This provides a common platform for the development of third party software.

Synthesis Software Solutions, Inc. of Sunnyvale, California is a company recently formed to ensure a large variety of third party software gets ported to the MIPS RISC architecture, with IDT participating as an investor. Synthesis will be porting software products from Oracle Corp., Informix Software, Relational Technology, Inc., Unify Corporation, Meta-Software, Language Processors, Inc., Verdix Corp., Applix, and others.

IDT is commited to provide the complete **Integrated RISC Solution**, combining our expertise in silicon process technology, in design support for leadership products, including development systems and software, and in providing volume, quality product to meet high performance system needs.

DESC SMD Products

- DESC SMD (Standard Military Drawing) program eliminates the need for multiple source control drawings. IC manufacturers, primes, and DOD share the same specification format. The benefits are improved availability to a military drawing, stable data sheet parameters, and an listed DESC SMD product.
- DESC SMD numbers, pending or listed, for 47 IDT products:
  - SRAM
  - DSP
  - MICROSLICE
  - DATA CONVERSION
  - HIGH SPEED FCT/FCTA LOGIC
- SMD numbers for the following packages
  - Cerpacks
  - Cerdips
  - LCC
  - Side brazed DIPs
  - Flatpacks
- IDT has a direct modem link to DESC to minimize turnaround time for pending SMDs.

DESC SMD No.	IDT Part No.	Status
SRAM		
84036	6116	LISTED
84132	6167	PENDING
5962-86015	7187	LISTED
5962-86859	6198/7198 /7188	LISTED
5962-86705	6168	LISTED
5962-85525	7164	LISTED
5962-88552	71256L	LISTED
5962-88611	71682L	PENDING
5962-88662	71256S	LISTED
5962-88681	71258S	LISTED
5962-88545	71258L	LISTED
5962-88544	71257L	LISTED
SMP		
5962-86875	7130/7140	LISTED
5962-87002	7132/7142	LISTED
5962-88610	7133S/7143S	PENDING
5962-88665	7133L/7143L	PENDING
DSP		
5962-87531	7201LA	LISTED
5962-86873	7216L	LISTED
5962-86846	72404	LISTED
5962-87686	7217	PENDING
5962-88669	7203S/7204S	PENDING
MICROSLICE		
5962-87708	39C10B & C	LISTED
5962-88535	39C01	LISTED
5962-88533	49C460A	LISTED
5962-88613	39C60A	LISTED
5962-88643	49C410	LISTED
DCP		
5962-88743	75C48	PENDING

DESC SMD No.	IDT Part No.	Status
LOGIC		
5962-87630	54FCT244	LISTED
5962-87629	54FCT245	LISTED
5962-86862	54FCT299	LISTED
5962-87644	54FCT373/FCTA373	LIST/PEND
5962-87628	54FCT374	LISTED
5962-87627	54FCT377	PENDING
5962-87654	54FCT138/138A	LIST/PEND
5962-87655	54FCT240	LISTED
5962-87656	54FCT273	LISTED
5962-87704	54FCT861	PENDING
5962-87667	54FCT827	PENDING
5962-88575	54FCT841	PENDING
	54FCT533	PENDING
	54FCT182	PENDING
5962-88608	54FCT821/821A	PENDING
	54FCT645	PENDING
	54FCT640	PENDING
	54FCT534	PENDING
5962-88543	54FCT521	PENDING
5962-88675	54FCT845A/845B	PENDING
5962-88640	54FCT161	PENDING
5962-88639	54FCT573	PENDING
5962-88656	54FCT823A/823B	PENDING
5962-88657	54FCT163/163A	LISTED
5962-88674	54FCT825A/B	PENDING
5962-88661	54FCT863A/B	PENDING
5962-88736	29FCT520A	PENDING
	54FCT646	PENDING
	54FCT139	PENDING
	54FCT824	PENDING

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High-Speed CMOS Static RAMs

- Extremely fast access times
- Low power consumption
- 2V data retention battery backup on all low-power devices
- Three-state outputs
- Available in military and commercial temperature ranges

Part Number	Description	Max. Speed (ns) Mil.	Com'l.	Typical Power (mW)	Avail.	Data Book Page
MONOLITHIC						
IDT6167	16K (16K x 1)	20	15	225	NOW	4-1
		15	**12**	225	Q1'89	CALL
IDT6168	16K (4K x 4)	20	15	275	NOW	4-11
		15	**12**	300	Q1'89	CALL
IDT71681	16K (4K x 4) with separate data inputs and outputs; outputs track inputs during write mode	25	20	225	NOW	4-22
		20	**15**	300	Q1'89	CALL
		15	**12**	300	1989	CALL
IDT71682	16K (4K x 4) with separate data inputs and outputs; outputs in high impedance state during write mode	25	20	225	NOW	4-22
		20	**15**	300	Q1'89	CALL
		15	**12**	300	1989	CALL
IDT6116	16K (2K x 8)	25	20	225	NOW	4-33
		20	**15**	275	1989	4-33
IDT7187	64K (64K x 1)	25	20	250	NOW	4-44
		20	**15**	300	1989	4-44
IDT7188	64K (16K x 4)	25	20	300	NOW	4-57
		20	**15**	350	1989	4-57
IDT6198	64K (16K x 4) with output enable ($\overline{OE}$) for added system flexibility	**25**	**20**	300	NOW	4-65
		20	**15**	350	1989	4-65
IDT7198	64K (16K x 4) output enable ($\overline{OE}$) and second chip select ($\overline{CS_2}$) for added system flexibility and memory control	25	20	300	NOW	4-74
		20	**15**	350	1989	4-74
IDT71981	64K (16K x 4) with separate data inputs and puts; outputs track inputs during write mode	25	20	300	NOW	4-84
		20	**15**	350	1989	4-84
IDT71982	64K (16K x 4) with separate data inputs and ouputs; outputs in high impedance state during write mode	25	20	300	NOW	4-84
		20	**15**	350	1989	4-84
IDT7164	64K (8K x 8)	**30**	**25**	250	NOW	4-94
		25	**20**	250	1989	CALL
IDT7165	64K (8K x 8) with asynchronous clear and high-speed chip select	35	30	250	NOW	4-196
		30	**25**	250	1989	CALL
IDT71C65	64K (8K x 8) with CMOS compatible I/O	35	30	250	NOW	4-206
		30	25	250	1989	CALL
IDT7186	64K (4K x 16)	—	35	300	NOW	4-103
		45	35	300	Q1'89	4-103
		35	**25**	300	1989	CALL
IDT71586	64K (4Kx 16) with address latches	—	35	300	NOW	CALL
		45	35	300	Q1'89	CALL
		35	**25**	300	1989	CALL
IDT71257	256K (256K x 1)	**—**	**—**	350	Q1'89	4-113
		35	**25**	350	1989	4-113
		25	**20**	350	1989	
IDT71258	256K (64K x 4)	35	**—**	350	NOW	4-124
		35	**25**	350	Q1'89	4-124
		25	**20**	350	1989	CALL

High-Speed CMOS Static RAMs (continued)

Part Number	Description	Max. Speed (ns) Mil.	Com'l.	Typical Power (mW)	Avail.	Data Book Page
IDT61298	256K (64K x 4) with output enable ($\overline{OE}$) for added system flexibility	45	—	350	Q1'89	4-133
		35	**25**	350	1989	4-133
		30	**20**	350	1989	CALL
IDT71281	256K (64K x 4) with separate data inputs and outputs; outputs track inputs during write mode	35	25	350	1989	4-143
		30	**20**	350	1989	CALL
IDT71282	256K (64K x 4) with separate data inputs and outputs; outputs in high impedance state during write mode.	35	25	350	1989	4-143
		30	**20**	350	1989	CALL
IDT71256	256K (32K x 8)	45	35	250	NOW	4-153
		35	**25**	250	1989	CALL
IDT71027	1 Megabit (1024K x 1)	**45**	**35**	500	1989	4-168
IDT71028	1 Megabit (256K x 4)	**45**	**35**	500	1989	4-171
IDT71024	1 Megabit (128K x 8)	**45**	**35**	500	Q1'89	4-173
IDT6178	16K (4K x 4) cache-tag with cache address comparator and asynchronous clear	15	12	300	Q1'89	4-184
		12	**10**	300	1989	CALL
IDT7174	64K (8K x 8) with cache address comparator, asynchronous clear and high-speed chip select	45	35	250	NOW	4-186
		35	**25**	250	1989	CALL
IDT71501	64K (64K x 1) synchronous RAM; all inputs and outputs latched	45	35	385	NOW	4-215
IDT71502	64K (4K x 16) registered RAM for writable control store use; has on-board serial load, parity, breakpoint and trace logic	45	35	350	NOW	4-224
HIGH-SPEED BiCMOS ECL STATIC RAMS						
IDT100490	64K (64K x 1) with ECL 100K compatible I/O	—	**10**	320	NOW	4-52
IDT10490	64K (64K x 1) with ECL 10K compatible I/O	—	**10**	420	NOW	4-52
IDT100494	64K (16K x 4) with ECL 100K compatible I/O	—	10	600	1Q'89	CALL
IDT10494	64K (16K x 4) with ECL 10K compatible I/O	—	10	600	1Q'89	CALL
IDT100496	64K (16K x 4) with ECL 100K compatible I/O and self-timed mode (STRAM)	—	12	800	1Q'89	CALL
IDT10496	64K (16K x 4) with ECL 10K compatible I/O and self-timed mode (STRAM)	—	12	800	1Q'89	CALL
STANDARD RAM MODULES						
For additional RAM sizes and.configurations from 80K to 4 Megabit, see page 6, High-Speed CMOS Module Products						

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High-Speed CMOS Module Products

- High density solutions
- 'M' type ceramic RAM modules are built with monolithic RAMs in LCC packages surface mounted onto multi-layered, co-fired ceramic substrates using IDT's high-reliability vapor phase reflow soldering process.
- 'MP' and 'MB' type commercial plastic modules are built using monolithic RAMs in SMD plastic packages, surface mounted onto epoxy laminate (FR4) substrates.
- 'MC' type ceramic SIP modules are constructed using monolithic RAMs in LCC packages on a vertically mounted substrate. This packaging configuration allows for very low profile modules with high packing density.
- Custom solutions are available to achieve the optimum system integration and performance.

Part Number	Description	Max. Speed (ns) Mil.	Com'l.	Typical Power (mW)	Avail.	Data Book Page
STANDARD RAM MODULES						
IDT8MP628	128K (8K x 16) plastic SIP RAM module	—	40	825	NOW	13-80
IDT8M628	128K (8K x 16) RAM module with monolithic pinout	50	40	825	NOW	13-99
IDT7MP156	256K (256K x 1) plastic SIP RAM module	—	**25**	600	NOW	13-17
IDT7MC156	256K (256K x 1) static RAM module (ceramic SIP)	—	**25**	600	NOW	13-3
IDT7MP456	256K (64K x 4) plastic SIP RAM module	—	**25**	1200	NOW	13-23
IDT7M856	256K (32K x 8) RAM module with monolithic pinout	50	40	950	NOW	13-63
IDT8M856	256K (32K x 8) RAM module with monolithic pinout (low-power)	55	45	350	NOW	13-113
IDT7MC4005	256K (16K x 16) static RAM module (ceramic SIP)	—	**25**	2235	NOW	CALL
IDT8MP656	256K (16K x 16) plastic SIP RAM module	—	40	825	NOW	13-80
IDT8M656	256K (16K x 16) RAM module with monolithic pinout	60	40	825	NOW	13-99
IDT7M656	256K (16K x 16, 32K x 8, 64K x 4) RAM module - customer configurable organization	30	25	3200	NOW	13-48
IDT7M812	512K (64K x 8) RAM module offering maximum addressable memory required by 8-bit MPs	35	**25**	2400	NOW	13-57
IDT7M912	512K (64K x 9) RAM module offering maximum addressable memory required by 8-bit MPs with parity	35	**25**	2700	NOW	13-57
IDT8MP612	512K (32K x 16) plastic SIP RAM module	—	40	875	NOW	13-74
IDT8M612	512K (32K x 16) RAM module with monolithic pinout	60	40	750	NOW	13-92
IDT7MC4032	512K (16K x 32) RAM module with separate I/O (ceramic dual SIP)	—	**25**	1400	NOW	13-15
IDT7MC4001	1 Megabit (1024K x 1) static RAM module (ceramic SIP)	—	45	675	Q4'88	13-9
IDT8MP824	1 Megabit (128K x 8) plastic SIP RAM module	—	40	500	NOW	13-86
IDT8M824	1 Megabit (128K x 8) RAM module with monolithic pinout	**50**	40	550	NOW	13-107
IDT8MP624	1 Megabit (64K x 16) plastic SIP RAM module	—	40	875	NOW	13-74
IDT8M624	1 Megabit (64K x 16) RAM module with monolithic pinout	**50**	40	875	NOW	13-92
IDT7M624	1 Megabit (64K x 16, 128K x 8, 256K x 4) RAM module - customer configurable organization	35	25	4800	NOW	13-41

High-Speed CMOS Module Products (continued)

Part Number	Description	Max. Speed (ns) Mil.	Com'l.	Typical Power (mW)	Avail.	Data Book Page
IDT7M4017	2 Megabit (64K x 32) RAM module	**50**	40	6200	NOW	13-72
IDT7MP4008	4 Megabit (512K x 8) RAM module (plastic SIP)	—	40	1950	NOW	13-35
IDT7M4016	4 Megabit (256K x 16) RAM module	TBD	45	6200	Q4'88	13-70
APPLICATION SPECIFIC MODULES — Synchronous RAM Modules						
IDT7MP6025	512K (64K x 8) registered static RAM module	—	25MHz	3500	NOW	13-123
IDT7M824	1 Megabit (128K x 8) RAM module with registered buffered/latched addresses and I/Os	60	45	1500	NOW	13-168
IDT7M6001	32K x 20 double buffered RAM module with registered, multiplexed address	20MHz	25MHz	3750	NOW	13-197
IDT7M6028	16K x 8 high-speed synchronous RAM module	TBD	TBD	TBD	Q4'88	CALL
IDT7M6029	16K x 9 high-speed synchronous RAM module	TBD	TBD	TBD	Q4'88	CALL
APPLICATION SPECIFIC MODULES — Writable Control Store Modules						
IDT7M6032	16K x 32 high-speed writable control store with SPC™	30	25	4500	NOW	13-199
IDT7MB6042	8K x 112 high-speed writable control store with SPC™	—	30	8000	NOW	13-121
IDT7M6052	4K x 80 high-speed writable control store with onboard sequencer	TBD	TBD	TBD	Q4'88	CALL
APPLICATION SPECIFIC MODULES — Dual-Port Modules						
IDT7M134	64K (8K x 8) dual-port RAM module	60	45	950	NOW	13-125
IDT7M144	64K (8K x 8) functions as slave with IDT7M134 to provide 16-bit words or wider; pin compatible with IDT7M134	60	45	950	NOW	13-142
IDT7M135	128K (16K x 8) dual-port RAM module	60	45	1600	NOW	13-125
IDT7M145	128K (16K x 8) functions as slave with IDT7M135 to provide 16-bit words or wider; pin compatible with IDT7M135	60	45	1600	NOW	13-142
IDT7M137	256K (32K x 8) dual-port RAM module where on-chip arbitration is not needed	60	55	1375	NOW	13-135
IDT7MB6036	4K x 36 to 9 BiFIFO module	TBD	TBD	TBD	Q4'88	CALL
APPLICATION SPECIFIC MODULES — Cache Modules						
IDT7MB6039	Dual (16K x 60) cache module for MIPS R2000/R3000 system	TBD	25MHz	TBD	Q4'88	CALL
APPLICATION SPECIFIC MODULES — FIFO Modules						
IDT7M203	2K x 9 FIFO module using four IDT7201s	50	40	550	NOW	13-146
IDT7M204	4K x 9 FIFO module using four IDT202s	50	40	550	NOW	13-146
IDT7M205	8K x 9 FIFO module using four IDT203s	60	60	840	NOW	13-157
IDT7M206	16K x 9 FIFO module using four IDT7204s	60	60	840	NOW	13-157
IDT7MB2001	4K x 36/8K x 18 BiFIFO module	TBD	TBD	TBD	Q3'88	CALL

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High-Speed CMOS Multi-Port RAMs

- High speed, low power
- Independent read or write access to any memory location from any port
- Each port has separate controls, address and I/O
- On-chip port arbitration logic (except for IDT7134 and IDT7M137)
- Fully asynchronous operation from any port
- Several handshaking options (busy, interrupt, semaphores and combinations)
- Automatic power-down feature controlled by $\overline{CE}$
- 2V data retention battery back-up on all low-power devices

Part Number	Description	Max. Speed (ns) Mil.	Com'l.	Typical Power (mW)	Avail.	Data Book Page
DUAL-PORT RAMs						
IDT7130	8K (1K x 8) industry's most popular dual-port SRAM	45	35	325	NOW	5-1
IDT7140	8K (1K x 8) functions as slave with IDT7130 to provide 16-bit words or wider; pin compatible with IDT7130	45	35	325	NOW	5-1
IDT7132	16K (2K x8) fastest available speeds in this industry standard product; now multiple sourced	45	35	325	NOW	5-16
IDT7142	16K (2K x 8) functions as slave with IDT7132 to provide 16-bit words or wider; pin compatible with IDT7132	45	35	325	NOW	5-16
IDT71321	16K (2K x 8) high-speed dual-port with interrupt output	45	35	325	NOW	5-29
IDT71421	16K (2K x 8) functions as slave with IDT71321 to provide 16-bit words or wider; pin compatible with IDT71321	45	35	325	NOW	5-29
IDT71322	16K (2K x 8) with Semaphores	45	45	500	NOW	5-44
IDT7133	32K (2K x 16)	70	55	375	NOW	5-56
IDT7143	32K (2K x 16) functions as slave with IDT7133 to provide 32-bit words or wider	70	55	375	NOW	5-56
IDT7134	32K (4K x 8) high-speed operation in systems where on-chip arbitration is not needed	45	45	500	NOW	5-69
IDT71342	32K (4K x 8) with Semaphores	45	45	500	NOW	5-77
IDT7135	64K (4K x 16) with busy, interrupt, semaphore and master/slave select, all on one device	45	35	750	Jun '89	CALL
IDT7136	64K (8K x 8) with busy, interrupt, semaphore and master/slave select, all on one device	45	35	750	Jun '89	CALL
IDT7138	128K (8K x 16) industry's largest monolithic dual-port RAM with all the handshaking options (busy, interrupt, semaphores and master/slave) on one device	45	30	750	May '89	CALL
IDT7139	128K (16K x 8) with busy, interrupt, semaphore and master/slave select, all on one device	45	35	750	Jun '89	CALL
FOUR-PORT RAMs						
IDT71240	8K (1K x 8) four-port SRAM offers increased-system performance in multiprocessor systems that have a need to communicate in real time	35	25	750	Mar '89	CALL
IDT71242	16K (2K x 8) four-port SRAM offers added benefits for high-speed systems in which multiple access is required in the same cycle	35	25	750	Jan '89	CALL

High-Speed CMOS FIFOs

- High speed, low power FIFO products
- TTL compatible
- All products MIL-STD-883 compliant

INDUSTRY STANDARD FIFOS

- Five pin-compatible versions
- Asynchronous, simultaneous read and write
- Simple width and depth expandability
- Space efficient packaging
- Full, empty and half-full flags
- Available in high reliability FIFO modules - up to 16K x 9

FLAGGED FIFOS

- Multiple flags - Full, empty, half-full, almost-empty, almost-full
- Incorporates output enable

PARALLEL/SERIAL FIFOS

- Input/Output is user configurable - P/S, S/P, P/P or S/S
- FLEXISHIFT™ allows for easy programmable serial word widths
- Multiple flags - Full, almost-full, full - 1, empty, almost-empty, empty +1 and half-full

BIDIRECTIONAL FIFO

- Matches different bus widths: 16-bit to 8-bit buses & 32-bit to 8-bit buses
- REQ/ACK interface built on-chip
- 8 programmable status flags (offset and polarity)

Part Number	Description	Max. Speed (ns) Mil.	Max. Speed (ns) Com'l.	Typical Power (mW)	Avail.	Data Book Page
STANDARD FIFOs						
IDT72401	64 x 4 (replaces 67401)	35MHz	45MHz	175	NOW	6-69
IDT72402	64 x 5 (replaces 67402)	35MHz	45MHz	175	NOW	6-69
IDT72403	64 x 4 with $\overline{OE}$ (replaces 67403)	35MHz	45MHz	175	NOW	6-69
IDT72404	64 x 5 with $\overline{OE}$ (replaces 67404)	35MHz	45MHz	175	NOW	6-69
IDT72413	64 x 5 with $\overline{OE}$, Half-Full, Almost-Empty, Almost-Full flags (replaces 67413)	35MHz	45MHz	300	NOW	6-80
IDT7200	256 x 9, 28-pin 300 mil DIP	30	25	312	NOW	6-1
IDT7201A	512 x 9 with Half-Full Flag	30	25	312	NOW	6-1
IDT7202A	1K x 9 with Half-Full Flag	**30**	**25**	312	NOW	6-14
IDT7203	2K x 9 with Half-Full Flag	**40**	**35**	375	NOW	6-28
IDT7M203	2K x 9 FIFO Module	50	40	550	NOW	13-146
IDT7204	4K x 9 with Half-Full Flag	**40**	**35**	375	NOW	6-28
IDT7M204	4K x 9 FIFO Module	50	40	550	NOW	13-146
IDT7M205	8K x 9 FIFO Module	60	40	840	NOW	13-157
IDT7M206	16K x 9 FIFO Module	60	40	840	NOW	13-157
FLAGGED FIFOs						
IDT72021	1K x 9 with Half-Full, Almost-Empty, Almost-Full flags and $\overline{OE}$	30	25	312	NOW	6-27
IDT72031	2K x 9 with Half-Full, Almost-Empty, Almost-Full flags and $\overline{OE}$	**40**	**35**	375	NOW	CALL
IDT72041	4K x 9 with Half-Full, Almost-Empty, Almost-Full flags and $\overline{OE}$	**40**	**35**	375	NOW	6-41
BIDIRECTIONAL FIFOs						
IDT7252	1K x 18—2K x 9 Bidirectional FIFO	**40**	**35**	350	Q1'89	6-91
IDT72520	1K x 18—2K x 9 Bidirectional FIFO	40	35	350	Q1'89	CALL
IDT72521	1K x 18—1K x 18 Bidirectional FIFO	40	35	350	Q1'89	CALL

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High-Speed CMOS FIFOs (continued)

Part Number	Description	Max. Speed (ns) Mil.	Com'l.	Typical Power (mW)	Avail.	Data Book Page
PARALLEL/SERIAL FIFOs						
IDT72103	2K x 9 configurable Parallel/Serial I/O, multiple flags, 50MHz serial rate and FLEXISHIFT™	**40**	**35**	450	NOW	6-43
IDT72104	4K x 9 configurable Parallel/Serial I/O, multiple flags, 50MHz serial rate and FLEXISHIFT™	**40**	**35**	450	NOW	6-43
IDT72131	2K x 9 dedicated Parallel-to-Serial I/O, 50MHz serial rate, multiple flags and FLEXISHIFT™	40	35	450	Nov '88	CALL
IDT72132	2K x 9 dedicated Serial-to-Parallel I/O, 50MHz serial rate, multiple flags and FLEXISHIFT™	40	35	450	Nov '88	CALL
IDT72141	4K x 9 dedicated Parallel-to-Serial I/O, 50MHz serial rate, multiple flags and FLEXISHIFT™	40	35	450	NOW	CALL
IDT72142	4K x 9 dedicated Serial-to-Parallel I/O, 50MHz serial rate, multiple flags and FLEXISHIFT™	40	35	450	Nov '88	CALL

High-Speed CMOS DSP Building Blocks

- High speed, low power DSP building blocks
- TTL-compatible
- All products MIL-STD-883 compliant

ADVANCED DSP BUILDING BLOCKS

- Very fast 50MHz components
- Supports both 16- and 32-bit integer formats
- Advanced ALU features for DSP performance

PARALLEL MULTIPLIERS

- Configured for easy array expansion
- User-controlled option for transparent output register mode
- Round Control for the MSP

PARALLEL MACs

- Selectable accumulation, rounding, and pre-loading
- Extended product output for multiple accumulations
- Pre-load function allows output register to be preset
- All devices perform subtraction and double-precision addition and multiplication

Part Number	Description	Max. Speed (ns) Mil.	Com'l.	Typical Power (mW)	Avail.	Data Book Page
ADVANCED DSP BUILDING BLOCKS						
IDT7320	16-bit eight-level Pipeline Register	15	10	150	Q2'89	7-68
IDT7321	16-bit seven-level Pipeline Register	15	10	150	Q2'89	CALL
IDT7317	16 x 16-bit Parallel Multiplier with 32-bit output	25	20	250	Q1'89	7-66
IDT7381	16-bit Cascadable ALU	**25**	**20**	150	Q1'89	7-70
IDT7383	16-bit Cascadable ALU	25	20	150	Q1'89	CALL
IDT7384	16-bit advanced Cascadable ALU	25	20	200	Q1'89	CALL
MACs						
IDT7209	12 x 12-bit, replaces TDC1009J	55	45	200	NOW	7-1
IDT7210	16 x 16-bit with 35-bit output, replaces TDC1010J	**30**	**25**	225	NOW	7-9
IDT7243	16 x 16-bit with 19-bit output, replaces TDC1043	55	45	225	NOW	7-9
MULTIPLIERS						
IDT7212	12 x 12-bit, replaces MPY012H	40	35	150	NOW	7-20
IDT7213	12 x 12-bit with single clock architecture	40	35	150	NOW	7-20
IDT7216	16 x 16-bit, replaces Am29516	**25**	**20**	200	NOW	7-55
IDT7217	16 x 16-bit with single clock architecture, replaces Am29517	**25**	**20**	200	NOW	7-55
FLOATING-POINT						
IDT721264	32- / 64-bit IEEE Multiplier, replaces WTL1264	(32-bit Ops) 12.5Mflop (64-bit Ops) 6.2Mflop	16.7Mflop 8.3Mflop	250	NOW	7-30
IDT721265	32- / 64-bit IEEE ALU, replaces WTL1265	(32-bit Ops) 12.5Mflop (64-bit Ops) 12.5Mflop	16.7Mflop 16.7Mflop	250	NOW	7-30

Integrated Device Technology

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High-Speed CMOS MICROSLICE™ Products

CMOS MICROPROGRAMMABLE MICROPROCESSOR FAMILY

- IDT49C400 products offer dramatically improved system performance through innovative architectures
- IDT39C00 products are pin-compatible, microcode-compatible, performance-enhanced Am2900 family replacements
- Faster than bipolar equivalent circuits: 20-40% faster
- Lower power than bipolar equivalent circuits: 70-80% less power
- Higher output drive than bipolar equivalent circuits

CMOS ERROR DETECTION AND CORRECTION FAMILY

- Provides soft and hard error checking and correcting scheme for high-density, high-reliability memory systems
- Corrects all single bit errors; detects all double bit errors

Part Number	Description	Speed	Typical Power (mW)	Avail.	Data Book Page
MICROPROCESSORS					
IDT39C01C	4-bit µP Slice —	A,B addr to Y = 40ns	125	NOW	8-1
IDT39C01D	replaces Am2901B/C, Am29C01,	A,B addr to Y = 30ns		NOW	8-1
IDT39C01E	CY7C901	A,B addr to Y = 22ns		NOW	8-1
IDT39C03A	4-bit µP Slice —	A,B addr to Y = 67ns	150	NOW	8-16
IDT39C03B	replaces Am2903/A	A,B addr to Y = 54ns		NOW	8-16
IDT49C402	16-bit µP Slice, quad 2901 with 8	A,B addr to Y = 47ns	350	NOW	8-139
IDT49C402A	additional destination functions and 64 x 16 register file capacity — superset of Am29C101, CY7C9101, WSI59016	A,B addr to Y = 37ns		NOW	8-139
IDT49C403	16-bit µP Slice, quad 2903/29203 with	A,B addr to Y = 49ns	450	NOW	8-150
IDT49C403A	64 x 16 register file, 4 Q registers, word/byte control, byte swap and SPC™	A,B addr to Y = 41ns		NOW	8-150
IDT49C404	32-bit µP Slice, 3-port with 32-bit	Cycle Time = 100ns	1250	Q1'89	8-182
IDT49C404A	ALU, 64 x 32 7-port register file, 64-bit cascadable funnel shifter, priority encoder, merge logic and mask generator — replaces two Am29334s and one Am29332	Cycle Time = 80ns		Q1'89	8-182
SEQUENCERS					
IDT39C10B	12-bit Sequencer with 33-deep stack —	D to Y = 20ns	150	NOW	8-63
IDT39C10C	replaces Am2910/A, CY7C910	D to Y = 12ns		NOW	8-63
IDT49C410	16-bit Sequencer with 33-deep stack	D to Y = 20ns	150	NOW	8-196
IDT49C410A	addresses up to 64K microcode	D to Y = 12ns		NOW	8-196
ERROR DETECTION AND CORRECTION					
IDT39C60	16-bit Cascadable EDC —	Detect Time = 32ns	265	NOW	8-209
IDT39C60-1	replaces Am2960,-1,A; N2960;	Detect Time = 25ns		NOW	8-209
IDT39C60A	MC74F2960,-1,A	Detect Time = 20ns		NOW	8-209
IDT49C460	32-bit Cascadable EDC —	Detect Time = 40ns	300	NOW	8-235
IDT49C460A	functional equivalent to DP8402;	Detect Time = 30ns		NOW	8-235
IDT49C460B	AS/ALS632	Detect Time = 25ns		NOW	8-235
IDT49C460C		Detect Time = 16ns		Q4'88	CALL
OTHER					
IDT39C02A	Carry Lookahead Generator — replaces Am2902A		80	NOW	8-12
IDT49C25	Microcycle Length Controller — replaces Am2925		80	NOW	8-117
IDT71502	4Kx16 Registered RAM for Writable Control Store applications		350	NOW	4-224

High-Speed CMOS Data Conversion Products

- High speed – low power
- Available in military and commercial temperature ranges
- Produced with advanced CEMOS™ high-performance technology

VIDEO DACs

- IDT75C18 is pin and function compatible with TRW 1018 with half the power consumption
- IDT75C19 is world's first CMOS 9-bit video DAC
- IDT75C451/7/8 PaletteDAC™ is pin and function compatible with Brooktree BT451/7/8 with reduced power consumption and faster speed grades. MIL-STD-883 compliant devices are available
- IDT75MB38 is a triple 8-bit, 125MHz module with on-board voltage reference.

FLASH A/D CONVERTERS

- IDT75C48 is pin and function compatible with TRW 1048 with half the power consumption, on-chip Error Detection and Correction, extended analog input range and improved output characteristics
- IDT75C58 has enhanced features such as overflow output and three state control which allows stacking two devices for 9-bit resolution
- IDT75MB58 is a complete Flash ADC module product with input buffer amplifier, reference voltage generator and optimized layout and decoupling.

Part Number	Description	Replaces	Typical Power (mW)	Avail.	Data Book Page
DAC					
IDT75C18	8-bit, 125MHz Video DAC with ECL inputs	TDC1018	400	NOW	11-1
IDT75C19	World's first 9-bit, 125MHz Video DAC		400	NOW	11-12
IDT75MB38	Triple 8-bit, 125MHz Video DAC Module	TDC1318, BT109	1500	NOW	11-23
IDT75C451	Triple 4-bit, 165MHz PaletteDAC™	BT451	1000	NOW	CALL
IDT75C457	Single 8-bit, 165MHz PaletteDAC™	BT457	1000	Q1'89	CALL
IDT75C458	Triple 8-bit, 165MHz PaletteDAC™	BT458	1000	NOW	11-29
ADC					
IDT75C48	8-bit, 20MHz Flash ADC	TDC1048	500	NOW	11-42
IDT75C58	8-bit, 20MHz Flash ADC with Overflow output		500	NOW	11-40
IDT75MB58	Complete Flash Module using IDT75C58s		800	Q4'88	11-58

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High-Speed CMOS Logic Products

- FCTXXXA devices 35%-50% faster then FAST™ with equivalent output drive but at dramatically lower CMOS power over full temperature and voltage supply extremes
- FCT devices same speed and output drive as FAST™ but at dramatically lower CMOS power
- 54/74FCT8XXA devices same speed and output drive as 29800, but dramatically lower CMOS power
- 54/74FCT8XXB devices 30%-40% faster than 29800 with equivalent output drive, but at dramatically lower CMOS power
- Both CMOS and TTL output compatible (eliminates need for pull-up resistors when driving CMOS static RAMs)
- Substantially lower input current levels than FAST™, ALS or 29800 (5μA max.)
- JEDEC standard pinout for DIP and LCC
- Pin-compatible with industry standard MSI logic
- Devices formerly designated 39CXXX are now designated 54/74FCT8XXXA or 29FCTXXXA

Part Number	Description	Max. Speed (ns) Mil.	Com'l.	Typical Power (mW)	Avail.	Data Book Page
IDT29FCT52A	Octal Registered Transceiver	11.0	10.0	10.0	NOW	10-1
IDT29FCT53A	Octal Registered Transceiver	11.0	10.0	10.0	NOW	10-1
IDT29FCT52B	Octal Registered Transceiver	8.0	7.5	10.0	NOW	10-1
IDT29FCT53B	Octal Registered Transceiver	8.0	7.5	10.0	NOW	10-1
IDT29FCT520A	Multilevel Pipeline Register	16.0	14.0	10.0	NOW	10-6
IDT29FCT520B	Multilevel Pipeline Register	**8.0**	**7.5**	10.0	NOW	10-6
IDT49FCT601	16-Bit Bidirectional Latch w/Byte-Swap	—	—	20.0	Q1'89	10-12
IDT49FCT618	16-Bit Register with SPC™	14.0	12.5	20.0	Q1'89	10-13
IDT49FCT661	16-Bit Synchronous Binary Counter	—	—	20.0	Q1'89	10-29
IDT49FCT818	Octal Register with SPC™	14.0	12.5	10.0	NOW	10-30
IDT49FCT818A	Octal Register with SPC™	**10.0**	**9.0**	10.0	NOW	10-30
IDT54/74FCT521B	8-Bit Comparator	7.3	5.5	10.0	NOW	10-113
IDT54/74FCT138A	1-of-8 Decoder	7.8	5.8	10.0	NOW	10-43
IDT54/74FCT139A	Dual 1-of-4 Decoder	7.8	5.9	10.0	NOW	10-48
IDT54/74FCT161A	Synchronous Binary Counter	7.5	7.2	10.0	NOW	10-52
IDT54/74FCT163A	Synchronous Binary Counter	7.5	7.2	10.0	NOW	10-52
IDT54/74FCT182A	Carry Lookahead Generator	10.7	7.0	10.0	NOW	10-57
IDT54/74FCT191A	Up/Down Binary Counter	10.5	7.8	10.0	Q1'89	10-62
IDT54/74FCT193A	Up/Down Binary Counter	6.9	6.5	10.0	Q1'89	10-67
IDT54/74FCT240A	Octal Buffer	5.1	4.8	10.0	NOW	10-72
IDT54/74FCT241A	Octal Buffer	5.1	4.8	10.0	NOW	10-76
IDT54/74FCT244A	Octal Buffer	5.1	4.8	10.0	NOW	10-76
IDT54/74FCT245A	Octal Bidirectional Transceiver	4.9	4.6	10.0	NOW	10-82
IDT54/74FCT273A	Octal D Flip-Flop	8.3	7.2	10.0	NOW	10-86
IDT54/74FCT299A	Octal Universal Shift Register	9.5	7.2	10.0	NOW	10-90
IDT54/74FCT373A	Octal Transparent Latch	5.6	5.2	10.0	NOW	10-95
IDT54/74FCT374A	Octal D Flip-Flop	7.2	6.5	10.0	NOW	10-99
IDT54/74FCT377A	Octal D Flip-Flop	8.3	7.2	10.0	NOW	10-103
IDT54/74FCT399A	Quad Dual-Port Register	7.5	7.0	10.0	NOW	10-107
IDT54/74FCT521A	8-Bit Comparator	9.5	7.2	10.0	NOW	10-113
IDT54/74FCT533A	Octal Transparent Latch	5.6	5.2	10.0	NOW	10-117
IDT54/74FCT534A	Octal D Flip-Flop	7.2	6.5	10.0	NOW	10-121

High-Speed CMOS Logic Products (continued)

Part Number	Description	Max. Speed (ns) Mil.	Max. Speed (ns) Com'l.	Typical Power (mW)	Avail.	Data Book Page
IDT54/74FCT540A	Octal Inverting Buffer	**5.1**	**4.8**	10.0	NOW	10-125
IDT54/74FCT541A	Octal Non-inverting Buffer	**5.1**	**4.8**	10.0	NOW	10-125
IDT54/74FCT543A	Octal Non-inverting Latched Transceiver	**7.5**	**6.5**	10.0	NOW	10-129
IDT54/74FCT573A	Octal Transparent Latch	5.6	5.2	10.0	NOW	10-135
IDT54/74FCT574A	Octal D Register	7.2	6.5	10.0	NOW	10-139
IDT54/74FCT640A	Octal Bidirectional Transceiver	5.3	5.0	10.0	NOW	10-143
IDT54/74FCT645A	Octal Bidirectional Transceiver	4.9	4.6	10.0	NOW	10-147
IDT54/74FCT646A	Octal Non-inverting Registered	7.7	6.3	10.0	Q1'89	10-151
IDT54/74FCT648A	Octal Inverting Registered Transceiver	6.3	5.6	10.0	Q1'89	10-151
IDT54/74FCT651A	Octal Non-inverting Registered Transceiver	—	—	10.0	Q1'89	10-157
IDT54/74FCT652A	Octal Inverting Registered Transceiver	—	—	10.0	Q1'89	10-157
IDT54/74FCT821A	10-Bit Non-inverting Register	12.0	12.0	10.0	NOW	10-164
IDT54/74FCT823A	9-Bit Non-inverting Register	12.0	12.0	10.0	NOW	10-164
IDT54/74FCT824A	9-Bit Inverting Register	12.0	12.0	10.0	NOW	10-164
IDT54/74FCT825A	8-Bit Non-inverting Register	12.0	12.0	10.0	NOW	10-164
IDT54/74FCT827A	10-Bit Non-inverting Buffer	10.0	8.0	10.0	NOW	10-171
IDT54/74FCT833A	8-Bit Transceiver w/Parity	14.0	10.0	10.0	NOW	10-177
IDT54/74FCT834A	8-Bit Transceiver w/Parity	14.0	10.0	10.0	Q4'88	10-177
IDT54/74FCT841A	10-Bit Non-inverting Latch	11.0	9.5	10.0	NOW	10-185
IDT54/74FCT843A	9-Bit Non-inverting Latch	11.0	9.5	10.0	NOW	10-185
IDT54/74FCT844A	9-Bit Inverting Latch	12.0	10.0	10.0	NOW	10-185
IDT54/74FCT845A	8-Bit Non-inverting Latch	11.0	9.5	10.0	NOW	10-185
IDT54/74FCT853A	8-Bit Transceiver w/Parity	14.0	10.0	10.0	Q4'88	10-177
IDT54/74FCT854A	8-Bit Transceiver w/Parity	14.0	10.0	10.0	Q4'88	10-177
IDT54/74FCT861A	10-Bit Non-inverting Transceiver	10.0	8.0	10.0	NOW	10-192
DT54/74FCT863A	9-Bit Non-inverting Transceiver	10.0	8.0	10.0	NOW	10-192
IDT54/74FCT864A	9-Bit Inverting Transceiver	9.5	8.5	10.0	NOW	10-192
IDT54/74FCT138	1-of-8 Decoder	12.0	9.0	10.0	NOW	10-43
IDT54/74FCT139	Dual 1-of-4 Decoder	12.0	9.0	10.0	NOW	10-48
IDT54/74FCT161	Synchronous Binary Counter	11.5	11.0	10.0	NOW	10-52
IDT54/74FCT163	Synchronous Binary Counter	11.5	11.0	10.0	NOW	10-52
IDT54/74FCT182	Carry Lookahead Generator	16.5	10.0	10.0	NOW	10-57
IDT54/74FCT191	Up/Down Binary Counter	16.0	12.0	10.0	Q1'89	10-62
IDT54/74FCT193	Up/Down Binary Counter	10.5	10.0	10.0	Q1'89	10-67
IDT54/74FCT240	Octal Buffer	9.0	8.0	10.0	NOW	10-72
IDT54/74FCT241	Octal Buffer	7.0	6.5	10.0	NOW	10-76
IDT54/74FCT244	Octal Buffer	7.0	6.5	10.0	NOW	10-76
IDT54/74FCT245	Octal Bidirectional Transceiver	7.5	7.0	10.0	NOW	10-82
IDT54/74FCT273	Octal D Flip-Flop	15.0	13.0	10.0	NOW	10-86
IDT54/74FCT299	Octal Universal Shift Transceiver	14.0	10.0	10.0	NOW	10-90
IDT54/74FCT373	Octal Transparent Latch	8.5	8.0	10.0	NOW	10-95
IDT54/74FCT374	Octal D Flip-Flop	11.0	10.0	10.0	NOW	10-99
IDT54/74FCT377	Octal D Flip-Flop	15.0	13.0	10.0	NOW	10-103

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Part Number	Description	Max. Speed (ns) Mil.	Com'l.	Typical Power (mW)	Avail.	Data Book Page
IDT54/74FCT399	Quad Dual-Port Register	11.5	10.0	10.0	NOW	10-107
IDT54/74FCT521	8-Bit Comparator	15.0	11.0	10.0	NOW	10-113
IDT54/74FCT533	Octal Transparent Latch	12.0	10.0	10.0	NOW	10-117
IDT54/74FCT534	Octal D Flip-Flop	11.0	10.0	10.0	NOW	10-121
IDT54/74FCT540	Octal Inverting Buffer	9.0	8.0	10.0	NOW	10-125
IDT54/74FCT541	Octal Non-inverting Buffer	9.0	8.0	10.0	NOW	10-125
IDT54/74FCT543	Octal Non-inverting Latched Transceiver	10.0	8.5	10.0	NOW	10-129
IDT54/74FCT573	Octal Transparent Latch	8.5	8.0	10.0	NOW	10-135
IDT54/74FCT574	Octal D Register	11.0	10.0	10.0	NOW	10-139
IDT54/74FCT640	Octal Bidirectional Transceiver	8.0	7.0	10.0	NOW	10-143
IDT54/74FCT645	Octal Bidirectional Transceiver	11.0	9.5	10.0	NOW	10-147
IDT54/74FCT646	Octal Non-inverting Reg. Transceiver	11.0	9.0	10.0	NOW	10-151
IDT54/74FCT648	Octal Inverting Registered Transceiver	9.0	8.0	10.0	Q1'89	10-151
IDT54/74FCT651	Octal Non-inverting Reg. Transceiver	10.0	9.0	10.0	Q1'89	10-157
IDT54/74FCT652	Octal Inverting Registered Transceiver	9.0	8.0	10.0	Q1'89	10-157
IDT54/74FCT821B	10-Bit Non-inverting Register	8.5	7.5	10.0	NOW	10-164
IDT54/74FCT823B	9-Bit Non-inverting Register	8.5	7.5	10.0	NOW	10-164
IDT54/74FCT824B	9-Bit Inverting Register	8.5	7.5	10.0	NOW	10-164
IDT54/74FCT825B	8-Bit Non-inverting Register	8.5	7.5	10.0	NOW	10-164
IDT54/74FCT827B	10-Bit Non-inverting Buffer	6.5	5.0	10.0	NOW	10-171
IDT54/74FCT833B	8-Bit Transceiver w/Parity	10.0	7.0	10.0	Q2'88	10-177
IDT54/74FCT834B	8-Bit Transceiver w/Parity	10.0	7.0	10.0	Q4'88	10-177
IDT54/74FCT841B	10-Bit Non-inverting Latch	7.5	6.5	10.0	NOW	10-185
IDT54/74FCT843B	9-Bit Non-inverting Latch	7.5	6.5	10.0	NOW	10-177
IDT54/74FCT844B	9-Bit Inverting Latch	9.0	8.0	10.0	NOW	10-177
IDT54/74FCT845B	8-Bit Non-inverting Latch	7.5	6.5	10.0	NOW	10-185
IDT54/74FCT853B	8-Bit Transceiver w/Parity	10.0	7.0	10.0	Q4'88	10-177
IDT54/74FCT854B	8-Bit Transceiver w/Parity	10.0	7.0	10.0	Q4'88	10-177
IDT54/74FCT861B	10-Bit Non-inverting Transceiver	6.5	6.0	10.0	NOW	10-192
IDT54/74FCT863B	9-Bit Non-inverting Transceiver	6.5	6.0	10.0	NOW	10-192
IDT54/74FCT864B	9-Bit Inverting Transceiver	6.5	5.5	10.0	NOW	10-192
IDT54AHCT138	1-of-8 Decoder	27.0	—	3.5	NOW	10-198
IDT54AHCT139	Dual 1-of-4 Decoder	25.0	—	3.5	NOW	10-202
IDT54AHCT161	Synchronous Binary Counter	20.0	—	3.5	NOW	10-206
IDT54AHCT163	Synchronous Binary Counter	20.0	—	5.0	NOW	10-206
IDT54AHCT182	Carry Lookahead Generator	20.5	—	3.5	NOW	10-211
IDT54AHCT191	Up/Down Binary Counter	22.0	—	5.0	NOW	10-216
IDT54AHCT193	Up/Down Binary Counter	19.0	—	3.5	NOW	10-220
IDT54AHCT240	Octal Buffer	12.0	—	3.5	NOW	10-225
IDT54AHCT244	Octal Buffer	13.0	—	3.5	NOW	10-229
IDT54AHCT245	Octal Bidirectional Transceiver	15.0	—	3.5	NOW	10-233
IDT54AHCT273	Octal D Flip-Flop	17.0	—	3.5	NOW	10-237
IDT54AHCT299	Universal Shift Register	17.0	—	3.5	NOW	10-241

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Part Number	Description	Max. Speed (ns) Mil.	Com'l.	Typical Power (mW)	Avail.	Data Book Page
IDT54AHCT373	Octal Transparent Latch	19.0	—	3.5	NOW	10-245
IDT54AHCT374	Octal D Flip-Flop	18.0	—	3.5	NOW	10-249
IDT54AHCT377	Octal D Flip-Flop	20.0	—	3.5	NOW	10-253
IDT54AHCT521	8-Bit Comparator	17.0	—	3.5	NOW	10-257
IDT54AHCT533	Octal Transparent Latch	24.0	—	3.5	NOW	10-261
IDT54AHCT534	Octal D Flip-Flop	18.0	—	3.5	NOW	10-265
IDT54AHCT573	Octal Transparent Latch	15.0	—	3.5	NOW	10-269
IDT54AHCT574	Octal D Register	15.0	—	3.5	NOW	10-273
IDT54AHCT640	Octal Bidirectional Transceiver	14.0	—	3.5	NOW	10-277
IDT54AHCT645	Octal Bidirectional Transceiver	15.0	—	3.5	NOW	10-281

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HIGH-SPEED BiCMOS ECL STATIC RAM 64K (64K x 1-BIT)

PRELIMINARY
IDT100490

FEATURES:

- 65,536-words x 1-bit organization
- Low power dissipation: 320mW (typ.)
- Fully compatible with 100K logic level
- Address access time: 10/12/15/20ns (max.)
- Write pulse width: 8ns (min.)
- Open emitter output for ease of memory expansion
- Static operation: no clocks or refresh required
- Separate data input and output
- JEDEC standard high-density 22-pin plastic DIP and CERDIP and 24-pin Small Outline J-Bend IC

DESCRIPTION:

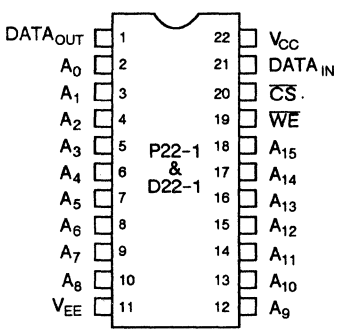
The IDT100490 is a 100K compatible 65,536-bit high-speed BiCEMOS™ ECL static RAM organized as 64K x 1.

The IDT100490 is available with address access times as fast as 10ns with a typical power consumption of only 320mW. This product offers the advantages of low-power operation, without sacrificing speed, by integrating a dense high-speed CMOS static RAM with internal level conversion. This allows the designer to reduce package count in an ECL system without increasing either power dissipation or access time.

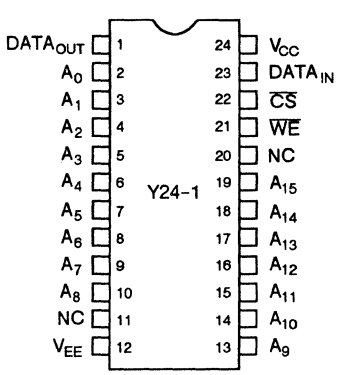
Designed for very high-speed applications, the IDT100490 is fully compatible with standard ECL 100K logic levels and offers extremely fast access times. The address access time of 10ns and write pulse width of 8ns assure that operations of this BiCEMOS part will be as fast as those available with less dense parts requiring external address decoding.

The IDT100490 is fabricated using IDT's high-performance, high-reliability BiCEMOS technology. Operating power dissipation is extremely low compared with most ECL-compatible bipolar devices, lowering power supply and cooling requirements.

PIN CONFIGURATIONS

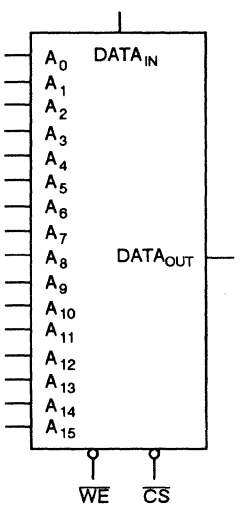


DIP, TOP VIEW

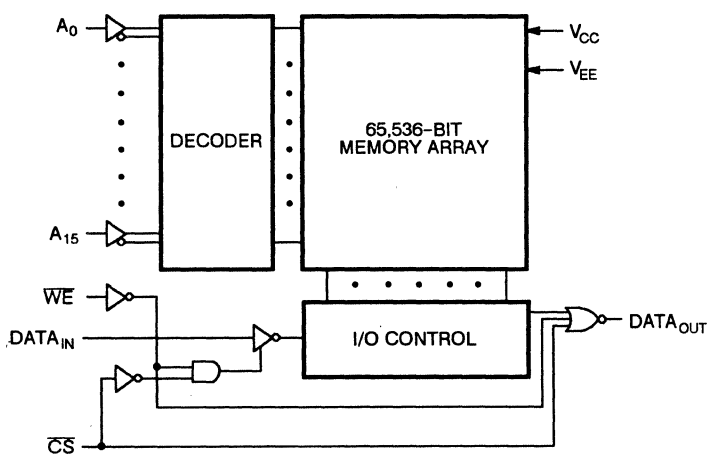


SOJ, TOP VIEW

LOGIC SYMBOL



FUNCTIONAL BLOCK DIAGRAM



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Integrated Device Technology, Inc

HIGH-SPEED BiCMOS ECL STATIC RAM 64K (64K x 1-BIT)

PRELIMINARY
IDT10490

FEATURES:

- 65,536-words x 1-bit organization
- Low power dissipation: 420mW (typ.)
- Fully compatible with 10K logic level
- Address access time: 10/12/15/20ns (max.)
- Write pulse width: 8ns (min.)
- Open emitter output for ease of memory expansion
- Static operation: no clocks or refresh required
- Separate data input and output
- JEDEC standard high-density 22-pin CERDIP

DESCRIPTION:

The IDT10490 is a 10K compatible 65,536-bit high-speed BiCEMOS™ ECL static RAM organized as 64K x 1.

The IDT10490 is available with address access times as fast as 10ns with a typical power consumption of only 420mW. This product offers the advantages of low-power operation, without sacrificing speed, by integrating a dense high-speed CMOS static RAM with internal level conversion. This allows the designer to reduce package count in an ECL system without increasing either power dissipation or access time.

Designed for very high-speed applications, the IDT10490 is fully compatible with standard ECL 10K logic levels and offers extremely fast access times. The address access time of 10ns and write pulse width of 8ns assure that operations of this BiCEMOS part will be as fast as those available with less dense parts requiring external address decoding.

The IDT10490 is fabricated using IDT's high-performance, high-reliability BiCEMOS technology. Operating power dissipation is extremely low compared with most ECL-compatible bipolar devices, lowering power supply and cooling requirements.

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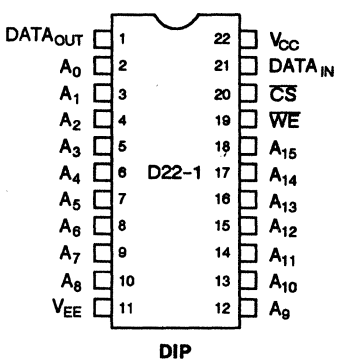
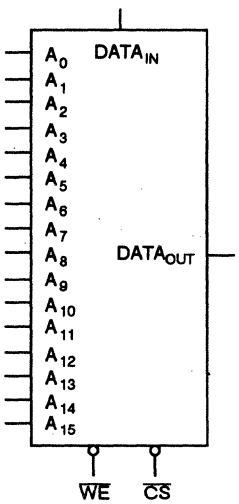
PIN CONFIGURATIONS

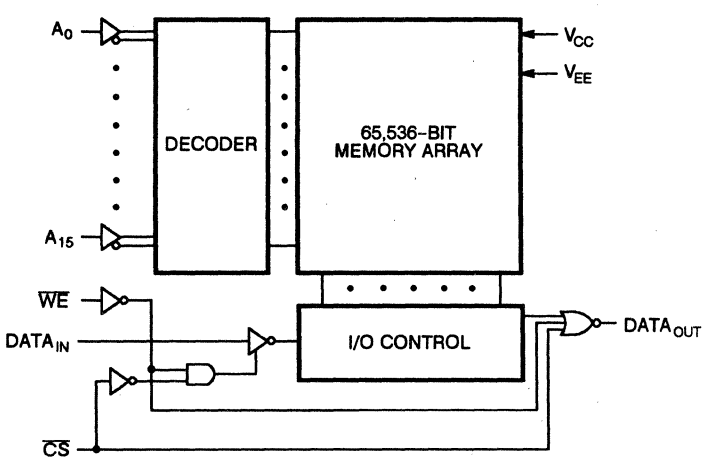


DIP
TOP VIEW

LOGIC SYMBOL



FUNCTIONAL BLOCK DIAGRAM



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HIGH-SPEED BiCMOS ECL STATIC RAM 64K (16K x 4-BIT)

ADVANCE INFORMATION
IDT10494
IDT100494

FEATURES:

- 16,384-words x 4-bit organization
- Address access time: 10/12/15ns (max.)
- Low power dissipation: 600mW (typ.)
- Fully compatible with ECL logic levels
- Open emitter output for ease of memory expansion
- Separate data input and output
- Static operation: no refresh required
- JEDEC standard through-hole and surface mount packages

DESCRIPTION:

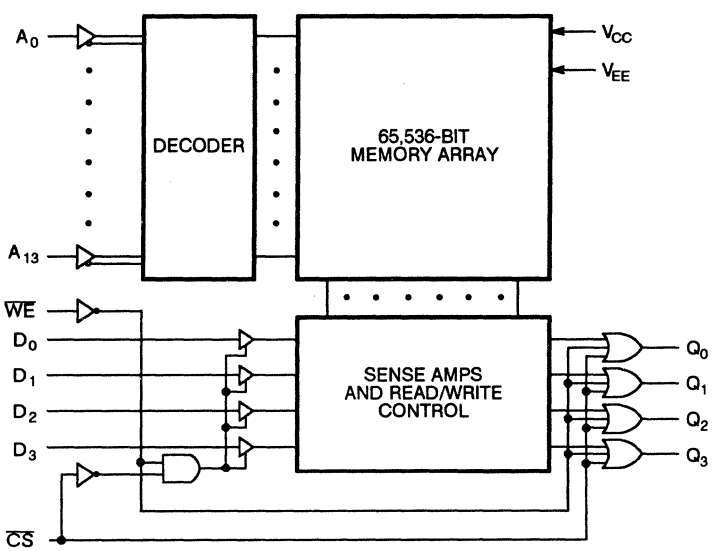
The IDT10494 and IDT100494 are 65,536-bit high-speed BiCEMOS™ ECL static random access memories organized as 16K x 4, with inputs and outputs fully compatible with ECL 10K and ECL 100K, respectively.

Available with address access times as fast as 10ns, these devices exhibit a typical power consumption of only 600mW. They offer the advantages of low-power operation, without sacrificing speed, by integrating a dense high-speed CMOS static RAM with internal level conversion. This allows the designer to reduce package count in an ECL system without increasing either power dissipation or access time.

Designed for very high-speed applications, the IDT10494 and IDT100494 offer open emitter outputs and separate data input and output, as well as extremely fast access times. The address access time of 10ns assures that operation of this BiCEMOS part will be as fast as with less dense parts requiring external address decoding.

The devices are fabricated using IDT's high-performance, high-reliability BiCEMOS technology. Operating power dissipation is extremely low compared with most ECL-compatible bipolar devices, lowering power supply and cooling requirements.

FUNCTIONAL BLOCK DIAGRAM



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HIGH-SPEED BiCMOS ECL SELF-TIMED STATIC RAM 64K (16K x 4-BIT) STRAM

ADVANCE INFORMATION
IDT10496LL
IDT100496LL

FEATURES:

- 16,384-words x 4-bit organization
- Self-timed, with latches on inputs and outputs
- Cycle time 15/18ns
- Address access time: 12/15ns (max.)
- Low power dissipation: 800mW (typ.)
- Fully compatible with ECL logic levels
- Open emitter output for ease of memory expansion
- Separate data input and output
- Static operation: no refresh required
- JEDEC standard through-hole and surface mount packages

DESCRIPTION:

The IDT10496LL and IDT100496LL are 65,536-bit high-speed BiCEMOS™ ECL static random access memories organized as 16K x 4, with inputs and outputs fully compatible with ECL 10K and ECL 100K, respectively. These devices have on-board self-timed circuitry to relax control timing, providing easier design and improved system level cycle times.

Clocked latches on inputs and outputs, and the self-generated write operation, provide enhanced system performance over conventional RAMs by removing the need to control any write pulse width, and relaxes timing of write enable ($\overline{WE}$). Combined with address access times as fast as 12ns, the IDT10496LL and IDT100496LL allow cycle times as fast as 15ns.

The IDT10496LL and IDT100496LL are fabricated using IDT's high-performance, high-reliability BiCEMOS technology. They offer the advantage of low-power operation without sacrificing speed by integrating a dense, high-speed CMOS static RAM and logic with internal level conversion. Power supply and cooling requirements are reduced, while the fast access time assures that operation of these BiCEMOS parts will be as fast as with less dense parts requiring external address decoding.

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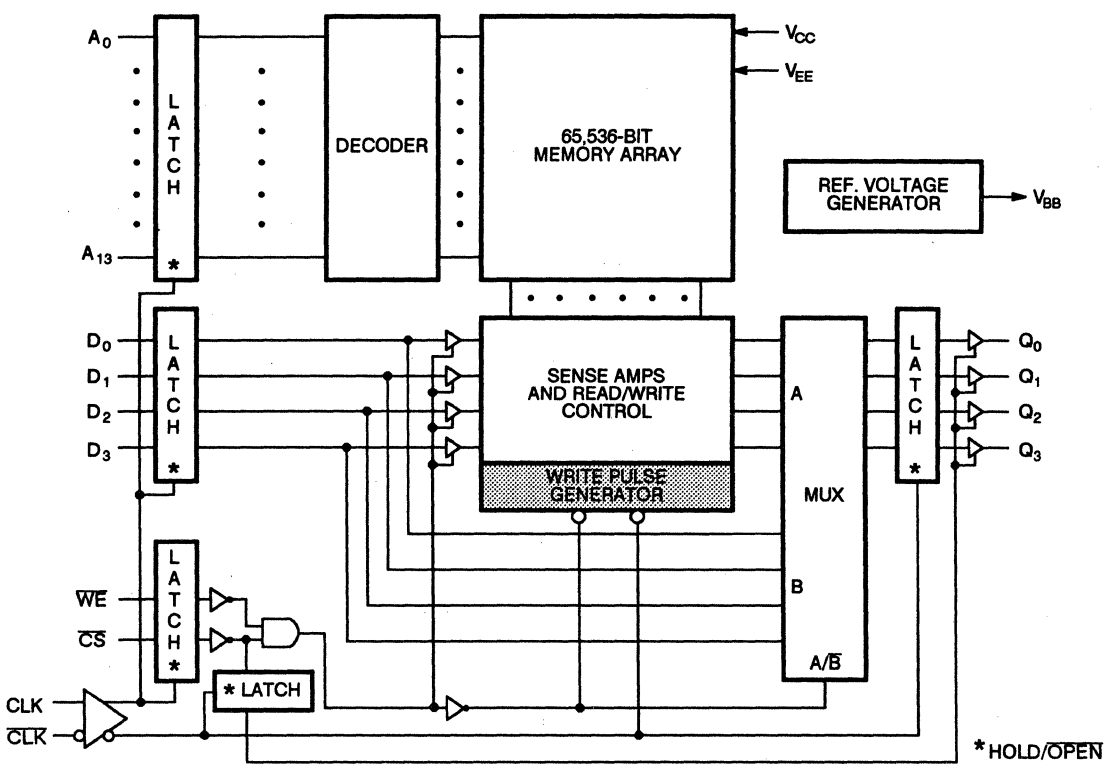
FUNCTIONAL BLOCK DIAGRAM



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16-BIT CMOS ERROR DETECTION AND CORRECTION UNIT

IDT39C60A
IDT39C60-1
IDT39C60

Integrated Device Technology, Inc.

MICROSLICE™ PRODUCT

FEATURES:

- Low power CEMOS™
  - Military: 100mA (max.)
  - Commercial: 85mA (max.)
- Fast
  - Data in to error detect
    IDT39C60A: 20ns (max.), IDT39C60-1: 25ns (max.)
    IDT39C60: 32ns (max.)
  - Data in to corrected data out
    IDT39C60A: 30ns (max.), IDT39C60-1: 52ns (max.)
    IDT39C60: 65ns (max.)
- Improves system memory reliability
  - Corrects all single-bit errors, detects all double and some triple-bit errors
- Cascadable
  - Data words up to 64 bits
- Built-in diagnostics
  - Capable of verifying proper EDC operation via software control
- Simplified byte operations
  - Fast byte writes possible with separate byte enables
- Available in 48-pin DIP, 52-pin PLCC and LCC, as well as space-efficient 48-pin Shrink-DIP (70 mil pin centers)
- Pin-compatible to all versions of the 2960
- Military product available compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT39C60 family are high-speed, low-power, 16-bit Error Detection and Correction Units which generate check bits on a 16-bit data field according to a modified Hamming Code and correct the data word when check bits are supplied. When performing a read operation from memory, the IDT39C60s will correct 100% of all single bit errors, will detect all double bit errors and some triple bit errors.

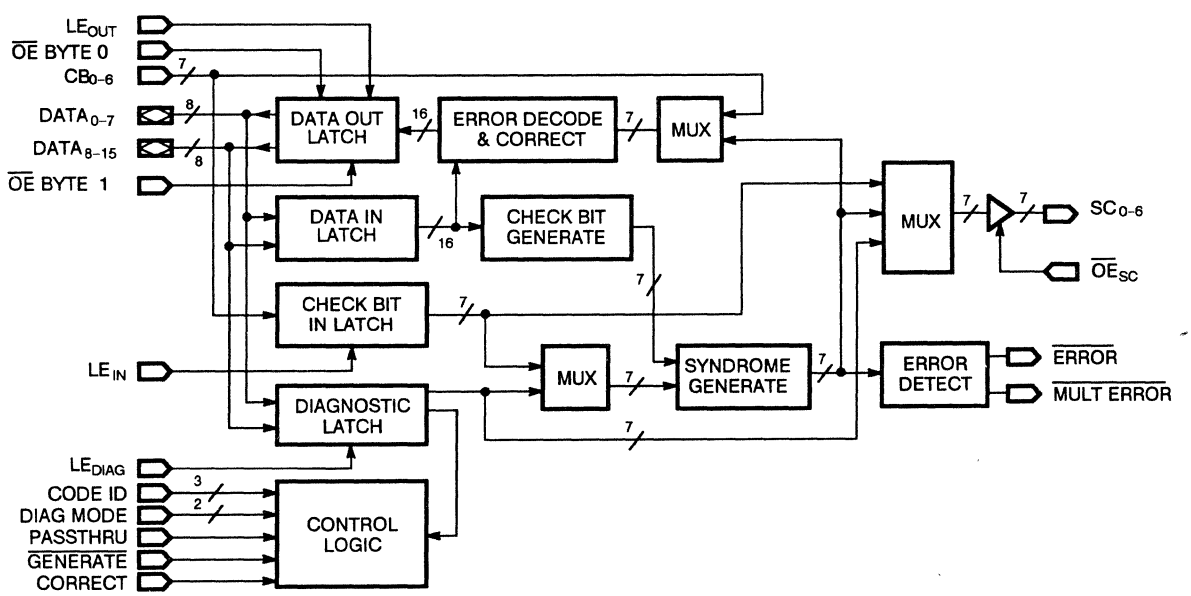
The IDT39C60s are easily cascadable from 16 bits up to 64 bits. Sixteen-bit systems use 6 check bits, 32-bit systems use 7 check bits and 64-bit systems use 8 check bits. For all three configurations, the error syndrome is made available.

All incorporate 2 built-in diagnostic modes. Both simplify testing by allowing for diagnostic data to be entered into the device and to execute system diagnostic functions.

The IDT39C60s are pin-compatible, performance-enhanced functional replacements for all versions of the 2960. They are fabricated using CEMOS, a CMOS technology designed for high-performance and high-reliability. The devices are packaged in either 48-pin DIPs and 52-pin PLCC and LCCs.

Military grade product is manufactured in compliance to the latest revision of MIL-STD-883, Class B.

FUNCTIONAL BLOCK DIAGRAM



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16-BIT CMOS MICROPROCESSOR SLICE

IDT49C402
IDT49C402A

Integrated Device Technology, Inc.

MICROSLICE™ PRODUCT

FEATURES:

- Functionally equivalent to four 2901s and one 2902
- IDT49C402A 45% faster than four 2901s and one 2902A
- Expanded two-address architecture with independent, simultaneous access to two 64 x 16 register files
- Expanded destination functions with 8 new operations allowing Direct Data to be loaded directly into the dual-port RAM and Q Register
- Clamp diodes on all inputs provide noise suppression
- Fully cascadable
- 68-pin plastic and ceramic PGA, Shrink-DIP (600 mil, 70 mil centers) and LCC (25 and 50 mil centers)
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

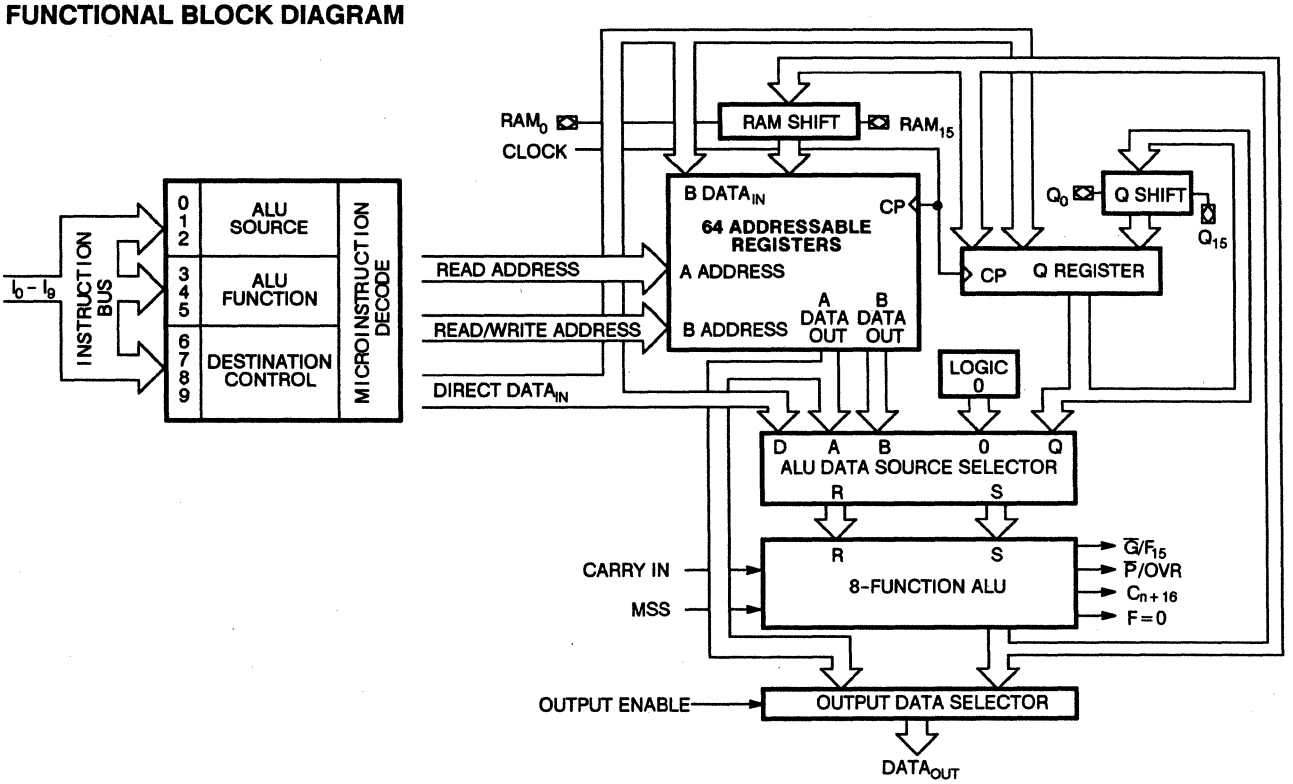
The IDT49C402s are high-speed, fully cascadable 16-bit CMOS microprocessor slice units which combine the standard functions of four 2901s and a 2902 with additional control features aimed at enhancing the performance of bit-slice microprocessor designs.

The IDT49C402s include all of the normal functions associated with standard 2901 bit-slice operation: (a) a 3-bit instruction field (I_0, I_1, I_2) which controls the source operand selection for the ALU; (b) a 3-bit microinstruction field (I_3, I_4, I_5) used to control the eight possible functions of the ALU; (c) eight destination control functions which are selected by the microcode inputs (I_6, I_7, I_8); and (d) a tenth microinstruction input, I_9, offering eight additional destination control functions. This I_9 input, in conjunction with I_6, I_7 and I_8, allows for shifting the Q Register up and down, loading the RAM or Q Register directly from the D inputs without going through the ALU and new combinations of destination functions with the RAM A port output available at the Y output pins of the device.

Also featured is an on-chip dual-port RAM that contains 64 words by 16 bits—four times the number of working registers in a 2901.

The IDT49C402s are fabricated using CEMOS, a CMOS technology designed for high performance and high reliability. These performance enhanced devices feature both bipolar speed and bipolar output drive capabilities while maintaining exceptional microinstruction speeds at greatly reduced CMOS power levels.

FUNCTIONAL BLOCK DIAGRAM



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32-BIT CMOS MICROPROGRAM MICROPROCESSOR

ADVANCE INFORMATION
IDT49C404
IDT49C404A

FEATURES:

- High speed CMOS
  - Microcycle Time: 80ns
- Three bi-directional 32-bit data I/O ports
  - DA, DB, Y
- 64-word x 32-bit expandable 7-port register file
  - 3 input ports and 4 output ports
  - Writes 3 operands and reads 4 operands in one cycle
- 64-bit in, 32-bit out cascadable funnel shifter
  - Fast alignment to any bit boundary
- 32-bit high-speed ALU cascadable to 64 bits
  - Selects status flags from any bit boundary
- Flexible mask generator and merge logic
  - Selects bit-fields on any width, on any boundary
- Priority encoder
- Powerful orthogonal instruction set
- Built-in multiplication/division support
- Counter function
- Includes Serial Protocol Channel (SPC™)
  - Flexible on-chip diagnostics
  - Serially monitors all pin states
  - Reads and writes to Register File
- Single 5V supply
- Available in 208-pin PGA
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT49C404 is a cascadable, microprogrammable, high-speed CMOS 32-bit microprocessor slice. This monolithic, highly parallel, 3-port device consists of a 7-port 64-word by 32-bit working RAM, 64 bits in/32 bits out cascadable funnel shifter, high-speed multi-function 32-bit ALU and 32-bit mask generation and merge logic.

The IDT49C404 uniquely incorporates shift, ALU and merge functions into a single cycle and utilizes an orthogonal instruction set to create a highly parallel architecture that achieves added performance.

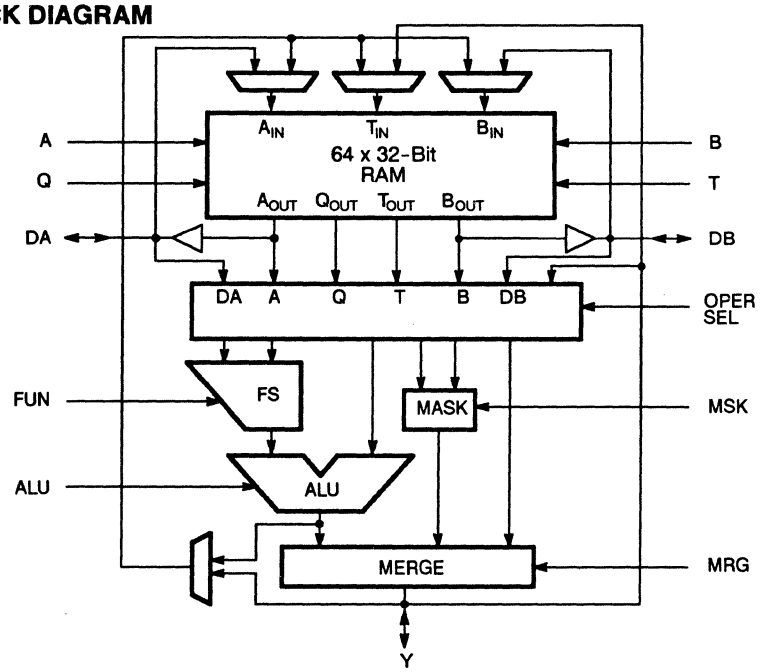
Supporting ultra-fast cycle times, the IDT49C404 offers a very-low-power CMOS alternative to existing bipolar counterparts.

This 32-bit device has been optimized, both architecturally and instruction set-wise, for use in all types of dedicated intelligent controllers such as high-speed graphics engines, array processors, fast disk and communication controllers, robotics, data base manipulation, design automation and AI.

Also featured on the IDT49C404 is an innovative diagnostics capability known as Serial Protocol Channel (SPC). This on-chip feature greatly simplifies the task of writing and debugging microcode, field maintenance debug and test, along with system testing during manufacturing.

The IDT49C404 is fabricated using CEMOS™, IDT's advanced CMOS technology designed for high-performance and high-reliability. The device is packaged in a 208-lead pin grid array. Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making them ideally suited to military temperature applications demanding the highest level of performance and reliability.

SIMPLIFIED BLOCK DIAGRAM



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DSO-9013/-

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32-BIT CMOS ERROR DETECTION AND CORRECTION UNIT

IDT49C460
IDT49C460A
IDT49C460B

FEATURES:

- Fast

	Detect	Correct
– IDT49C460B	25ns (max.)	30ns (max.)
– IDT49C460A	30ns (max.)	36ns (max.)
– IDT49C460	40ns (max.)	49ns (max.)

- Low-power CMOS
  - – Commercial: 95mA (max.)
  - – Military: 125mA (max.)
- Improves system memory reliability
  - – Corrects all single bit errors, detects all double and some triple-bit errors
- Cascadable
  - – Data words up to 64-bits
- Built-in diagnostics
  - – Capable of verifying proper EDC operation via software control
- Simplified byte operations
  - – Fast byte writes possible with separate byte enables
- Functional replacement for 32- and 64-bit configurations of the 2960
- Available in PGA, Sidebraze Shrink-DIP, LCC and PLCC
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT49C460s are high-speed, low-power, 32-bit Error Detection and Correction Units which generate check bits on a 32-bit data field according to a modified Hamming Code and correct the data word when check bits are supplied. The IDT49C460s are performance-enhanced functional replacements for 32-bit versions of the 2960. When performing a read operation from memory, the IDT49C460s will correct 100% of all single bit errors and will detect all double bit errors and some triple bit errors.

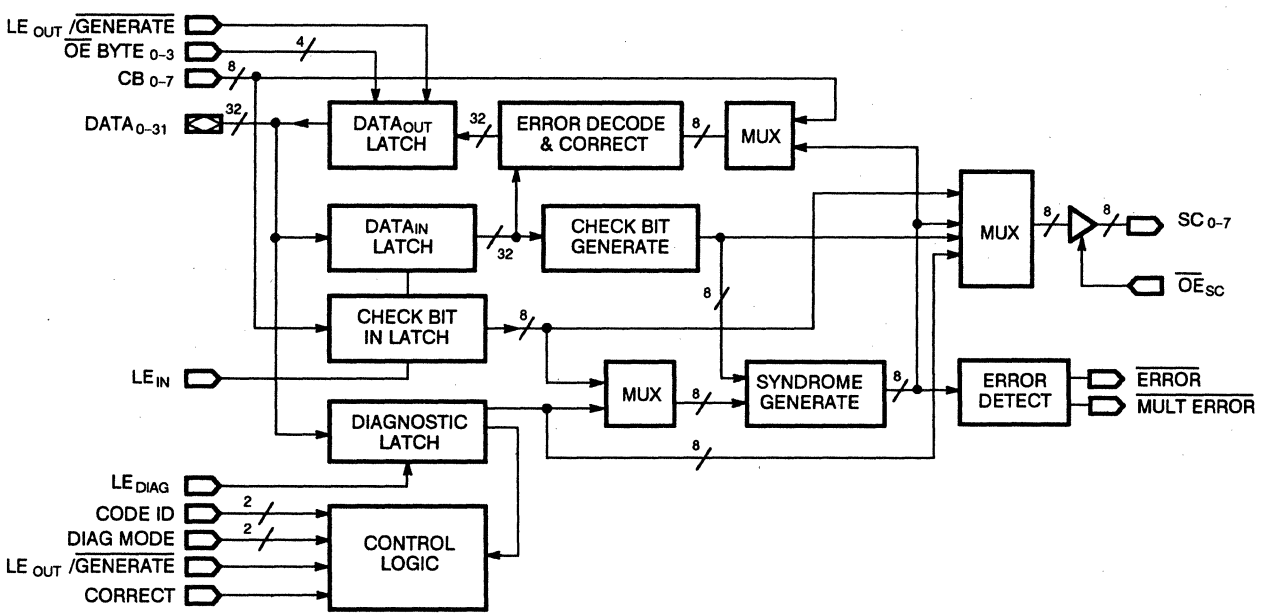
The IDT49C460s are easily cascadable to 64-bits. Thirty-two-bit systems use 7 check bits and 64-bit systems use 8 check bits. For both configurations, the error syndrome is made available.

The IDT49C460s incorporate two built-in diagnostic modes. Both simplify testing by allowing for diagnostic data to be entered into the device and to execute system diagnostic functions.

They are fabricated using CEMOS™, a CMOS technology designed for high-performance and high-reliability. The devices are packaged in a 68-pin PGA, sidebraze Shrink-DIP (600 mil, 70 mil centers), LCC (25 mil and 50 mil centers) and PLCC.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM



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CMOS STATIC RAM 16K (2K x 8-BIT)

IDT6116SA
IDT6116LA

FEATURES:

- High-speed
  - Military: 25/30/35/45/55/70/90/120/150ns (max.)
  - Commercial: 15/20/25/30/35/45ns (max.)
- Low-power operation
  - IDT6116SA
    Active: 180mW (typ.)
    Standby: 100µW (typ.)
  - IDT6116LA
    Active: 160mW (typ.)
    Standby: 20µW (typ.)
- Battery backup operation—2V data retention voltage (LA version only)
- Produced with advanced CEMOS™ high-performance technology
- CEMOS process virtually eliminates alpha particle soft-error rates
- Single 5V (±10%) power supply
- Input and output directly TTL-compatible
- Static operation: no clocks or refresh required
- Available in standard 24-pin DIP, 24-pin THINDIP and plastic DIP, 24-, 28- and 32-pin LCC, 24-pin SOIC and 24-lead CERPACK and Flatpack
- Military product compliant to MIL-STD-883, Class B
- Standard Military Drawing# 84036 is listed on this function. Refer to Section 2/page 2-4.

DESCRIPTION:

The IDT6116SA/LA is a 16,384-bit high-speed static RAM organized as 2K x 8. It is fabricated using IDT's high-performance, high-reliability technology—CEMOS. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost-effective alternative to bipolar and fast NMOS memories.

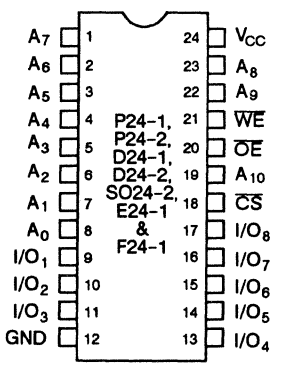
Access times as fast as 25ns are available with maximum power consumption of only 666mW. The circuit also offers a reduced power standby mode. When $\overline{CS}$ goes high, the circuit will automatically go to, and remain in, a standby power mode as long as $\overline{CS}$ remains high. In the standby mode, the low-power device consumes less than 20µW typically. This capability provides significant system level power and cooling savings. The low-power (LA) version also offers a battery backup data retention capability where the circuit typically consumes only 1µW to 4µW operating off a 2V battery.

All inputs and outputs of the IDT6116SA/LA are TTL-compatible and operation is from a single 5V supply, simplifying system designs. Fully static asynchronous circuitry is used, requiring no clocks or refreshing for operation, providing equal access and cycle times for ease of use.

The IDT6116SA/LA is packaged in 24-pin 600 and 300 mil plastic or ceramic DIP, 24-, 28- and 32-pin leadless chip carriers, 24-lead CERPACK and flatpack, and a 24-lead gull-wing SOIC, providing high board-level packing densities.

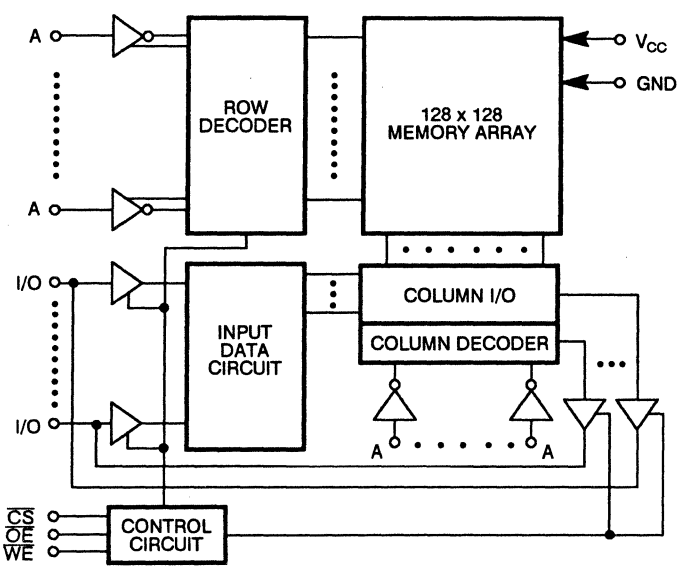
Military grade product is manufactured in compliance to the latest version of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

PIN CONFIGURATION



DIP/SOIC/FLATPACK/CERPACK
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



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CMOS STATIC RAM 16K (4K x 4-BIT)

IDT6168SA
IDT6168LA

FEATURES:

- High-speed (equal access and cycle time)
  - Military: 15/20/25/35/45/55/70/85/100ns (max.)
  - Commercial: 15/20/25/35ns (max.)
- Low power consumption
  - IDT6168SA
    Active: 225mW (typ.)
    Standby: 100µW (typ.)
  - IDT6168LA
    Active: 225mW (typ.)
    Standby: 10µW (typ.)
- Battery backup operation—2V data retention voltage (IDT6168LA only)
- Available in high-density 20-pin CERDIP and plastic DIP, 20-pin SOIC, 20-pin Flatpack and CERPACK and 20-pin leadless chip carrier
- Produced with advanced CEMOS™ high-performance technology
- CEMOS process virtually eliminates alpha particle soft-error rates
- Bidirectional data input and output
- Single 5V (±10%) power supply
- Input and output directly TTL-compatible
- Three-state outputs
- Static operation: no clocks or refresh required
- Military product compliant to MIL-STD-883, Class B
- Standard Military Drawing# 5962-86705 is listed on this function. Refer to Section 2/page 2-4.

DESCRIPTION:

The IDT6168 is a 16,384-bit high-speed static RAM organized as 4K x 4. It is fabricated using IDT's high-performance, high-reliability technology—CEMOS. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost effective alternative to bipolar and fast NMOS memories.

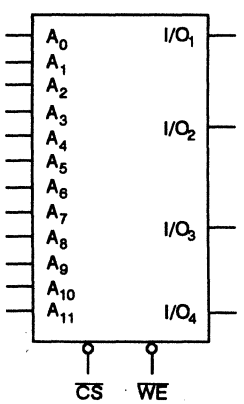
Access times as fast as 15ns are available with maximum power consumption of only 550mW. The circuit also offers a reduced power standby mode. When $\overline{CS}$ goes high, the circuit will automatically go to, and remain in, a standby mode as long as $\overline{CS}$ remains high. In the standby mode, the device consumes less than 10µW, typically. This capability provides significant system-level power and cooling savings. The low-power (LA) version also offers a battery backup data retention capability where the circuit typically consumes only 1µW operating off a 2V battery.

All inputs and outputs of the IDT6168 are TTL-compatible and operate from a single 5V supply, thus simplifying system designs. Fully static asynchronous circuitry is used, which requires no clocks or refreshing for operation, and provides equal access and cycle times for ease of use.

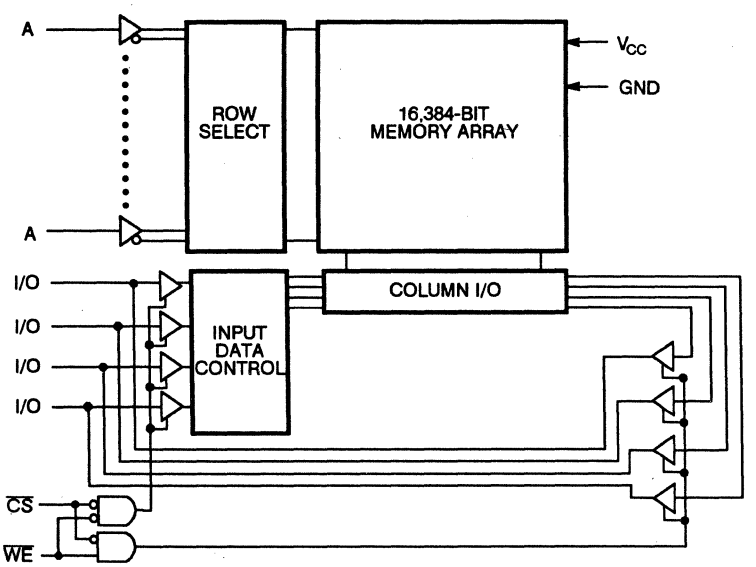
The IDT6168 is packaged in either a space saving 20-pin, 300 mil CERDIP or plastic DIP, 20-pin flatpack or CERPACK, 20-pin SOIC, or 20-pin leadless chip carrier, providing high board-level packing densities.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

LOGIC SYMBOL



FUNCTIONAL BLOCK DIAGRAM



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CMOS STATIC RAM 256K (32K x 8-BIT)

PRELIMINARY
IDT71256S
IDT71256L

FEATURES:

- High-speed address/chip select time
  - Military: 45/55/70/85/100ns (max.)
  - Commercial: 35/45/55/70ns (max.)
- Low-power operation
  - IDT71256S
    Active: 300mW (typ.)
    Standby: 200μW (typ.)
  - IDT71256L
    Active: 250mW (typ.)
    Standby: 15μW (typ.)
- Battery Backup operation—2V data retention
- Produced with advanced high-performance CEMOS™ technology
- Single 5V(±10%) power supply
- Input and output directly TTL-compatible
- Static operation: no clocks or refresh required
- Available in standard 28-pin CERDIP and plastic DIP (600 mil), 28-pin SOIC, 28-pin Cerpack and 32-pin LCC and PLCC
- Military product compliant to MIL-STD-883, Class B
- Standard Military Drawing# 5962-88552 is pending listing on this function. Refer to Section 2/page 2-4.

DESCRIPTION:

The IDT71256 is a 262,144-bit high-speed static RAM organized as 32K x 8. It is fabricated using IDT's high-performance, high-reliability CEMOS technology. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost-effective alternative to bipolar and fast NMOS memories.

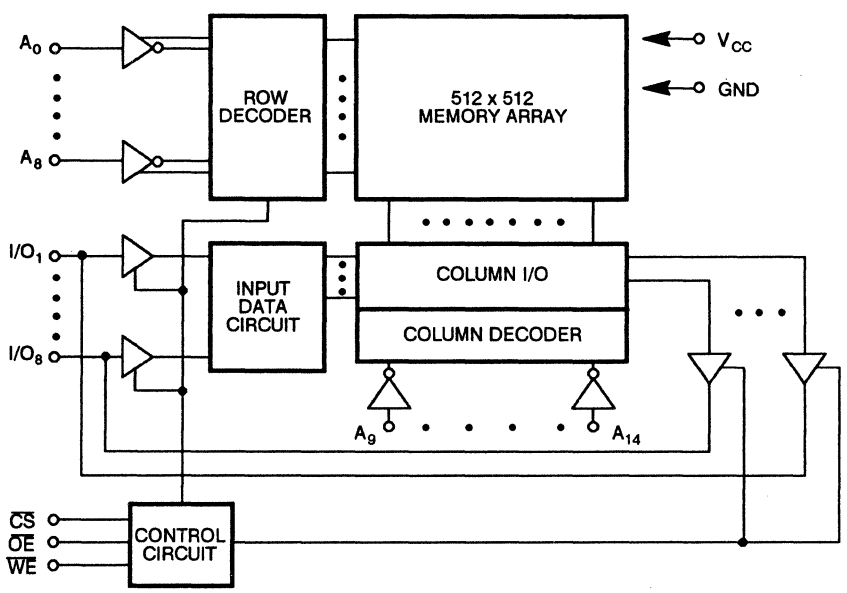
Address access times as fast as 35ns are available with power consumption of only 300mW (typ.). The circuit also offers a reduced power standby mode. When $\overline{CS}$ goes high, the circuit will automatically go to, and remain in, a low-power standby mode as long as $\overline{CS}$ remains high. In the full standby mode, the low-power device consumes less than 15μW, typically. This capability provides significant system level power and cooling savings. The low-power (L) version also offers a battery backup data retention capability where the circuit typically consumes only 5μW when operating off a 2V battery.

All inputs and outputs of the IDT71256 are TTL-compatible and operation is from a single 5V supply, simplifying system designs. Fully static asynchronous circuitry is used, requiring no clocks or refreshing for operation, providing equal access and cycle times for ease of use.

The IDT71256 is packaged in a 28-pin SOIC, a 28-pin 600 mil CERDIP or plastic DIP, 28-pin Cerpack and 32-pin leadless chip carrier and PLCC, providing high board-level packing densities.

The IDT71256 military RAM is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM



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CMOS STATIC RAM 256K (256K x 1-BIT)

PRELIMINARY
IDT71257S
IDT71257L

FEATURES:

- High-speed (equal access and cycle time)
  - Military: 35/45/55/70ns (max.)
  - Commercial: 25/35/45/55ns (max.)
- Low-power operation
  - IDT71257S
    Active: 400mW (typ.)
    Standby: 400µW (typ.)
  - IDT71257L
    Active: 350mW (typ.)
    Standby: 100µW (typ.)
- Battery backup operation—2V data retention (L version only)
- Produced with advanced CEMOS™ high-performance technology
- Single 5V (±10%) power supply
- Input and output directly TTL-compatible
- Static operation: no clocks or refresh required
- Available in high-density industry standard 24-pin, 300 mil DIP and 24-pin SOIC
- Three-state outputs
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT71257 is a 262,144-bit high-speed static RAM organized as 256K x 1. It is fabricated using IDT's high-performance, high-reliability CEMOS technology. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost-effective alternative to bipolar and fast NMOS memories.

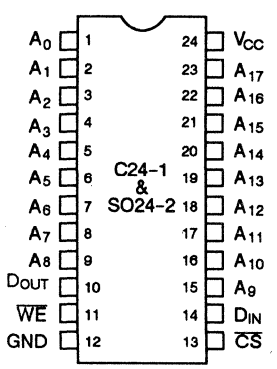
Access times as fast as 25ns are available with typical power consumption of only 350mW. The IDT71257 offers a reduced power standby mode, I_{SB1}, which enables the designer to greatly reduce device power requirements. This capability provides significant system level power and cooling savings. The low-power (L) version also offers a battery backup data retention capability where the circuit typically consumes only 100µW operation off a 2V battery.

All inputs and outputs of the IDT71257 are TTL-compatible and operation is from a single 5V supply, simplifying system designs. Fully static asynchronous circuitry is used, requiring no clocks or refreshing for operation, providing equal access and cycle times for ease of use.

The IDT71257 is packaged in a 24-pin 300 mil DIP and a 24-pin SOIC, providing high board-level packing densities.

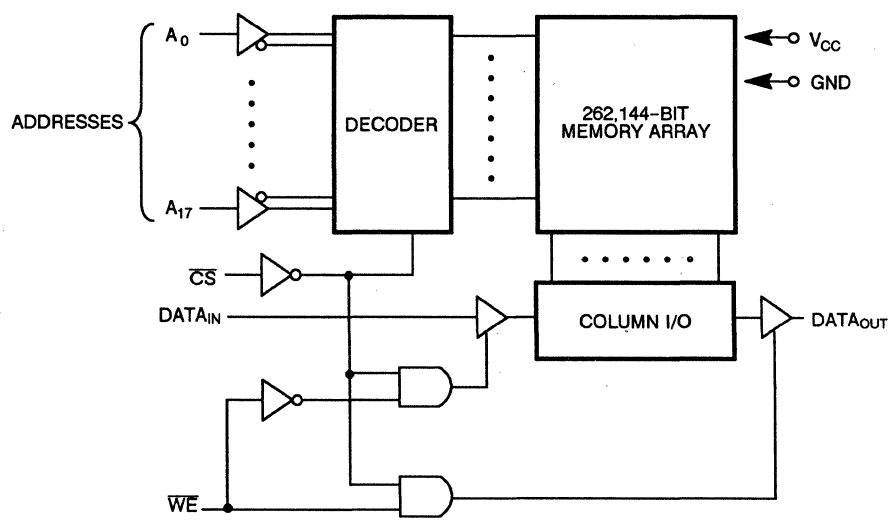
Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

PIN CONFIGURATION



DIP/SOIC TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



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CMOS STATIC RAM 256K (64K x 4-BIT)

PRELIMINARY
IDT71258S
IDT71258L

FEATURES:

- High-speed (equal access and cycle time)
  - Military: 35/45/55/70ns (max.)
  - Commercial: 25/35/45/55/ns (max.)
- Low-power operation
  - IDT71258S
    - Active: 400mW (typ.)
    - Standby: 400µW (typ.)
  - IDT71258L
    - Active: 350mW (typ.)
    - Standby: 100µW (typ.)
- Battery backup operation—2V data retention (L version only)
- Produced with advanced CEMOS™ high-performance technology
- Single 5V (±10%) power supply
- Input and output directly TTL-compatible
- Static operation: no clocks or refresh required
- Available in high-density industry standard 24-pin, 300 mil DIP and 24-pin SOIC
- Three-state outputs
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT71258 is a 262,144-bit high-speed static RAM organized as 64K x 4. It is fabricated using IDT's high-performance, high-reliability CEMOS technology. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost-effective alternative to bipolar and fast NMOS memories.

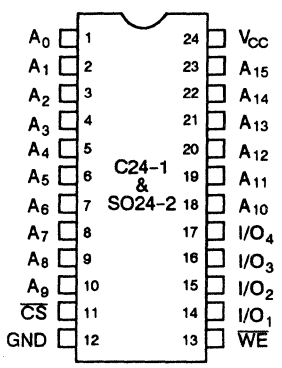
Access times as fast as 25ns are available with typical power consumption of only 350mW. The IDT71258 offers a reduced power standby mode, I_{SB1}, which enables the designer to greatly reduce device power requirements. This capability provides significant system level power and cooling savings. The low-power (L) version also offers a battery backup data retention capability where the circuit typically consumes only 100µW operation off a 2V battery.

All inputs and outputs of the IDT71258 are TTL-compatible and operation is from a single 5V supply, simplifying system designs. Fully static asynchronous circuitry is used, requiring no clocks or refreshing for operation, providing equal access and cycle times for ease of use.

The IDT71258 is packaged in a 24-pin 300 mil DIP and a 24-pin SOIC providing high board-level packing densities.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

PIN CONFIGURATION

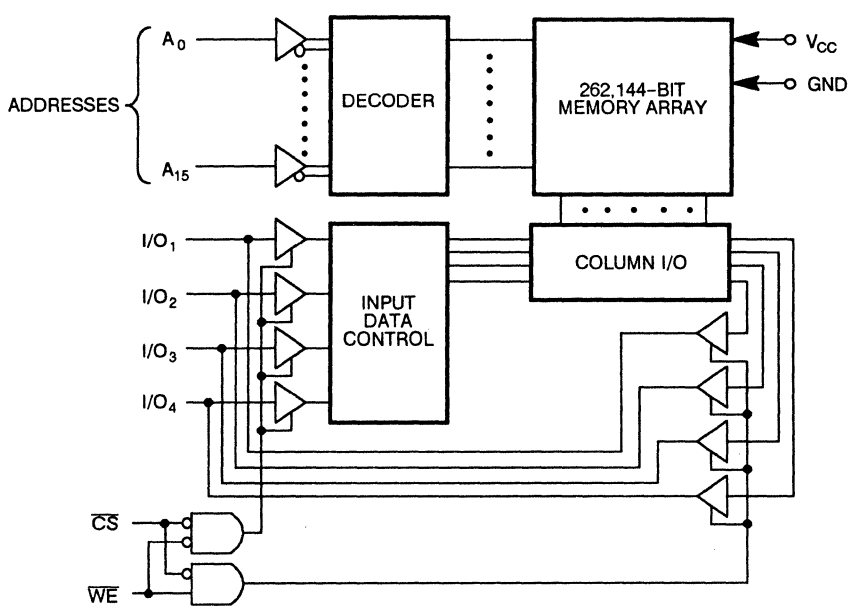


DIP/SOIC TOP VIEW

PIN NAMES

$A_0 - A_{15}$	Addresses
$I/O_1 - I/O_4$	Data Input/Output
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
GND	Ground
V_{CC}	Power

FUNCTIONAL BLOCK DIAGRAM



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CMOS DUAL-PORT RAMS 8K (1K x 8-BIT)

IDT7130SA/LA
IDT7140SA/LA

FEATURES:

- High-speed access
  - Military: 45/55/70/90/100/120ns (max.)
  - Commercial: 35/45/55/70/90/100ns (max.)
- Low-power operation
  - IDT7130/40SA
    Active: 325mW (typ.)
    Standby: 5mW (typ.)
  - IDT7130/40LA
    Active: 325mW (typ.)
    Standby: 1mW (typ.)
- MASTER IDT7130 easily expands data bus width to 16-or-more-bits using SLAVE IDT7140
- On-chip port arbitration logic (IDT7130 only)
- $\overline{BUSY}$ output flag on IDT7130; $\overline{BUSY}$ input on IDT7140
- $\overline{INT}$ flag for port-to-port communication
- Fully asynchronous operation from either port
- Battery backup operation—2V data retention
- TTL-compatible, single 5V±10% power supply
- Military product compliant to MIL-STD-883, Class B
- Standard Military Drawing# 5962-86875 is pending listing on this function. Refer to Section 2/page 2-4.

DESCRIPTION:

The IDT7130/IDT7140 are high-speed 1K x 8 dual-port static RAMs. The IDT7130 is designed to be used as a stand-alone 8-bit dual-port RAM or as a "MASTER" dual-port RAM together with the IDT7140 "SLAVE" dual-port in 16-bit-or-more word width systems. Using the IDT MASTER/SLAVE dual-port RAM approach in 16-or-more-bit memory system applications results in full-speed, error-free operation without the need for additional discrete logic.

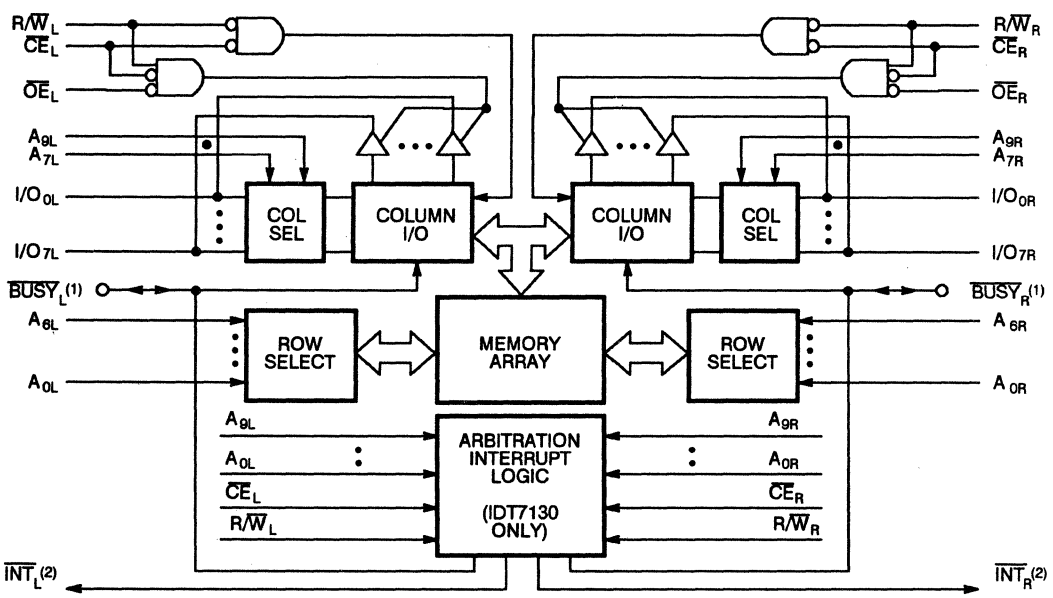
Both devices provide two independent ports with separate control, address and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. An automatic power down feature, controlled by $\overline{CE}$, permits the on-chip circuitry of each port to enter a very low standby power mode.

Fabricated using IDT's CEMOS™ high-performance technology, these devices typically operate on only 325mW of power at maximum access times as fast as 35ns. Low-power (LA) versions offer battery backup data retention capability, with each dual-port typically consuming 200μW from a 2V battery.

The IDT7130/7140 devices are packaged in 48-pin sidebraze or plastic DIPs, 48- or 52-pin LCCs, 52-pin PLCCs, and 48-lead flatpacks.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

FUNCTIONAL BLOCK DIAGRAM



NOTES:

1. IDT7130 (MASTER): $\overline{BUSY}$ is open drain output and requires pullup resistor.
   IDT7140 (SLAVE): $\overline{BUSY}$ is input.
2. Open drain output: requires pullup resistor.

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CMOS DUAL-PORT RAM 16K (2K x 8-BIT)

IDT7132SA/LA
IDT7142SA/LA

FEATURES:

- High-speed access
  - Military: 45/55/70/90/100/120ns (max.)
  - Commercial: 35/45/55/70/90/100ns (max.)
- Low-power operation
  - IDT7132/42SA
    Active: 325mW (typ.)
    Standby: 5mW (typ.)
  - IDT7132/42LA
    Active: 325mW (typ.)
    Standby: 1mW (typ.)
- MASTER IDT7132 easily expands data bus width to 16-or-more bits using SLAVE IDT7142
- On-chip port arbitration logic (IDT7132 only)
- $\overline{BUSY}$ output flag on IDT7132; $\overline{BUSY}$ input on IDT7142
- Fully asynchronous operation from either port
- Battery backup operation—2V data retention
- TTL-compatible, single 5V ±10% power supply
- Military product compliant to MIL-STD-883, Class B
- Standard Military Drawing# 5962-87002 is pending listing on this function. Refer to Section 2/page 2-4.

DESCRIPTION:

The IDT7132/IDT7142 are high-speed 2K x 8 dual-port static RAMs. The IDT7132 is designed to be used as a stand-alone 8-bit dual-port RAM or as a "MASTER" dual-port RAM together with the IDT7142 "SLAVE" dual-port in 16-bit-or-more word width systems. Using the IDT MASTER/SLAVE dual-port RAM approach in 16-or-more-bit memory system applications results in full-speed, error-free operation without the need for additional discrete logic.

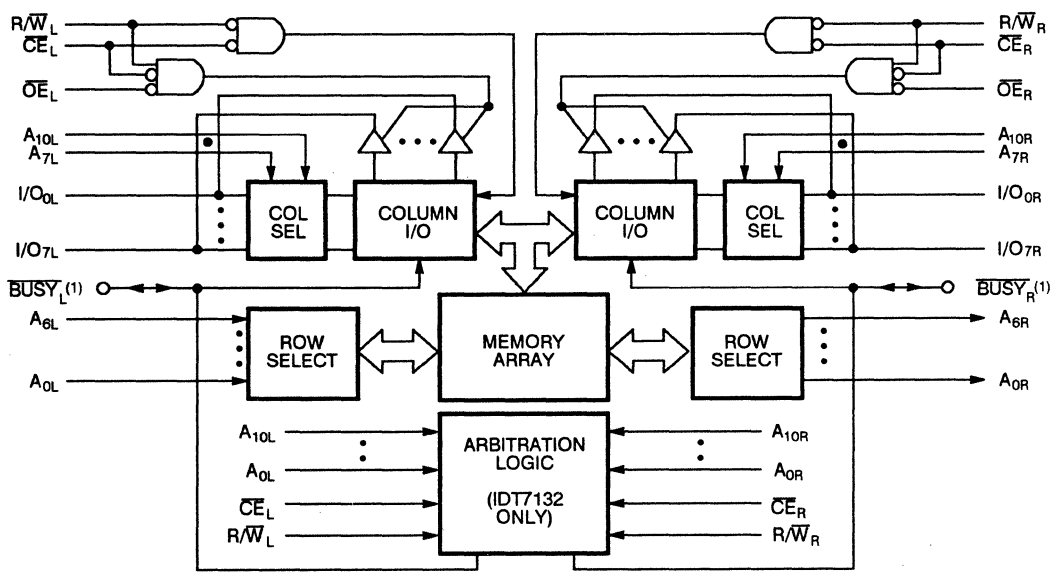
Both devices provide two independent ports with separate control, address and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. An automatic power down feature, controlled by $\overline{CE}$, permits the on-chip circuitry of each port to enter a very low standby power mode.

Fabricated using IDT's CEMOS™ high-performance technology, these devices typically operate on only 325mW of power at maximum access times as fast as 35ns. Low-power (LA) versions offer battery backup data retention capability, with each dual-port typically consuming 200μW from a 2V battery.

The IDT7132/7142 devices are packaged in a 48-pin sidebraze or plastic DIP, 48- or 52-pin LCC, 52-pin PLCC, and a 48-lead flatpack.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

FUNCTIONAL BLOCK DIAGRAM



NOTES:

1. IDT7132 (MASTER): $\overline{BUSY}$ is open drain output and requires pullup resistor.
   IDT7142 (SLAVE): $\overline{BUSY}$ is input.

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CMOS DUAL-PORT RAMS 16K (2K x 8-BIT) WITH INTERRUPTS

IDT71321SA/LA
IDT71421SA/LA

FEATURES:

- High-speed access
  - Military: 45/55/70ns (max.)
  - Commercial: 35/45/55ns (max.)
- Low-power operation
  - IDT71321/421SA
    Active: 325mW (typ.)
    Standby: 5mW (typ.)
  - IDT71321/421LA
    Active: 325mW (typ.)
    Standby: 1mW (typ.)
- Two $\overline{INT}$ flags for port-to-port communications
- MASTER IDT71321 easily expands data bus width to 16-or-more-bits using SLAVE IDT71421
- On-chip port arbitration logic (IDT71321 only)
- $\overline{BUSY}$ output flag on IDT71321; $\overline{BUSY}$ input on IDT71421
- Fully asynchronous operation from either port
- Battery backup operation—2V data retention
- TTL-compatible, single 5V ±10% power supply
- Available in popular hermetic and plastic packages
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT71321/IDT71421 are high-speed 2K x 8 dual-port static RAMs with internal interrupt logic for interprocessor communications. The IDT71321 is designed to be used as a stand-alone 8-bit dual-port RAM or as a "MASTER" dual-port RAM, together with the IDT71421 "SLAVE" dual-port, in 16-bit-or-more word width systems. Using the IDT MASTER/SLAVE dual-port RAM approach in 16-or-more-bit memory system applications results in full-speed, error-free operation without the need for additional discrete logic.

Both devices provide two independent ports with separate control, address and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. An automatic power down feature, controlled by $\overline{CE}$, permits the on-chip circuitry of each port to enter a very low standby power mode.

Fabricated using IDT's CEMOS™ high-performance technology, these devices typically operate on only 325mW of power at maximum access times as fast as 35ns. Low-power (LA) versions offer battery backup data retention capability with each port typically consuming 200μW from a 2V battery.

The IDT71321/71421 devices are packaged in 52-pin LCCs and PLCCs. Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

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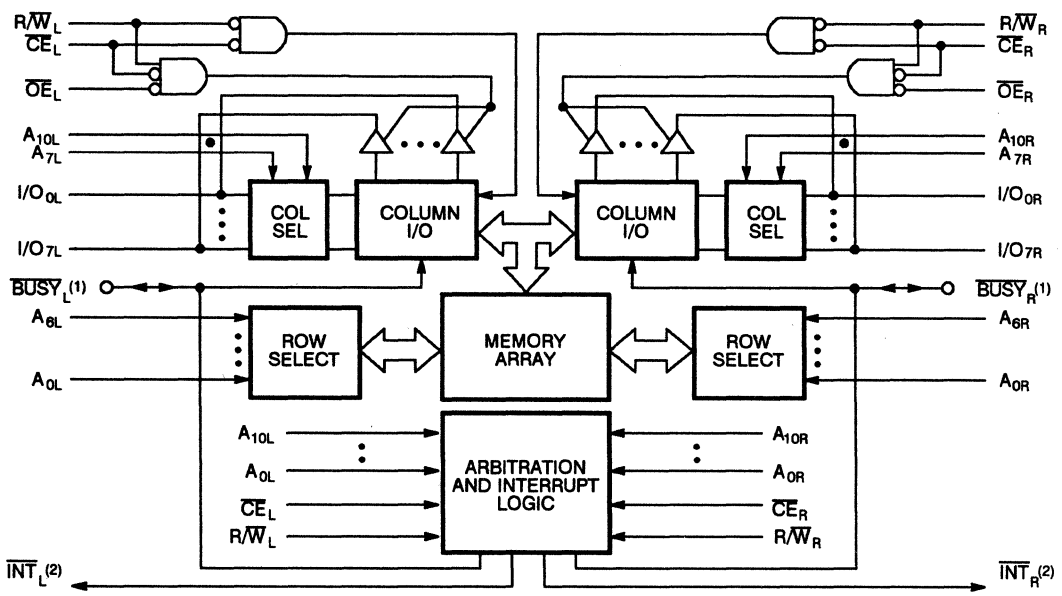
FUNCTIONAL BLOCK DIAGRAM



NOTES:

1. IDT71321 (MASTER): $\overline{BUSY}$ is open drain output and requires pullup resistor. IDT71421 (SLAVE): $\overline{BUSY}$ is input.
2. Open drain output: requires pullup resistor.

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CMOS DUAL-PORT RAM 16K (2K x 8-BIT) WITH SEMAPHORE

PRELIMINARY
IDT71322S
IDT71322L

FEATURES:

- High-speed access
  - Military: 45/55/70ns (max.)
  - Commercial: 45/55/70ns (max.)
- Low-power operation
  - IDT71322S
    Active: 500mW (typ.)
    Standby: 5mW (typ.)
  - IDT71322L
    Active: 500mW (typ.)
    Standby: 1mW (typ.)
- Fully asynchronous operation from either port
- Full on-chip hardware support of semaphore signalling between ports
- Battery backup operation—2V data retention
- TTL-compatible, single 5V(±10%) power supply
- Available in a variety of plastic and hermetic packages for both through hole and surface mount applications
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

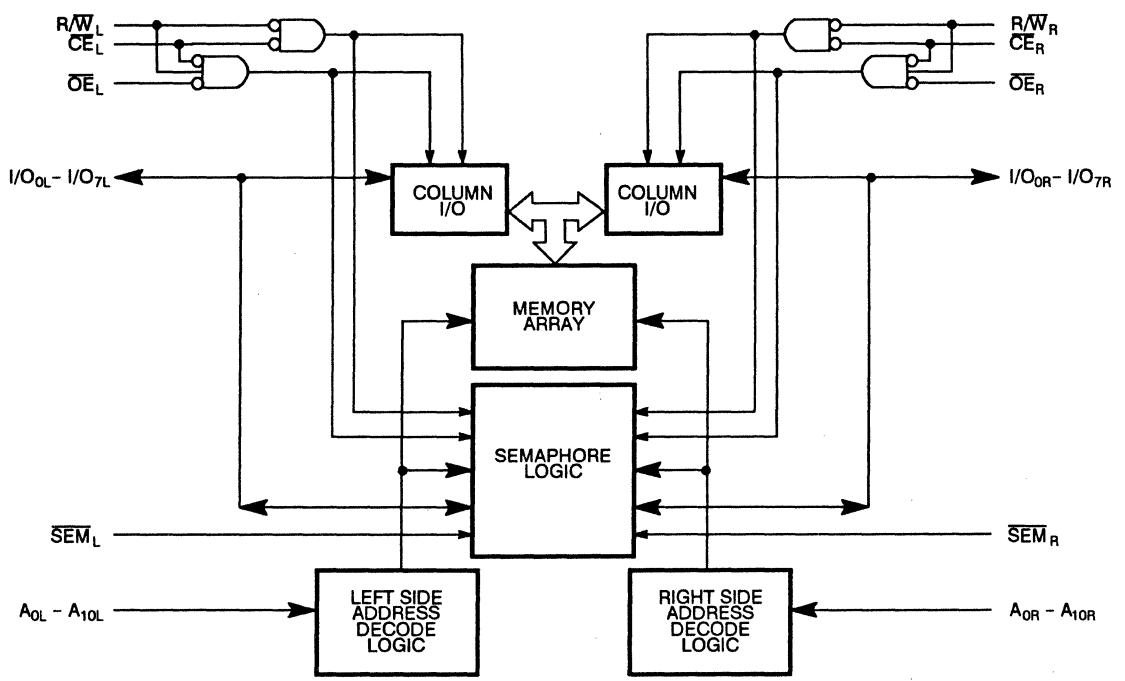
The IDT71322 is an extremely high-speed 2K x 8 dual-port static RAM with full on-chip hardware support of semaphore signalling between the two ports.

The IDT71322 provides two independent ports with separate control, address and I/O pins that permit independent, asynchronous access for reads and writes to any location in memory. To assist in arbitrating between ports, a fully independent semaphore logic block is provided. This block contains unassigned flags which can be accessed by either side; however, only one side can control the flag at any time. An automatic power down feature, controlled by $\overline{CE}$ and $\overline{SEM}$, permits the on-chip circuitry of each port to enter a very low standby power mode.

Fabricated using IDT's CEMOS™ high-performance technology, this device typically operates on only 500mW of power at maximum access times as fast as 45ns. Low-power (L) versions offer battery backup data retention capability, with each port typically consuming 200μW from a 2V battery.

The IDT71322 is packaged in a 48-pin sidebraze or plastic DIP or 52-pin LCC and PLCC. Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

FUNCTIONAL BLOCK DIAGRAM



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CMOS DUAL-PORT RAM 32K (2K x 16-BIT)

IDT7133S/L
IDT7143S/L

FEATURES:

- High-speed access
  - Military: 70/90ns (max.)
  - Commercial: 55/70/90ns (max.)
- Low-power operation
  - IDT7133/43S
    Active: 375mW (typ.)
    Standby: 5mW (typ.)
  - IDT7133/43L
    Active: 375mW (typ.)
    Standby: 1mW (typ.)
- Versatile control for write: separate write control for lower and upper byte of each port
- MASTER IDT7133 easily expands data bus width to 32 bits or more using SLAVE IDT7143
- On-chip port arbitration logic (IDT7133 only)
- $\overline{BUSY}$ output flag on IDT7133; $\overline{BUSY}$ input on IDT7143
- Fully asynchronous operation from either port
- Battery backup operation—2V data retention
- TTL-compatible, single 5V (±10%) power supply
- Available in 68-pin PGA, DIP (600 mil, 70 mil centers), LCC and PLCC
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT7133/7143 are high-speed 2K x 16 dual-port static RAMs. The IDT7133 is designed to be used as a stand-alone 16-bit dual-port RAM or as a "MASTER" dual-port RAM together with the IDT7143 "SLAVE" dual-port in 32-bit-or-more word width systems. Using the IDT MASTER/SLAVE dual-port RAM approach in 16-bit-or-wider memory system applications results in full-speed, error-free operation without the need for additional discrete logic.

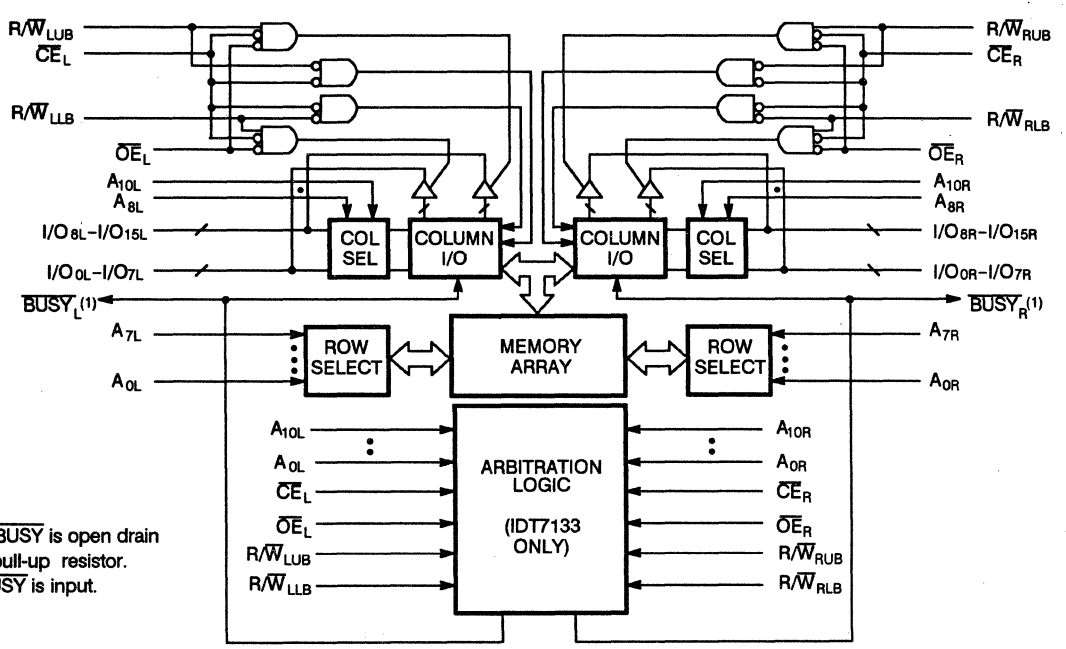
Both devices provide two independent ports with separate control, address and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. An automatic power down feature, controlled by $\overline{CE}$, permits the on-chip circuitry of each port to enter a very low standby power mode.

Fabricated using IDT's CEMOS™ high-performance technology, these devices typically operate on only 375mW of power at maximum access times as fast as 55ns. Low-power (L) versions offer battery backup data retention capability, with each port typically consuming 1mW from a 2V battery.

The IDT7133/7143 devices have identical pinouts. Each is packaged in a 68-pin PGA, 68-pin LCC, 68-pin PLCC, and 70 mil center DIPs.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM



NOTES:

1. IDT7133 (MASTER): $\overline{BUSY}$ is open drain output and requires pull-up resistor. IDT7143 (SLAVE): $\overline{BUSY}$ is input.
2. LB = LOWER BYTE
   UB = UPPER BYTE

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CMOS DUAL-PORT RAM 32K (4K x 8-BIT) WITH SEMAPHORE

IDT71342S
IDT71342L

FEATURES:

- High-speed access
  - Military: 45/55/70ns (max.)
  - Commercial: 45/55/70ns (max.)
- Low-power operation
  - IDT71342S
    Active: 500mW (typ.)
    Standby: 5mW (typ.)
  - IDT71342L
    Active: 500mW (typ.)
    Standby: 1mW (typ.)
- Fully asynchronous operation from either port
- Full on-chip hardware support of semaphore signalling between ports
- Battery backup operation—2V data retention
- TTL-compatible; single+5V(±10%) power supply
- Available in popular hermetic and plastic packages
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

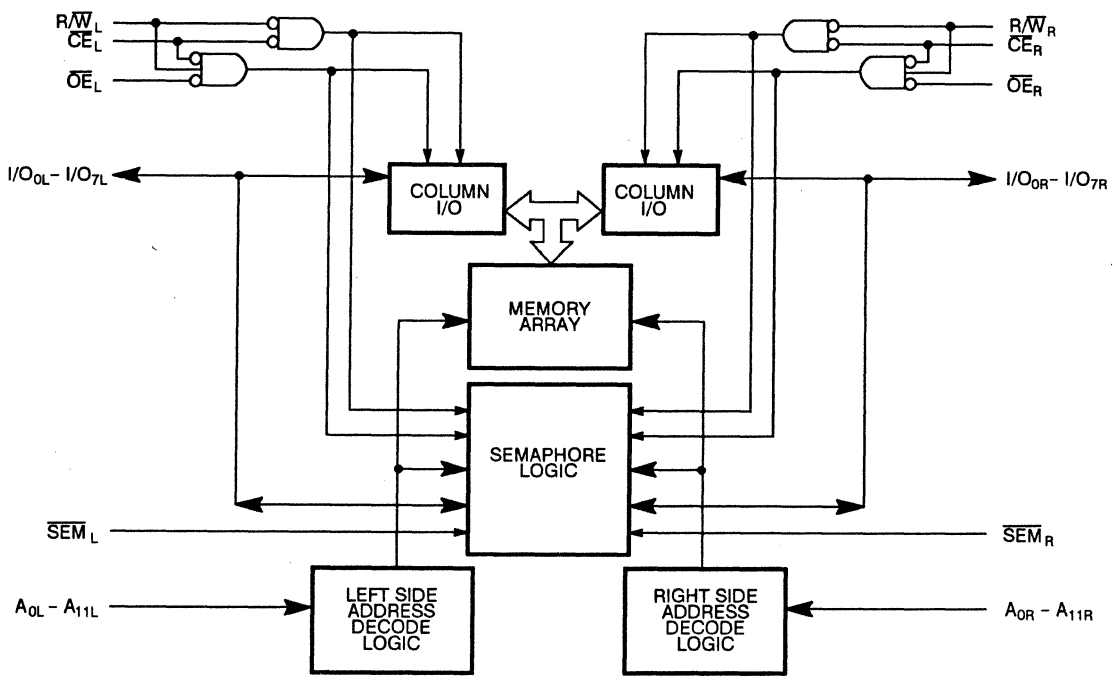
The IDT71342 is an extremely high-speed 4K x 8 dual-port static RAM with full on-chip hardware support of semaphore signalling between the two ports.

The IDT71342 provides two independent ports with separate control, address and I/O pins that permit independent, asynchronous access for reads and writes to any location in memory. To assist in arbitrating between ports, a fully independent semaphore logic block is provided. This block contains unassigned flags which can be accessed by either side; however, only one side can control the flag at any time. An automatic power down feature, controlled by $\overline{CE}$ and $\overline{SEM}$, permits the on-chip circuitry of each port to enter a very low standby power mode (both $\overline{CE}$ and $\overline{SEM}$ high).

Fabricated using IDT's CEMOS™ high-performance technology this device typically operates on only 500mW of power at maximum access times as fast as 45ns. Low-power (L) versions offer battery backup data retention capability, with each port typically consuming 200μW from a 2V battery. The device is packaged in either a hermetic 52-pin leadless chip carrier or a 52-pin PLCC.

The IDT71342 military devices are manufactured in compliance with the latest revision of MIL-STD-883, Class B.

FUNCTIONAL BLOCK DIAGRAM



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CMOS STATIC RAM 64K (4K x 16-BIT) REGISTERED RAM w/SPC™

IDT71502S
IDT71502L

FEATURES:

- 4K x 16 RAM with registered outputs, serial or parallel load and readback capability in only 48 pins
- Serial Protocol Channel allows serial load and readback of RAM over a 4-wire channel
- RAM address counter speeds RAM load and readback
- Outputs may be programmed to be registered or non-registered in groups of 8 bits
- Initialize register allows initial microword selection
- Synchronous and asynchronous output enables allow for depth expansion and bus driving
- Programmable chip selects enable depth & width expansion without any external decode logic
- Breakpoint comparator supports system diagnostics
- Parity check on outputs for high reliability designs
- High-speed (address set-up before clock)
  - Military: 45/55/70ns (max.)
  - Commercial: 35/45/55ns (max.)
- Low-power consumption
  - IDT71502S - Active: 300mW (typ.)
  - IDT71502L - Active: 250mW (typ.)
- Input and output directly TTL-compatible
- Standard 48-pin DIP, 48-pin THINDIP, 48-pin LCC and 52-pin PLCC.
- Military product 100% compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT71502 Registered RAM is a 65.536 high speed static RAM organized as 4K x 16, with a high speed register at the RAM outputs and serial load and readback capability using the IDT Serial Protocol Channel, SPC™.

This device is the first in a family of multifeatured RAM's with a built-in Serial Protocol Channel SPC™ letting the user set the best configuration for his system:

- SELF-ADDRESSING RAM
- WRITABLE CONTROL STORE
- LOGIC ANALYZER/RECORDER

The 71502 is fabricated using IDT's high-performance, high-reliability technology—CEMOS™. This technology gives the 71502 the combination of low power, high speed, and high density that makes it a cost effective solution.

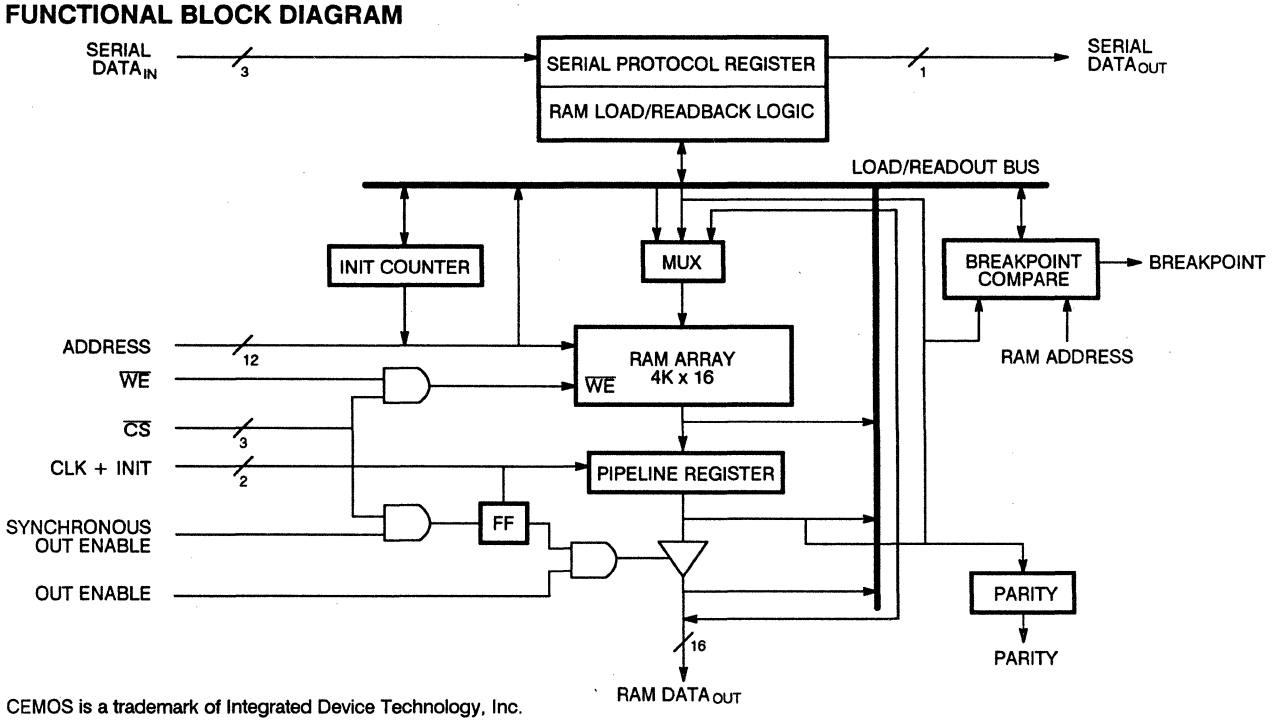
The IDT71502 is available with address set up before clock times as fast as 35ns. These times are available with a maximum power consumption of only xxx mW.

All inputs and outputs of the IDT71502 are TTL-compatible, and the device operates from a single 5V supply. Fully static, asynchronous circuitry is used, requiring no clocks (with the exception of the register clock) or refreshing for operation.

The IDT71502 is packaged in plastic and ceramic versions of either a 48-pin, 600 mil DIP; a 48-pin, 400 mil THINDIP; or a 52-pin leadless chip carrier providing high board level packing densities.

The IDT71502 is 100% processed in compliance to the test methods of MIL-STD-883, Method 5004.

FUNCTIONAL BLOCK DIAGRAM



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CMOS STATIC RAMS 64K (4K x 16-BIT)

ADVANCE INFORMATION
IDT71586S
IDT71586L

FEATURES:

- Wide 4K x 16 Organization
- High-speed access
  - Commercial: 35/45/55ns (max.)
  - Military: 45/55ns (max.)
- Internal fast 12-bit address latch (5ns set-up & hold times)
- Best fit for popular cache configurations:
  - Intel 82385 cache controller (for 80386)
  - IDTR3000 RISC CPU instruction & data caches
- Fast Output Enable - 11ns (max.)
- Separate enables for upper and lower bytes
- Packaged in 40 pin, 600 mil CERDIP or plastic DIP, or 44 pin PLCC
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT71586 is a fast 4K x 16 latched address CMOS static RAM designed to enhance cache memory designs. This device offers improved circuit board densities over designs using traditional RAM architectures in caches for the Intel 80386/82385, and the IDT79R3000 RISC CPU.

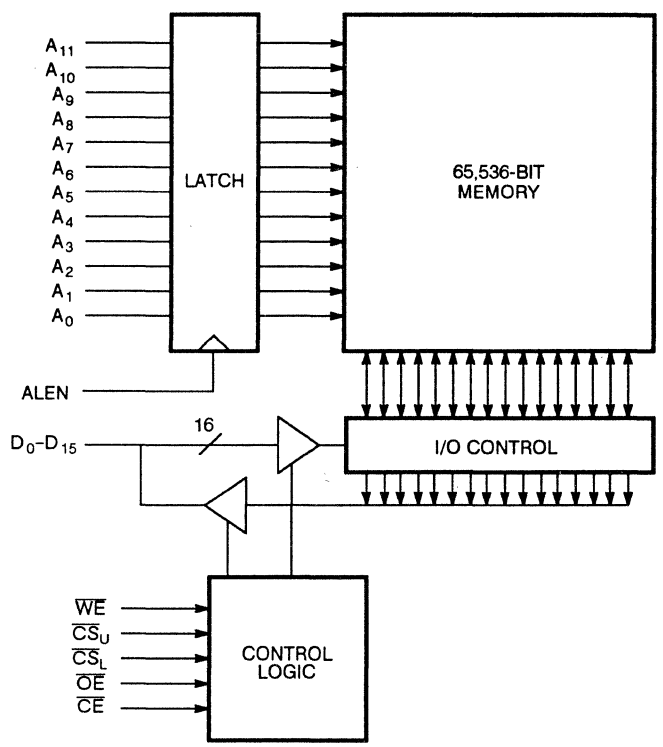
The IDT71586 boasts a fast address access time down to 35ns (max.), a very fast 11ns (max.) Output Enable pin, and short set-up and hold times (5ns max.) on the address input latch. All of these features help the IDT71586 to make the most efficient use of CPU-local buses.

Fabricated using IDT's CEMOS™ high-performance technology, the IDT71586 achieves this high throughput at a typical operating power of only 300mW.

All inputs and outputs of the IDT71586 are TTL-compatible, and the device operates from a standard 5V supply, simplifying system design. The IDT71586 is offered in a 40 pin CERDIP or plastic DIP, or a 44 pin plastic leadless chip carrier, providing high board level packing densities.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

FUNCTIONAL BLOCK DIAGRAM



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CMOS STATIC RAM 64K (8K x 8 BIT)

IDT7164S
IDT7164L

FEATURES:

- High-speed address/chip select access time
  - Military: 30/35/45/55/70/85/100/120/150/200ns (max.)
  - Commercial: 25/30/35/45ns (max.)
- Low power consumption
  - IDT7164S
    Active: 300mW (typ.)
    Standby: 100µw (typ.)
  - IDT7164L
    Active: 250mW (typ.)
    Standby: 30µw (typ.)
- Battery backup operation—2V data retention voltage (L Version only)
- Produced with advanced CEMOS™ high-performance technology
- Single 5V (±10%) power supply
- Input and output directly TTL-compatible
- Three-state output
- Static operation: no clocks or refresh required
- Available in standard 28-pin DIP (600 mil), 28-pin THINDIP (300 mil), 28-pin LCC, 32-pin LCC and PLCC and 28-pin SOIC
- Pin-compatible with standard 64K static RAM and EPROM
- Military product available compliant to MIL-STD-883, Class B
- Standard Military Drawing# 5962-85525 is listed on this function. Refer to Section 2/page 2-2.

DESCRIPTION:

The IDT7164 is a 65,536 bit high-speed static RAM organized as 8K x 8. It is fabricated using IDT's high-performance, high-reliability CEMOS technology.

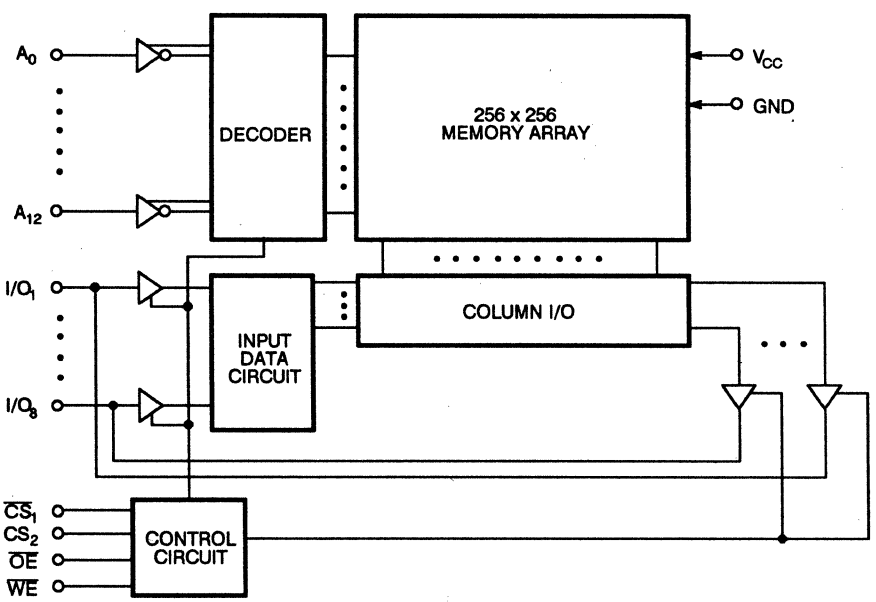
Address access times as fast as 25ns are available with typical power consumption of only 250mW. The circuit also offers a reduced power standby mode. When $\overline{CS}_1$ goes high or CS_2 goes low, the circuit will automatically go to, and remain in, a low-power standby mode. In the full standby mode, the low-power device typically consumes less than 30µW. The low-power (L) version also offers a battery backup data retention capability where the circuit typically consumes only 10µW operating off a 2V battery.

All inputs and outputs of the IDT7164 are TTL-compatible and operation is from a single 5V supply, simplifying system designs. Fully static asynchronous circuitry is used, requiring no clocks or refreshing for operation.

The IDT7164 is packaged in a 28-pin, 300 mil THINDIP; 28-pin, 600 mil DIP; 32-pin LCC and PLCC and 28-pin LCC and SOIC, providing high board-level packing densities.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM



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CMOS SRAM 64K (4K x 16)

ADVANCE INFORMATION
IDT7186S
IDT7186L

FEATURES:

- 16-bit word width, with separate control of upper and lower bytes
- High-speed access
  - Military: 55/70/85ns (max.)
  - Commercial: 45/55ns (max.)
- Low power consumption
  - IDT7186S
    Active: 400mW (typ.)
    Standby: 100µW (typ.)
  - IDT7186L
    Active: 300mW (typ.)
    Standby: 30µW (typ.)
- Separate upper-byte and lower-byte control for multiplexed bus compatibility
- JEDEC compatible pinout
- Battery backup operation—2V data retention
- Available in 40-pin, 600 mil plastic and sidebraze DIP
- TTL-compatible
- Single 5V (±10%) power supply
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

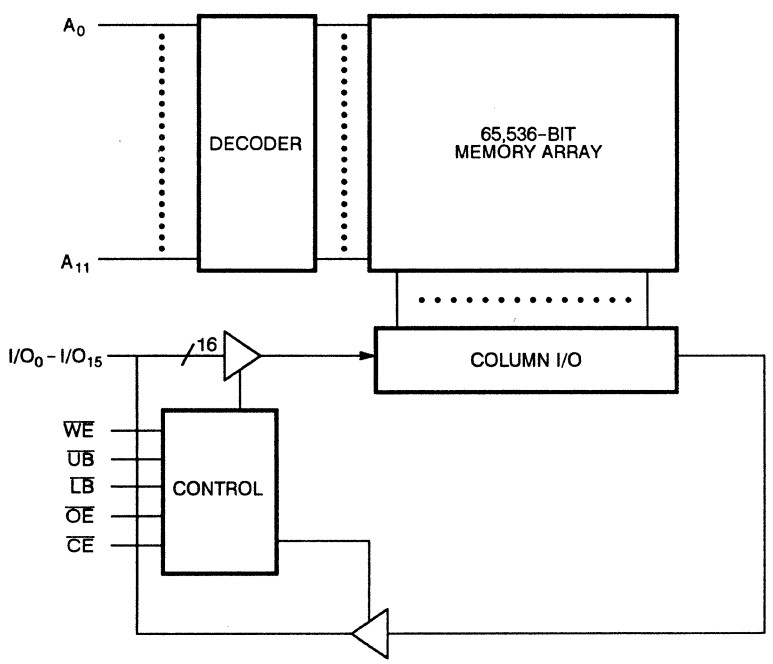
The IDT7186 is an extremely high-speed 4K x 16-bit static RAM designed for use in wide-word systems where high speed, low power and board density are of the utmost importance.

The IDT7186 uses sixteen bidirectional input/output lines to provide simultaneous access to all bits in a word and has two byte enable lines to allow the upper and lower byte of a word to be accessed either together or independently. A high-speed output enable pin allows designers to turn on the IDT7186's outputs at a speed much higher than the already fast address access time and achieve a considerable throughput advantage. An automatic power down feature, controlled by $\overline{CE}$, permits the on-chip circuitry to enter a very low standby mode.

Fabricated using IDT's CEMOS™ high-performance technology, the IDT7186 typically operates on only 300mW of power at maximum access times as fast as 45ns. Low-power (L) versions offer battery backup data retention capability, typically consuming 30µW from a 2V battery.

The IDT7186 is packaged in either a sidebraze or plastic 40-pin DIP. Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM



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CMOS STATIC RAM 64K (64K x 1-BIT)

IDT7187S
IDT7187L

FEATURES:

- High speed (equal access and cycle time)
  - Military: 25/30/35/45/55/70/85ns (max.)
  - Commercial: 15/20/25/30/35/45ns (max.)
- Low power consumption
  - IDT7187S
    Active: 300mW (typ.)
    Standby: 100µw (typ.)
  - IDT7187L
    Active: 250mW (typ.)
    Standby: 30µw (typ.)
- Battery backup operation—2V data retention (L version only)
- JEDEC standard high-density 22-pin plastic and hermetic DIP, 24-pin plastic SOIC, 22-pin and 28-pin leadless chip carrier and 24-pin flatpack and CERPACK
- Produced with advanced CEMOS™ high-performance technology
- Separate data input and output
- Input and output directly TTL-compatible
- Three-state output
- Static operation: no clocks or refresh required
- Military product compliant to MIL-STD-883, Class B
- Standard Military Drawing# 5962-86015 is pending listing on this function. Refer to Section 2/page 2-4.

DESCRIPTION:

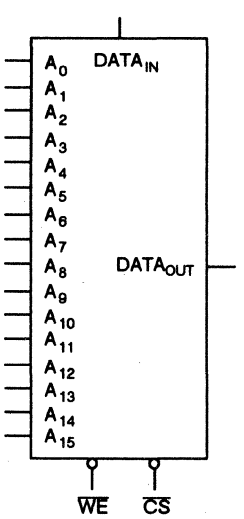
The IDT7187 is a 65,536-bit high-speed static RAM organized as 64K x 1. It is fabricated using IDT's high-performance, high-reliability technology, CEMOS. Access times as fast as 15ns are available with maximum power consumption of 880mW.

Both the standard (S) and low-power (L) versions of the IDT7187 provide two standby modes—I_{SB} and I_{SB1}. I_{SB} provides low-power operation (358mW max.); I_{SB1} provides ultra-low-power operation (5mW max.). The low-power (L) version also provides the capability for data retention using battery backup. When using a 2V battery, the circuit typically consumes only 30µW.

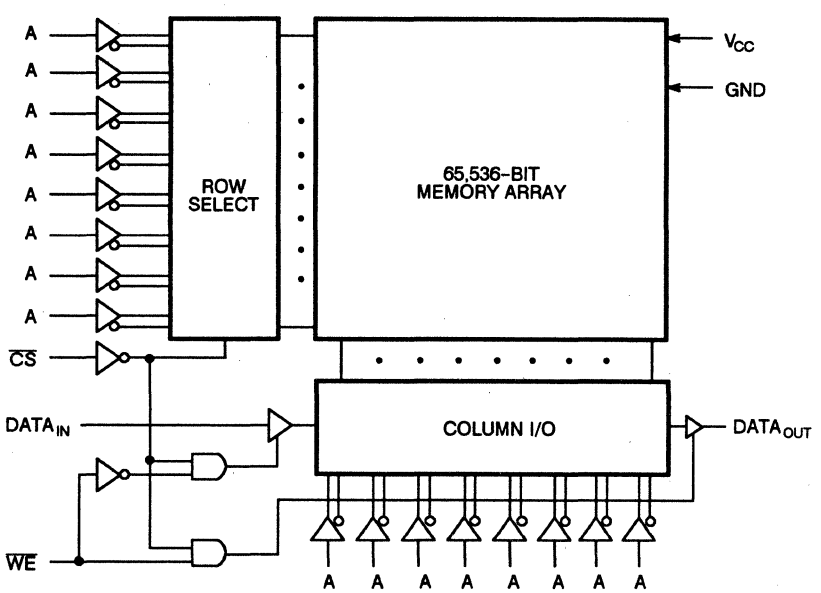
Ease of system design is achieved by the IDT7187 with full asynchronous operation, along with matching access and cycle times. The device is packaged in an industry standard 22-pin, 300 mil plastic or hermetic DIP, 24-pin plastic SOIC, 22- and 28-pin leadless chip carriers, or 24-pin flatpack or CERPACK.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

LOGIC SYMBOL



FUNCTIONAL BLOCK DIAGRAM



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CMOS PARALLEL FLAGGED FIFO WITH $\overline{OE}$ 1K x 9, 2K x 9, 4K x 9

IDT72021
IDT72031
IDT72041

FEATURES:

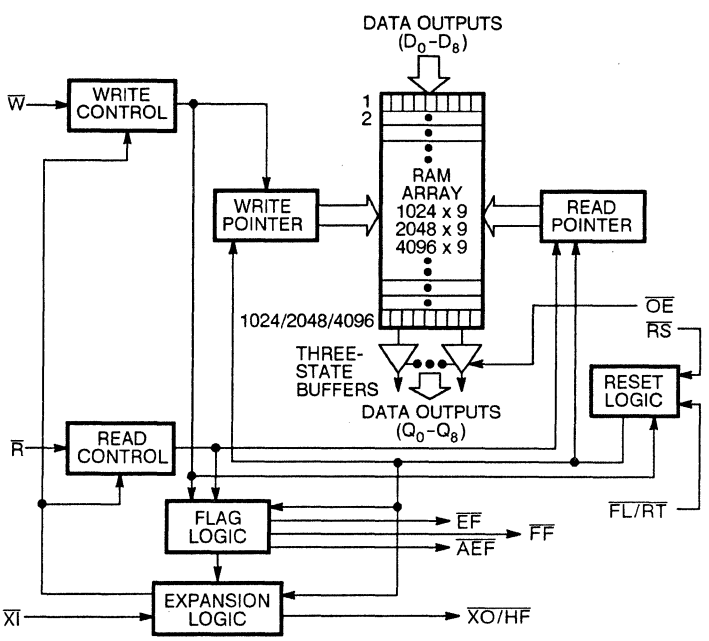
- First-In/First-Out dual-port memory
- Bit organization
  - IDT72021 – 1K x 9
  - IDT72031 – 2K x 9
  - IDT72041 – 4K x 9
- Ultra high speed
  - IDT72021 – 25ns access time, 35ns cycle time
  - IDT72031 – 35ns access time, 45ns cycle time
  - IDT72041 – 35ns access time, 45ns cycle time
- Low power CMOS
- Easily expandable in word depth and/or width
- Asynchronous and simultaneous read and write
- Functionally equivalent to IDT7202/03/04 with Output Enable ($\overline{OE}$) and Almost Empty/Almost Full Flag ($\overline{AEF}$)
- Four status flags: Full, Empty, Half-Full (single device mode), and Almost-Empty/Almost-Full (7/8 empty or 7/8 full in single device mode)
- Output Enable controls the data output port
- Auto-retransmit capability
- Available in 32-pin DIP and surface mount 32-pin LCC and PLCC
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

IDT72021/031/041s are high-speed, low-power, dual-port memory devices commonly known as FIFOs (First-In/First-Out). Data can be written into and read from the memory at independent rates. The order of information stored and extracted does not change, but the rate of data entering the FIFO might be different than the rate leaving the FIFO. Unlike a static RAM, no address information is required because the read and write pointers advance sequentially. The IDT72021/031/041s can perform asynchronous and simultaneous read and write operations. There are four status flags ($\overline{HF}$, $\overline{FF}$, $\overline{EF}$, $\overline{AEF}$) to monitor data overflow and underflow. Output Enable ($\overline{OE}$) is provided to control the flow of data through the output port. Additional key features are Write ($\overline{W}$), Read ($\overline{R}$), Retransmit ($\overline{RT}$), First Load ($\overline{FL}$), Expansion In ($\overline{XI}$) and Expansion Out ($\overline{XO}$). The IDT72021/031/041s are designed for those applications requiring data control flags and Output Enable ($\overline{OE}$) in multiprocessing and rate buffer applications.

The IDT72021/031/041s are fabricated using IDT's high-performance CEMOS™ technology. Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, for high reliability systems.

FUNCTIONAL BLOCK DIAGRAM



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CMOS PARALLEL FIRST-IN/FIRST-OUT FIFO 2048 x 9-BIT & 4096 x 9-BIT

IDT7203S/L
IDT7204S/L

FEATURES:

- First-In/First-Out dual-port memory
- 2048 x 9 organization (IDT7203)
- 4096 x 9 organization (IDT7204)
- Low power consumption
  - Active: 660mW (max.)
  - Power down: 66mW (max.)
- Asynchronous and simultaneous read and write
- Fully expandable by both word depth and/or bit width
- Pin and functionally compatible with IDT7201A/7202A
- IDT7204 allows 4096 word structure without expansion
- Half-Full Flag capability in single device mode
- Master/Slave multiprocessing applications
- Bidirectional and rate buffer applications
- Empty and full warning flags
- Auto retransmit capability
- High-performance CEMOS™ technology
- Available in CERDIP, Plastic DIP, PLCC and LCC
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT7203/7204 are dual-port memories that utilize a special First-In/First-Out algorithm that loads and empties data on a first-in/first-out basis. The device uses Full and Empty flags to prevent data overflow and underflow and expansion logic to allow for unlimited expansion capability in both word size and depth.

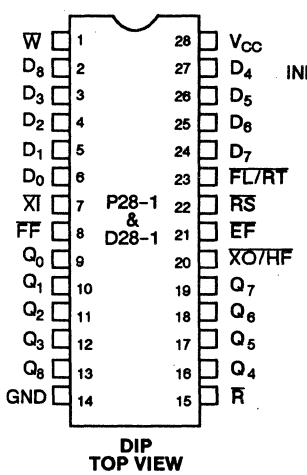
The reads and writes are internally sequential through the use of ring pointers, with no address information required to load and unload data. Data is toggled in and out of the device through the use of the Write ($\overline{W}$) and Read ($\overline{R}$) pins. The device has a read/write cycle time of 45ns (22.2MHz).

The device utilizes a 9-bit wide data array to allow for control and parity bits at the user's option. This feature is especially useful in data communications applications where it is necessary to use a parity bit for transmission/reception error checking. It also features a Retransmit ($\overline{RT}$) capability that allows for reset of the read pointer to its initial position when $\overline{RT}$ is pulsed low to allow for retransmission from the beginning of data. A Half-Full Flag is available in the single device mode and width expansion modes.

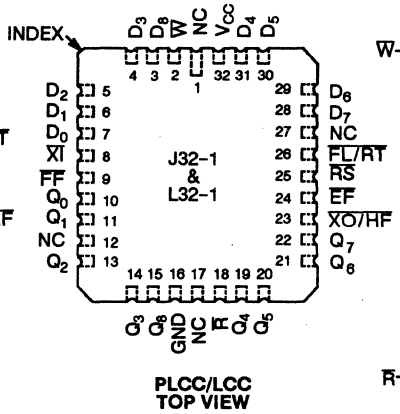
The IDT7203/7204 is fabricated using IDT's high-speed CEMOS technology. They are designed for those applications requiring asynchronous and simultaneous read/writes in multiprocessing and rate buffer applications. The 4096 x 9 organization for the IDT7204 allows a 4096 deep word structure without the need for expansion.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

PIN CONFIGURATIONS

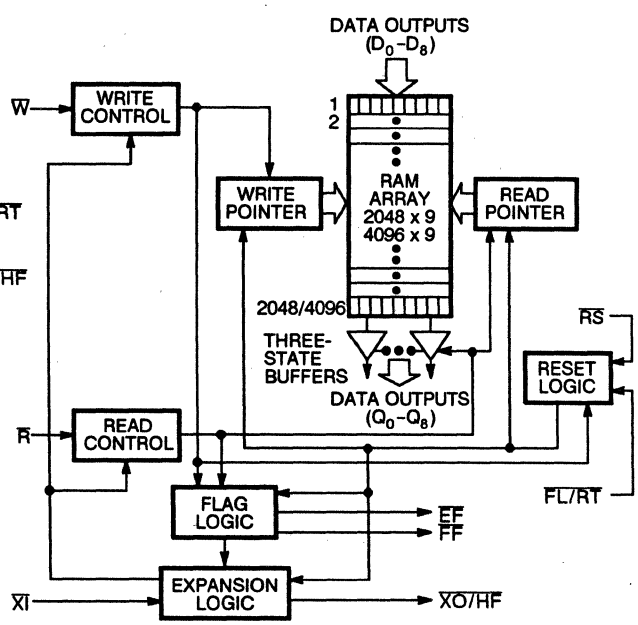


DIP
TOP VIEW



PLCC/LCC
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



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2048 x 9 Bit & 4096 x9Bit PARALLEL-to-SERIAL CMOS FIFO

IDT72131/ IDT72141

FEATURES:

- 35ns parallel port access time
- 50MHz serial port shift rate
- Easily expandable in depth and width
- Programmable word lengths of 7-9, 16-18, and 32 bits using Flexishift™ serial output without using any additional components
- Multiple status flags: Full, Almost-Full (1/8 from full), Half-Full, Almost-Empty (1/8 from empty), and Empty
- Asynchronous and simultaneous read and write operations
- Dual-ported zero fall-through time architecture
- Retransmit capability in single device mode
- Produced with high performance, low-power CEMOS™ technology
- Available in 28-pin ceramic and plastic DIP, 32-pin LCC and J-leaded PLCC
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

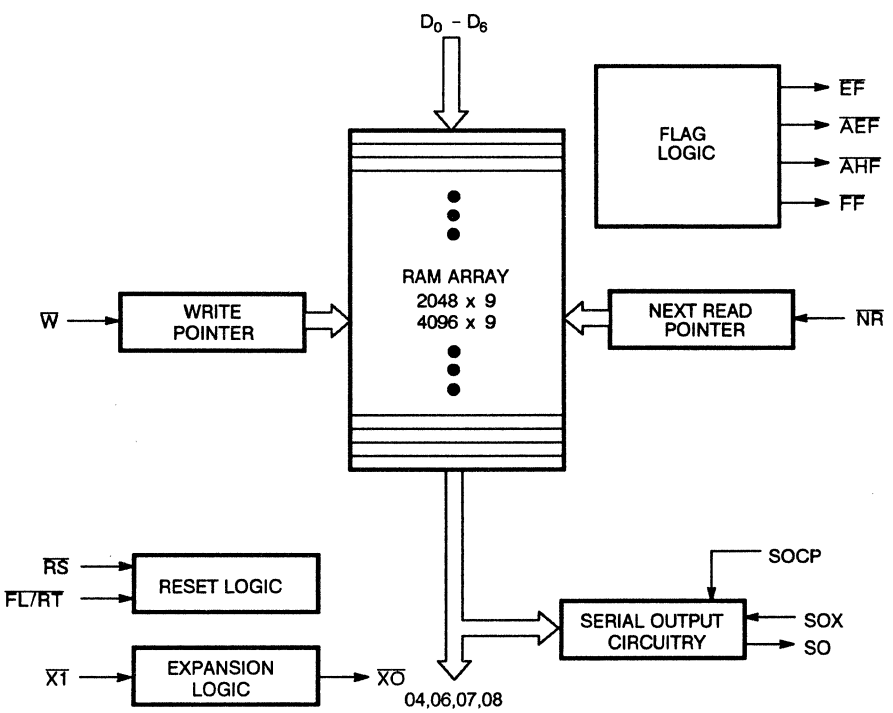
The IDT72131/72141 are high-speed, low power parallel-to-serial FIFOs. These FIFOs are ideally suited to serial communications applications, tape/disk controllers, and local area networks (LANs). The IDT72131/72141 can be configured with the IDT's serial-to-parallel FIFOs (IDT72132/72142) for bidirectional serial data buffering.

The FIFO has a 9-bit parallel input port and a serial output port. Wider and deeper parallel-to-serial data buffers can be built using multiple IDT72131/72141 chips. IDT's unique Flexishift™ serial expansion logic (SOX, NR) makes width expansion possible with no additional components. These FIFOs will expand to a variety of word widths including 8, 9, 16, and 32 bits. The IDT72131/141 can also be directly connected for depth expansion.

Five flags are provided to monitor the FIFO. The full and empty flags prevent any FIFO data overflow or underflow conditions. The almost-full (7/8), half-full, and almost-empty (1/8) flags signal memory utilization within the FIFO.

The IDT72131/72141 is fabricated using IDT's high-speed submicron CEMOS™ technology. Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

FUNCTIONAL BLOCK DIAGRAM



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2048 x 9 Bit 7 4096 x 9 Bit PARALLEL-to-SERIAL CMOS FIFO

IDT72132/ IDT72142

FEATURES:

- 35ns parallel port access time
- 50 MHz serial port shift rate
- Easily expandable in depth and width
- Programmable word lengths of 8, 9, 16-18, and 32 bits using Flexishift™ serial input without any additional components
- Multiple status flags: Full, Almost-Full (1/8 from full), Half-Full, Almost-Empty (1/8 from empty), and Empty
- Asynchronous and simultaneous read and write operations
- Dual-ported zero fall-through time architecture
- Retransmit capability in single device mode
- Produced with high-performance, low-power CEMOS ™ technology
- Available in a 28-pin ceramic and plastic DIP, 32-pin LCC and J-leaded PLCC
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT72132/72142 are high-speed, low-power serial-to-parallel FIFOs. These FIFOs are ideally suited to serial communications applications, tape/disk controllers, and local area networks (LANs). The IDT72132/72142 can be configured with the IDT's parallel-to-serial FIFOs (IDT72131/72141 for bidirectional serial data buffering.

The FIFO has a serial input port and a 9-bit parallel output port. Wider and deeper serial-to-parallel data buffers can be built using multiple IDT72132/72142 chips. IDT's unique Flexishift™ serial expansion logic (SIX, NW) makes width expansion possible with no additional components. These FIFOs will expand to a variety of word widths including 8, 9, 16, and 32 bits. The IDT72132/142 can also be directly connected for depth expansion.

Five flags are provided to monitor the FIFO. The full and empty flags prevent any FIFO data overflow or underflow conditions. The Almost-Full (7/8), Half-Full, and Almost-Empty (1/8) flags signal memory utilization within the FIFO.

The IDT72132/72142 is fabricated using IDT's high-speed submicron CEMOS™ technology. Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

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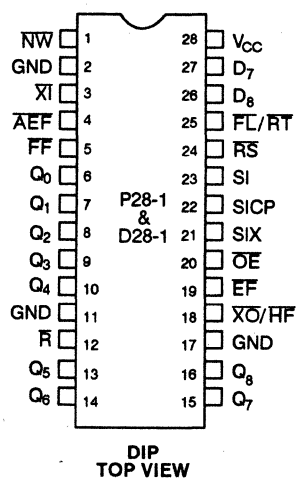
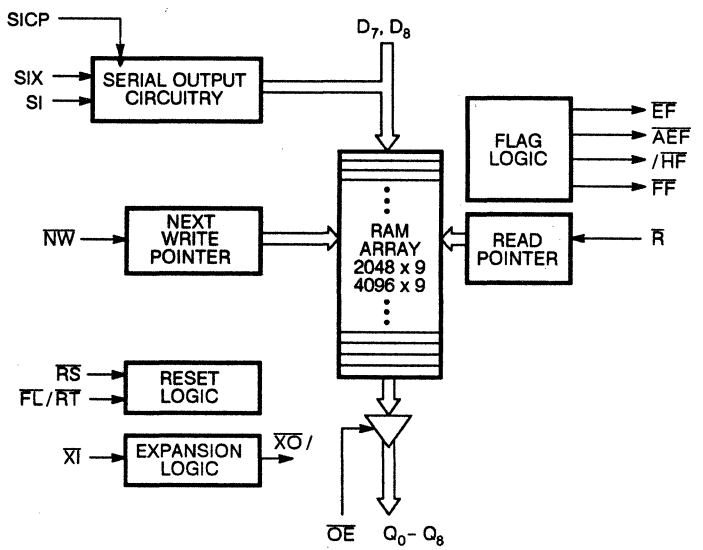
PIN CONFIGURATIONS



DIP
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



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1K x 18-BIT – 2K x 9-BIT CMOS BiFIFO™

ADVANCE INFORMATION
IDT7252

FEATURES:

- Bidirectional First-In/First-Out (FIFO) memory
- Back-to-back 1Kx18-bit and 2Kx9-bit FIFO organization
- Facilitates processor-to-peripheral and processor-to-processor communication
- Matches mixed bus widths: 16-bit to 8-bit buses and 32-bit to 8-bit buses
- Easy interface to microprocessor bus
- Asynchronous and simultaneous read and write operations
- Parity check and generate
- Convenient request/acknowledge interface program option for interface to peripherals
- Eight software programmable status Empty/Full Flags (offset and polarity) selectable onto four output pins
- Typical interface applications include microprocessor to floppy/hard disk controllers, microprocessor to SCSI bus, microprocessor to Local Area Network (LAN) controllers and microprocessor to 8-bit microcontroller
- Available in 48-pin DIP, and 70 mil center SHRINK-DIP and surface mount 52-pin LCC and PLCC
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

FIFOs are used to link microprocessors and peripherals together asynchronously for sending and receiving data and commands. Often the data or commands must be sent in both directions. The IDT7252 BiFIFO is a compact, highly integrated solution to simplifying data transfer between two processors or a processor and peripheral of different bus bandwidths. Using the BiFIFO can quadruple system throughput performance of the peripheral interface by eliminating inefficiencies associated with widely varying, mismatched bus widths. The BiFIFO can handle data transfers between 16-bit to 8-bit buses and 32-bit to 8-bit buses.

The BiFIFO can be accessed on either side by a microprocessor or bit-slice machine. It contains a1Kx18-bit FIFO in both directions. The 8-bit port views a 2Kx9-bit FIFO instead of a 1Kx18-bit FIFO. The ninth bit of this FIFO is available for control or parity and can be stored in the FIFO array or parity can be checked or generated. A unique data bypass mode allows for synchronous communication between two devices for initialization. Later asynchronous communications can occur via the FIFOs.

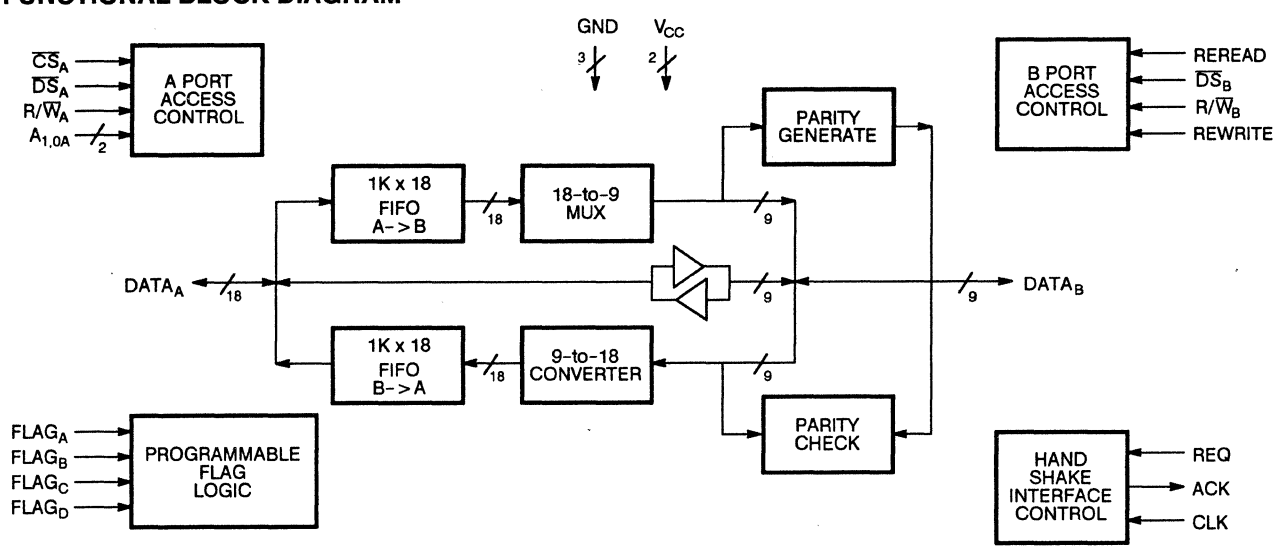
To ease connection to peripherals and reduce parts count, a request/acknowledge-type handshake is included that utilizes Request (REQ) and Acknowledge (ACK) signals. A microprocessor-type interface generates read and write strobes and accesses the internal read and write pointers.

Four status flags can be programmed to access any one of eight internal flags. Four Full/Empty Flags can be chosen, as well as four Full + Offset or Empty + Offset Flags. The offset value can be determined by the user. The polarity of the flags can also be set by the user.

The BiFIFO has an innovative Reread (RER) and Rewrite (REW) capability. The internal read and write pointers can be set to a position determined by the user through a control register. Then, upon signalling the RER input, the read pointer is reset to the initial position and data is read again. With signalling REW, the write pointer is reset to the initial position and data is written again.

The BiFIFO is available in a 48-pin DIP, 48-pin 70 mil center SHRINK-DIP and surface mount 52-pin LCC and PLCC packages. Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

FUNCTIONAL BLOCK DIAGRAM



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16 x 16-BIT PARALLEL CMOS MULTIPLIER WITH 32-BIT OUTPUT

PRELIMINARY
IDT7317

FEATURES

- 16 x 16-bit parallel multiplier with 32-bit output available immediately
- 20ns clocked multiply time
- Low power consumption: 400mW Max.
- One clock and three register enables
- Unsigned, Two's Complement or Mixed-Mode operations
- Flexible output scaling shifter
- Pipeline or Flow-through modes
- TTL-compatible input/output
- Three-state outputs
- Produced with advanced submicron CEMOS™ technology
- Available in 84-pin PLCC and 84-lead Pin Grid Array (PGA)
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION

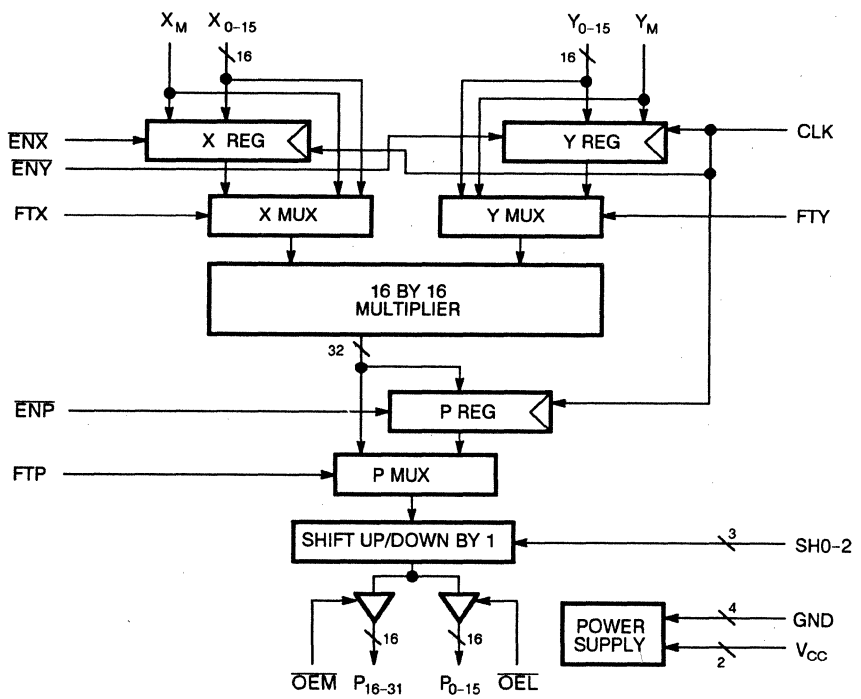
The IDT7317 is high-speed, low-power 16 x 16-bit multiplier that has double the throughput of comparable devices by virtue of a full 32-bit output product bus. The Most Significant Product (MSP) and Least Significant Product (LSP) can be independently enabled on an external 16-bit bus or simultaneously enabled on an external 32-bit bus. IDT's high-performance CEMOS™ technology produces very fast (20ns) clocked multiply times.

The output structure includes a programmable one-bit shifter for improved dynamic range algorithms using block floating point. This multiplier offers flexible configurations for clocked and flowed-through multiplications.

The IDT7317 is ideal for digital signal processing (DSP) applications requiring single-cycle 32-bit integer products. Some typical applications for this multiplier are 1-D and 2-D fast Fourier transforms (FFT), matrix multiplications, FIR and IIR filtering.

Military versions of the IDT7317 are manufactured in compliance with the latest revision of MIL-STD-883, Class B for high-reliability systems.

FUNCTIONAL BLOCK DIAGRAMS



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CMOS TRIPLE 8-BIT PALETTEDAC™

PRELIMINARY
IDT75C458

FEATURES:

- 125/110/80MHz operating speed
- Fixed pipeline delay: 8 clock cycles
- Triple 8-bit DACs
- Integral and differential linearity < 1/2LSB
- 256 x 24 Dual-Ported Color Palette RAM
- 4 x 24 Dual-Ported Overlay Palette RAM
- Multiplexed TTL pixel and overlay inputs
- RS-343A compatible RGB outputs
- Universal 8-bit MPU interface
- CEMOS™ monolithic construction
- Single 5V power supply
- 84-pin ceramic and plastic PGA package
- Typical power dissipation: 1000mW
- Pin- and function-compatible with Brooktree BT458
- Military product is compliant to MIL-STD-883, Class B

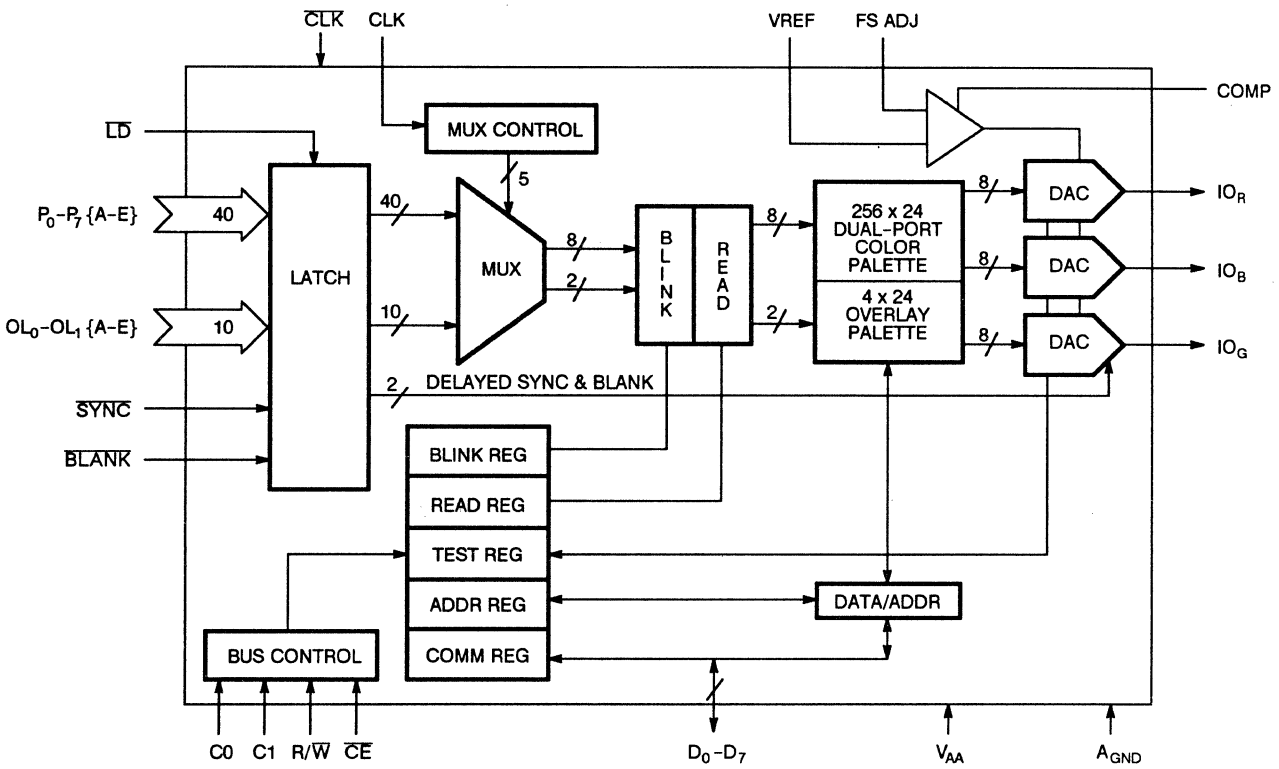
DESCRIPTION:

The IDT75C458 is a triple 8-bit video DAC with on-chip, dual-ported color palette memory. This chip is specifically designed for the display of high resolution color graphics. The architecture eliminates the ECL pixel interface by providing multiple TTL-compatible pixel ports and by multiplexing the pixel data on-chip.

The IDT75C458 supports up to 259 simultaneous colors from a palette of 16.8 million. Other features included on-chip are programmable blink rates, bit plane masking and blinking as well as a color overlay capability. The IDT75C458 generates RS-343A compatible red, green, and blue video outputs which are capable of directly driving a doubly terminated 75Ω coaxial cable.

The IDT75C458 military DACs are manufactured in compliance with the latest revision of MIL-STD-883, Class B, making them ideally suited to military temperature applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM



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CMOS FLASH A/D CONVERTER

IDT75C48

FEATURES:

- 8-bit resolution
- 30 MSPS conversion rate
- Guaranteed no missing codes
- Pin- and function-compatible with TRW 1048
- Low power consumption: 500mW
- Extended analog input range
- On-chip EDC (Error Detection and Correction)
- Improved output logic HIGH drive, no pull-up needed
- No sample and hold required
- Differential Phase < 1 Degree
- Differential Gain < 2%
- Selectable output formats
- TTL-compatible
- Available in 28-pin Plastic DIP, CERDIP and LCC
- Military product is compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT75C48 is a 30 MegaSample per Second (MSPS), fully parallel, 8-bit Flash Analog to Digital Converter. The wide input analog bandwidth of 10 MHz permits the conversion of analog input signals with full-power frequency components up to this limit with no input sample and hold. Low power consumption, due to CEMOS™ processing, virtually eliminates thermal considerations. The IDT75C48 is available in 28-pin plastic and hermetic DIPs and a 28-pin LCC.

The IDT75C48 consists of a reference voltage generator, 255 comparators, encoding and EDC (Error Detection and Correction) logic and an output data register. A single clock starts the conversion process and controls all internal operations. Two control inputs allow the output coding format to be programmed for straight binary or offset two's complement in either the true or inverted form.

The IDT75C48 military Flash A/D Converters are manufactured in compliance with the latest revision of MIL-STD-883, Class B, making them ideally suited to military temperature applications demanding the highest level of performance and reliability.

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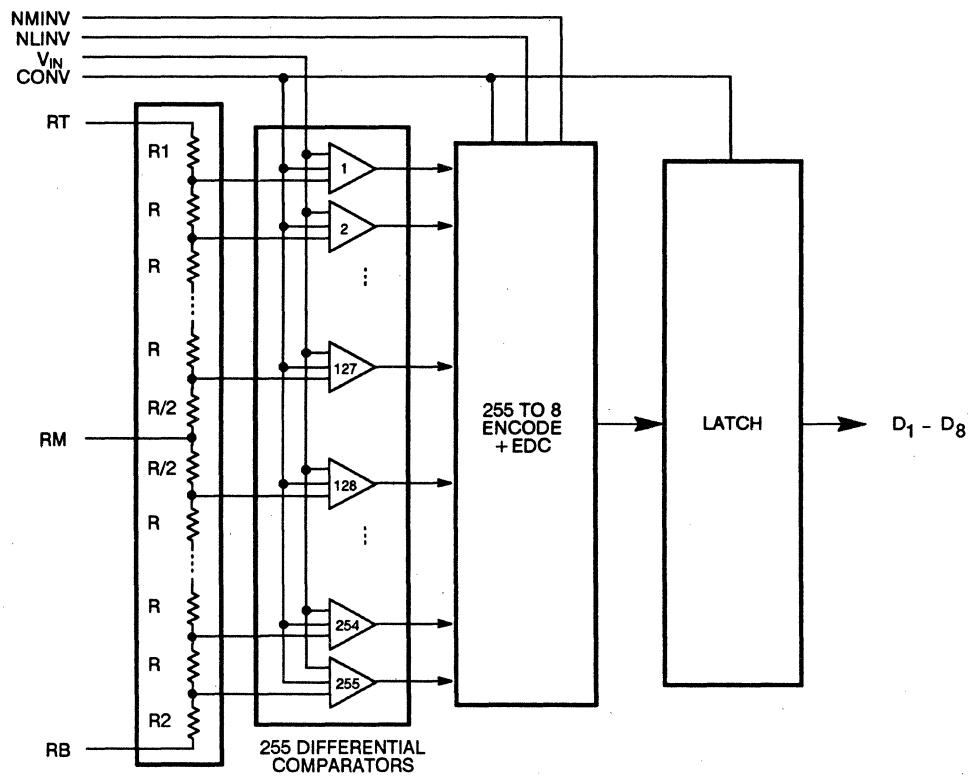
FUNCTIONAL BLOCK DIAGRAM



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CMOS FLASH A/D CONVERTER

PRELIMINARY
IDT75C58

FEATURES:

- 8-bit resolution
- 30 MSPS conversion rate
- Overflow Output
- Low power consumption: 500mW
- Guaranteed no missing codes
- Power-Down mode
- Extended analog input range
- On-chip EDC (Error Detection and Correction)
- Tri-state outputs
- Improved output logic HIGH drive, no pull-up needed
- No sample and hold required
- Differential Phase = 1 Degree
- Differential Gain = 2%
- TTL-compatible
- Available in 28-pin CERDIP and Plastic DIP or LCC
- Military product is compliant to MIL-STD-883, Class B

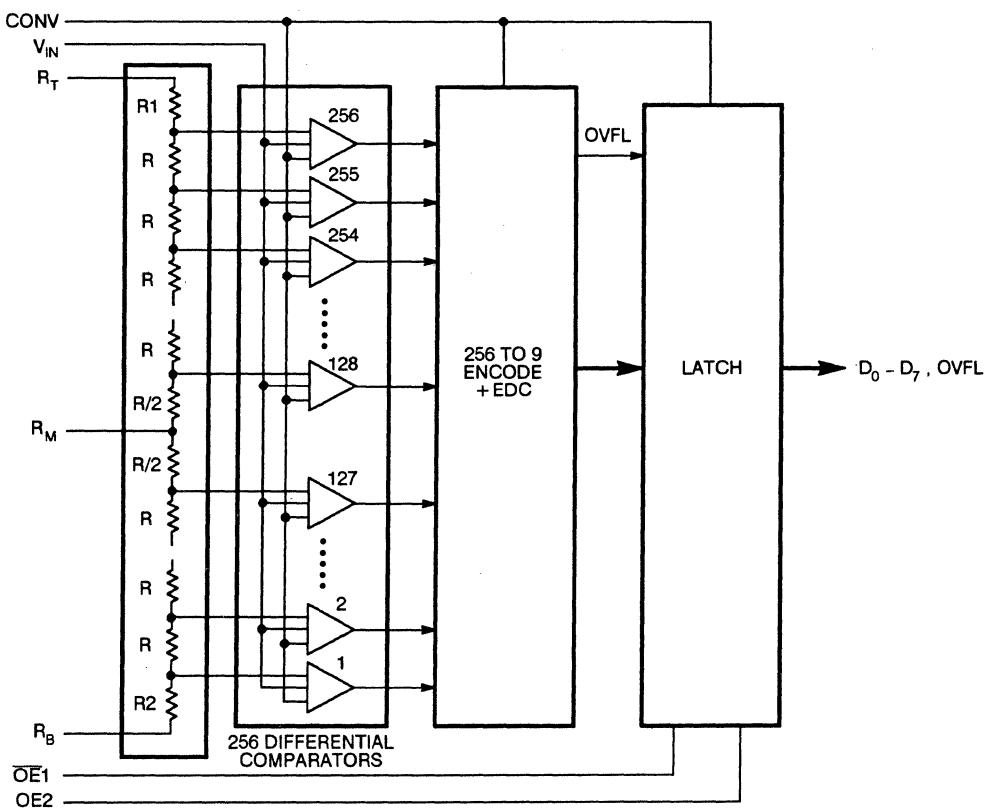
DESCRIPTION:

The IDT75C58 is a 30 MegaSample per Second (MSPS), fully parallel, 8-bit Flash Analog to Digital Converter. The wide input analog bandwidth of 10MHz permits the conversion of analog input signals with full-power frequency components up to this limit with no input sample and hold. Low power consumption due to CEMOS™ processing virtually eliminates thermal considerations. The IDT75C58 is available in 28-pin plastic and hermetic DIPs and a 28-pin LCC.

The IDT75C58 consists of a reference voltage generator, 256 comparators, encoding and EDC (Error Detection and Correction) logic and an output data register. A single clock starts the conversion process and controls all internal operations. An additional comparator detects an Overflow condition (V_{IN} more positive than Full-Scale + 1LSB) and activates the OVFL output. This output, together with two output enable inputs ($\overline{OE1}$ and OE2), allow the stacking of two IDT75C58s for 9-bit resolution with no external components.

The IDT75C58 military Flash A/D Converters are manufactured in compliance with the latest revision of MIL-STD-883, Class B, making them ideally suited to military temperature applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM



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RISC CPU PROCESSOR

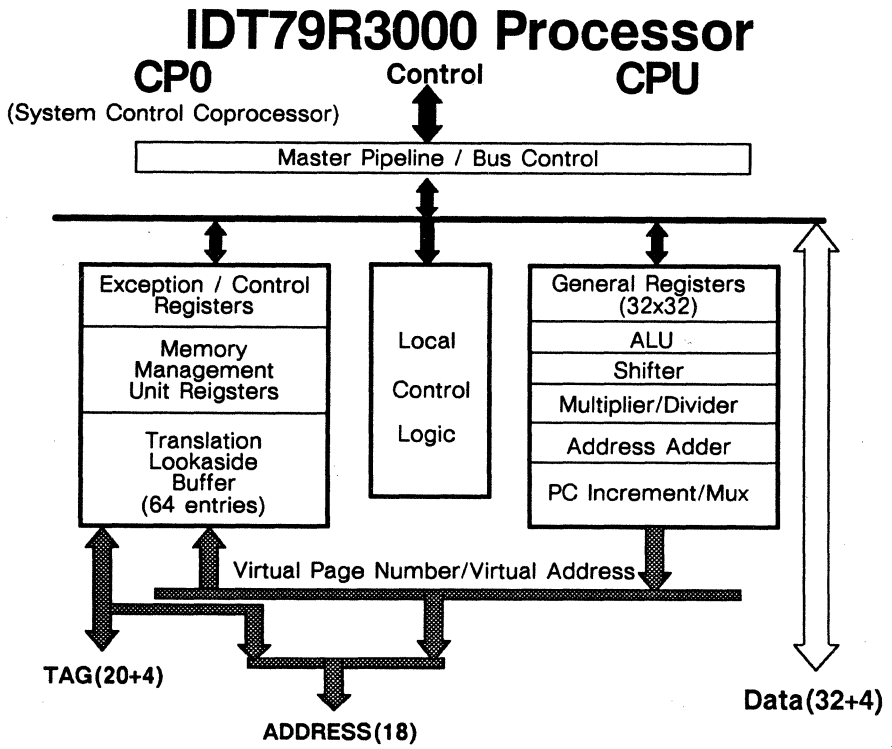
PRELIMINARY
IDT79R3000

FEATURES:

- Enhanced version of the IDT79R2000 RISC CPU
- Full 32-bit Operation—Thirty-two 32-bit registers and all instructions and addresses are 32-bit
- Efficient Pipelining—The CPU's 5-stage pipeline design assists in obtaining an execution rate approaching one instruction per cycle. Pipeline stalls and exceptions are handled precisely and efficiently
- On-Chip Cache Control—The IDT79R3000 provides a high bandwidth memory interface that handles separate external Instruction and Data Caches ranging in size from 4 to 256 Kbytes each. Both the caches are accessed during a single CPU cycle. All cache control is on-chip
- On-Chip Memory Management Unit—A fully-associative, 64 entry Transition Lookaside Buffer (TLB) provides fast address translation for virtual-to-physical memory mapping of the 4 Gigabyte virtual address space
- Coprocessor Interface—The IDT79R3000 generates all addresses and handles memory interface control for up to three additional tightly coupled external processors
- Optimizing Compilers are available for C, Fortran and Pascal
- UNIX™ System V.3 and BSD 4.3 operating systems supported
- High-speed CEMOS™ technology
- Instruction set compatible with the IDT79R2000 RISC CPU
- 16.7MHz and 25MHz clock rates yield 12 and 20 MIPS sustained throughput.
- Supports multiword block refill of both the instruction and data caches.
- Supports concurrent refill and execution of instructions.
- Partial word stores are executed as read-modify-write operations.
- The IDT79R3000 directly drives the cache control signals.
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT79R3000 processor consists of two tightly-coupled processors implemented on a single chip. The first processor is a full 32-bit CPU incorporating RISC (Reduced Instruction Set Computer) techniques to achieve a new standard of microprocessor performance. The second processor is a system control coprocessor (CP0), containing a TLB (Translation Lookaside Buffer) and control registers to support a virtual memory subsystem with a dual-cache bandwidth of up to 133 Mbytes/second. Figure 1 shows the functions incorporated within the IDT79R3000.



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RISC FLOATING-POINT ACCELERATOR (FPA)

PRELIMINARY
IDT79R3010

FEATURES:

- Hardware Support of Single- and Double-Precision Operations:
  - Floating-Point Add
  - Floating-Point Subtract
  - Floating-Point Multiply
  - Floating-Point Divide
  - Floating-Point Comparisons
  - Floating-Point Conversions
- Sustained performance:
  - 7 MFLOPS single precision LINPACK
  - 4 MFLOPS double precision LINPACK
- Cycle Time: 40-60ns (16-25MHz)
- Direct, High-Speed Interface to IDT79R3000 Processor
- Supports Full Conformance With IEEE 754-1985 Floating-Point Specification
- Floating-Point Registers: Sixteen 64-bit registers
- High-speed CEMOS™ technology
- Pin, functionally and software compatible with the MIPS Computer Systems R2010 RISC FPA
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT79R3010 Floating-Point Accelerator (FPA) operates in conjunction with the IDT79R3000 Processor and extends the IDT79R3000's instruction set to perform arithmetic operations on values in floating-point representations. The IDT79R3010 FPA, with associated system software, fully conforms to the requirements of ANSI/IEEE Standard 754-1985, "IEEE Standard for Binary Floating-Point Arithmetic." In addition, the architecture fully supports the standard's recommendations.

- **Full 64-bit Operation** - The IDT79R3010 contains sixteen, 64-bit registers that can each be used to hold single-precision or double-precision values. The FPA also includes a 32-bit status/control register that provides access to all IEEE-Standard exception handling capabilities.
- **Load/Store instruction set** - like the IDT79R3000 processor, the IDT79R3010 uses a load/store-oriented instruction set, with single-cycle loads and stores. Floating-point operations are started in a single cycle and their execution is overlapped with other fixed point or floating-point operations.
- **Tightly-coupled coprocessor interface** - the FPA connects to the IDT79R3000 RISC processor to form a tightly-coupled unit with a seamless integration of floating point and fixed point instruction sets. Since each unit receives and executes instructions in parallel, some floating point instructions can execute at the same single-cycle per instruction rate as fixed point instructions.

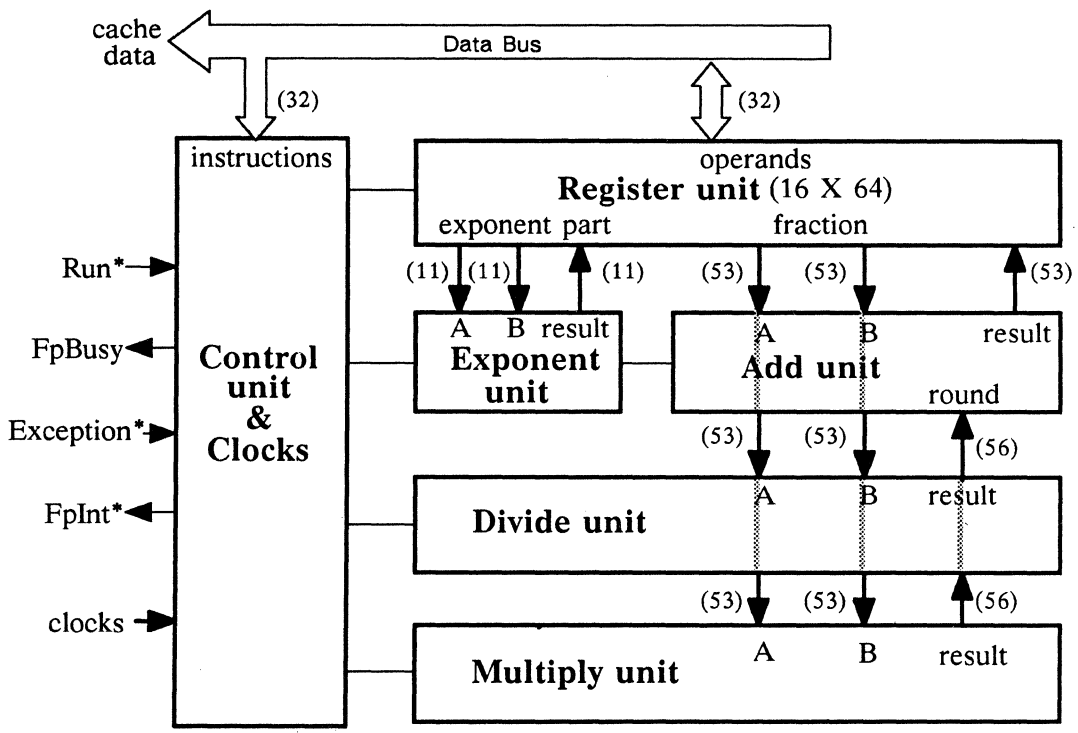

Figure 1. IDT79R3010 Functional Block Diagram

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RISC CPU WRITE BUFFER

PRELIMINARY
IDT79R3020

FEATURES

- Temporary storage buffers to enhance the performance of the IDT79R3000 RISC CPU processor
- Allows for write operations by the RISC CPU processor during Run cycles
- Each Write Buffer has four locations to handle an 8-bit address slice and a 9-bit data slice (including a parity bit)
- High-speed CEMOS™ technology
- Pin, functionally and software compatible with the MIPS Computer Systems R2020 Write Buffer
- Military product complaint to MIL-STD-883, Class B

DESCRIPTION

The IDT79R3020 Write Buffer enhances the performance of IDT79R3000 systems by allowing the processor to perform write operations during Run cycles instead of resorting to time-consuming stall cycles. Each IDT79R3020 device handles an 8-bit slice of address, and a 9-bit slice of data (one parity bit per byte); thus, four IDT79R3020s provide 4-deep buffering of 32 bits of address and 36 bits of data and parity. Figure 1 illustrates the functional position of the Write Buffer in an IDT79R3000 system.

Whenever the processor performs a write operation, the write buffer captures the output data and its address (including the access type bits). The write buffer can hold up to four data-address sets while it waits to pass the data on to main memory. Transfers from the processor to the write buffers occur synchronously at the cycle rate of the processor and the write buffer signals the processor if it is unable to accept data. The write buffer also provides a set of handshake signals to communicate with a main memory controller and coordinate the transfer of write data to main memory.

The sections that follow describe these IDT79R3020 Write Buffer interfaces:

- the processor-write buffer interface
- the write buffer-main memory interface
- a miscellaneous, write buffer-board control interface.

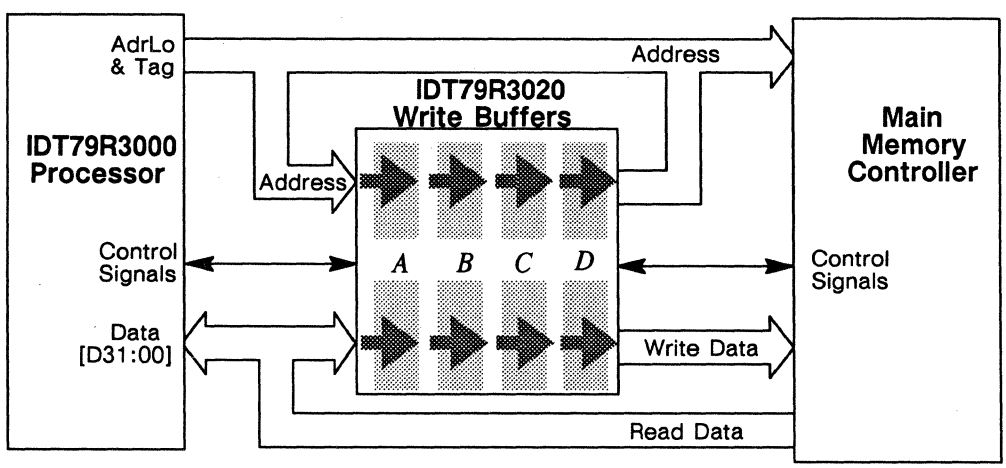

Figure 1. The IDT79R3020 Write Buffer in an IDT79R3000 System.

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256K (32K x 8-BIT) DUAL-PORT CMOS STATIC RAM MODULE

IDT7M137

FEATURES:

- High-density 256K-bit CMOS dual-port RAM module
- 32K x 8 organization
- Low power consumption
- CEMOS™ process virtually eliminates alpha particle soft error rates (with no organic die coating)
- Battery backup operation—2V data retention
- Fully asynchronous operation from either port
- Single 5V(±10%) power supply
- Dual V_{CC} and GND pins for maximum noise immunity
- Inputs and outputs directly TTL-compatible
- Fully static operation
- Modules available with semiconductor components compliant to MIL-STD-883, Class B

DESCRIPTION:

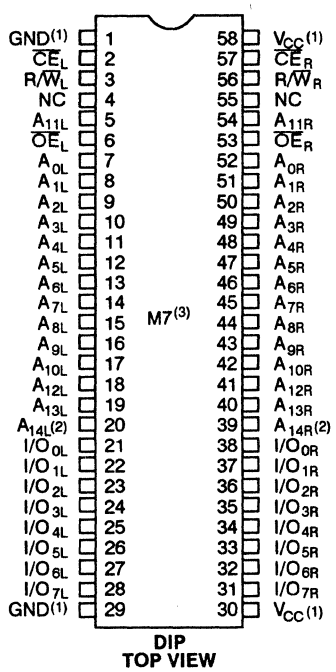
The IDT7M137 is a 256K-bit high-speed CMOS dual-port static RAM module constructed on a multi-layered ceramic substrate using eight IDT7134 dual-port RAMs in leadless chip carriers. The full 32K bytes of dual-port RAM are directly addressable by utilization of the two on-board IDT54/74FCT138 decoder circuits that interpret the higher order addresses A_{L12-14} and A_{R12-14} to select one of the eight 4K x 8 dual-port RAMs. Extremely high speeds are achieved in this fashion due to the use of the IDT7134 dual-port RAM, fabricated in IDT's high-performance CEMOS technology.

The IDT7M137 provides two ports with separate control, address and I/O pins that permit independent, asynchronous access for reads or writes to any location in the memory. The IDT7M137 is designed to be used in systems where on-chip hardware port arbitration is not needed. It is the user's responsibility to ensure data integrity when simultaneously accessing the same memory location from both ports.

The IDT7M137 is available with access times as fast as 55ns commercial and 60ns military temperature range, with operating power consumption of only 4W (max.) The modules also offer a standby power mode of 3.6W (max.) and full standby mode of 1.3W (max.).

All IDT military module semiconductor components are manufactured in compliance to the latest revision of MIL-STD-883, Class B, making them ideally suited to applications demanding the highest level of performance and reliability.

PIN CONFIGURATION



DIP
TOP VIEW

PIN NAMES

LEFT PORT	RIGHT PORT	NAMES
$\overline{CE}_L$	$\overline{CE}_R$	Chip Enable
$R/\overline{W}_L$	$R/\overline{W}_R$	Read/Write Enable
$\overline{OE}_L$	$\overline{OE}_R$	Output Enable
A_{0L-14L}	A_{0R-14R}	Address
I/O_{0L-7L}	I/O_{0R-7R}	Data Input/Output
V_{CC}		Power
GND		Ground

NOTES:

1. Both V_{CC} pins need to be connected to the 5V supply and both GND pins need to be grounded for proper operation.
2. On 16K x 8 IDT7M136 option, A_{14L} and A_{14R} need to be externally connected to ground for proper operation.
3. For module dimensions, please refer to module drawing M7 in the packaging section.

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16K x 9 FIFO/8K x 9 FIFO

ADVANCE INFORMATION
IDT7M205
IDT7M206

FEATURES:

- First-In/First-Out memory module
- 8K x 9 organization (IDT7M205S)
- 16K x 9 organization (IDT7M206S)
- Low power consumption
  - Active: 840mW (typ. Com'l.)
  - Power Down: 176mW (max. Com'l)
- Asynchronous and simultaneous read and write
- Fully expandable by both word depth and/or bit width
- Assembled with IDT's high-reliability vapor phase solder reflow process
- Single 5V (±10%) power supply
- MASTER/SLAVE multiprocessing applications
- Bidirectional and rate buffer applications
- Empty and Full warning flags
- High-performance CEMOS™ technology
- Pin-compatible with IDT7201 and Mostek MK4501, but with 16 times word depth (IDT7M205S) or 32 times (IDT7M206S)
- Module available with semiconductor components compliant to MIL-STD-883, Class B

DESCRIPTION:

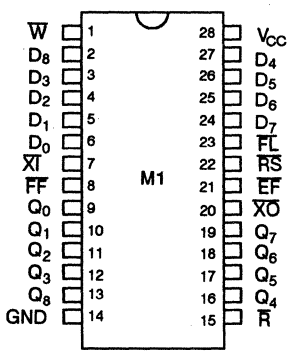
The IDT7M205S/206S are FIFO memory modules constructed on a multi-layered ceramic substrate using four IDT7203 (2K x 9) or four IDT7204 (4K x 9) FIFOs in leadless chip carriers. Extremely high speeds are achieved in this fashion due to the use of IDT7203s and IDT7204s fabricated in IDT's high-performance CEMOS technology. These devices utilize a special First-In/First-Out algorithm that loads and empties data on a first-in/first-out basis. The device uses Full and Empty flags to prevent data overflow and underflow and expansion logic to allow for unlimited expansion capability in both word size and depth.

The reads and writes are internally sequential through the use of ring pointers, with no address information required to load and unload data. Data is toggled in and out of the device through the use of the WRITE ($\overline{W}$) and READ ($\overline{R}$) pins. The devices have a read/write cycle time of 50ns (25MHz) for commercial and 65ns (15MHz) for military temperature ranges.

The devices utilize a 9-bit wide data array to allow for control and parity bits at the user's option. This feature is especially useful in data communications applications where it is necessary to use a parity bit for transmission/reception error checking.

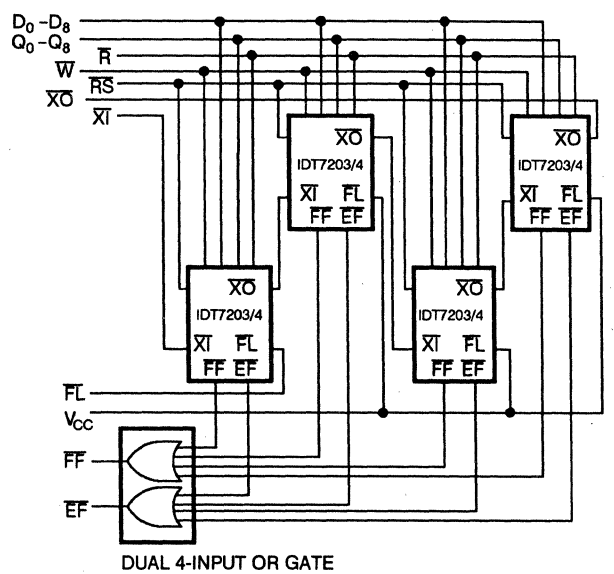
IDT's Military FIFO modules have semiconductor components manufactured in compliance with the latest revision of MIL-STD-883, Class B, making them ideally suited to applications demanding the highest level of performance and reliability.

PIN CONFIGURATION



DIP
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



DUAL 4-INPUT OR GATE

PIN NAMES

$\overline{W}$ = WRITE	$\overline{FL}$ = FIRST LOAD	$\overline{XI}$ = EXPANSION IN	$\overline{EF}$ = EMPTY FLAG
$\overline{R}$ = READ	D = $DATA_{IN}$	$\overline{XO}$ = EXPANSION OUT	V_{CC} = 5V
$\overline{RS}$ = RESET	Q = $DATA_{OUT}$	$\overline{FF}$ = FULL FLAG	GND = GROUND

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4 MEGABIT (256K X 16) CMOS SRAM

IDT7M4016

FEATURES:

- High-density 4 megabit (256K x 16) CMOS static RAM module
- Low power consumption
- Assembled with IDT's high-reliability vapor phase solder reflow process
- Available in 48-pin, 900 mil wide ceramic sidebraze DIP
- 4X the density of the IDT7M624 (1024K RAM module) in the same size package
- Multiple GND pins for maximum noise immunity
- Single 5V (±10%) power supply
- Inputs and outputs directly TTL-compatible
- Modules available with semiconductor components compliant to MIL-STD-883, Class B

DESCRIPTION:

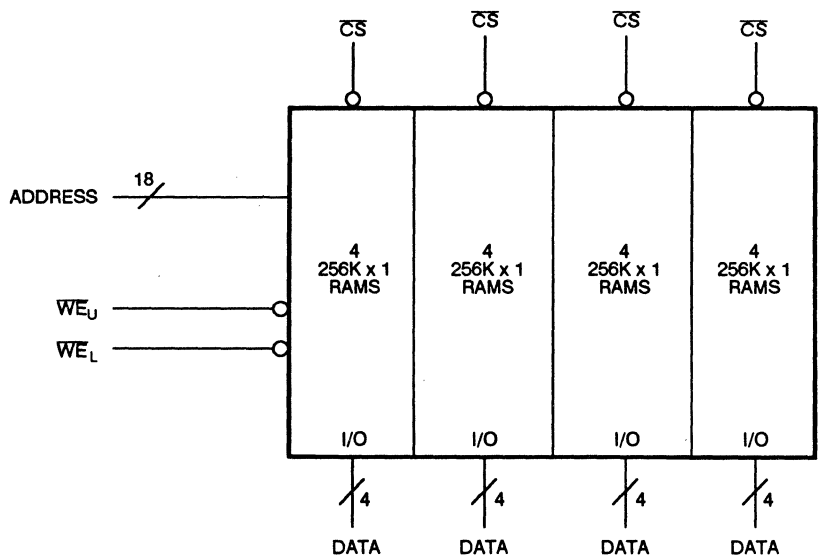
The IDT7M4016 is a 4-megabit high-speed CMOS static RAM module constructed on a multi-layered ceramic substrate using sixteen (256K x 1) static RAMs in leadless chip carriers. The IDT7M4016 is an upgrade from the IDT7M624 (1024K RAM module) offering four times the memory density in the same size package. Making four chip select lines available (one for each group of four RAMs) allows the user to configure the memory into a 256K x 16, 512K x 8 or 1024K x 4 organization.

The IDT7M4016 is packaged in a 48-pin, 900 mil center sidebraze DIP to take advantage of the compact leadless chip carriers. This enables four megabits of static RAM memory to be placed in less than 2.2 square inches of board space.

All inputs and outputs of the IDT7M4016 are TTL-compatible and operate from a single 5V supply. Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation, and providing equal access and cycle times for ease of use.

All IDT military module semiconductor components are compliant to the latest revision of MIL-STD-883, Class B, making them ideally suited to applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM



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2 MEGABIT (64K X 32) CMOS STATIC RAM MODULE

IDT7M4017

FEATURES:

- High-density 2 megabit (64K x 32) CMOS static RAM module
- Fast access times
  - Military: 50ns (max.)
  - Commercial: 40ns (max.)
- Individual byte selects
- Upper and lower word write enables
- CEMOS™ process virtually eliminates alpha particle soft error rates (with no organic die coating)
- Available in 60-pin, 600 mil wide ceramic sidebraze DIP
- Single 5V (±10%) power supply
- Inputs and outputs directly TTL-compatible
- Modules available with semiconductor components compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT7M4017 is a 2 megabit (64K x 32) high-speed static RAM module constructed on a co-fired ceramic substrate using eight IDT71256 32K x 8 static RAMs in leadless chip carriers. On-board decoders use A_{15} to select the upper or lower bank of RAMs. Four chip selects control individual byte selection. Extremely fast speeds can be achieved due to use of 256K static RAMs and the decoder fabricated in IDT's high-performance, high-reliability CEMOS technology.

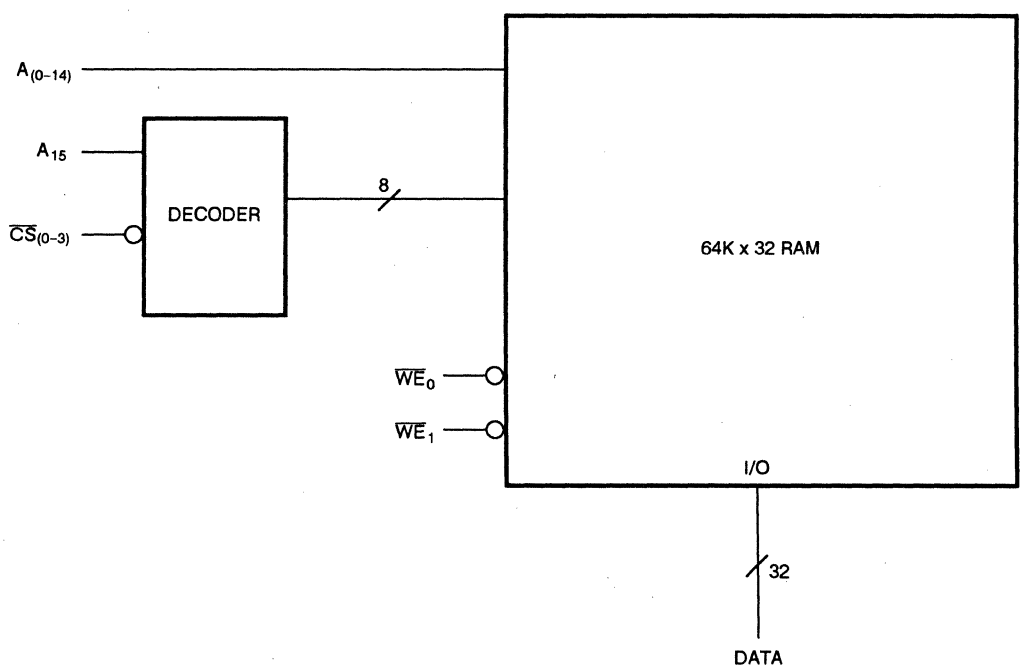
The IDT7M4017 is offered in a 60-pin, 600 mil center sidebraze DIP which enables two megabits of memory to be placed in less than 1.9 square inches of board space.

The IDT7M4017 is available with fast access times over the commercial and military temperature ranges, with minimal power consumption. The circuit also offers a reduced power standby mode. When $\overline{CS}$ goes high, the circuit will automatically go to a substantially lower power mode.

All inputs and outputs of the IDT7M4017 are TTL-compatible and operate from a single 5V supply. Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation, and providing equal access and cycle times for ease of use.

All IDT military module semiconductor components are manufactured in compliance with MIL-STD-883, Class B, making them ideally suited to applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM



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512K (64K x 8 or 64K x 9) CMOS SYNCHRONOUS RAM MODULE

PRELIMINARY
IDT7M6028
IDT7M6029

FEATURES:

- Internal pipeline registers on address, data and control lines
- Very fast write cycle time
- High-speed
  - Military: 35ns (max.)
  - Commercial: 25ns (max.)
- Low power consumption
- All inputs/outputs TTL-compatible (V_{OL} = 0.4V @ I_{OL} = 8mA)
- Separate, registered data input and output
- Three-state output
- Available in 42-pin, 600 mil sidebraze DIP
- Utilizes the IDT71501 high-performance synchronous RAM fabricated with advanced CEMOS™ high-performance technology
- Modules available with semiconductor components compliant to MIL-STD-883, Class B
- Finished modules tested at room, hot and cold temperatures for all AC and DC parameters

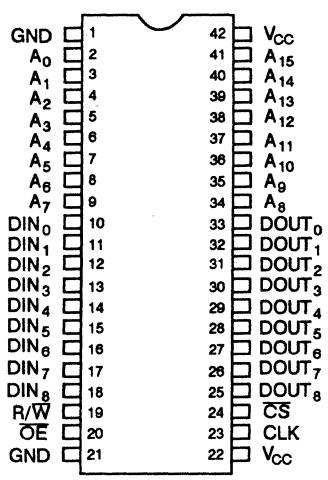
DESCRIPTION:

The IDT7M6028/IDT7M6029 is a high-speed static RAM module organized as either 64K x 8 or 64K x 9, constructed on a co-fired ceramic substrate using 8 IDT71501s (7M6028) or 9 IDT71501s (7M6029) high-speed synchronous RAMs in leadless chip carriers. Extremely fast speeds can be obtained using 64K RAMs fabricated in IDT's high-performance, high-reliability CEMOS™ technology. The module is synchronized with pipeline registered on the Address, Data, Chip Select ($\overline{CS}$) and Write Enable ($\overline{WE}$) pins and is designed for pipelined processing systems by removing the need for external pipeline registers. The internal registers offer speed improvements through higher integration of system functions.

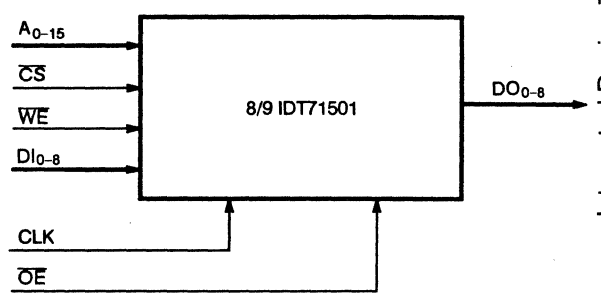
Read cycle times are as fast as 25ns, with higher speed Output Enable ($\overline{OE}$) and Clock to Valid Data Output functions to permit the maximum throughput possible in an efficient, large-memory pipelined system. Write cycles are as fast as 15ns. The IDT7M6028 and IDT7M6029 are packaged in a 42-pin, 600 mil wide sidebraze DIP.

All IDT military module semiconductor components are compliant with the latest revision of MIL-STD-883, Class B, making them ideally suited to applications demanding the highest level of performance and reliability.

PIN CONFIGURATION



FUNCTIONAL BLOCK DIAGRAM



PIN NAMES

GND	Ground
V_{CC}	Power
A_0 - A_{15}	Addresses
DIN_0 - DIN_8	Data Input
$DOUT_0$ - $DOUT_8$	Data Output
R/$\overline{W}$	Read/Write Enable
$\overline{OE}$	Output Enable
$\overline{CS}$	Chip Select
CLK	Clock Input

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4K x 80 WRITABLE CONTROL STORE STATIC RAM MODULE WITH ON-BOARD SEQUENCER

PRELIMINARY
IDT7M6052

FEATURES:

- Serial Protocol Channel (SPC™) reading, writing and interrogation
- Seperate chip select, write enable and output enable memory controls
- High fanout pipeline register
- Fully width expandable
- Designed for high-speed writable control store applications
- Assembled with IDT's high-reliability vapor phase solder reflow process
- Compact 128-pin ceramic QIP (quad in-line package)
- Single 5V (+/- 10%) power supply
- Inputs and outputs directly TTL-compatible
- Military modules available with semiconductor components manufactured in compliance to MIL-STD-883, Class B

DESCRIPTION:

The IDT7M6052 is a 4K x 80 Writable Control Store with on-board sequencer, on a multilayer co-fired ceramic substrate, using five IDT71502 (4K x 16 registered RAMs), an IDT39C10 (12-bit sequencer) and an IDT54/74FCT521 (8-bit comparator) for parity verification. The IDT7M6052 is offered in a 128-pin, 600 mil wide quad in-line package (QIP).

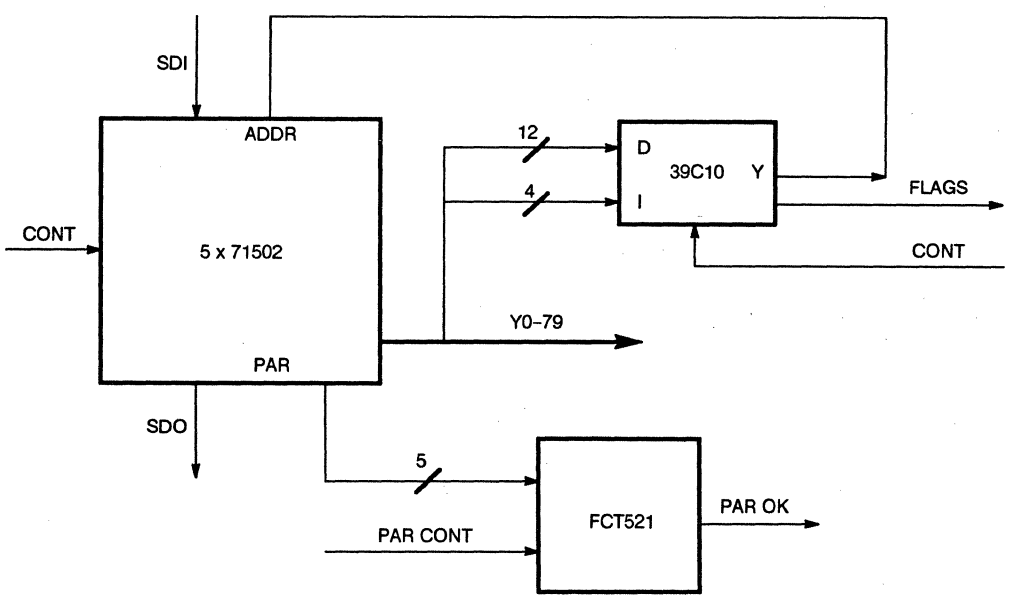
In normal operation (Read Mode), the D(0:11) inputs of the sequencer are driven the Y(0:11) outputs of the first RAM and the I(0:3) inputs are driven by the Y(16:19) outputs of the second RAM. Since each of the RAMs has its own external output enable, either or both of these fields can be overridden from an external source, i.e. by negating $\overline{OE}$ (0-15). Y(0:15) is placed in the Hi-Z mode, allowing the D(0:11) inputs to the sequencer to be driven from an external source (similarly for Y(16:32), which includes the I(0:3) field). The output from the sequencer drives the addresses of all of the RAMs. All the control, clocks and flags of the sequencer are connected directly to module pins for external control. (For additional details on how the sequencer operates, please refer to the IDT39C10 data sheet.) All controls and clocks, except for output enables, parity and the serial data path, are bussed to all RAMs and connected to module pins for external control. The serial data path is daisy chained through the five RAMs to give an 80-bit SPC configuration. (For additional information on the RAM operation, please refer to the IDT71502 data sheet).

The WCS can be loaded using either the serial data path and the SPC controls, or in parallel from the Y(0:79) pins, again using the SPC controls. The addrtess for the RAMs will either be from the internal counetr in each RAM for loading sequenctial loactions, or by external control of the sequencer.

The parity output from each RAM is connected to a module pin and also to an input of the on-board comparator. The five RAM parities, together with 3 additional parity inputs (PAR_0 to PAR_2), are compared to PAR_P (tied to all 8 inputs of the other side of the comparator) to generate $\overline{PAR_OK}$.

The semiconductor components used on all IDT milatary modules are maufactured in compliance with the latest revision of MIL-STD-883, Class B, making them ideally suited to applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM



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256K (16K x 16) CMOS STATIC RAM DUAL SIP MODULE

IDT7MC4005

FEATURES:

- High-density 16-bit word 256K (16K x 16) static RAM module
- Low profile 36-pin sidebraze ceramic DSIP (dual single-in-line package)
- Fast access time: 20ns (max.)
- Surface mounted LCC components mounted on a co-fired ceramic substrate
- CEMOS™ process virtually eliminates alpha particle soft error rates (with no organic die coating)
- Single 5V (±10%)
- Inputs/outputs directly TTL-compatible
- Multiple GND pins for maximum noise immunity

DESCRIPTION:

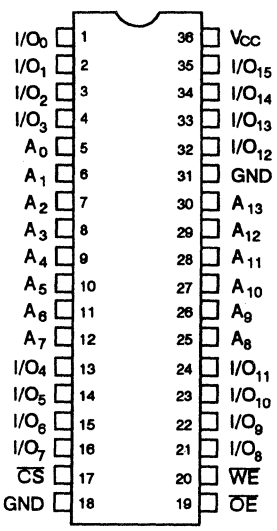
The IDT7MC4005 is a 16-bit wide 256K (16K x 16) static RAM module constructed on a co-fired ceramic substrate using four IDT7198 16K x 4 static RAMs in leadless chip carriers. Extremely fast speeds can be achieved due to the use of 64K static RAMs fabricated in IDT's high-performance, high-reliability CEMOS technology. The IDT7MC4005 is available with access times as fast as 20ns, with minimal power consumption.

The IDT7MC family of ceramic DSIPs offers the optimum in packing density and profile height. The IDT7MC4005 is packaged in a 36-pin ceramic DSIP (dual single-in-line package). The dual row configuration allows 36 pins to be placed on a package 1.8 inches long and .27 inches wide. At only .500 inches high, this low profile package is ideal for systems with minimum board spacing. Extremely high packing density can also be achieved, allowing four IDT7MC4005 modules to be stacked per 1.2 inches of board space.

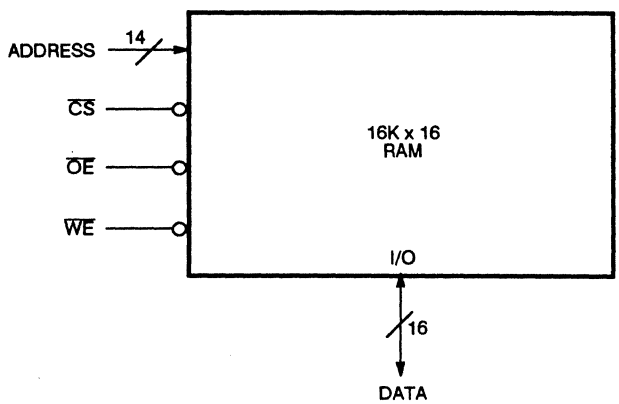
All inputs and outputs of the IDT7MC4005 are TTL-compatible and operate from a single 5V supply. Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation, and providing equal access and cycle times for ease of use.

All IDT military module semiconductor components are manufactured in compliance to the latest revision of MIL-STD-883, Class B, making them ideally suited to applications demanding the highest level of performance and reliability.

PIN CONFIGURATION



FUNCTIONAL BLOCK DIAGRAM



PIN NAMES

I/O_{0-15}	Data Inputs/Outputs
A_{0-13}	Addresses
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
V_{CC}	Power
GND	Ground

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512K(16Kx32) CMOS STATIC RAM DUAL CERAMIC SIP MODULE

IDT7MC4032

FEATURES:

- High-density 32-bit word 512K (16K x 32) static RAM module
- Available in low profile 88-pin sidebraze dual ceramic SIP (dual single in-line package)
- Separate I/O
- Fast access time: 20ns (max.)
- Surface mounted LCC components mounted on a co-fired ceramic substrate
- High impedance outputs during write mode
- CEMOS™ process virtually eliminates alpha particle soft error rates (with no organic die coating)
- Single 5V (±10%) power supply
- Inputs/outputs directly TTL-compatible
- Multiple GND pins for maximum noise immunity

DESCRIPTION:

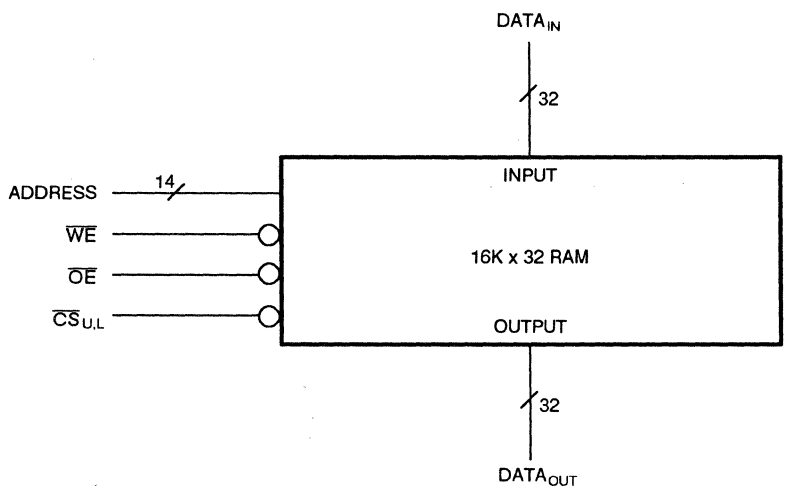
The IDT7MC4032 is a 32-bit wide 512K (16K x 32) static RAM module with separate I/O constructed on a co-fired ceramic substrate using eight IDT71982 16K x 4 static RAMs in leadless chip carriers. Extremely fast speeds can be achieved due to the use of 64K static RAMs fabricated in IDT's high-performance, high-reliability CEMOS™ technology. The IDT7MC4032 is available with access time as fast as 20ns, with minimal power consumption.

The 7MC family of ceramic SIPs offers the optimum is packing density and profile height. The IDT7MC4032 is packaged in a 88-pin dual ceramic SIP. The dual row configuration allows 88 pins to be placed on a package less than 4.5 inches long and .27 inches wide. At only 520 mils high, this low profile package is ideal for systems with minimum board spacing. Extremely high packing density can also be achieved allowing four IDT7MC4032 modules to be stacked per inch of board space.

All inputs and outputs of the IDT7MC4032 are TTL-compatible and operate from a single 5V supply. Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation, and providing equal access and cycle times for ease of use.

All IDT military module semiconductor components are manufactured in compliance to the latest revision of MIL-STD-883, Class B, making them ideally suited to applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM



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4 MEGABIT (512K x 8) CMOS STATIC RAM PLASTIC SIP MODULE

IDT7MP4008S

FEATURES:

- High-density 4 megabit (512K x 8) CMOS static RAM module
- Cost-effective plastic surface mounted RAM packages on an epoxy laminate (FR4) substrate
- Available in 36-pin SIP (single in-line package) for maximum space saving
- Fast access times
  - 45ns (max.)
- Low power consumption
  - Dynamic: 2.6W (max.)
  - Full standby: 1.9 (max.)
- CEMOS™ process virtually eliminates alpha particle soft error rates (with no organic die coating)
- Single 5V (±10%) power supply
- Inputs and outputs directly TTL-compatible

DESCRIPTION:

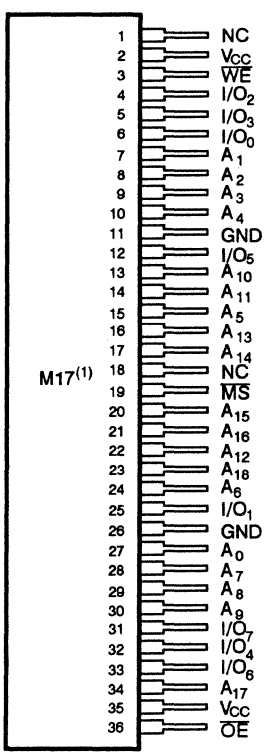
The IDT7MP4008 is a 4 megabit (512K x 8-bit) high-speed static RAM module constructed on an epoxy laminate surface using sixteen IDT71256 32K x 8 static RAMs in plastic surface mount packages. Extremely fast speeds can be achieved with this technique due to the use of 256K static RAMs fabricated in IDT's high-performance, high-reliability CEMOS technology.

The 7MP family of surface mounted SIP technology is a cost-effective solution allowing for very high packing density. The IDT7MP4008 is offered in a 36-pin SIP. The 7MP4008 can be stacked on 300 mil centers, yielding greater than 12 megabits of RAM in less than 5 square inches of board space.

The IDT7MP4008 is available with maximum access times as fast as 45ns with maximum power consumption of 2.6 watts. The IDT7MP4008 also offers a full standby mode of 1.9W (max.).

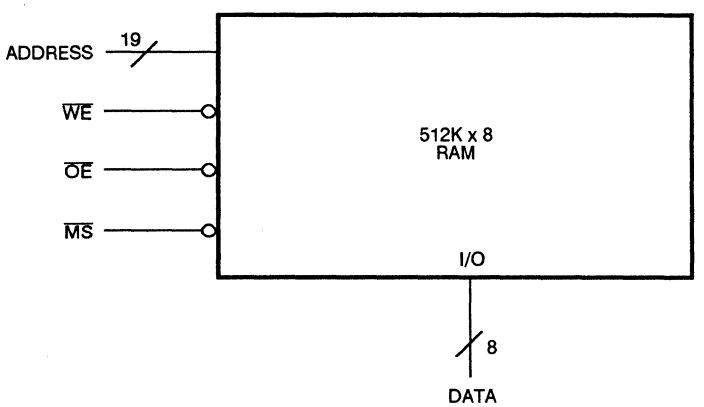
All inputs and outputs of the IDT7MP4008 are TTL-compatible and operate from a single 5V supply. Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation and providing equal access and cycle times for ease of use.

PIN CONFIGURATION



SIP
SIDE VIEW

FUNCTIONAL BLOCK DIAGRAM



PIN NAMES

A_{0-18}	Addresses
I/O_{0-7}	Data Inputs/Outputs
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
$\overline{MS}$	Module Select
V_{CC}	Power
GND	Ground

NOTE:

1. For module dimensions, please refer to module drawing M17 in the packaging section.

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1 MEGABIT (128K x 8-BIT) CMOS STATIC RAM MODULE

IDT8M824S

FEATURES:

- High-density 1024K (128K x 8) CMOS static RAM module
- Equivalent to JEDEC standard for future monolithic 128K x 8 static RAMs
- High-speed
  - Military: 60ns (max.)
  - Commercial: 40ns (max.)
- Low power consumption
  - Active: less than 550mW (typ.)
  - Standby: less than 20mW (typ.)
- CEMOS™ process virtually eliminates alpha particle soft error rates (with no organic die coating)
- Assembled with IDT's high-reliability vapor phase solder reflow process
- Offered in the JEDEC standard 32-pin, 600 mil wide ceramic sidebraze DIP
- Single 5V (±10%) power supply
- Inputs and outputs directly TTL-compatible
- Modules available with semiconductor components compliant to MIL-STD-883, Class B
- Finished modules tested at Room, Hot and Cold temperatures for all AC and DC parameters

DESCRIPTION:

The IDT8M824S is a1024K (131,072 x 8-bit) high-speed static RAM constructed on a co-fired ceramic substrate using four IDT71256 32K x 8 static RAMs in leadless chip carriers. Functional equivalence to proposed monolithic one megabit static RAMs is achieved by utilization of an on-board decoder that interprets the higher order address A_{15} and A_{16} to select one of the four 32K x 8 RAMs. Extremely fast speeds can be achieved with this technique due to use of 256K static RAMs and the decoder fabricated in IDT's high-performance, high-reliability CEMOS technology.

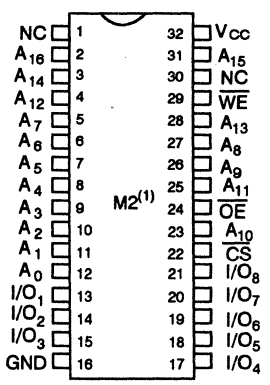
The IDT8M824S is available with maximum access times as fast as 40ns for commercial temperature range, with maximum power consumption of 1.2 watts. The module offers a full standby mode of 440mW (max.).

The IDT8M824S is offered in a 32-pin, 600 mil center sidebraze DIP, adhering to JEDEC standards for one megabit monolithic pinouts, allowing for compatibility with future monolithics.

All inputs and outputs of the IDT8M824S are TTL-compatible and operate from a single 5V supply. Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation, and providing equal access and cycle times for ease of use.

All IDT military module semiconductor components are manufactured in compliance to the latest revision of MIL-STD-883, Class B, making them ideally suited to applications demanding the highest level of performance and reliability.

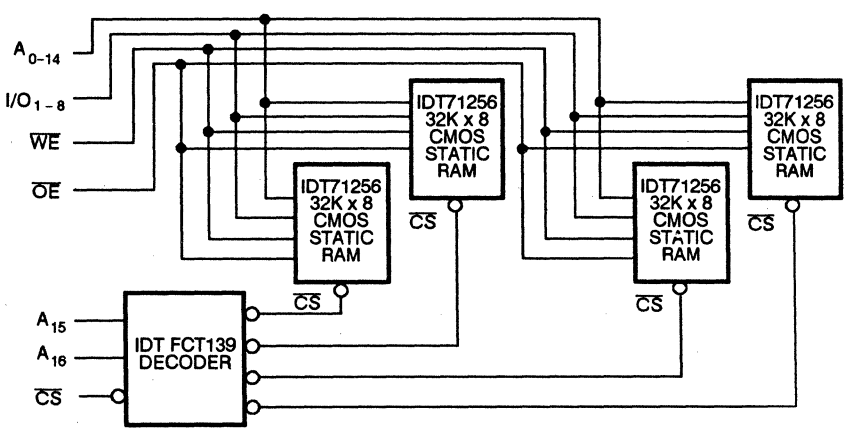
PIN CONFIGURATION



DIP
TOP VIEW

1. For module dimensions, please refer to module drawing M2 in the packaging section.

FUNCTIONAL BLOCK DIAGRAM



PIN NAMES

A_{0-16}	Addresses
I/O_{0-8}	Data Input/Output
$\overline{CS}$	Chip Select
V_{CC}	Power

$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
GND	Ground

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MILITARY AND COMMERCIAL TEMPERATURE RANGES **DECEMBER 1987**

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FAST CMOS COMPATIBLE (FCT) LOGIC SERIES

IDT54/74FCT
IDT54/74FCT/A

FEATURES:

- FCT equivalent to FAST™ speeds and output drive over full temperature and voltage supply extremes
- **"A" Version approximately 35% faster than FAST**
- CMOS power levels (5μW typ. static)
- Both CMOS and TTL output compatible
- Substantially lower input current levels than FAST (5μA max.)
- JEDEC standard pinout for DIP and LCC
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The "FCT" series is a family of industry standard memory interface circuits that are pin compatible, functional equivalent replacements to the Fairchild FAST series, but at CMOS power levels (1/10 operation, 1/100 standby).

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
V_{LC} = 0.2V; V_{HC} = -0.2V
Commercial: T_A = 0°C to +70°C; V_{CC} = 5.0V ±5%
Military: T_A = -55°C to +125°C; V_{CC} = 5.0V ±10%

SYMBOL	PARAMETER	TEST CONDITIONS [1]		MIN.	TYP.[2]	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	–	–	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		–	–	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.,	V_I = V_{CC}	–	–	5	μA
			V_I = 2.7V	–	–	5	
I_{IL}	Input LOW Current		V_I = 0.4V	–	–	-5	
			V_I = GND	–	–	-5	
I_{OZ}	Off State (High Impedance) Output Current	V_{CC} = Max.,	V_O = V_{CC}	–	–	10	μA
			V_O = 2.7V	–	–	10	
			V_O = 0.4V	–	–	-10	
			V_O = GND	–	–	-10	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = -18mA		–	-0.7	-1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.,[3] V_O = GND		-60	-120	–	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32μA		V_{HC}	V_{CC}	–	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -300μA	V_{HC}	V_{CC}	–	
			I_{OH} = -12mA MIL.	2.4	4.3	–	
			I_{OH} = -15mA COM'L.	2.4	4.3	–	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300μA		–	GND	V_{LC}	
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300μA	–	GND	V_{LC}	
			I_{OL} = 32mA MIL.	–	0.3	0.5	
			I_{OL} = 48mA COM'L.	–	0.3	0.5	
V_{OL}	Output LOW Voltage (Buffers and Transceivers)	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300μA		–	GND	V_{LC}	
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300μA	–	GND	V_{LC}	
			I_{OL} = 48mA MIL.	–	0.3	0.55	
			I_{OL} = 64mA COM'L.	–	0.3	0.55	
I_{CCQ}	Quiescent Power Supply Current	V_{CC} = Max. V_{IN} ≥ V_{HC} ; V_{IN} ≤ V_{LC} f_{CP} = f_I = 0		–	0.001	1.5	mA
I_{CCT}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[4]		–	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max. Outputs Open One Bit Toggling 50% Duty Cycle	V_{IN} ≥ V_{HC} V_{IN} ≤ V_{LC}	–	0.15	0.25	mA/ MHz

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.

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HIGH-PERFORMANCE SYSTEMS SOLUTIONS

Integrated Device Technology

	16	18	20	22	24	28	32	40	44	48	52	64	68	84	108	144	172	208
THROUGH HOLE TECHNOLOGY																		
Plastic DIP (300 mil)	●	●	●	●	●	●												
Plastic DIP (600 mil)					●	●	●	●		●								
Plastic DIP (900 mil)												●						
CERDIP (300 mil)	●	●	●	●	●	●												
CERDIP (600 mil)					●	●		●										
Sidebraze DIP (300 mil)			●	●	●	●												
Sidebraze DIP (400 mil)						●												
Sidebraze DIP (400 mil Fine Pitch)										●								
Sidebraze DIP (600 mil)					●	●	●	●		●								
Sidebraze DIP (600 mil Fine Pitch)													●					
Sidebraze DIP (900 mil)												●						
Topbraze DIP (900 mil)												●						
Pin Grid Array (Cavity Up)													●		●	●		●
Pin Grid Array (Cavity Down)													●	●		●		
SURFACE MOUNT TECHNOLOGY																		
Plastic Small Outline (SOIC)	●	●	●		●	●												
Leadless Chip Carrier (Sq.)			●			●			●	●	●		●					
Leadless Chip Carrier (Rect.)			●	●	●	●	●											
Leadless Chip Carrier (Fine Pitch)										●			●					
Plastic Leaded Chip Carrier (Sq.)			●			●			●		●	●	●	●				
Plastic Leaded Chip Carrier (Rect.)				●			●											
CERPACK	●		●		●	●												
Flatpack			●		●	●				●		●					●	
Ceramic Quad Flatpack										●			●	●				
Plastic Quad Flatpack															●			
Plastic Pin Grid Array (Cavity Up)													●	●				●
Plastic Pin Grid Array (Cavity Dwn)													●	●				

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INTERNATIONAL CMOS
TECHNOLOGY, INC.

High-Speed CMOS UV-Erasable PROMs

Features

- **Advanced CMOS EPROM Technology**
- **High Performance**
- **Low Power Consumption**
- **TTL-Compatible I/O**
- **Reprogrammability**
  - — Adds convenience, reduces costs
  - — Windowed package for UV erasure
  - — Allows 100% factory testing
- **Bipolar PROM replacement**
  - — Pin-compatible with Bipolar PROMs
  - — Higher speed
  - — Lower power consumption
  - — 300-mil and 600-mil packages

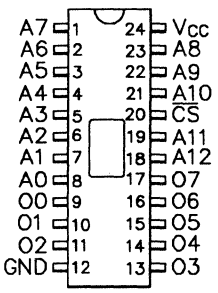
General Description

ICT's CMOS high-speed UV-erasable PROMs provide a low-power reprogrammable alternative to bipolar fuse-link PROMs. Available in both 600mil (27CX641/321) and 300mil (27CX642/322) packages, these devices are pin/socket-compatible with many popular bipolar PROMs.

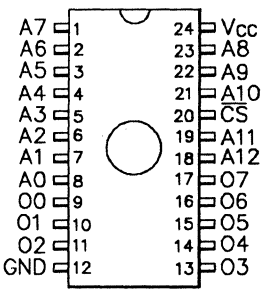
These memories are designed in an advanced CMOS EPROM technology and use differential memory cell techniques to provide access times comparable to high-speed bipolar PROMs (as fast as 35ns) with a significant improvement in power consumption. Reprogrammability not only adds convenience and reduces development and field retrofit costs, but enhances factory testability, allowing for 100% field programmability and function.

Pin Configurations

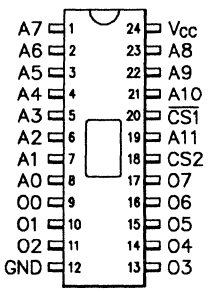
27CX642 (300mil)



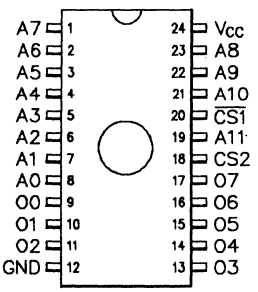
27CX641 (600mil)



27CX322 (300mil)



27CX321 (600mil)



ICT High-Speed Erasable PROM Selection Guide

Device	Pins	Package	Organization	Speed	Power Consumption
27CX321-35	24	600 mil	4k X 8	35ns	40mA max, 500µA typ. standby
27CX321-40	24	600 mil	4k X 8	40ns	40mA max, 500µA typ. standby
27CX321-45	24	600 mil	4k X 8	45ns	40mA max, 500µA typ. standby
27CX322-35	24	300 mil	4k X 8	35ns	40mA max, 500µA typ. standby
27CX322-40	24	300 mil	4k X 8	40ns	40mA max, 500µA typ. standby
27CX322-45	24	300 mil	4k X 8	45ns	40mA max, 500µA typ. standby
27CX641-40	24	600 mil	8k X 8	40ns	60mA max
27CX641-45	24	600 mil	8k X 8	45ns	60mA max
27CX641-55	24	600 mil	8k X 8	55ns	60mA max
27CX642-40	24	300 mil	8k X 8	40ns	60mA max
27CX642-45	24	300 mil	8k X 8	45ns	60mA max
27CX642-55	24	300 mil	8k X 8	55ns	60mA max

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INTERNATIONAL CMOS
TECHNOLOGY, INC.

93C46
1,024-Bit Serial (5V only) CMOS Electrically Erasable Programmable Read Only Memory (EEPROM)

Features

- **Advanced CMOS EEPROM Technology**
- **Read/Write Non-volatile Memory**
  - 5V supply operation
  - Low-voltage operation version available
  - 1,024 bits, 64 x 16 organization
  - Versatile, easy to use serial data interface
- **Low Power Consumption**
  - 3mA max Active
  - 1mA max Standby, TTL interface
  - 100µA max Standby, CMOS interface
- **Special Features**
  - Automatic write cycle time-out
  - Ready/Busy status signal
  - Software controlled write protection
- **Ideal For Low-Density Data Storage**
  - Low cost, space saving, 8-pin package
  - Commercial, industrial, & military versions
  - Interfaces with popular microcomputers (ie., COP4XX, 8048, 8049, 8051, 8096, 6805, 6801, TMS1000, Z8)
- **Application Versatility**
  - Alarms, Electronic Locks, Appliances, Terminals, Smart Cards, Robotics, Meters, Telephones, Tuners, etc.
- **Superset Compatibility**
  - National: NMC9306/COP494, NMC9346/COP495
  - General Instruments: ER59256, ER5911
  - NCR: 59306, 59308

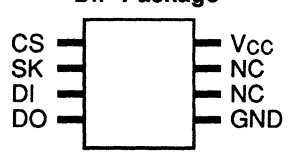
General Description

The ICT 93C46 is a 1024-bit, 5V-only, serial read/write, non-volatile memory device fabricated using an advanced CMOS EEPROM technology. Its 1024 bits of memory are organized into 64 registers each. Each register is individually addressable for serial read or write operations. A versatile serial interface consisting of chip select, clock, data-in and data-out, can easily be controlled by popular microcontrollers (ie., COP4XX, 8048, 8049, 8051, 6805, 6801, TMS1000,Z8) or standard microprocessors.

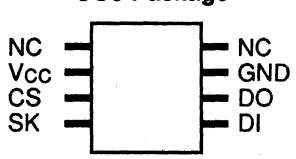
Low power consumption, low cost, and space efficiency make the ICT 93C46 an ideal candidate for high volume, low density data storage applications. Special features of the 93C46 include: automatic write time-out, ready/busy status signal, software controlled write protection, and ultra-low standby power mode when deselected (CS low). Additionally the 93C46 offers functional compatibility with existing NMOS serial EEPROMs. The 93C46 is designed for applications requiring up to 10,000 erase/write cycles per register.

Connection Diagrams

DIP Package

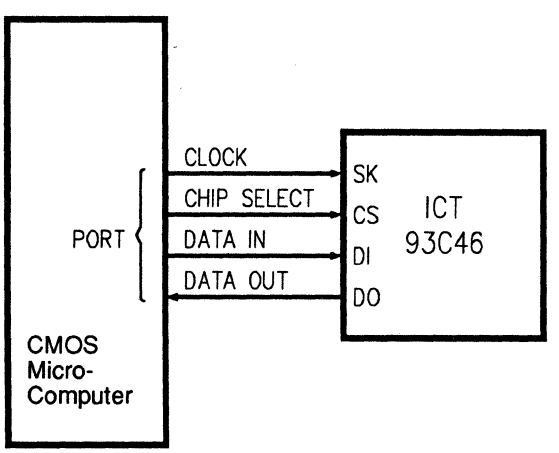


SO8 Package



Pin Names

CS	= Chip Select
SK	= Serial Data Clock
DI	= Serial Data Input
DO	= Serial Data Output
GND	= Ground
Vcc	= Power Supply
NC	= Not Connected



Interfacing the 93C46 to a microcomputer

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International CMOS Technology

The Krueger Company

2219 SOUTH 48TH STREET
TEMPE, ARIZONA 85282

(602) 438-1570 • (800) 245-2235
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TELEX 165251 KRUEGER UD

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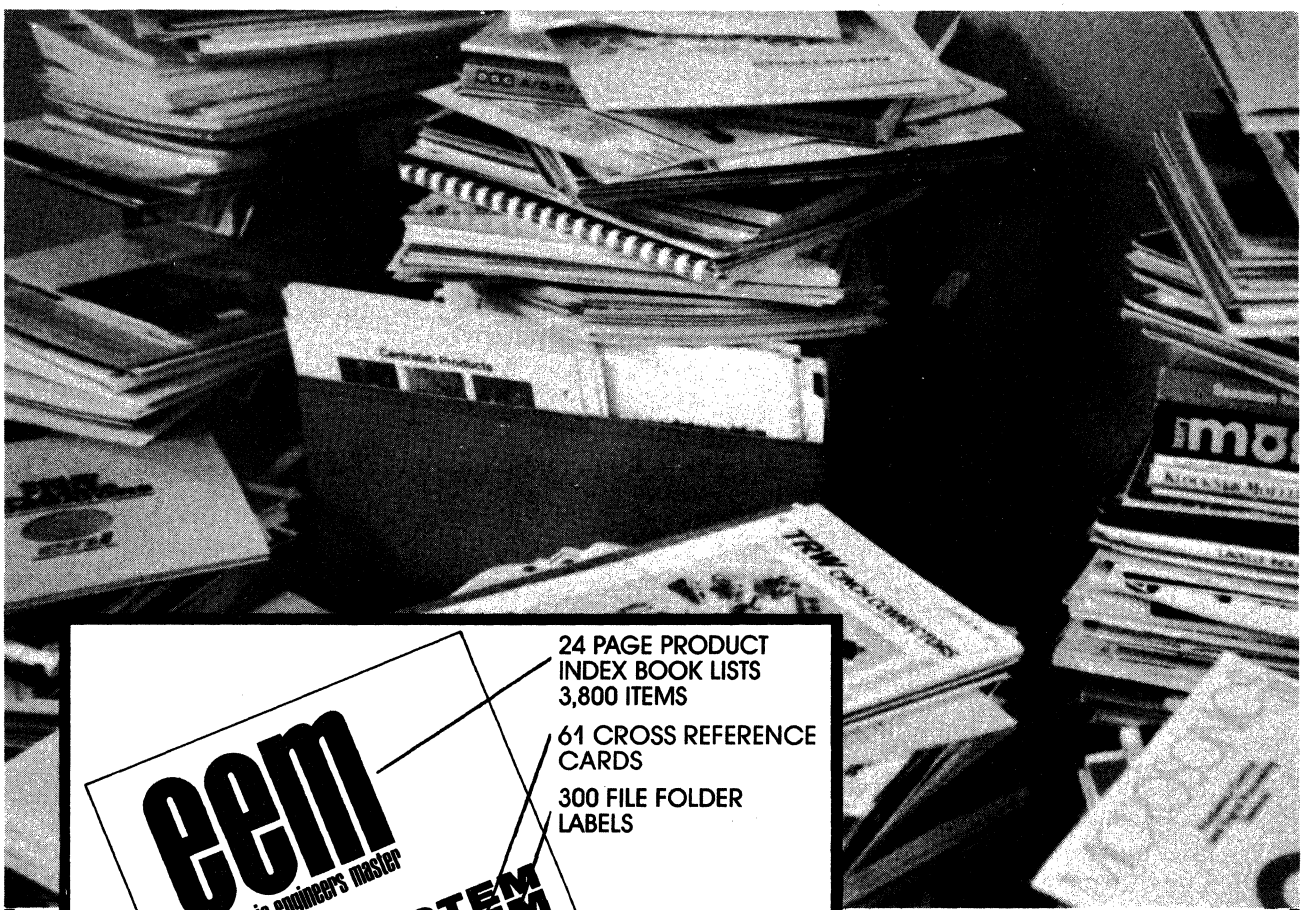
The KRUEGER COMPANY has provided the electronics industry with the benefits of the KRUEGER process in the form of high quality refurbished ICs in two ways.

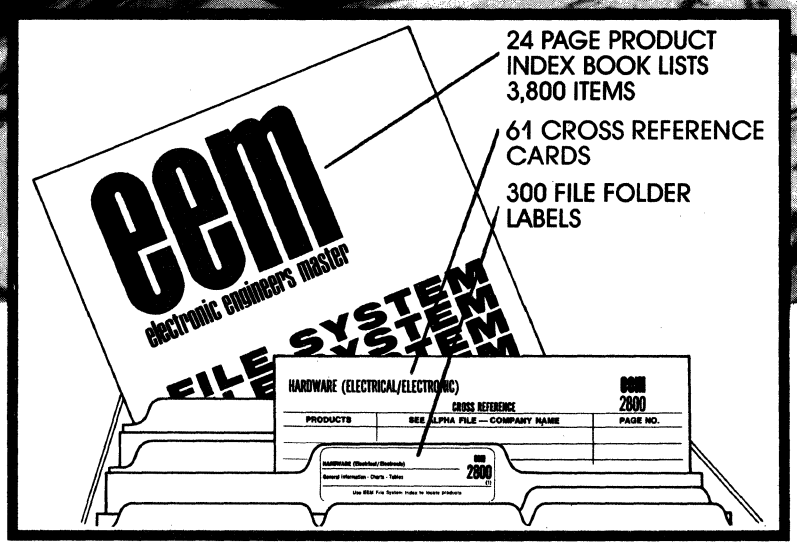
1. The KRUEGER COMPANY offers a component retrieval service which enables the IC user to recover and reuse any IC or other component on existing PC boards. The KRUEGER COMPANY retrieval service offers the electronics industry a way to obtain needed parts at a small fraction of their cost and lead time while helping gain maximum value from obsolete boards.
2. The KRUEGER COMPANY also obtains boards from which parts are retrieved, refurbished and made available to IC purchasers worldwide. The KRUEGER COMPANY maintains an inventory of refurbished ICs and may well be able to supply your immediate needs for any category of IC.

Krueger Company

The list below is a typical example of parts commonly available from KRUEGER COMPANY.

Dynamic RAMs	Static RAMs		EPROMs	Processors/other	
511000	62256		27010	68020	8088
514256	6264		27512	68010	8087
41256	6116		27256	68000	8086
41264 VIDEO	2128		27128	68564	8085
4464	Above in DIP, FP or		68766	68901	8080
4164	skinny DIP package		2764	68881	Z80
4416	6167	2147	2564	80286	146818
4161 VIDEO	6168	2148	2732	80186	48C02
4116	2186	2149	2532	80287	16450
2118	6288	2114	2716	80586	8250





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PHOENIX, AZ 85019

AVAILABLE PARTS

LANSDALE PART MARKINGS

XX XXXX XX

- XX — ORIGINAL MFG — LANSDALE
- XXXX — DEVICE
- XX — LEVEL OF PROCESSING / PACKAGING

LANSDALE ORDERING INFO

AM{XXXX} - AMD	AL{XXXX} - LANSDALE EQUIVALENT
MC{XXXX} - MOTOROLA	ML{XXXX} - LANSDALE EQUIVALENT
HPROM{XXXX} - HARRIS	HL{XXXX} - LANSDALE EQUIVALENT
RM{XXXX} - RAYTHEON	RL{XXXX} - LANSDALE EQUIVALENT
SE{XXXX} - SIGNETICS	SL{XXXX} - LANSDALE EQUIVALENT
S{XXXX} - SIGNETICS	SL{XXXX} - LANSDALE EQUIVALENT

AMD

AMD P/N	Lansdale Direct Replacement
AM 2506	AL2506
AM2905	AL2905

HARRIS

Harris P/N	Lansdale Direct Replacement
HPROM-0512	HL0512
HDI234WB	HLI234
HD245WB	HL245
HD246WB	HL246
HD248WB	HL248

MOTOROLA

MTTL I Motorola P/N	Lansdale Direct Replacement
MC400	ML400
MC401	ML401
MC402	ML402
MC403	ML403
MC404	ML404
MC405	ML405
MC406	ML406
MC407	ML407
MC408	ML408
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MTTL II	
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MC2003	ML2003
MC2004	ML2004
MC2005	ML2005
MC2006	ML2006
MC2007	ML2007
MC2011	ML2011
MC2012	ML2012
MC2013	ML2013
MC2016	ML2016

Motorola P/N	Lansdale Direct Replacement
MC2023	ML2023
MC2024	ML2024
MC2025	ML2025
MC2026	ML2026
MC2028	ML2028
MC2050	ML2050
MC2051	ML2051
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MC2066	ML2066
MC2073	ML2073
MC2074	ML2074
MC2075	ML2075
MC2076	ML2076
MC2078	ML2078
MC2100	ML2100
MC2101	ML2101
MC2102	ML2102
MC2103	ML2103
MC2104	ML2104
MC2105	ML2105
MC2106	ML2106
MC2107	ML2107
MC2111	ML2111
MC2112	ML2112
MC2113	ML2113
MC2116	ML2116
MC2123	ML2123
MC2124	ML2124
MC2125	ML2125
MC2126	ML2126
MC2128	ML2128
MC2150	ML2150
MC2151	ML2151
MC2152	ML2152
MC2153	ML2153
MC2154	ML2154
MC2155	ML2155
MC2156	ML2156
MC2157	ML2157
MC2161	ML2161
MC2162	ML2162
MC2163	ML2163
MC2165	ML2165
MC2166	ML2166
MC2173	ML2173
MC2174	ML2174
MC2175	ML2175
MC2176	ML2176
MC2178	ML2178
MTTL III	
MC3000	ML3000
MC3001	ML3001
MC3002	ML3002
MC3003	ML3003
MC3004	ML3004
MC3005	ML3005
MC3006	ML3006
MC3007	ML3007
MC3008	ML3008
MC3009	ML3009
MC3010	ML3010
MC3011	ML3011
MC3012	ML3012
MC3015	ML3015
MC3016	ML3016
MC3020	ML3020
MC3021	ML3021
MC3022	ML3022
MC3023	ML3023
MC3024	ML3024
MC3025	ML3025
MC3026	ML3026
MC3028	ML3028
MC3029	ML3029
MC3031	ML3031
MC3032	ML3032
MC3051	ML3051
MC3052	ML3052
MC3060	ML3060
MC3061	ML3061
MC3062	ML3062
MC3100	ML3100
MC3101	ML3101
MC3102	ML3102
MC3103	ML3103
MC3104	ML3104
MC3105	ML3105
MC3106	ML3106
MC3107	ML3107
MC3108	ML3108
MC3109	ML3109
MC3110	ML3110
MC3111	ML3111
MC3112	ML3112
MC3115	ML3115
MC3116	ML3116
MC3120	ML3120
MC3121	ML3121
MC3122	ML3122
MC3123	ML3123
MC3124	ML3124
MC3125	ML3125
MC3126	ML3126
MC3128	ML3128
MC3129	ML3129
MC3131	ML3131
MC3132	ML3132
MC3151	ML3151
MC3152	ML3152
MC3160	ML3160
MC3161	ML3161
MC3162	ML3162
MTTL 54/7400 SERIES	
MC54/7400	ML54/7400
MC54/7401	ML54/7401
MC54/7402	ML54/7402
MC54/7403	ML54/7403
MC54/7404	ML54/7404
MC54/7405	ML54/7405
MC54/7406	ML54/7406
MC54/7407	ML54/7407
MC54/7408	ML54/7408
MC54/7409	ML54/7409
MC54/7410	ML54/7410
MC54/7413	ML54/7413
MC54/7414	ML54/7414
MC54/7416	ML54/7416
MC54/7417	ML54/7417
MC54/7420	ML54/7420
MC54/7423	ML54/7423
MC54/7425	ML54/7425
MC54/7426	ML54/7426
MC54/7427	ML54/7427
MC54/7430	ML54/7430
MC54/7437	ML54/7437
MC54/7438	ML54/7438
MC54/7440	ML54/7440
MC54/7442	ML54/7442
MC54/7443	ML54/7443
MC54/7444	ML54/7444
MC54/7450	ML54/7450
MC54/7451	ML54/7451
MC54/7453	ML54/7453
MC54/7454	ML54/7454
MC54/7470	ML54/7470
MC54/7472	ML54/7472
MC54/7473	ML54/7473
MC54/7474	ML54/7474
MC54/7475	ML54/7475
MC54/7476	ML54/7476
MC54/7477	ML54/7477
MC54/7479	ML54/7479
MC54/7480	ML54/7480
MC54/7482	ML54/7482
MC54/7483	ML54/7483
MC54/7485	ML54/7485
MC54/7486	ML54/7486
MC54/7490A	ML54/7490A
MC54/7491A	ML54/7491A
MC54/7492A	ML54/7492A
MC54/7493A	ML54/7493A
MC54/7494	ML54/7494
MC54/7495A	ML54/7495A
MC54/7496	ML54/7496
MC54/7497	ML54/7497
MC54/74100	ML54/74100
MC54/74107	ML54/74107
MC54/74120	ML54/74120
MC54/74121	ML54/74121
MC54/74122	ML54/74122
MC54/74123	ML54/74123
MC54/74132	ML54/74132
MC54/74136	ML54/74136
MC54/74146	ML54/74146
MC54/74150	ML54/74150
MC54/74151	ML54/74151
MC54/74152	ML54/74152
MC54/74153	ML54/74153
MC54/74154	ML54/74154
MC54/74155	ML54/74155
MC54/74160	ML54/74160
MC54/74161	ML54/74161
MC54/74162	ML54/74162
MC54/74163	ML54/74163
MC54/74165	ML54/74165
MC54/74167	ML54/74167
MC54/74174	ML54/74174
MC54/74175	ML54/74175
MC54/74176	ML54/74176
MC54/74177	ML54/74177
MC54/74180	ML54/74180
MC54/74181	ML54/74181

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Motorola P/N	Lansdale Direct Replacement
MC54/74182	ML54/74182
MC54/74190	ML54/74190
MC54/74191	ML54/74191
MC54/74192	ML54/74192
MC54/74193	ML54/74193
MC54/74194	ML54/74194
MC54/74195	ML54/74195
MC54/74196	ML54/74196
MC54/74197	ML54/74197
MC54/74290	ML54/74290
MC54/74293	ML54/74293
MC54/74298	ML54/74298
MTTL-SUHL II	
MC5090	ML5090
MC5092	ML5092
MC5111	ML5111
MC5113	ML5113
MC5121	ML5121
MC5123	ML5123
MC5131	ML5131
MC5133	ML5133
MC5141	ML5141
MC5143	ML5143
MC5151	ML5151
MC5153	ML5153
MC5161	ML5161
MC5163	ML5163
MC5171	ML5171
MC5173	ML5173
MC5181	ML5181
MC5183	ML5183
MC5191	ML5191
MC5193	ML5193

RAYTHEON

DTL

Raytheon P/N	Lansdale Direct Replacement
RM201	RL201
RM202	RL202
RM204	RL204
RM206	RL206
RM208	RL208
RM210	RL210
RM211	RL211
RM212	RL212
RM213	RL213
RM214	RL214
RM215	RL215
RM216	RL216
RM217	RL217
RM220	RL220
RM224	RL224
RM225	RL225
RM226	RL226
RM227	RL227
RM231	RL231
RM234	RL234
RM236	RL236
RM241	RL241
RM246	RL246
RM261	RL261
RM266	RL266

Raytheon P/N	Lansdale Direct Replacement
RM286	RL286
RM288	RL288
RM296	RL296
RC8200	RL8200
RC8201	RL8201
RC8202	RL8202
RC8203	RL8203
RC8230	RL8230
RC8231	RL8231
RC8232	RL8232
RC8233	RL8233
RC8234	RL8234
RC8241	RL8241
RC8243	RL8243
RC8251	RL8251
RC8252	RL8252
RC8261	RL8261
RC8263	RL8263
RC8264	RL8264
RC8267	RL8267
RC8270	RL8270
RC8271	RL8271
RC8273	RL8273
RC8274	RL8274
RC8275	RL8275
RC8277	RL8277
RC8280	RL8280
RC8285	RL8285
RC8290	RL8290
RC8291	RL8291
RC8293	RL8293
RC8T20	RL8T20
RF100	ML523
RF101	ML573
RF110	ML524
RF111	ML574
RF120	ML2123
RF121	ML2173
RF130	ML2124
RF131	ML2174
RF200	ML2125
RF210	ML2175
RF211	ML2126
RF250	ML2109
RF251	ML2159
RF260	ML2110
RF261	ML2160
RF30	ML521
RF31	ML571
RF50	ML515
RF51	ML565
RF60	ML516
RF61	ML566
RG110	ML505
RG111	ML555
RG120	ML506
RG121	ML556
RG130	ML507
RG131	ML557
RG140	ML508
RG141	ML558
RG150	ML509
RG151	ML599
RG160	ML519
RG161	ML569
RG170	ML510
RG171	ML560

Raytheon P/N	Lansdale Direct Replacement
RG180	ML511
RG181	ML561
RG190	ML512
RG191	ML562
RG200	ML2111
RG201	ML2161
RG210	ML2100
RG211	ML2150
RG220	ML2101
RG221	ML2151
RG230	ML2102
RG231	ML2152
RG240	ML2103
RG241	ML2153
RG250	ML2104
RG251	ML2154
RG260	ML2105
RG261	ML2155
RG270	ML2106
RG271	ML2156
RG280	ML527
RG281	ML577
RG290	ML528
RG291	ML578
RG300	ML2112
RG301	ML2162
RG310	ML2113
RG311	ML2163
RG320	ML2107
RG321	ML2157
RG370	ML529
RG371	ML2166
RG380	ML2116
RG40	ML500
RG41	ML550
RG50	ML501
RG51	ML551
RG60	ML502
RG61	ML552
RG70	ML520
RG71	ML570
RG80	ML526
RG81	ML576
RG90	ML503
RG91	ML553

SIGNETICS

DTL

Signetics P/N	Lansdale Direct Replacement
SE101	SL101
SE102	SL102
SE105	SL105
SE106	SL106
SE110	SL110
SE111	SL111
SE112	SL112
SE113	SL113
SE115	SL115
SE116	SL116
SE124	SL124
SE125	SL125

Signetics P/N	Lansdale Direct Replacement
SE150	SL150
SE155	SL155
SE156	SL156
SE157	SL157
SE160	SL160
SE161	SL161
SE162	SL162
SE170	SL170
SE180	SL180
SE181	SL181
SE415	SL415
SE416	SL416
SE417	SL417
SE424	SL424
SE425	SL425
SE440	SL440
SE455	SL455
SE470	SL470
SE471	SL471
SE480	SL480
SE481	SL481
SE490	SL490
SE511	SL511
SE526	SL526
SE616	SL616
SE620	SL620
SE629	SL629
SE631	SL631
SE659	SL659
SE670	SL670
SE680	SL680
SE690	SL690
SE700	SL700
SE701	SL701
SE704	SL704
SE716	SL716
SE720	SL720
SE721	SL721
SE727	SL727
SE730	SL730
SE731	SL731
SE732	SL732
S8415	SL8415
S8416	SL8416
S8417	SL8417
S8424	SL8424
S8425	SL8425
S8440	SL8440
S8455	SL8455
S8470	SL8470
S8471	SL8471
S8480	SL8480
S8481	SL8481
S8490	SL8490
UTiLOGIC II	
SE300	SL300
SE301	SL301
SE302	SL302
SE304	SL304
SE305	SL305
SE306	SL306
SE314	SL314
SE315	SL315
SE316	SL316
SE317	SL317
SE320	SL320

Signetics P/N	Lansdale Direct Replacement
SE321	SL321
SE322	SL322
SE328	SL328
SE331	SL331
SE332	SL332
SE333	SL333
SE334	SL334
SE337	SL337
SE352	SL352
SE356	SL356
SE357	SL357
SE358	SL358
SE362	SL362
SE363	SL363
SE370	SL370
SE374	SL374
SE375	SL375
SE377	SL377
SE380	SL380
SE381	SL381
SE384	SL384
SE387	SL387
SE391	SL391
S3271	SL3271
S3281	SL3281
TTL - Interface	
S8T04	SL8T04
S8T05	SL8T05
S8T06	SL8T06
S8T14	SL8T14
S8T15	SL8T15
S8T16	SL8T16
S8T18	SL8T18
S8T20	SL8T20
S8T26	SL8T26
S8T31	SL8T31
S8T32	SL8T32
S8T33	SL8T33
S8T35	SL8T35
S8T36	SL8T36
S8T80	SL8T80
S8T90	SL8T90
S8T96	SL8T96
S8162	SL8162
S8200	SL8200
S8201	SL8201
S8202	SL8202
S8203	SL8203
S8221	SL8221
S8224	SL8224
S8230	SL8230
S8231	SL8231
S8232	SL8232
S8233	SL8233
S8234	SL8234
S8235	SL8235
S8241	SL8241
S8242	SL8242
S8243	SL8243
S8250	SL8250
S8251	SL8251
S8252	SL8252
S8260	SL8260
S8261	SL8261
S8263	SL8263
S8264	SL8264

Signetics P/N	Lansdale Direct Replacement
S8266	SL8266
S8267	SL8267
S8269	SL8269
S8270	SL8270
S8273	SL8273
S8274	SL8274
S8275	SL8275
S8277	SL8277
S8280	SL8280
S8281	SL8281
S8284	SL8284
S8285	SL8285
S8288	SL8288
S8290	SL8290
S8291	SL8291
S8292	SL8292
S8293	SL8293
S8806	SL8806
S8808	SL8808
S8815	SL8815
S8816	SL8816
S8821	SL8821
S8822	SL8822
S8824	SL8824
S8825	SL8825
S8827	SL8827
S8829	SL8829
S8848	SL8848
S8855	SL8855
S8870	SL8870
S8875	SL8875
S8880	SL8880
S8881	SL8881
S8885	SL8885
S54H00	SL54H00
S54H01	SL54H01
S54H08	SL54H08
S54H10	SL54H10
S54H11	SL54H11
S54H20	SL54H20
S54H30	SL54H30
S54H40	SL54H40
S54H52	SL54H52
S54H53	SL54H53
S54H54	SL54H54
S54H60	SL54H60
S54H71	SL54H71
S54H72	SL54H72
S54H73	SL54H73
S54H74	SL54H74
S54H76	SL54H76
S54H103	SL54H103
S5401	SL5401
S5402	SL5402
S5409	SL5409
S5447	SL5447
S5448	SL5448
S5453	SL5453
S5460	SL5460
S5470	SL5470
S5472	SL5472
S5480	SL5480
S54100	SL54100
S54152	SL54152
S54182	SL54182
S54198	SL54198

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MEET THE HARDEST WORKING CHIPS IN THE BUSINESS

LSI COMPUTER SYSTEMS INC. Manufacturers of Custom and Standard LSI Circuits

PROGRAMMABLE INTEGRATED CONTROLLER/SEQUENCER

Microprocessor designed for applications requiring simple decision-making, not computation.

LS7270: Performs logical sequencing, timing, and controlling functions. Far more easily programmed than any other μP, and program can be stored in any standard ROM, PROM, EPROM, or RAM. Low-cost, reliable replacement for hard-wired controls and relay networks. 40-pin DIP.

DIGITAL LOCK CIRCUITS

For automotive/marine anti-theft.

LS7220: 5,040 4-digit combinations; out-of-sequence detection logic; 25μA standby. "Save" mode for valet parking settable in "Unlock"; built-in convenience delay hard wired programming. 14-pin DIP.

Keyboard Programmable Keyless Locks.

LS7222-LS7223: Stand alone lock logic with 38416, 4 digit codes: 3 different user programmable codes; momentary static lock control outputs; tamper detection output; high noise immunity. 20-pin DIP.

For area access and machine access.

LS7225-LS7226: 5,040 4-digit combinations; toggle output (set and reset with application of code); momentary output; tamper output. 14-pin DIP.

For serial address decoding or 2-pushbutton keyless locks.

LS7228-LS7229: Address decoder/digital lock; code programmable through 9 parallel pins; serial decoding input can be applied through dual pulse train or two pushbuttons; pulse output; duration between entries capacitor programmable; cascadable; hard wired programming. 16-pin DIP.

BRUSHLESS DC MOTOR SPEED CONTROLLERS

LS 7260-LS7261/62: 3 or 4-phase commutator chips; overcurrent sensing; brake; reverse. 20-pin DIP.
LS7263: Crystal controlled 3-phase motor speed controller; for fixed speed applications; accuracy 0.1%. 18-pin DIP.
LS7264: Crystal controlled 4-phase motor speed controller; for fixed speed applications; accuracy 0.1%. 16-pin DIP.

PROGRAMMABLE DIGITAL DELAY TIMER

For delaying the starting or stopping of an operation.

LS7210: Can generate delays of ms to infinity, or add auto reset to μP system; programmed by 5 binary weighted input bits plus on chip oscillator or external clock. Operable in 4 modes; delayed operate or release, dual delay, or one-shot. All inputs CMOS, MOS, and TTL compatible. 14-pin DIP.

TOUCH SENSITIVE LAMP DIMMER/AC MOTOR SPEED CONTROLLER

Circuits digitally determine firing angle of a triac. Phase locked loop synchronization makes triac output "Pure AC", allowing triac to drive motor or transformer windings directly.

LS7231-35: Momentary touch turns triac off, if on: if off, momentary touch turns triac to maximum or to firing angle stored in MEMORY (depending on circuit). Prolonged touch causes firing angle to vary. 8 pin mini-DIP.
LS7237: A touch causes firing angle to advance to next state in sequence. Three state input pin ("1", "0", or "open") selects one of 3 modes of firing angle sequence: MAX/OFF; LOW/MED/MAX/OFF; MIN/LOW/MED/MAX/OFF. Pin compatible with LS7231-LS7235. 8 pin mini-DIP.
LS7310-LS7315: Ten level Power control with on, off and momentary control, touch or switch causes Triac firing angle to change to preprogrammed levels for AC motors and brightness control of incandescent lamps.
LS7331-LS7332: Momentary touch turns triac on or off; prolonged touch causes firing angle to vary. Allows computer control of triac firing with outputs to computer when lamp is at full brightness, varying in brightness or when power loss has occurred.

DISPLAY DRIVERS

For liquid crystal displays requiring up to 60V.

LS7100: BCD to 7 segment latch/decoder/driver.
LS7110: Binary addressable latched 8-channel demultiplexer/driver. Both are ion-implanted P Channel MOS circuits, compatible with CMOS and TTL systems. 16-pin DIPS.

CMOS DIVIDERS

For generating time bases from 50/60 Hz input. All feature input shaping network; resettable; division select input 50/60 Hz; clock enable input; 8-pin mini-DIP.
RED 5/6: 10 pulses/sec.
RED 50/60: 1 pulse/sec.
RED 100/120: 1 pulse/2 seconds.
RED 300/360: 1 pulse/0.1 minute.
RED 500/600: 1 pulse/10 seconds.
RED 3000/3600: 1 pulse/minute.

For generating decade-related time bases.

RDD104: Addressable divider; divides by 10, 100, 1000, or 10,000. Input may be controlled by crystal or external frequency source. 8-pin mini-DIP.

TONE ACTIVATED, TELEPHONE LINE ISOLATION DEVICE

LS7501-LS7510: Frequency discriminator circuits which can disconnect or switch a telephone line upon detection of a specific frequency tone. 10 standard frequency circuit versions. Telephone line checking or automatic meter reading applications.

COUNTERS

LS7066: 24-bit multimode counter. Programmable by microprocessor, via three-state I/O bus, to operate in the following modes: binary, BCD, 24-hour clock, up, down, ÷n, quadrature, and single cycle. Modes can co-exist in different combinations. DC to 5 MHz in all modes. Includes 24-bit comparator for pre-set count comparison; readable status register. Input/output TTL compatible. 20-pin plastic DIP.
LS7060: DC to 10 MHz 32-bit binary up counter with 32-bit latch and multiplexer; 8-bit three-state multiplexed outputs; input/output TTL compatible; bus compatible. 18-pin DIP.
LS7062: Identical except that it is a dual 16-bit counter, with two inputs.
LS7061: DC to 10 MHz 32-bit binary up counter with 40-bit latch and multiplexer; access to 8 LSB latches allows attachment of prescalers for counting to 2.56 GHz; 8-bit three-state multiplexed outputs; input/output TTL compatible; bus compatible. 24-pin DIP.
LS7063: Identical, except that it is a dual 16-bit counter, with two inputs.
LS7030: DC to 5 MHz eight decade up counter with 8-decade latch and multiplexer, multiplexed BCD and 7 segment outputs; inputs CMOS and TTL compatible; outputs CMOS compatible; counter output latches; leading zero blanking. 40-pin DIP.
LS7031: DC to 5 MHz six decade up counter with 8-decade latch and multiplexer, access to LSD latches allows attachment of prescalers for counting to 500 MHz; multiplexed BCD outputs; leading zero blanking; inputs CMOS and TTL compatible; outputs CMOS compatible. 40-pin DIP.
LS7055: DC to 250 KHz six decade up/down counter with integral preset, presignal, and main signal store; automatic or manual preset/reset control; 3 comparators with output flags; multiplexed BCD, 7 segment outputs and blanking override; internal oscillator; high noise immunity; all inputs CMOS compatible. 40-pin DIP.
LS7056: Identical, except that it has lamp test input instead of blanking override.

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LSI Computer Systems

LSI LOGIC

SPARC Architecture High Performance RISC Microprocessors

Preliminary

Description

The L64801 and L64811 CPUs are high-speed HCMOS implementations of the SPARC RISC (Reduced Instruction Set Computer) architecture. The SPARC architecture was developed by Sun Microsystems based on advanced microprocessor research done at the University of California, Berkeley. SPARC stands for Scalable Processor ARChitecture. Because of its relative simplicity, the SPARC architecture will scale well as advanced semiconductor manufacturing techniques allow the architecture to be implemented in smaller geometries with higher operating speeds, resulting in even higher performance. The L64801 and L64811 are the first two commercially available implementations of the SPARC architecture.

The L64801 and L64811 execute high performance integer operations for general computing and embedded controller applications. The integer units are complemented with high performance floating-point devices for number-intensive applications and memory management devices, allowing the system designer maximum flexibility to configure a system to meet his specific requirements.

Features

- Reduced Instruction Set Computer (RISC) architecture
  - SPARC instruction set
  - Simple 32-bit instructions
  - Large windowed register file
    - L64801 120 registers 7 windows
    - L64811 136 registers 8 windows
- High performance
  - Single-cycle execution for most instructions
  - Efficient four-stage instruction pipeline with hardware interlocks
- Multitasking support with user and supervisor modes
- Multiprocessing support with tightly coupled coprocessor interfaces
- Artificial intelligence support using tagged arithmetic instructions
- SunOs operating system based on UNIX 4.3 BSD
- Optimized high level language compilers: C, FORTRAN, Ada, Pascal, LISP

LSI Logic

SPARC Shortform Matrix

Device Type	Part Number	Description	Clock Rate (MHz)	Packages	Performance
Central Processing Unit (CPU)	L64801GC-20 L64801GC-25	High Performance RISC Integer Unit Fujitsu Compatible	20 25	179 PPGA 179 CPGA 160 PFP	12 MIPS 15 MIPS
Floating-Point Controller (FPC)	L64802GC-20 L64802GC-25	Floating-Point Interface to TI8847	20 25	299 CPGA 299 CPGA	2.5 MFLOPS 3.0 MFLOPS
Memory Management Unit (MMU)	L64803__C-20 L64803__C-25	SPARC Reference MMU	20 25	160 PFP	
Central Processing Unit (CPU)	L64811GC-25 L64811GC-33	High Performance RISC Integer Unit Cypress Compatible	25 33	208 CPGA 208 PPGA 160 PFP	15 MIPS 20 MIPS
Floating-Point Controller (FPC)	L64812GC-25 L64812GC-33	Floating-Point Interface to TI8847	25 33	299 CPGA	3.0 MFLOPS 4.0 MFLOPS
Floating-Point Unit	L64814GC-25 L64814GC-33	Integrated FPC/FPP	25 33	120 CPGA	3.0 MFLOPS 4.0 MFLOPS
MMU/Cache Controller (MCT)	L64815GC-25 L64815GC-33	Integrated MMU/Cache Controller w/Tags	25 33	196 PFP	

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MIPS Architecture High Performance RISC Microprocessors

Preliminary

Description

The LR2000 and LR3000 CPUs are high-speed HCMOS implementations of the MIPS RISC (Reduced Instruction Set Computer) microprocessor architecture. The MIPS architecture was initially developed at Stanford University under the auspices of DARPA. Both the LR2000 and LR3000 RISC microprocessors are extensions of the Stanford MIPS architecture developed by MIPS Computer Systems Inc. This architecture makes possible a microprocessor that can execute instructions for high-level language programs at rates approaching one instruction per processor clock.

The LR2000 and LR3000 microprocessors include on-chip memory management and support for up to three tightly-coupled coprocessors including the single-chip LR2010 and LR3010 Floating-Point Accelerators.

Features

- Reduced Instruction Set Computer (RISC) architecture
  - MIPS instruction set
  - Simple 32-bit instructions
  - Register-to-register load-store operation
  - All instructions (except MPY and DIV) execute in a single cycle
- High performance
  - Fast instruction cycle with five-stage pipeline
  - Efficient handling of pipeline stalls and exceptional events
- Optional devices tightly coupled for high performance
  - LR2010/LR3010
    - Floating-Point Accelerator (FPA)
  - LR2020/LR3020
    - Write Buffers (WB)
- 32 general-purpose registers
- On-chip cache control
- On-chip memory management unit (MMU)
  - Fully-associative, 64-entry translation lookaside buffer (TLB)
  - Supports 4 Gbyte virtual address space
- Multi-tasking support
  - User and kernel (supervisor) modes
- Tightly coupled coprocessor interface
  - Generates all addresses and handles memory interface control
  - Supports up to three external coprocessors
- Strong, integrated software support
  - UMIPS operating system
    - System V.3, 4.3 BSD
  - Optimizing compilers
    - C, Ada (Verdix)
    - FORTRAN, LPI-COBOL
    - Pascal, LPI-PL-1

Product Outline

Device Type	Part Number	Description	Clock Rate (MHz)	Packages
Central Processing Unit (CPU)	LR2000	High Performance RISC Processor with Memory Management	12.5	144 CPGA
	LR2000A		16.7	144 CPGA
	LR3000		16.7	172 CLDCC
	LR3000A		25.0	155 CPGA
Floating-Point Accelerator (FPA)	LR2010	Tightly Coupled Coprocessor	12.5	84 CLDCC
	LR2010A		16.7	84 CLDCC
	LR3010		16.7	84 CLDCC
	LR3010A		25.0	84 CLDCC
Write Buffer (WB)	LR2020	Write Through Cache Interface	12.5	68 PLDCC
	LR2020A		16.7	68 CPGA
	LR3020		16.7	68 PLDCC
	LR3020A		25.0	68 CPGA

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LSI Logic

L64500
MIL-STD-1750A
Microprocessor

Description

The LSI Logic L64500 is a monolithic 0.9-micron channel length (1.5-micron gate length) HCMOS chip which implements the MIL-STD-1750A (Notice 1) Instruction Set Architecture (ISA). The L64500 is a 16-bit Central Processing Unit (CPU) used for real-time processing. The CPU uses a sophisticated ALU architecture which is expandable up to 32 bits depending on the opertion. The L64500 uses separate address and data buses to improve system performance and has advanced look-ahead capability with the optional L64550 (MBU) to minimize the probability of wait-state insertion.

The L64500 can be augmented with an L64550 (MBU) chip to implement optional enhancements of the MIL-STD-1750A. The L64550 includes the Memory Management Unit (MMU) with memory expansion capabilities up to 1 M words of memory, the Block Protect Unit (BPU), Memory Fault Status Register (MFSR), the Bus Arbitration Unit (BAU) with six bus masters, Start-up ROM interface, Discrete I/O Port, Trigger-go Counter and other options.

The L64500 CPU and the L64550 MBU chips were designed as a system to optimize performance.

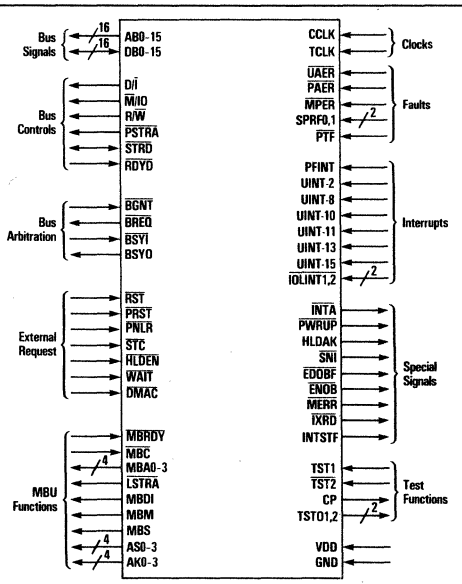
The L64500 and L64550 are included in MDE™, LSI Logic's design system, as ASIC library elements. These elements can be used as Gigacells™ when combined with gate arrays or standard cells, or they can be used in multi-chip system simulations when adding new ASIC chips to the system.

The L64500 is available in several speed grades from 15 MHz to 30 MHz over the full military temperature range of −55°C to 125°C.

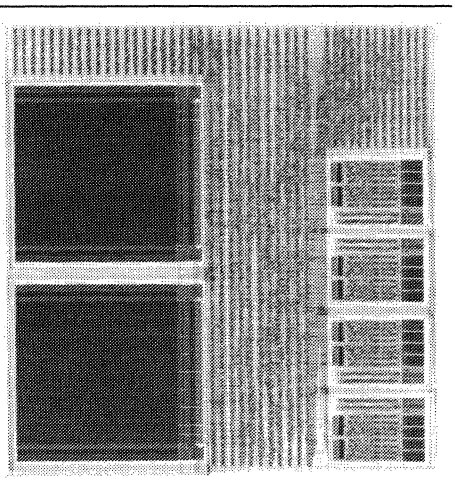
Features

- Single-chip high performance microprocessor
- Implements MIL-STD-1750A (Notice 1) Instruction Set
- 0.9-micron channel length (1.5-micron gate length) HCMOS 2-layer metal cell-based technology
- 30 MHz operation over full military range
- Power dissipation ≤ 1 W
- TTL compatible interface
- Flexible packaging capability
- Available as ASIC library element
- Performance optimized architecture
  - Split data and address bus
  - Variable width ALU: up to 32 bits
  - Instruction pre-fetch
  - Multiport register files
- Timers A and B on-chip
- 64K word address space expandable to 3M word with optional MBU chip

Logic Symbol and Chip Layout



Logic Symbol



Chip Layout

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L64550
MIL-STD-1750A
MBU Peripheral Device

Description

The LSI Logic L64550 Memory Management and Block Protection Unit device is a monolithic 0.9-micron channel length (1.5-micron gate length) HCMOS chip designed to support the L64500 CPU (MIL-STD-1750A ISA). The L64550 contains a number of MIL-STD-1750A support options including the Memory Management Unit (MMU) with mapping RAM, Block Protect Unit (BPU) with protection RAM, Memory Fault Status Register (MFSR), Watch-Dog timer and start-up ROM interface. In addition, the L64550 contains other options such as; a Bus Arbitrator with up to 6 bus masters, extended addressing capability to 8 M words, discrete I/O port, sophisticated CPU/MBU handshake to increase performance and bus time-out timer.

The MMU allows addressing of up to 1 M word of memory. In applications not requiring adherence to the standard, addressing can be extended to 8 M words. The MMU performs the logical-to-physical address translation and protection of logical space.

The BPU provides write protection in 1 K page granularity for up to 1 M word of physical memory for both L64500 CPU and DMA access.

If desired, the MMU and the BPU can be individually disabled.

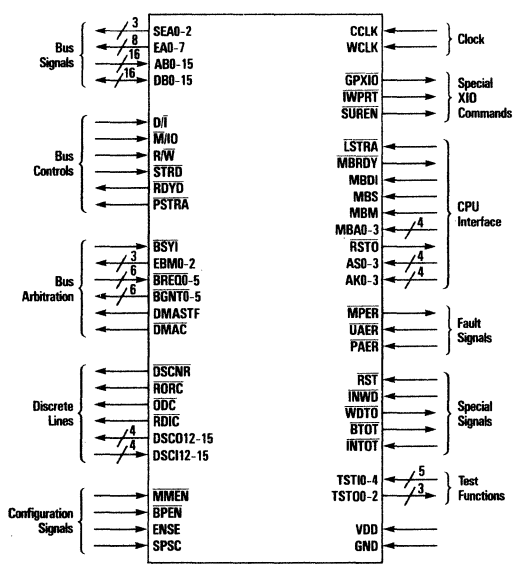
The L64550 MBU and L64500 CPU are included in MDE™, LSI Logic's design system, as ASIC library elements. These elements can be used as Gigacells™ when combined with gate arrays or standard cells, or they can be used in multi-chip system simulations when adding new ASIC chips to the system.

The L64550 is available in several speed grades from 15 MHz to 30 MHz over the full military temperature range of −55°C to 125°C.

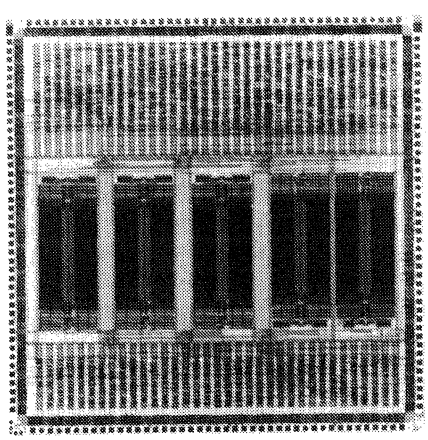
Features

- 0.9-micron channel length (1.5-micron gate length) HCMOS technology
- 30 MHz operation over full military range
- Power dissipation < 1 W
- Memory Management Unit (MMU) with 512 × 16 cache RAM
- Block Protect Unit (BPU) with 128 × 16 cache RAM
- Hit/miss mechanism
- Discrete I/O ports
- Extended addressing to 8 M words
- Bus Arbitration Unit with up to 6 bus masters
- Memory Fault Status Register (MFSR)
- Start-up ROM interface
- Bus time-out timer
- Watch-Dog timer
- TTL compatible interface
- Flexible packaging capability

Logic Symbol and Chip Layout



Logic Symbol



Chip Layout

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LSI LOGIC

Signal and Image Processing Devices

Description

LSI Logic's family of high-speed digital signal and image processing devices perform common DSP operations such as convolution/correlation, template matching, median filtering, binary and multi-bit filtering, histogram/Hough transform processing and edge detection or enhancement. Designed to operate independently, as an integrated suite or with non-LSI Logic devices, the components work in stand-alone or in multi-processing configurations to enhance window size and/or precision. Component architecture includes features that maximize application flexibility, such as adjustable window size and shape and variable coefficients or mask values. The products described below are available in both commercial and military versions and may be integrated as megafunctions/megacells into LSI Logic ASIC designs.

Variable-Length Video Shift Registers
The L64210, L64211 and L64212 are high-speed Variable-Length Video Shift Registers for use separately or as video line delays for the L64200 series filter processors.

Rank-Value Filter
The L64220 Rank-Value Filter processes sorted input values in a moving window and outputs a rank value. Rank values include maximum, minimum and median outputs. The device is reconfigurable for operation as an 8×8, 4×16, or 2×32 two-dimensional filter or as a 1×64 one-dimensional filter.

Binary Filter and Template Matcher
The L64230 Binary Filter and Template Matcher offers high performance for real-time image processing applications including video pattern matching, noise removal and morphological erosion and dilation operations. With data rates up to 20 MHz, the L64230 is also suitable for radar processing.

Multi-Bit Filters
The L64240 and L64243 Multi-Bit Filters are ideally suited for real-time image processing applications including convolution, correlation, inverse filtering, edge enhancement and edge detection. Output formatting circuitry ensures total system compatibility by allowing users to control gain, threshold data and data format.

Histogram/Hough Transform Processor
The L64250 Histogram/Hough Transform Processor can be configured to perform a number of tasks including histograms and modified transforms for data sets up to 2^{24} points or images up to 4096×4096 pixels.

Versatile FIR Filter Processors
The L64260 and L64261 high-speed Versatile FIR Filter Processors compute inner products on 16-bit data. Four MAC elements, each with four coefficient and four data registers, allow implementation of FIR filters with decimation or interpolation, 4×4 convolution and matrix-matrix or matrix-vector multiplication. The L64261 is functionally equivalent to the L64260 except that fewer I/O pins are provided allowing the device to be packaged in a lower pin count package.

Crossbar Switch
The L64270 Crossbar Switch allows any of 64 inputs to be converted to any of 64 outputs. The device can be operated in either a clocked pipeline mode or an unclocked flow through mode. Input and output signals can be configured as either unidirectional signals or bi-directional signals to simplify design of bus switching systems.

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Signal and Image Processing Devices

Device Type	Part Number	Description	Clock Rate (MHz) Commercial	Clock Rate (MHz) Military	Packages
Variable-Length Video Shift Register (VSR)	L64210 L64210A	1K × 4 × 8 Line Delay	15 20	12 16	68 PLDCC, 68 CPGA
	L64211 L64211A	512 × 8 × 8 Line Delay	15 20	12 16	120 CPGA, 120 PPGA
High Speed Variable-Length Video Shift Register	L64212 L64212A	1K × 4 × 9 Line Delay	30 40	20 30	84 CPGA
Rank-Value Filter (RVF)	L64220 L64220A	12-Bit, 64-Tap Rank-Value Filter	15 20	12 16	155 CPGA
Binary Filter and Template Matcher (BFIR)	L64230 L64230A	1024-Tap Binary Data FIR Filter	15 20	12 16	155 CPGA
8 × 8 Multi-Bit Filter (MFIR)	L64240 L64240A	64-Tap, 8-Bit Data or 32-Tap, 16-Bit Data FIR Filter	15 20	12 16	155 CPGA
3 × 3 Multi-Bit Filter (MFIR)	L64243 L64243A L64243B	9-Tap, 8-Bit Data FIR Filter	20 30 40	20 30 40	68 CPGA, 68 PLDCC
Histogram/Hough Transform Processor (HHP)	L64250 L64250A	4096 × 4096 Pixel Histogram and Hough Transform Processor	15 20	12 16	68 CPGA, 68 PLDCC
Versatile FIR Filter Processor	L64260 L64260A	Multi-Tap 16-Bit FIR Filter Processor	20 40	20 30	223 CPGA, 144 CPGA
	L64261 L64261A	Multi-Tap 16-Bit FIR Filter Processor	20 40	20 30	144 CPGA
Crossbar Switch	L64270 L64270A	64 to 64 Crossbar Switch	30 40	25 30	160 PQFP

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L64032
32×32-Bit
Multiplier-Accumulator

LSI LOGIC

Description

The L64032 is a high-speed 32×32-bit parallel multiplier-accumulator which provides single precision (32×32) and multiple precision (64×64) fixed-point multiplication and single precision multiplication with accumulation. The device is fabricated with a 0.9-micron channel length (1.5-micron gate length) silicon-gate HCMOS process. High speed is obtained through the use of modified Booth encoding, Wallace tree adders and a high-speed carry-select adder.

The L64032 is useful in digital signal processing (DSP) applications such as Fourier transforms, digital filtering, power series expansions and correlations. In these applications, the 32-bit word length yeilds a signal-to-noise ratio and dynamic range of up to 192 dB. This device is also useful for general computational tasks such as matrix manipulations, graphics processing, and arithmetic acceleration.

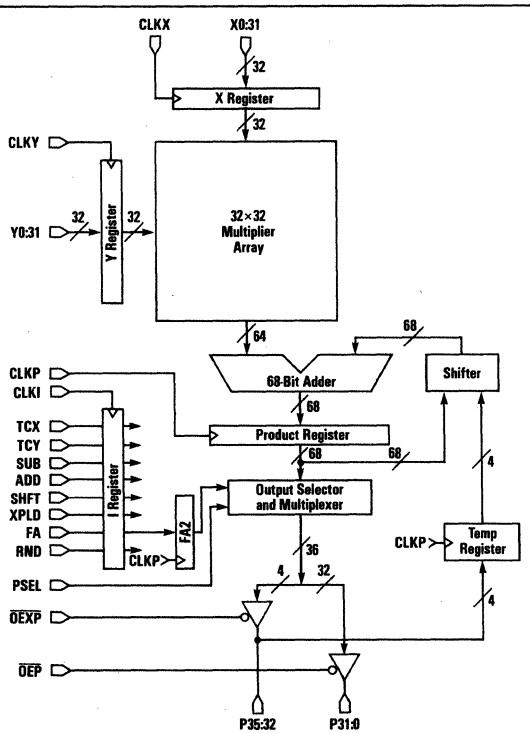
Features

- 32×32-bit parallel multiplication and product accumulation
- 64×64-bit fixed-point multiplication
- High speed

L64032	125 ns cycle time	commercial
	160 ns cycle time	military
L64032A	100 ns cycle time	commercial
	125 ns cycle time	military
L64032B	80 ns cycle time	commercial
	100 ns cycle time	militay

- 0.9-micron channel length (1.5-micron gate length) silicon-gate HCMOS process for high speed and low power consumption—900 mW at 10 MHz
- Supports unsigned integer, two's complement integer, unsigned fractional and two's complement fractional input formats
- Supports unsigned integer, two's complement integer, unsigned fractional, two's complement fractional (shifted) and two's complement fractional (unshifted) output formats
- Positive and negative product accumulation
- TEMP register supports product register preloading
- Full rounding capability
- All registers offer full built-in scan testing capability
- 132-pin grid array (PGA) package

Block Diagram



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L64133
32-Bit HCMOS IEEE Floating-Point Processor
Preliminary

LSI LOGIC

Description

The L64133 is a high-speed processor which contains a full 32-bit floating-point multiplier and a full 32-bit floating-point ALU on a single chip. This three-bus device has a clean architecture with no internal pipelines. It is ideally suited for high-speed graphics and digital signal processing applications.

The L64133 supports the ANSI/IEEE Standard P754-1985 (commonly called IEEE) format. The device has been implemented in a 1.0-micron HCMOS process for high-speed with low power dissipation, and is packaged in an industry standard 144-lead ceramic pin grid array.

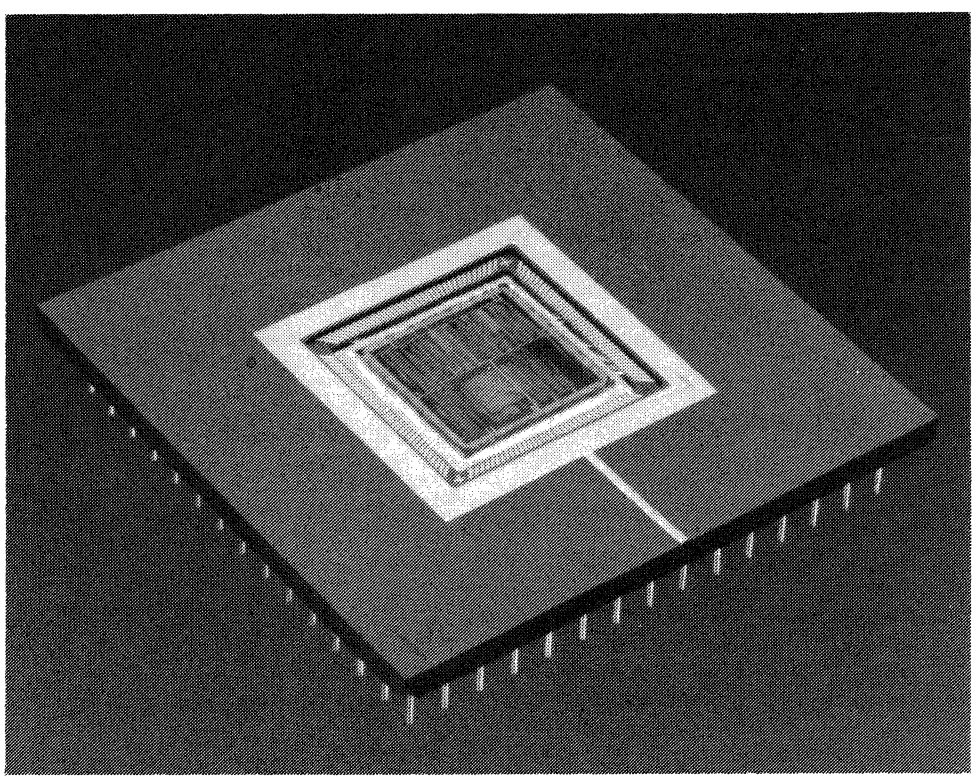
Features

- Provides separate 32-bit floating-point multiplier and floating-point ALU on a single chip
- Fully supports all boundary conditions of the IEEE format except operations with denormalized numbers, which are treated as zero
- Three-bus architecture for high throughput
- Fast cycle times
- Separate register enable signals

	Commercial	Military
L64133B	60 ns	80 ns
L64133A	80 ns	100 ns
L64133	100 ns	125 ns

- No internal pipelines for high throughput with low latency
- Architecture optimized for sum of products and product of sums calculations
- All input registers can be selected as edge-triggered flip-flops or level-triggered latches
- All output registers can be selected as edge-triggered flip-flops or transparent buffers
- Single master clock
- Four separate input registers
- Provides conversion from integer to floating point and from floating point to integer formats
- Performs (2 minus X) for Newton-Raphson division
- Special Graphics operation such as Min and Max
- Full serial scan test mode for all input and output registers eases board and system level testing

L64133 Device in 144-Lead Ceramic Pin Grid Array Package



LSI Logic

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Now! 32MHz and 40 MHz

DSP320C10

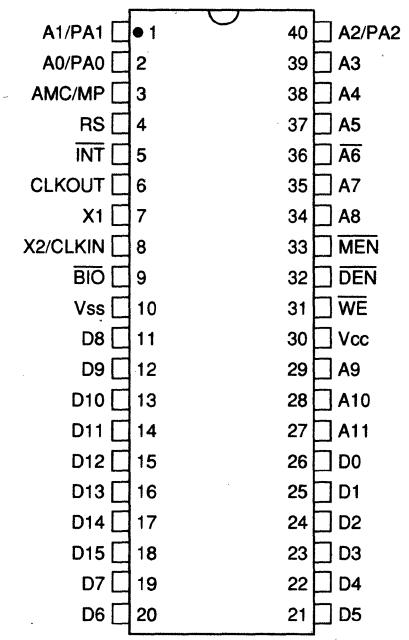
CMOS Digital Signal Processor

FEATURES

- 98ns instruction cycle (max)
- 144 word on-chip data RAM
- ROMless version DSP320C10
- 1.5K word on-chip program ROM—DSP320CM10
- External memory expansion to a total of 4K words at full speed
- 16-bit instruction/data word
- 32-bit ALU/accumulator
- 16 x 16-bit multiply in 98ns (max)
- 0 to 15-bit barrel shifter
- Eight input and eight output channels
- 16-bit bidirectional data bus with 50-Mbps transfer rate
- Interrupt with full context save
- Signed two's complement fixed-point arithmetic
- CMOS technology
- Single 5 volt supply
- Three versions available:
  - DSP320C10 .....20.5MHz clock
  - DSP320C10-25 .....25.6MHz clock
  - DSP320C10-32 .....32.8MHz clock
  - DSP320C10-40 .....40.96MHz clock
- Fully compatible with T.I.'s TMS320C10
- Meet DESC SMD 5962-87633

PIN CONFIGURATION

Top View



DESCRIPTION

The DSP320C10 is the first low power CMOS member of the Microchip Technology DSP320 family of digital signal processors, designed to support a wide range of high-speed or numeric-intensive applications. This device is a CMOS pin-for-pin compatible version of the industry standard DSP32010 digital signal processor. The 16/32-bit single-chip microcomputer combines the flexibility of a high-speed controller with the numerical capability of an array processor, thereby offering an inexpensive alternative to multichip bit-slice processors. The DSP320 family contains MOS microcomputers capable of executing six million instructions per second. This high throughput is the result of the comprehensive, efficient, and easily programmed instruction set and of the highly pipelined architecture. Special instructions have been incorporated to speed the execution of digital signal processing (DS) algorithms. The DSP320 family's unique versatility and power give the design engineer solutions to a variety of complicated applications. In addition, these microcomputers are capable of providing the multiple functions often required for a single application. For example, the DSP320 family can enable an industrial robot to synthesize and recognize speech, sense objects with radar or optical intelligence, and perform mechanical operations through digital servo loop computations.

Part Number	Speed (MHz)	Package
DSP320C10-32/P	32.8	40P DIP
DSP320C10-32/L	32.8	44P PLCC
DSP320C10-25/P	25.6	40P DIP
DSP320C10-25/L	25.6	44P PLCC
DSP320C10/P	20.5	40P DIP
DSP320C10/L	20.5	44P PLCC
DSP320EE12/P	20.5	40P DIP
DSP320C10-32BQA 883C	32.8	40P CER
DSP320C10-25BQA 883C	25.6	40P CER
DSP320C10BQA 883C	20.5	40P CER

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Microchip

MILITARY

Product Summary

Device	Ceramic X/Q(Pins)	LCC U	Access Time (nsec)	Reliability Level: MIL-883C Compliant	Reliability Level: DESC SMD	DESC SMD Number	Remarks
EPROMs							
27C64	X	✔	150, 170, 200, 250	Yes	Pending	9562-87102	8Kx8 28 CER, 32 LCC
27C128	X	✔	150, 170, 200, 250	Yes	Released	9562-87661	16Kx8 28 CER, 32 LCC
27C256	X	✔	150, 170, 200, 250	Yes	Pending	5962-86063	32x8 28 CER, 32 LCC
27C512	X	✔	150, 170, 200, 250	Yes	Released	5962-87648	64Kx8 28 CER, 32 LCC
27HC64	X	✔	55, 70	Pending	Pending	5962-87102	8Kx8 RELEASE DATE JAN 89
27HC256	X	✔	55, 70	Pending			32Kx8 RELEASE DARE JAN 89
27256	X	✔	170, 200, 250	Yes		5962-84111	32Kx8
27HC641	X	✔	55, 70		Pending	5962-87515	8Kx8 W.S.I. Pin Outs
EEPROMs							
28C64A	X	✔	150, 200, 250	Yes	Released	5962-87514	8Kx8 28 CER, 32 LCC, 28 FLAT
28CP256	Q	✔	90*, 120, 150, 200		Pending	5962-88525	32Kx8 RELEASE DATE JUNE 89
28CP64	X	✔	90*, 120, 150, 200		Pending	5962-87514	8Kx 8 RELEASE DATE JULY 89
28HC64	X	✔	90*, 120, 150, 200		Pending	5962-87514	8Kx8 RELEASE DATE JULY 89
28HC416	Q	✔	90*, 120, 150, 200		TBA	5962-88634	4Kx16 ON HOLD
28HC256	Q	✔	90*, 120, 150, 200		Pending		32Kx8 RELEASE DATE JULY 89
			*90nsec In Development				
DSPs			**Operating Freq.**				
32010	Q	✔	6.7 to 20.5 MHz		Released	84053	900mw Power Diss., Typ.
320C10	Q	✔	6.7 to 20.5 MHz		Released	5962-87633	320mw Power Diss., Typ.
320C10-25	Q	✔	15.0 to 25.6 MHz		Released	5962-87633	380mw Power Diss., Typ.
320CF10-25	Q	✔	6.7 to 25.6 MHz		Released	5967-87633	380mw Power Diss., Typ.

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World's Fastest 16-bit Microcontroller!

6.4 MIPS!

Microchip

DSC320C14

Digital Signal Controller™

FEATURES

320C14 CPU

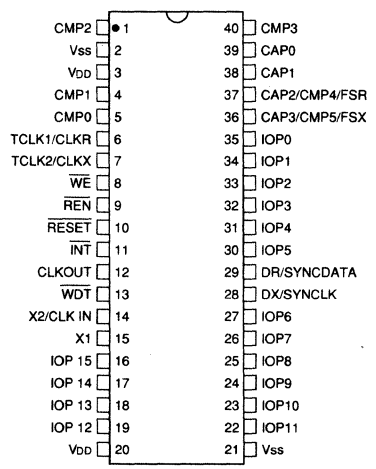
- 160/200ns instruction cycle time, 25.6MHz and 20.5MHz versions available
- 4K x 16 on-chip program ROM
- 256 x 16 on-chip data RAM
- Double precision 32 bit ALU/accumulator
- Signed two's complement fixed point arithmetic
- 16 x 16 multiply in 160ns max at 25.6MHz
- 0—15 bit barrel shifter
- Accumulator output shifter
- Data logic operations, AND, OR, XOR
- DSP320C10 instruction set
- Internal and external memory expansion to a total of 8K words, program, data, and I/O
- 16-bit instruction/data word

320C14 Peripherals

- 16 separate I/O pins, bit direction software programmable with compare capabilities
- Two 16 bit internal timer/counters with period and prescale control, external clock inputs with Schmitt triggers
- Serial I/O
  - —Internal baud rate generator
  - —Async/full duplex, sync/half duplex (6.4MHz)
  - —6 to 9 bit data
  - —Even/odd parity
  - —Codec mode
  - —Communication protocol support
- —Watchdog timer, external output pin available for direct RESET pin tieback
- —Six high speed compare output channels that may also be reconfigured as 6 PWM channels
- —Four/16 bit x 4 deep FIFO timer event capture, with up to 4 external Schmitt trigger inputs
- —13 internal, maskable interrupt sources and external interrupt and NMI input pins
- —Two I/O configuration versions available- microcontroller or microprocessor
- —Three package styles - 40 lead DIP (P), 44 lead PLCC (L), and 68 lead PLCC (L).

PIN CONFIGURATION

Top View



DESCRIPTION

The DSC320C14 Digital Signal Controller™ is the first low power CMOS processor designed specifically to meet real time control applications. The DSC320C14 is a 16 bit controller, a microcontroller that contains a DSP core and a high level of peripheral integration, all in a single device. This digital signal controller is an assembler code level compatible device version of the industry standard DSP320C10 digital signal processor.

The DSC320C14 is truly the first microprocessor that bridges the gap between stand-alone microcontrollers, microprocessors and dedicated digital signal processors. The DSC320C14 is a third generation stand-alone microcontroller, a microcontroller that satisfies the following criteria: a CPU plus I/O and memory (first generation), 16 bit internal architecture (second generation), and dedicated instructions for DSP and numeric intensive applications (third generation).

The DSC320C14 provides the best performance/cost ratio for high speed control and numeric or DSP intensive applications because the DSC320C14 has its own control, communication, and numeric operation functions on one single chip. The DSC320C14 provides three flexible channels of data communication/command passing to a central processing unit - serial I/O, dedicated parallel I/O, and a memory interface. The DSC320C14 can execute up to 6.4 MIPs (million instructions per second) because of its typical 1 machine cycle per instruction speed, and its pipelined architecture.

Microchip Technology, Inc.

Preliminary Information

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MicroWorkshop Series 16

Digital Signal Processor Development Tools

The MicroWorkshop™

The Microworkshop™ Series 16 is a PC-based in-circuit emulator for the DSP320C1X family of digital signal processors from Microchip Technology Incorporated (formerly General Instrument Microelectronics). The Microworkshop simplifies code development and displays code, text, and captured waveform graphics simultaneously -- an industry first for PCs.

INNOVATION

The MicroWorkshop™ Series 16 development system represents a breakthrough in PC-based workstations in terms of performance and ease of use for the system designer. Consisting of custom enhancement boards and editor/assembler/testing software written under Microsoft Windows, the MicroWorkshop turns any IBM PC, XT, AT, 386 or compatible personal computer into a highly advanced workstation.

The MicroWorkshop™ is a complete development system offering in-circuit emulation and operation up to 40 MHz allowing the user to test all functions at the full speed of the application. A signal capture capability permits the acquisition and storage of signals in digital form from either the 320 DSP or from an external source. This allows precisely repeatable validation tests from real data.

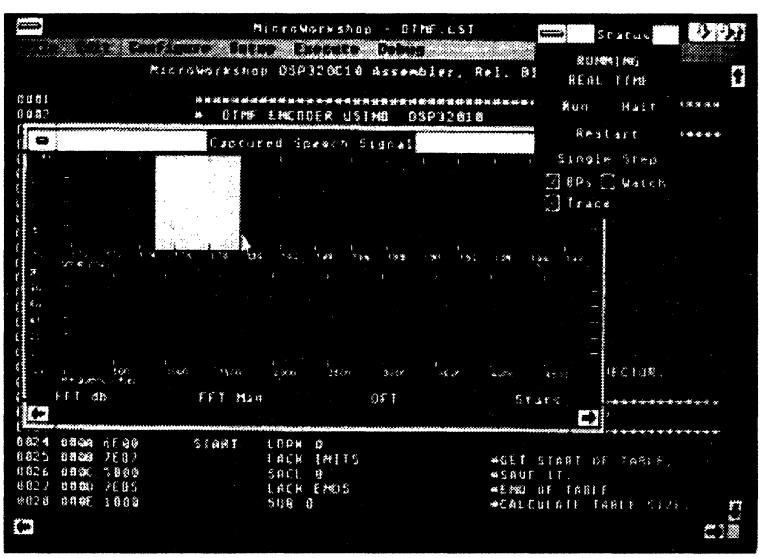
The development system emulates the Microchip Technology line of DSP320 Series digital signal processors -- from the CMOS DSP320C10, through the new 32-MHz, eight MIPs DSP320C10-32. Microchip's new Digital Signal Controller™, the DSC320C14, is also supported. Built-in expansion capability will enable the system to accommodate future products in the series. An integrated waveform display function with autoranging is provided. Waveforms can be stacked or overlapped for easy comparison and evaluation, and user-selected portions of the displayed signal can be processed through an FFT algorithm to provide a spectral display.

KEY BENEFITS

- In-circuit emulation
- Signal capture and inject
- Multi-processor emulation

AND MORE . . .

- Operates under Microsoft® Windows
- Simulation capability
- Editor-assembler with syntax checking
- Supports both MS-DOS and OS/2 operating systems
- Easy setting of complex and conditional breakpoints and traces
- Integral communication link to VAX
- Built-in expansion capability
- Unparalleled price/performance value



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AY0438I

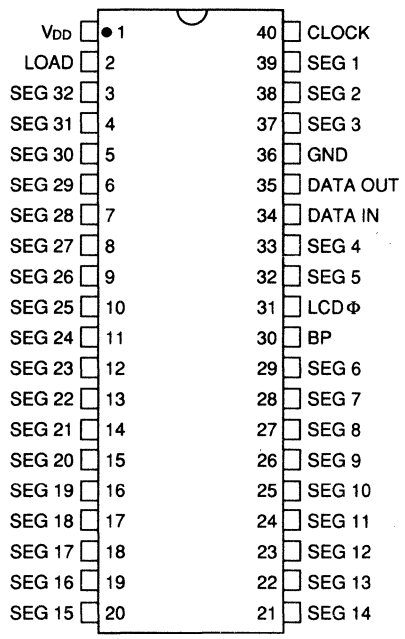
32-Segment CMOS LCD Driver

FEATURES

- Drives up to 32 LCD Segments of arbitrary configuration
- CMOS process for: wide supply voltage range, low power operation, high noise immunity, wide temperature range
- CMOS, NMOS and TTL-compatible inputs
- Electrostatic discharge protection on all pins
- Cascadable
- On-chip oscillator
- Requires only three control lines
- Can be used to drive relays, solenoids, print head drives, etc.

PIN CONFIGURATION

Top View



DESCRIPTION

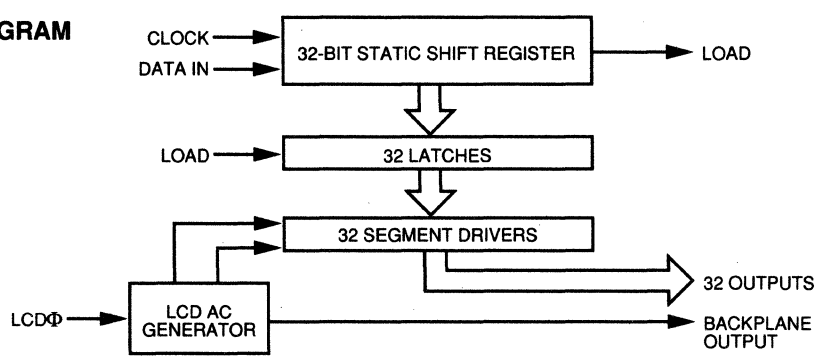
The AY0438I is a CMOS LSI circuit that drives a liquid crystal display, usually under microprocessor control. The part acts as a smart peripheral that drives up to 32 LCD segments. It needs only three control lines due to its serial input construction. It latches the data to be displayed and relieves the microprocessor from the task of generating the required waveforms.

The AY0438I can drive any standard or custom parallel drive LCD display, whether it be field effect or dynamic scattering; 7-, 9-, 14-, or 16-segment characters; decimals; leading + or -; or special symbols. Several AY0438I devices can be cascaded. The AC frequency of the LCD waveforms can either be supplied by the user or generated by attaching a capacitor to the LCDΦ input, which controls the frequency of an internal oscillator.

The device also acts as a versatile peripheral, able to drive displays, motors, relays, and solenoids within its output limitations.

The AY0438I is available in 40 lead dual-in-line ceramic and plastic packages. Plastic leaded chip carrier and unpackaged dice are also available.

BLOCK DIAGRAM



Preliminary Information

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AY8930

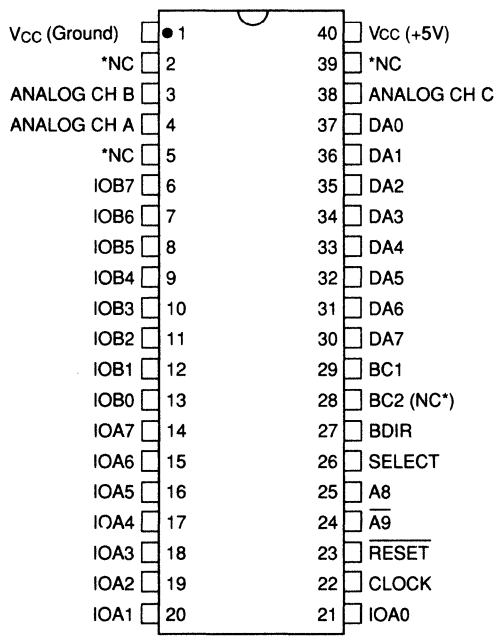
Enhanced Programmable Sound Generator

FEATURES

- Two modes available on-chip
  —AY8930 expanded mode
  —AY-3-8910A-compatible mode
- Improved frequency range
- Three independently programmable analog output channels with separate frequency, duty cycle and envelope controls for each channel
- 5-bits of logarithmic digital-to-analog conversion per channel
- Bus interface independent of clock frequency
- Input clock frequency: 2 or 4MHz
- Two 8-bit general purpose I/O ports

PIN CONFIGURATION

Top View



*NC - no connect

DESCRIPTION

The AY8930 Enhanced Programmable Sound Generator (EPSG) is an LSI circuit than can produce a wide variety of complex sounds under software control. The AY8930 is manufactured in the Microchip Technology Inc. n-channel silicon gate process. The AY8930 is an enhanced version of the company's industry standard AY-3-8910A sound generator. Enhanced features include improved frequence range and noise synthesis and independent control of each channel's envelope and duty cycle.

The PSG is easily interfaced to any bus-oriented system. Its flexibility makes it useful in applications such as music synthesis, sound effects generation, audible alarms, tone signalling, and home computer usage. In order to generate sound effects while allowing the processor to perform other tasks, the PSG can continue to produce sound after the initial commands have been given by the control processor. The fact that realistic sound production often involves more than one effect is satisified by the three independently controllable analog sound output channels available in the device. These analog sound output channels can each provide five bits of logarithmic digital-to-analog conversion, greatly enhancing the dynamic range of the sounds produced.

All circuit control signals are digital in nature and can be provided directly by a microprocessor/microcomputer. Therefore, one PSG can produce the full range of required sounds with no change in external circuitry. Since the frequency response of the PSG ranges from sub-audible at its lowest frequency to post-audible at its highest frequency, there are few sounds which are beyond reproduction with only the simplest electrical connections.

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AY-3-8910A
AY-3-8912A

Programmable Sound Generators

FEATURES

- Full software control of sound generation
- Interfaces to most 8-bit and 16-bit microprocessors
- Three independently programmable analog outputs
- One or two 8-bit I/O ports
- Single 5 volt supply
- 0° C to 70° C operation

DESCRIPTION

The AY-3-8910A/8912A Programmable Sound Generator (PSG) is an LSI circuit which can produce a wide variety of complex sounds under software control. The AY-3-8910A/8912A is manufactured using the Microchip Technology N-channel ion implant process. Operation requires a single +5V power process. Operation requires a single +5V power supply, a TTL compatible clock, and a 16-microprocessor or one of the PIC series of 8-bit microcontrollers.

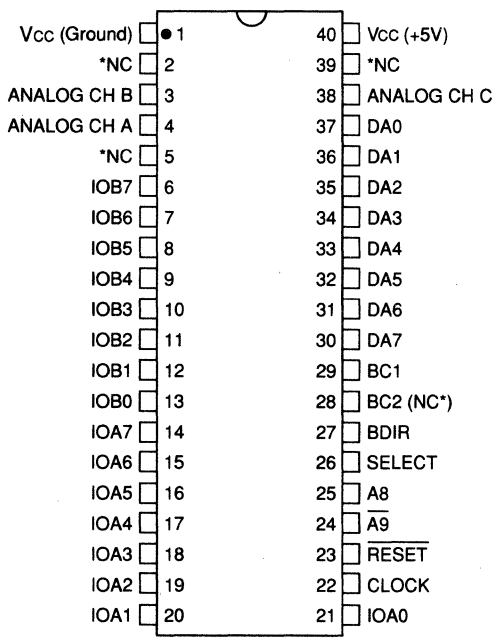
The PSG is easily interfaced to any bus oriented system. Its flexibility makes it useful in applications such as music synthesis, sound effects generation, audible alarms, tone signaling, PC and home computer usage. In order to generate sound effects while allowing the processor to perform other tasks, the PSG can continue to produce sound after the initial commands have been given by the control processor. The fact that realistic sound production often involves more than one component is satisfied by the three independently controllable analog sound output channels available in the PSG. The analog sound output channels can each provide 4 bits of logarithmic digital to analog conversion, greatly enhancing the dynamic range of the sounds produced.

All circuit control signals are digital in nature and may be provided directly bya microprocessor/microcomputer. Therefore, one PSG can produce the full ranges of required sounds with no change in external circuitry. Since the frequency response of the PSG ranges from sub-audible at its lowest frequency to post-audible at its highest frequency, there are few sounds which are beyond reproduction.

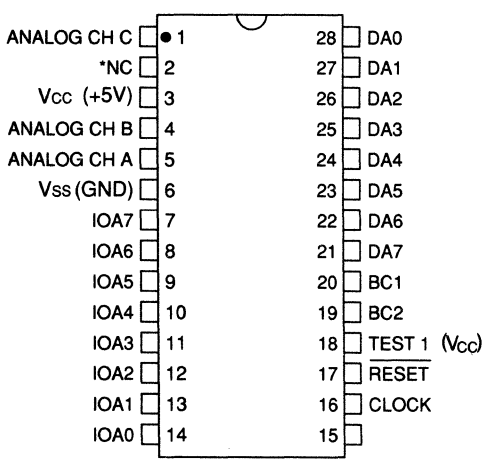
PIN CONFIGURATION

Top View

AY-3-8910A



AY-3-8912A



*NC - no connect

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SP0256B

Narrator™ Speech Processor

FEATURES

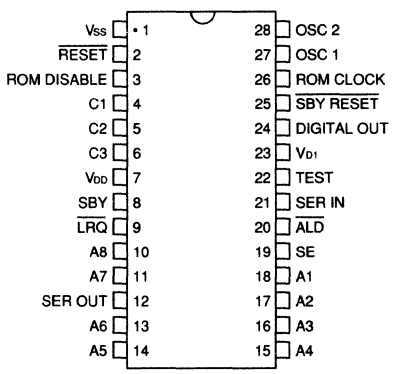
- Natural speech
- Stand alone operation with inexpensive support components
- Wide operating voltage
- Word, phrase or sentence library, ROM expandable
- Directly expandable to a total of 480K ROM
- Simple interface to most microcomputers or microprocessors
- Supports L.P.C. synthesis; formant synthesis; and allophone synthesis
- Upward compatible with the SP0264 speech processor
- Available in -40° C to 85° C version SP0526B-I

APPLICATIONS

- Telecommunications
- Appliances
- Computer peripherals
- Automotive
- Personal computers
- Toys/games
- Educational aids
- Warning systems
- Security systems
- Electronic musical instruments
- Aids to the blind
- Narrow bandwidth communication systems

PIN CONFIGURATION

Top View



DESCRIPTION

The SP0256B Speech Processor (SP) is a single chip N-Channel silicon gate MOS LSI device that is able, using its stored program, to synthesize speech or complex sounds.

The achievable output is equivalent to a flat frequency response ranging from 0 to 5kHz, a dynamic range of 42 dB, and a signal to noise ratio of approximately 35dB.

The SP0256B incorporates four basic functions:

- A software programmable digital filter that can be made to model a VOCAL TRACT.
- A 16K ROM which stores both data and instructions.
- A MICROCONTROLLER which controls the data flow from the ROM to the digital filter.
- A PULSE WIDTH MODULATOR that creates a digital output which is converted to an analog signal when filtered by an external low pass filter.

ALLOPHONE BASED SPEECH PROCESSOR - SP0256AL2

One example of a preprogrammed SP0256B is the AL2 pattern.

The SP0256AL2 is available preprogrammed with a standard ROM Pattern containing 64 allophones. Through the concatenation of selected allophones the user can construct any word in the English language, thereby providing an unlimited vocabulary.

A complete description of the SP0256AL2 is contained in the SP0256AL2 Data Sheet.

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SP0264

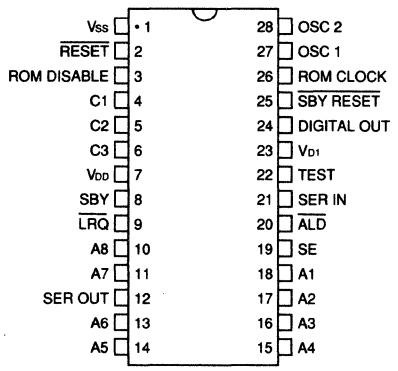
Narrator™ Speech Processor

FEATURES

- Natural speech
- Standalone operation with inexpensive support components
- Wide operating voltage
- Word, phrase, or sentence library, ROM expandable
- Expandable to 480K of ROM directly
- Simple interface to most microcomputers or microprocessors
- Supports L.P.C. synthesis; formant synthesis; and allophone synthesis
- 28-pin dual-in-line package
- Available in -40° C to 85° C version, SP0264-I
- Pin compatible with the SP0256B speech processor

PIN CONFIGURATION

Top View



DESCRIPTION

The SP0264 Speech Processor (SP) is a single chip N-Channel MOS LSI device that uses its stored program to synthesize speech or complex sounds.

The achievable output is equivalent to a flat frequency response ranging from 0 to 5 KHz, a dynamic range of 42dB, and a signal-to-noise ratio of approximately 35dB.

The SP0264 incorporates four basic functions:

- A software programmable digital filter than can be made to model a VOCAL TRACT.
- A 64K ROM that stores both data and instructions.
- A MICROCONTROLLER that controls the data flow from the ROM to the digital filter, the assembly fo the "word strings" necessary for linking speech elements; and the amplitude and pitch information to excite the digital filter.
- A PULSE WIDTH MODULATOR that creates a digital output that is converted to analog signal when filtered by an external low-pass filter.

APPLICATIONS

- Telecommunications
- Appliances
- Computer peripherals
- Automotive
- Personal computers
- Toys/games
- Educational aids
- Warning systems
- Security systems
- Electronic musical instruments
- Aids to the blind
- Narrow bandwidth communication systems

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RISC Single Cycle Instruction

PIC16C5X

EPROM-Based 8-Bit CMOS Microcontrollers

FEATURES

- Low-cost PIC 8-bit microcontroller family
- Designed with fully static CMOS EPROM technology
- User or factory programmable production
- Ultra wide performance ranges:
  —Frequency: 25kHz-20MHz (200ns instruction rate)
  —Voltage: 3.25V-6.25V single supply
  —Current: <5μA (standby mode/3.25V)
  2.5mA (4MHz/5V)
  20mA (20MHz/6.25V)
- Low-cost RC oscillator or crystal oscillator
- Security EPROM fuse for code protection
- Free running watchdog timer
- Oscillator start-up timer
- 8-bit real-time clock counter (RTCC) with optional 8-bit programmable prescaler
- 18-pin or 28-pin DIP and surface mount packaging
- Available in four temperature ranges:
  —Commercial (C) = 0° C to 70° C
  —Industrial (I) = -40° C to 85° C
  —Automotive (A) = -40° C to 110° C
  —Military (M) = -55° C to 125° C (2nd Q'89)
- Low-cost PC-based software development system

DESCRIPTION

Now Microchip Technology Inc introduces the next generation of microcontrollers...the first to incorporate the speed and low power operation of RISC and CMOS plus the time-saving flexibility of EPROM.

PIC15C5X 8-bit microcontrollers are low power, high speed CMOS devices containing RAM, I/O, a CPU and customer-defined EPROM on a single chip. A proprietary Harvard RISC design employs a powerful register file concept, with separate data and instruction busses. A set of thirty-three single-cycle instructions provide extremely high throughput speed. The 12-bit instruction bus allows for instruction "pipelining" which gives users an exceptional 5:1 speed advantage over competitive architectures, permitting real time algorithm execution as compared with less precise look-up approaches.

The efficiency of single operation instructions, when benchmarked against competative, multiple-instruction operation microcontrollers, also provides a very significant 2:1 software compaction.

Now customers can enjoy the many benefits of EPROM-based microcontrollers at costs similar to those for older, less versatile ROM-based microprocessors.

Microchip Technology, Inc.

PIC16C5X Microcontroller Selection Guide

PRODUCT	PINS	I/O	RAM	EPROM	OSC. RANGE	MIN INSTR CYCLE	AVAILABLE
PIC16C52	18	12	32 X 8	256 X 12	25kHz - 20MHz	200ns	NOW
PIC16C53	28	20	32 X 8	256 X 12	25kHz - 20MHz	200ns	NOW
PIC16C54	18	12	32 X 8	512 X 12	25kHz - 20MHz	200ns	NOW
PIC16C55	28	20	32 X 8	512 X 12	25kHz - 20MHz	200ns	NOW
PIC16C56	18	12	48 X 8	1024 X 12	25kHz - 20MHz	200ns	1Q'89
PIC16C57	28	20	80 X 8	2048 X 12	25kHz - 20MHz	200ns	1Q'89

Low-Cost NMOS Microcontrollers...
for highly cost sensitive applications where the superior performance of the PIC16C5X series is not require.

PRODUCT	PINS	I/O	RAM	ROM	INSTRUCTION SPEED(μs)
PIC1652	18	12	32 X 8	256 X 12	2
PIC1654	18	12	32 X 8	512 X 12	2
PIC1655	28	20	32 X 8	512 X 12	4
PIC1657	28	20	32 X 8	512 X 12	2
PIC1670	40	32	64 X 8	1024 X 13	2
PIC1672	40	32	64 X 8	2048 X 13	2

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PIC7000

8-Bit Microcontroller

FEATURES

- Pin-for-pin compatible with the Texas Instruments TMS7000 series microcontrollers
- 8-bit instruction data word
- Microprocessor and/or emulator—PIC7000
- 2048 bytes of on-chip ROM—PIC7020
- 4096 bytes of on-chip ROM—PIC7040
- External memory expansion capability
- 128 memory-mapped registers
- Full-feature data/program stack
- Two external mask-programmable interrupts
- On-chip 13-bit timer/event counter with interrupt and capture latch
- 32-bits general purpose input/output
- 5V power supply
- TTL-compatible I/O pins
- Single instruction BCD add and subtract
- Microprogrammable instruction set

DESCRIPTION

The Microchip Technology Inc PIC 7000 series is a powerful line of 8-bit microcontrollers with a memory-mapped architecture. Each PIC7000-series device contains 128 bytes of RAM, ROM (except the 7000 and 7001 devices), a microprogrammable CPU, and 32 reconfigurable I/O lines. A serial I/O port and a baudrate generator are provided on the PIC7001 and PIC7041 versions for telecommunications applications. The 32 I/O lines can be used as individual control lines in what is called the single-chip mode, or they can be converted to various address and data bus configuration modes for interfacing peripheral devices or external memories. Up to 64K bytes of external address space are supported. The PIC7000 series, with its 61-command microprogrammable instruction set, its on-chip ROM options, and its I/O configurations, will meet the needs of the most demanding applications. The entire series is specifically designed to allow customers to easily vary their products in response to market demand.

Features	Family Members				
	7000	**7020**	**7040**	**7001**	**7041**
On-Chip ROM (Bytes)	None	2K	4K	None	4K
On-Chip RAM (Bytes)	128	128	128	128	128
Interrupt Levels	4	4	4	6	6
General-Purpose Internal Registers	128	128	128	128	128
Timers	13-Bit	13-Bit	13-Bit	13-Bit (Two)	13-Bit (Two)
I/O LInes:					
Bi-Directional	16	16	16	22	22
Input Only	8	8	8	2	2
Output Only	8	8	8	8	8
Additional I/O	—	—	—	Serial Port	Serial Port

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PICES III
PIC PAK

PIC Development Systems

PC-Hosted Systems Simplify Software Development

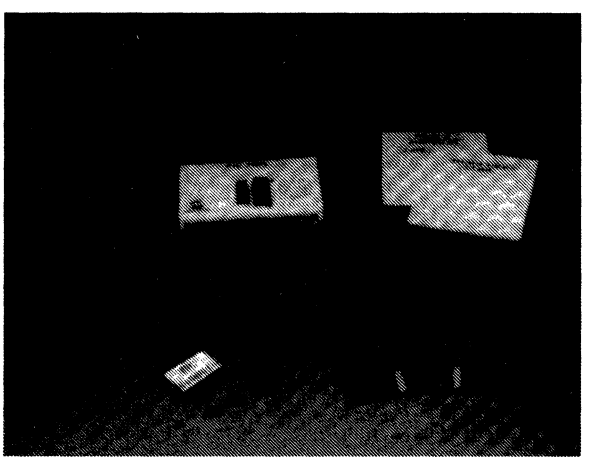
Two advanced PC-hosted systems, the PICES III and PIC PAK, are available to help users develop applications software and program PIC16C5X devices quickly and easily. Both operate with IBM PC, XT, AT, or compatibles. A version for the Apple Macintosh will be available in 1989.

PICES III

PICES III provides low-cost in-circuit emulation and debugging and includes an integrated 18-pin and 28-pin EPROM PIC programmer. This low profile module has a handy carrying case and comes with an external power supply, ribbon cabling, PICAL-C cross assembler, samples and a manual. Key features include a DC to 20MHz operating range, a built-in desassembler and up to 2000 hardware breakpoints. The kit comes with a handy carrying case.

PIC PAK

The PIC PAK (PIC Applications Kit) is a powerful yet low-cost software development tool that combines assembler and simulator software to compile, execute, debug and analyze microcode in a non-real time environment. An EPROM PIC programmer (PIC PRO) and EPROM PIC samples are included for code verification.



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Microchip

Serial CMOS EEPROM

24C01

1K (128 x 8) CMOS Serial Electrically Erasable PROM

FEATURES

- Low power CMOS technology
- Organization as 128 bytes (128 x 8)
- PCD 8572 replacement
- Two wire serial interface bus
- 5 volt only operation
- Self-timed write cycle (including auto-erase)
- Page-write buffer for up to 2 bytes
- 1ms write cycle time for single byte
- 8 Pin DIP or SOIC Package
- Available for extended temperature ranges:
  —Commercial (C) = 0° C to 70° C
  —Industrial (I) = -40° C to 85° C

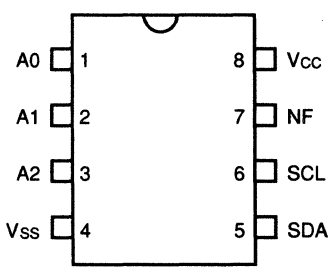
DESCRIPTION

The Microchip Technology Inc 24C01 is a 1K bit Electrically Erasable PROM. The device is organized as 128 x 8 bit memory with a two wire serial interface. Advanced CMOS technology allows a significant reduction in power over NMOS serial devices. Up to 8 24C01s may be connected to the two wire bus. The 24C01 is available in the standard 8-pin DIP and a surface mount SOIC package.

Microchip Technology, Inc.

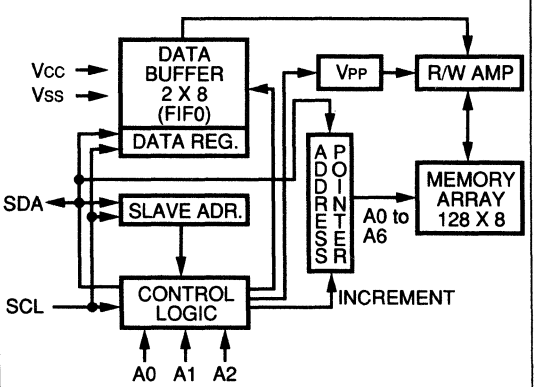
PIN CONFIGURATION

Top View



Note: NF = No Functionality

BLOCK DIAGRAM



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Microchip

Serial CMOS EEPROM

24C02

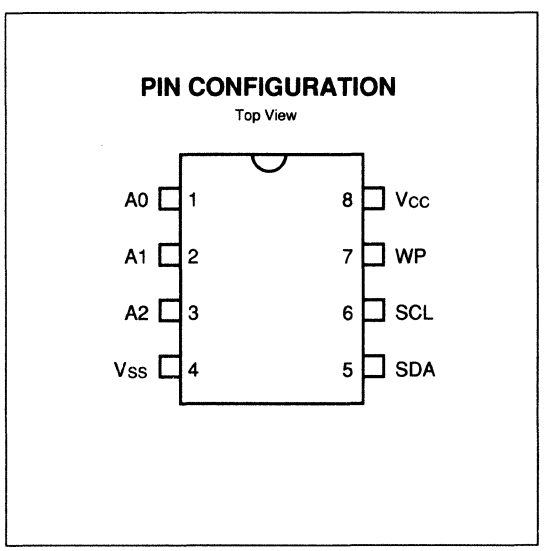
2K (256 x 8) CMOS Serial Electrically Erasable PROM

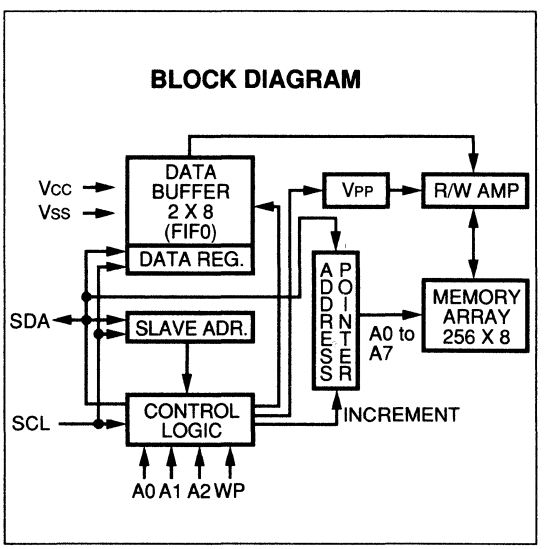
FEATURES

- Low power CMOS technology
- Organization as 256 bytes (256 x 8)
- PCD 8582 replacement
- Hardware write protect for upper 1K (128 x 8)
- Two wire serial interface bus
- 5 volt only operation
- Self-timed write cycle (including auto-erase)
- Page-write buffer for up to 2 bytes
- 1ms write cycle time for single byte
- 8-pin DIP or SOIC package
- Available for extended temperature ranges:
  —Commercial (C) = 0° C to 70° C
  —Industrial (I) = -40° C to 85° C

DESCRIPTION

The Microchip Technology Inc 24C02 is a 2K bit Electrically Erasable PROM. The device is organized as 256 x 8 bit memory with a two wire serial interface. Advanced CMOS technology allows a significant reduction in power over NMOS serial devices. A special feature allows a write protection for the upper 1K (128 x 8). The 24C02 also has a page-write capability for up to 2 bytes of data. Up to 8 24C02s may be connected to the two wire bus. The 24C02 is available in the standard 8-pin DIP and a surface mount SOIC package.





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Microchip

24C04

4K (2 x 256 x 8) CMOS Serial Electrically Erasable PROM

FEATURES

- Low power CMOS technology
- Organization as two blocks each 256 bytes (256 x 8)
- Hardware write protect for upper block
- Two wire serial interface bus
- 5 volt only operation
- Self-timed write cycle (including auto-erase)
- Page-write buffer for up to 8 bytes
- 1ms write cycle time for single byte
- 8-pin DIP or SOIC Package
- Available for extended temperature ranges:
  —Commercial (C) = 0° C to 70° C
  —Industrial (I) = -40° C to 85° C

DESCRIPTION

The Microchip Technology Inc 24C04 is a 4K bit Electrically Erasable PROM. The device is organized as two blocks of 256 x 8 bit memory with a two wire serial interface. Advanced CMOS technology allows a significant reduction in power over NMOS serial devices. A special feature allows a write protection for the upper 256 byte block. The 24C04 also has a page-write capability for up to 8 bytes of data. Up to 4 24C04s may be connected to the two wire bus. The 24C04 is available in the standard 8-pin DIP and a surface mount SOIC package.

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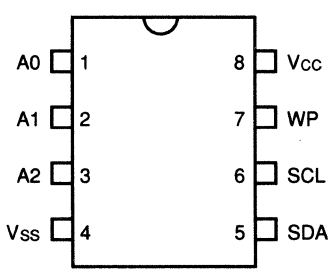
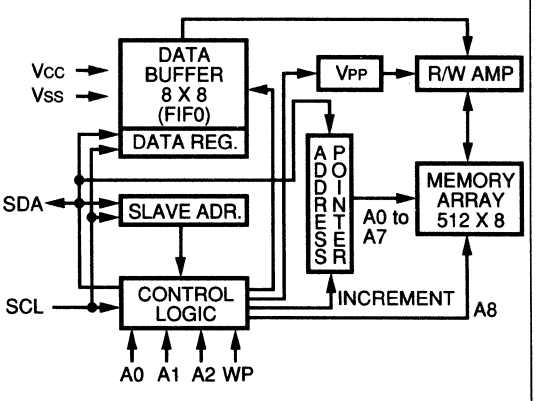
PIN CONFIGURATION

Top View



BLOCK DIAGRAM



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Very High Speed EPROM

27HC64

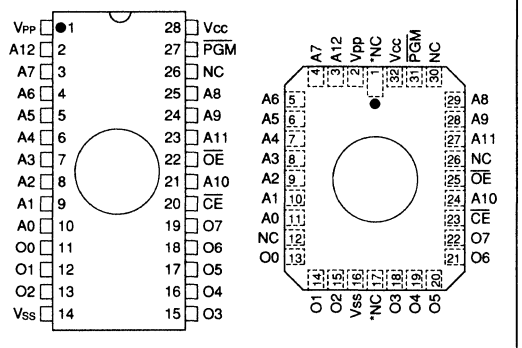
64K (8K x 8) High Speed CMOS UV Erasable PROM

FEATURES

- Bipolar performance
  —45ns maximum access time
- CMOS technology for low power consumption
  —80mA active current
  —100µA standby current (low power option)
- OTP (one time programming) available
- Auto-insertion-compatible plastic packages
- Auto ID™ aids automated programming
- Separate chip enable and output enable controls
- Two programming algorithms allow improved programming times
  —Fast programming
  —Rapid-pulse programming
- Organized 8K x 8: JEDEC standard pinouts
  —28-pin dual-in-line package
  —32-pin chip carrier (leadless or plastic)
- Extended temperature ranges available:
  —Commercial (C) = 0° C to 70° C
  —Industrial (I) = -40° C to 85° C
  —Military** (M) = -55° C to 125° C

PIN CONFIGURATION

Top View



●Pin 1 indicator on PLCC on top of package

* DC (don't connect on PLCC package)

PRODUCT SPECIFICATION GUIDE

PART NUMBER	ACCESS TIME	VCC RANGE	ACTIVE Icc*	STANDBY ICC*	TEMPERATURE RANGE
27HC64-45	45ns	5V ±10%	80mA	40mA	C
27HC64-55	55ns	5V ±10%	80mA	40mA	C & I
27HC64-70	70ns	5V ±10%	80mA	40mA	C & I
27HC64L-45	45ns	5V ±10%	80mA	100uA	C
27HC64L-55	55ns	5V ±10%	80mA	100uA	C & I
27HC64L-70	70ns	5V ±10%	80mA	100uA	C & I

*Commercial temperature range

** See 27HC64 Military Data sheet DS60006A

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CMOS Bi-polar PROM Replacement

27HC641

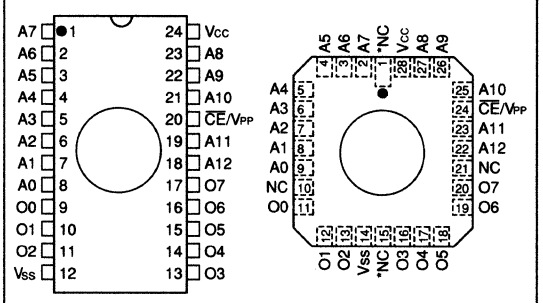
64K (8K x 8) High Speed CMOS UV Erasable PROM

FEATURES

- Bipolar performance
  —45ns maximum access time
- CMOS technology for low power consumption
  —80mA active current
  —100µA standby current (low power option)
- OTP (one time programming) available
- Auto-insertion-compatible plastic packages
- Auto ID™ aids automated programming
- Two programming algorithms allow improved programming times
  —Fast programming
  —Rapid-pulse programming
- Organized 8K x 8: JEDEC standard pinouts
  —24-pin dual-in-line package
  —28-pin chip carrier (leadless or plastic)
- Extended temperature ranges available:
  —Commercial (C) = 0° C to 70° C
  —Industrial (I) = -40° C to 85° C
  —Military** (M) = -55° C to 125° C

PIN CONFIGURATION

Top View



● Pin 1 indicator on PLCC on top of package
* DC (don't connect on PLCC package)

PRODUCT SPECIFICATION GUIDE

PART NUMBER	ACCESS TIME	VCC RANGE	ACTIVE Icc*	STANDBY ICC*	TEMPERATURE RANGE
27HC641-45	45ns	5V ±10%	80mA	40mA	C
27HC641-55	55ns	5V ±10%	80mA	40mA	C & I
27HC641-70	70ns	5V ±10%	80mA	40mA	C & I
27HC641L-45	45ns	5V ±10%	80mA	100uA	C
27HC641L-55	55ns	5V ±10%	80mA	100uA	C & I
27HC641L-70	70ns	5V ±10%	80mA	100uA	C & I

*Commercial temperature range

**See 27HC641 Military Data Sheet DS60007A

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CMOS Bi-polar PROM Replacement

27HC191/27HC291

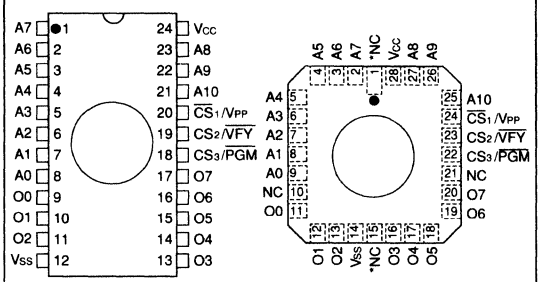
16K (2K x 8) High Speed CMOS UV Erasable PROM

FEATURES

- Bipolar performance
  —35ns maximum access time
- CMOS technology for low power consumption
  —65mA active current
  —100µA standby current (low power option)
- OTP (one time programming) available
- Auto-insertion-compatible plastic packages
- Auto ID™ aids automated programming
- Two programming algorithms allow improved programming times
  —Fast programming
  —Rapid-pulse programming
- Organized 2K x 8: bipolar PROM pinouts
  —24-pin dual-in-line package
  —28-pin chip carrier (leadless or plastic)
- Extended temperature ranges available:
  —Commercial (C) = 0° C to 70° C
  —Industrial (I) = -40° C to 85° C
  —Military** (M) = -55° C to 125° C

PIN CONFIGURATION

Top View



●Pin 1 indicator on PLCC on top of package
* DC (don't connect on PLCC package)

PRODUCT SPECIFICATION GUIDE

PART NUMBER	ACCESS TIME	VCC RANGE	ACTIVE Icc*	STANDBY ICC*	TEMPERATURE RANGE
27HC191-35 27HC291-35	35ns	5V ±10%	65mA	35mA	C
27HC191-45 27HC291-45	45ns	5V ±10%	65mA	35mA	C & I
27HC191-55 27HC291-55	55ns	5V ±10%	65mA	35mA	C & I
27HC191L-35 27HC291L-35	35ns	5V ±10%	65mA	100uA	C
27HC191L-45 27HC291L-45	45ns	5V ±10%	65mA	100uA	C & I
27HC191L-55 27HC291L-55	55ns	5V ±10%	65mA	100uA	C & I

*Commercial temperature range

**See 27HC191/27HC291 Military Data Sheet DS60008A

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Microchip

Very High Speed EPROM

27HC256

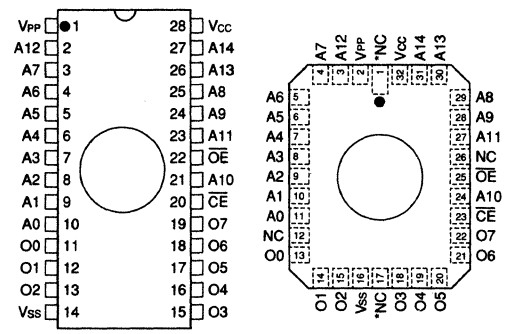
256K (32K x 8) High Speed CMOS UV Erasable PROM

FEATURES

- High speed performance
  —55ns maximum access time
- CMOS technology for low power consumption
  —65mA active current
  —100μA standby current (low power option)
- OTP (one time programming) available
- Auto-insertion-compatible plastic packages
- Auto ID™ aids automated programming
- Two programming algorithms allow improved programming times
  —Fast programming
  —Rapid-pulse programming
- Organized 32K x 8: JEDEC standard pinouts
  —28-pin dual-in-line package
  —32-pin chip carrier (leadless or plastic)
- Extended temperature ranges available:
  —Commercial (C) = 0° C to 70° C
  —Industrial (I) = -40° C to 85° C
  —Military** (M) = -55° C to 125° C

PIN CONFIGURATION

Top View



●Pin 1 indicator on PLCC on top of package

* DC (don't connect on PLCC package)

PRODUCT SPECIFICATION GUIDE

PART NUMBER	ACCESS TIME	VCC RANGE	ACTIVE Icc*	STANDBY ICC*	TEMPERATURE RANGE
27HC256-55	55ns	5V ±10%	65mA	35mA	C
27HC256-70	70ns	5V ±10%	65mA	35mA	C & I
27HC256-90	90ns	5V ±10%	65mA	35mA	C & I
27HC256L-55	55ns	5V ±10%	65mA	100uA	C
27HC256L-70	70ns	5V ±10%	65mA	100uA	C & I
27HC256L-90	90ns	5V ±10%	65mA	100uA	C & I

*Commercial temperature range

**See 27HC256 Military Data Sheet DS60009A

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CMOS EPROM

27C64

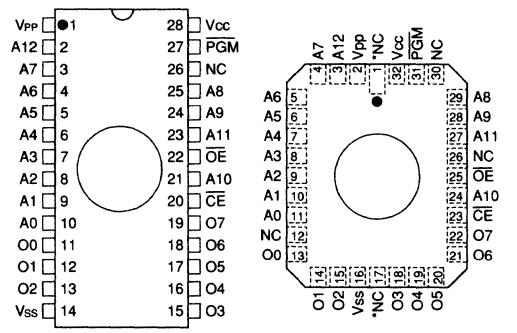
64K (8K x 8) CMOS UV Erasable PROM

FEATURES

- High speed performance
  —120ns maximum access time
- CMOS technology for low power consumption
  —20mA active current
  —100μA standby current
- OTP (one time programming) available
- Auto-insertion-compatible plastic packages
- Auto ID™ aids automated programming
- Seperate chip enable and output enable controls
- Two programming algorithms allow improved programming times
  —Fast programming
  —Rapid-pulse programming
- Organized 8K x 8: JEDEC standard pinouts
  —28-pin dual-in-line package
  —32-pin chip carrier (leadless or plastic)
- Extended temperature ranges available:
  —Commercial (C) = 0° C to 70° C
  —Industrial (I) = -40° C to 85° C
  —Military** (M) = -55° C to 125° C

PIN CONFIGURATION

Top View



●Pin 1 indicator on PLCC on top of package

* DC (don't connect on PLCC package)

PRODUCT SPECIFICATION GUIDE

PART NUMBER	ACCESS TIME	VCC RANGE	ACTIVE Icc*	STANDBY ICC*	TEMPERATURE RANGE
27C64-12	120ns	5V ±10%	20mA	100μA	C
27C64-15	150ns	5V ±10%	20mA	100μA	C & I
27C64-17	170ns	5V ±10%	20mA	100μA	C & I
27C64-20	200ns	5V ±10%	20mA	100uA	C & I
27C64-25	250ns	5V ±10%	20mA	100uA	C & I

*Commercial temperature range

** See 27C64 Military Data sheet DS60011

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CMOS EPROM

27C128

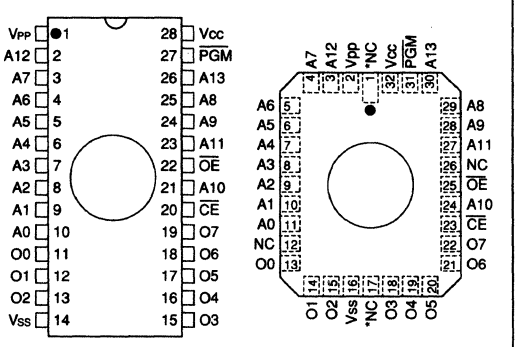
128K (16K x 8) CMOS UV Erasable PROM

FEATURES

- High speed performance
  —120ns maximum access time
- CMOS technology for low power consumption
  —20mA active current
  —100µA standby current
- OTP (one time programming) available
- Auto-insertion-compatible plastic packages
- Auto ID™ aids automated programming
- Seperate chip enable and output enable controls
- Two programming algorithms allow improved programming times
  —Fast programming
  —Rapid-pulse programming
- Organized 16K x 8: JEDEC standard pinouts
  —28-pin dual-in-line package
  —32-pin chip carrier (leadless or plastic)
- Extended temperature ranges available:
  —Commercial (C) = 0° C to 70° C
  —Industrial (I) = -40° C to 85° C
  —Military** (M) = -55° C to 125° C

PIN CONFIGURATION

Top View



●Pin 1 indicator on PLCC on top of package

* DC (don't connect on PLCC package)

PRODUCT SPECIFICATION GUIDE

PART NUMBER	ACCESS TIME	VCC RANGE	ACTIVE Icc*	STANDBY ICC*	TEMPERATURE RANGE
27C128-12	120ns	5V ±10%	20mA	100µA	C
27C128-15	150ns	5V ±10%	20mA	100µA	C & I
27C128-17	170ns	5V ±10%	20mA	100µA	C & I
27C128-20	200ns	5V ±10%	20mA	100uA	C & I
27C128-25	250ns	5V ±10%	20mA	100uA	C & I

*Commercial temperature range

** See 27C128 Military Data sheet DS60012

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Microchip

CMOS EPROM

27C256

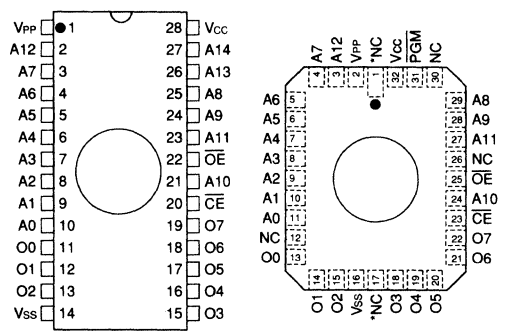
256K (32K x 8) CMOS UV Erasable PROM

FEATURES

- High speed performance
  —150ns maximum access time
- CMOS technology for low power consumption
  —20mA active current
  —100µA standby current
- OTP (one time programming) available
- Auto-insertion-compatible plastic packages
- Auto ID™ aids automated programming
- Seperate chip enable and output enable controls
- Two programming algorithms allow improved programming times
  —Fast programming
  —Rapid-pulse programming
- Organized 32K x 8: JEDEC standard pinouts
  —28-pin dual-in-line package
  —32-pin chip carrier (leadless or plastic)
- Extended temperature ranges available:
  —Commercial (C) = 0° C to 70° C
  —Industrial (I) = -40° C to 85° C
  —Military** (M) = -55° C to 125° C

PIN CONFIGURATION

Top View



●Pin 1 indicator on PLCC on top of package

* DC (don't connect on PLCC package)

PRODUCT SPECIFICATION GUIDE

PART NUMBER	ACCESS TIME	VCC RANGE	ACTIVE Icc*	STANDBY ICC*	TEMPERATURE RANGE
27C256-15	150ns	5V ±10%	20mA	100µA	C & I
27C256-17	170ns	5V ±10%	20mA	100µA	C & I
27C256-20	200ns	5V ±10%	20mA	100µA	C & I
27C256-25	250ns	5V ±10%	20mA	100uA	C & I

*Commercial temperature range

** See 27C256 Military Data sheet DS60013

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CMOS EPROM

27C512

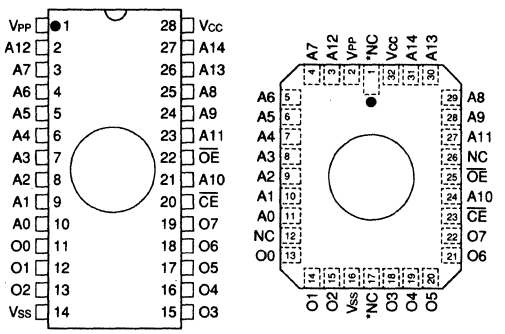
512K (64K x 8) CMOS UV Erasable PROM

FEATURES

- High speed performance
  —120ns maximum access time
- CMOS technology for low power consumption
  —40mA active current
  —100μA standby current
- OTP (one time programming) available
- Auto-insertion-compatible plastic packages
- Auto ID™ aids automated programming
- Two programming algorithms allow improved programming times
  —Fast programming
  —Rapid-pulse programming
- Organized 64K x 8: JEDEC standard pinouts
  —28-pin dual-in-line package
  —32-pin chip carrier (leadless or plastic)
- Extended temperature ranges available:
  —Commercial (C) = 0° C to 70° C
  —Industrial (I) = -40° C to 85° C
  —Military** (M) = -55° C to 125° C

PIN CONFIGURATION

Top View



●Pin 1 indicator on PLCC on top of package

* DC (don't connect on PLCC package)

PRODUCT SPECIFICATION GUIDE

PART NUMBER	ACCESS TIME	VCC RANGE	ACTIVE Icc*	STANDBY ICC*	TEMPERATURE RANGE
27C512-12	120ns	5V ±10%	40mA	100μA	C
27C512-15	150ns	5V ±10%	40mA	100μA	C & I
27C512-17	170ns	5V ±10%	40mA	100μA	C & I
27C512-20	200ns	5V ±10%	40mA	100uA	C & I
27C512-25	250ns	5V ±10%	40mA	100uA	C & I

*Commercial temperature range

**See 27C512 Military Data Sheet DS60014

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CMOS EPROM

28C04A

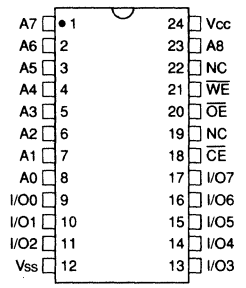
4K (512 x 8) CMOS Electrically Erasable PROM

FEATURES

- Fast read access time—150ns maximum
- CMOS technology for low power dissipation
  - —30mA active
  - —100µA standby
- Fast byte write time—200µs or 1ms
- Data retention >10 years
- High endurance 10^4 erase/write cycles
- Automatic write operation
  - —Internal control timer
  - —Auto-clear before write operation
  - —On-chip address and data latches
- Data polling
- Chip clear operation
- Enhanced data protection
  - —Vcc detector
  - —Power-up timer
- 5-volt-only operation
- Organized 512 x 8: JEDEC standard pinout
  - —24-pin dual-in-line package
- Available for extended temperature ranges:
  - —Commercial (C) = 0° C to 70° C
  - —Industrial (I) = -40° C to 85° C

PIN CONFIGURATION

Top View



PRODUCT SPECIFICATION GUIDE

PART NUMBER	READ ACCESS	WRITE CYCLE	VCC RANGE	ACTIVE Icc*	STANDBY ICC*	TEMPERATURE RANGE
28C04A-15	150ns	200µs/1ms	5V ±10%	30mA	100µA	C & I
28C04A-20	200ns	1ms	5V ±10%	30mA	100µA	C & I
28C04A-25	250ns	1ms	5V ±10%	30mA	100µA	C & I

*Commercial temperature range

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CMOS EPROM

28C16A

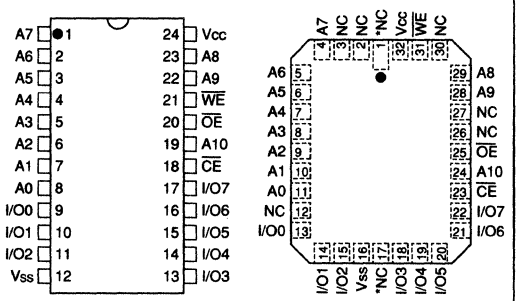
16K (2K x 8) CMOS Electrically Erasable PROM

FEATURES

- Fast read access time—150ns maximum
- CMOS technology for low power dissipation
  —30mA active
  —100μA standby
- Fast byte write time—200μs or 1ms
- Data retention >10 years
- High endurance 10^4 erase/write cycles
- Automatic write operation
  —Internal control timer
  —Auto-clear before write operation
  —On-chip address and data latches
- Data polling
- Chip clear operation
- Enhanced data protection
  —Vcc detector
  —Power-up timer
- 5-volt-only operation
- Organized 2K x 8: JEDEC standard pinout
  —24-pin dual-in-line package
  —32-pin chip carrier (leadless of plastic)
- Available for extended temperature ranges:
  —Commercial (C) = 0° C to 70° C
  —Industrial (I) = -40° C to 85° C

PIN CONFIGURATION

Top View



●Pin 1 indicator on PLCC on top of package

* DC (Don't connect to PLCC package.)

PRODUCT SPECIFICATION GUIDE

PART NUMBER	READ ACCESS	WRITE CYCLE	VCC RANGE	ACTIVE Icc	STANDBY ICC	TEMPERATURE RANGE
28C16A-15	150ns	200μs/1ms	5V ±10%	30mA	100μA	C & I
28C16A-20	200ns	1ms	5V ±10%	30mA	100μA	C & I
28C16A-25	250ns	1ms	5V ±10%	30mA	100μA	C & I

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CMOS EPROM

28C17A

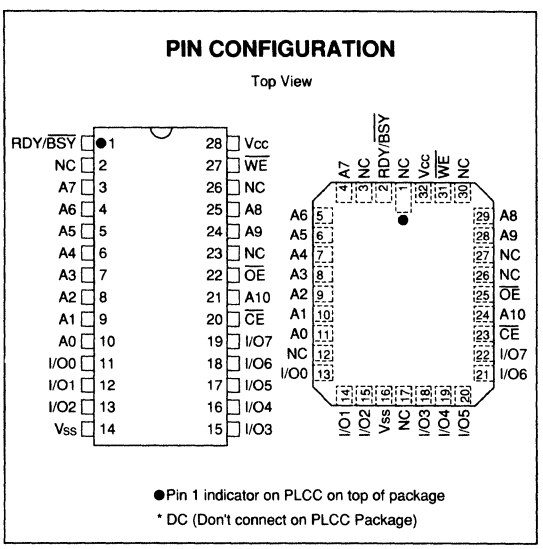
16K (2K x 8) CMOS Electrically Erasable PROM

FEATURES

- Fast read access time—150ns maximum
- CMOS technology for low power dissipation
  - —30mA active
  - —100µA standby
- Fast byte write time—200µs or 1ms
- Data retention >10 years
- High endurance 10^4 erase/write cycles
- Automatic write operation
  - —Internal control timer
  - —Auto-clear before write operation
  - —On-chip address and data latches
- Data polling
- Ready/busy
- Chip clear operation
- Enhanced data protection
  - —Vcc detector
  - —Power-up timer
- 5-volt-only operation
- Organized 2K x 8: JEDEC standard pinout
  - —28-pin dual-in-line package
  - —32-pin chip carrier (leadless of plastic)
- Available for extended temperature ranges:
  - —Commercial (C) = 0° C to 70° C
  - —Industrial (I) = -40° C to 85° C

PIN CONFIGURATION

Top View



●Pin 1 indicator on PLCC on top of package

* DC (Don't connect on PLCC Package)

PRODUCT SPECIFICATION GUIDE

PART NUMBER	READ ACCESS	WRITE CYCLE	VCC RANGE	ACTIVE Icc	STANDBY ICC	TEMPERATURE RANGE
28C17A-15	150ns	200µs/1ms	5V ±10%	30mA	100µA	C & I
28C17A-20	200ns	1ms	5V ±10%	30mA	100µA	C & I
28C17A-25	250ns	1ms	5V ±10%	30mA	100µA	C & I

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CMOS EPROM

28C64A

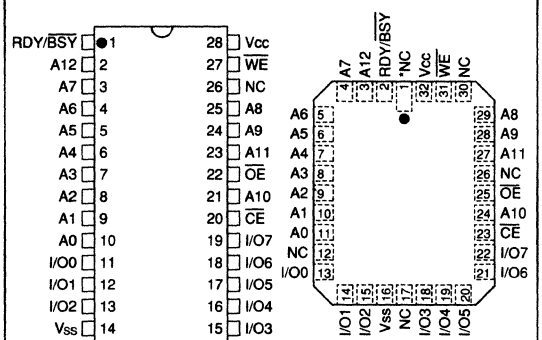
64K (8K x 8) CMOS Electrically Erasable PROM

FEATURES

- Fast read access time—150ns maximum
- CMOS technology for low power dissipation
  - —30mA active
  - —100µA standby
- Fast byte write time—200µs or 1ms
- Data retention >10 years
- High endurance 10^4 erase/write cycles
- Automatic write operation
  - —Internal control timer
  - —Auto-clear before write operation
  - —On-chip address and data latches
- Data polling
- Ready/busy
- Chip clear operation
- Enhanced data protection
  - —Vcc detector
  - —Power-up timer
- 5-volt-only operation
- Organized 8K x 8: JEDEC standard pinout
  - —28-pin dual-in-line package
  - —32-pin chip carrier (leadless of plastic)
- Available for extended temperature ranges:
  - —Commercial (C) = 0° C to 70° C
  - —Industrial (I) = -40° C to 85° C
  - —Military** (M) = -55° C to 125° C

PIN CONFIGURATION

Top View



●Pin 1 indicator on PLCC on top of package

* DC (Don't connect on PLCC package)

PRODUCT SPECIFICATION GUIDE

PART NUMBER	READ ACCESS	WRITE CYCLE	VCC RANGE	ACTIVE Icc	STANDBY ICC	TEMPERATURE RANGE
28C64A-15	150ns	200µs/1ms	5V ±10%	30mA	100µA	C & I
28C64A-20	200ns	1ms	5V ±10%	30mA	100µA	C & I
28C64A-25	250ns	1ms	5V ±10%	30mA	100µA	C & I

** See Military Data Sheet DS60003A

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Microchip

COB654XXXX

Envoy™ COB Memory Cards

DESCRIPTION

The Microchip Technology Inc COB654XXXX comprises a family of nonvolatile CMOS memory IC Envoy™ cards available in EEPROM, EPROM and ROM technologies. They are mounted using Chip-On-Board (COB) technology and packaged in credit card size ABS plastic. These versatile devices provide users with a ready-made portable medium for software storage and are ideally suited for end systems requiring add-on or replacement memory.

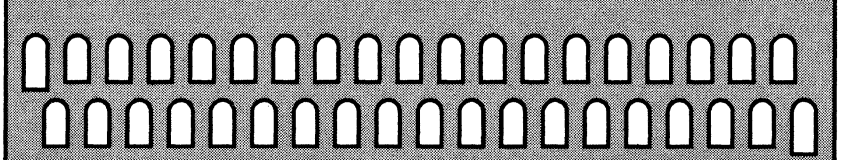
Envoy™ accessories include: 38Q-V/38Q-H 38-pin vertical or horizontal connectors, a gang programmer, AC101 programming adapter, EV101 evaluation kit and RW250 development kits.

FEATURES - EPROM & EEPROM

- 8-bit organization (EPROM/EEPROM)
- 256-bit serial EEPROM available
- 200ns and 250ns access times (EPROM)
- 150ns and 250ns access times (EEPROM)
- Inputs and outputs TTL compatible
- OTP (on-time-programmabe) available
- Auto ID™ aids automated programming
- Separate chip enable and output enable
- Rapid-pulse programming algorithm(EPROM)
- Fast byte-write time—200µs or 1ms (EEPROM)
- Overall dimensions: 3.37" wide x 2.16" high x .074" thick
- 0° C to 70° C

PRODUCT GUIDE

Device Type	Part Number	Density
EPROM	COB654128E	128K
EPROM	COB654C256E	256K
EPROM	COB654512E	512K
EPROM	COB654512X2E	1024K
EEPROM	COB654256B	256bit
EEPROM	COB65464AEE	64K



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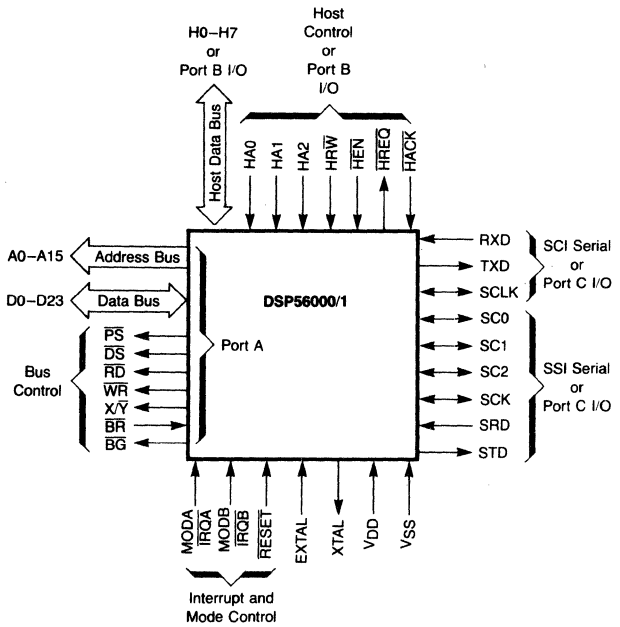
Digital Signal Processing

The DSP56000 and DSP56001 Digital Signal Processors Set The Pace



With a run rate of 10.25 million instructions per second, coupled with significant advances in chip architecture, the HCMOS DSP56000 Family offers unmatched performance in digital signal processing. The chip architecture combines 24 x 24-bit multiplication and 56-bit accumulation with two parallel data moves in a single 97.5 ns instruction cycle. Four data buses and three address buses make this throughput-enhancing parallelism possible. In fact, many of the critical DSP benchmarks (see table above) run at their theoretical maximum on this processor.

The core of the DSP56000/1 consists of three single-cycle execution units — the Data ALU, the Address Arithmetic Unit, and the Program Controller — which operate in parallel at speeds up to 10 MHz. X data, Y data and Program data memories are provided on-chip, and each is expandable off-chip so that a total of 192K words of 24-bit data can be addressed. The I/O is flexible, with two serial ports and a parallel Host port being implemented on the chip.

An MPU-like instruction set, together with a user-friendly cross assembler and simulator which run on an IBM personal computer, Macintosh II system, VAX and Sun work station, simplify algorithm development and programming. The DSP56000CLASA software package permits immediate implementation of system design, including code generation and debugging, even prior to hardware availability. The DSP56KCC C Compiler offers high-level language support.

The DSP56000 has on-chip factory-programmable Data and Program ROMs. The DSP56001 is a RAM-based version of the DSP56000 that also includes preprogrammed Data ROM. The DSP56001, therefore, is user programmable for immediate implementation. In this version, the preprogrammed Data ROMs contain MU-Law and A-Law tables and sine-wave generation tables.

DSP56000/1 Benchmarks

Benchmark	Execution Time
Finite-Impulse Response Filter with Data Shift	0.1 μs per Tap
Infinite-Impulse Response Biquadratic Filter	0.4 μs
64-Point Complex Fast Fourier Transform	0.147 ms
256-Point Complex Fast Fourier Transform	0.713 ms
1024-Point Complex Fast Fourier Transform	5 ms

Core Features

- 10.25 Million Instructions Per Second (MIPS)
- Single Cycle Data ALU
  - — 24 x 24 → 56-Bit Parallel Multiply/Accumulate
  - — Two 56-Bit Accumulators
  - — Ten Data Registers
  - — Two Data Bus Shifter/Limiters
- DSP Oriented Address ALU
  - — 24 Address Registers
  - — Dual Modulo Arithmetic Units
  - — Linear, Modulo, and Bit Reversed Address Generation
- Advanced Program Controller
  - — 15 Level Hardware Stack
  - — Nested Hardware DO Loops
  - — No Overhead Auto-Return Fast Interrupts
- Highly Orthogonal Instruction Set
  - — 62 MPU-Style Instruction Types
  - — Makes Pipeline Invisible
  - — Suitable for High Level Language (HLL) Compilers
- Multiple Buses
  - — Four Data Buses
  - — Three Address Buses

On-Chip MCU-Style Peripherals

- 24 Programmable I/O Port Pins or a Combination of I/O Port Pins and
  - — 8-Bit Parallel Host MPU/DMA Interface
  - — Serial Communication Interface with Baud Rate Generator/Timer
  - — Synchronous Serial (Codec) Interface with Clock Generator

On-Chip Memory

- Two Independent 256 x 24-Bit Data RAMs
- Two Independent 256 x 24-Bit Data ROMs (DSP56000)
- 2K x 24-Bit Program ROM (DSP56000)
- Two Independent Preprogrammed Data ROMs (DSP56001)
- 512 x 24-Bit Program RAM (DSP56001)

Off-Chip Memory Expansion

- 128K x 24-Bit Data Memory
- 64K x 24-Bit Program Memory
- Programmable Off-Chip Access Times (Wait States)

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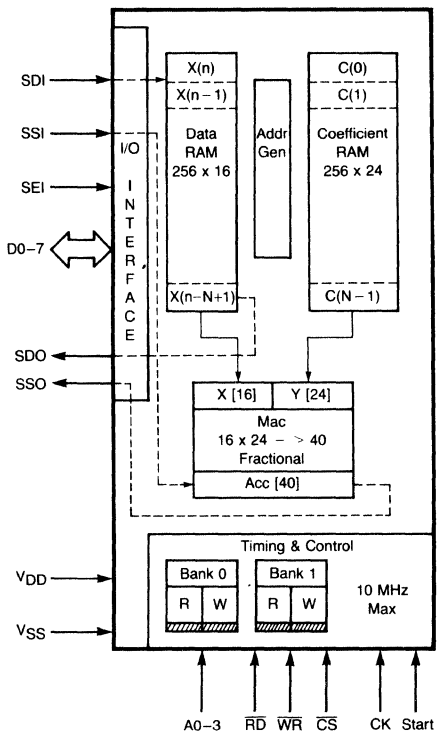
The CAFIR Filter, DSP56200

an Algorithm Specific DSP Peripheral

Features

- Low Power HCMOS
- 28 pins
- 100 ns per Tap Throughput
- 256 x 16-Bit Data RAM
- 256 x 24-Bit Coefficient RAM
- 16 x 24-Bit Multiplier, 40-Bit Accumulation
- Two FIR Modes:
  - — Single Channel
  - — Dual Channel
- Single Channel Adaptive FIR Mode
  - — Uses the Least-Mean-Squared (LMS) Coefficient Update Algorithm
- Programmable Tap Lengths Up to:
  - — 256 Taps in Single Channel Mode
  - — 128 Taps per Channel in Dual Mode
- Cascadable in Single Channel Mode
  - — Higher Sampling Frequencies
  - — Sharper Filters
  - — Longer Echoes Cancelled
- Programmable Leakage
  - — Adapting to Narrow Band Signals
- Programmable Gain
  - — Changing the Rate of Adaptation
- 8-Bit I/O Port with 7 Control Lines
- DC Tap Option
- Scratch Pad Memory
  - — Unused Data and Coefficient Memory is Available
- Power Down Mode

DSP56200



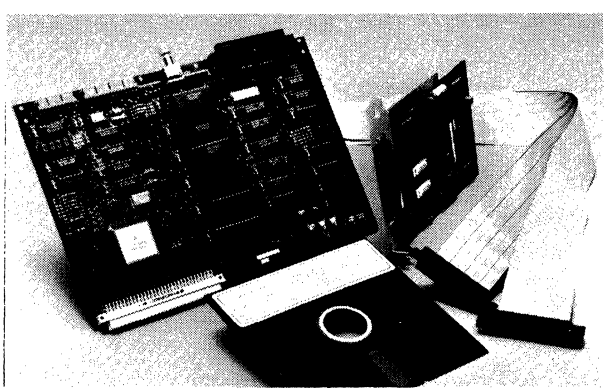
The DSP56200 Cascadable Adaptive Finite Impulse Response (CAFIR) Digital Filter is an algorithm-specific DSP peripheral chip capable of implementing two algorithms — the convolution sum and the least-mean-square (LMS) algorithm for updating coefficients — the CAFIR Filter is useful as a general-purpose linear phase filter and in applications requiring an adaptive filter, such as echo cancelling.

DSP56000ADS Development System

The DSP56000 family is Motorola's entry into the Digital Signal Processor arena. It represents one of the latest and certainly one of the most powerful signal processing capabilities, and to simplify its implementation Motorola now offers the DSP56000ADS Applications Development System.

The DSP56000ADS is a three-component development tool for designing, debugging, and evaluating DSP56000 and DSP56001 target systems. It simplifies evaluation of the user's prototype hardware/software product by making all of the essential DSP56000 timing and I/O circuitry easily accessible.

The three ADS components are an Application Development Module (ADM) board, an IBM PC bus interface board, and a MS-DOS based user interface program that runs on the IBM PC and interacts with the user, controlling as many as eight ADMs simultaneously. Using a low cost IBM PC or Macintosh II personal computer as a medium between the user and the DSP56000 hardware significantly decreases the overall hardware complexity and cost of development while increasing the capabilities of the system. With this system, DSP programs may be executed real-time, single instruction traced, or multiple instruction stepped with registers and/or memory block contents displayed.



Features:

- **Full speed operation at 20.48 MHz**
- **Single/multiple stepping through DSP56000 object programs**
- **Conditional or unconditional breakpoints**
- **Program patching using a single-line assembler/disassembler**
- **Session and/or command logging for later reference**
- **Loading and saving of files to/from ADM memory**
- **Macro command definition and execution**
- **Display enable/disable of registers and memory**
- **Debug commands that support multiple ADM development**
- **Hexadecimal/decimal/binary calculator**

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DSP56000/1 Software

DSP56000CLASx Simulator Package

This Simulator/Macro-Assembler/Linker/Librarian software package is a development system support tool. The simulator program simulates the operation of the DSP56000 on a clock-cycle by clock-cycle basis and gives an accurate measurement of code execution time. All on-chip peripheral operations, memory and register updates, and exception processing activities are simulated exactly.

The full-featured Macro Cross Assembler translates one or more source files containing instruction mnemonics, operands and assembler directives into an object file which is directly loadable by the Simulator. It supports the full instruction set, memory spaces and parallel transfer fields of the DSP56000.

The package is an upgrade of the earlier DSP56000SASM, adding the Linker/Librarian, a multiprocessor simulator, and a macro-assembler that produces relocatable code to the former package. Registered users of the preceding package may purchase the upgrade at a reduced price.

The DSP56000CLAS software is available for the following host stations:

Host	Operating System	Part Number
IBM-PC	DOS 2.X, 3.X	DSP56000CLASA
Macintosh II	MAC OS 4.1	DSP56000CLASB
Sun-3	UNIX BSD 4.2	DSP56000CLASC
VAX	VMS 4.X	DSP56000CLASD
VAX	UNIX BSD 4.2	DSP56000CLASE

The upgrade version may be ordered by adding a suffix "U" to the original part number (i.e., DSP56000SASMxU).

The DSP56KCCx C-Compiler Package

A full Kernighan and Ritchie C implementation, this compiler provides high efficiency, with compiler overhead as low as 20%. It has full in-line code capability and a C-language preprocessor supporting MACRO expansion, file inclusion and conditional compilation. It allows programmers to perform the entire compilation process in a single step. The package includes the C Compiler, a Macro Cross Assembler program and a Linker/Librarian, as well as all applicable user and reference manuals. For the various host computers, the software package is available as follows:

Host	Operating System	Part Number
IBM-PC	DOS 2.X, 3.X	DSP56KCCA
Macintosh II	MAC OS 4.1	DSP56KCCB
Sun-3	UNIX BSD 4.2	DSP56KCCC
VAX	VMS 4.X	DSP56KCCD
VAX	UNIX BSD 4.2	DSP56KCCE

DSP320to56001 Package Converts 32010 Code to DSP56000/1

This software package translates 32010 .lod modules to Motorola DSP56000/1 source code.

The converted code may be executed on the DSP56000ADS application development system, or may be executed with the SIM56000 simulator program on an IBM PC or equivalent.

The conversion program runs on an IBM PC under MS-DOS or PC-DOS. The C source code is provided on diskette which the user may modify for 32020 or 320C25 translation. The conversion programs are delivered on one double-sided, double-density 5¼-inch floppy disk and may be run from either a floppy disk drive or hard disk. They require only enough disk space to hold the converted source file.

Minimum hardware requirements for the conversion programs are:

IBM-PC, XT, AT (or Compatible) with 256K bytes of RAM, and one floppy disk drive.

PC-DOS/MS-DOS, V2.0 or later.

The M68000 MPU Family

. . . the upward compatible 8-/16-/32-Bit Microprocessor Family

An MPU For All Functions

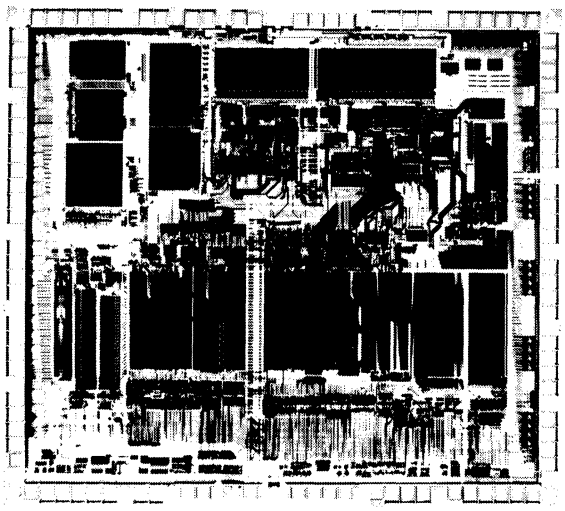
To designers of the most advanced microcomputer systems, the Motorola M68000 Family of microprocessors needs no introduction. Products based on its members have become the standard for systems utilizing the UNIX operating system and for CAD/CAM engineering workstations. They are invading the next generation designs of personal computers and color graphics systems, and they find widespread implementation in multi-user/multi-tasking applications and in small business systems. M68000 MPUs are found in the leading products in fault-tolerant systems requiring high performance and parallel processing, and they are the preferred components for artificial intelligence engines requiring large linear addressing capabilities. Control applications include graphics, numerical controllers, robotics, telecommunications, switching and PBX voice/data transmission.

Upward Compatibility

The M68000 MPU Family consists of a line of processors based on a 32-bit flexible register set, a large linear address space, a simple yet powerful instruction set and flexible addressing modes. The internal architecture of the 8-, 16-, and 32-bit MPU versions, and the common instruction set, provide software compatibility and offer an easy upward migration path for products requiring increasing levels of processing power.

A Host of Peripherals

A large selection of full-function peripheral chips complements the processor family. Compatible LSI and VLSI chips for memory management, data communications, DMA control, network control, system interfacing, general I/O and graphics, all simplify system design and reduce design and manufacturing cost while improving system performance. Then there is a comprehensive assortment of board-level products for modular integration, making Motorola the leading manufacturer of VMEmodules and VMEsystems based on the industry-standard VMEbus.



MC68030 — The Second-Generation 32-Bit MPU

The Compatible Processors

MC68030RC
The Second Generation 32-Bit MPU

The MC68030, oh thirty, sets the highest performance standards ever for 32-bit general-purpose microprocessors by providing up to twice the performance of the industry leading MC68020, oh twenty. The 030 takes 32-bit computing to the next logical step, while maintaining 100% upward software code compatibility with the entire M68000 product family.

The 030 started with a high performance 020 core and added many performance improvement features including increased internal parallelism, dual on-chip caches with a burst fillable mode, dual internal data and address buses, improved bus interface, and on-chip paged memory management unit.

Two independent 32-bit address buses and two 32-bit data buses allow the CPU, caches, MMU, and the bus controller to operate in parallel, so the 030 can, for example, simultaneously access an instruction from the instruction cache, data from the data cache and instruction/data from external memory. These parallel operations result in the highest performance ever.

Performance is further enhanced by on-chip instruction and data caches. Separate 256-byte data and instruction caches reduce the access time and increase CPU throughput by providing data and instructions on-chip.

Overall bus requirements are reduced and multiple processors can run more efficiently thanks to increased bandwidth of the 030 bus, achieved by the enhanced bus controller allowing high speed fills of both data and instruction caches.

The on-chip paged memory management unit translates logical addresses to the corresponding physical addresses in 1/2 the time required by the 020 and MC68851 Paged Memory Management Unit. Pipelining permits this translation to be performed in parallel with other functions so that no translation time is added to any bus cycle.

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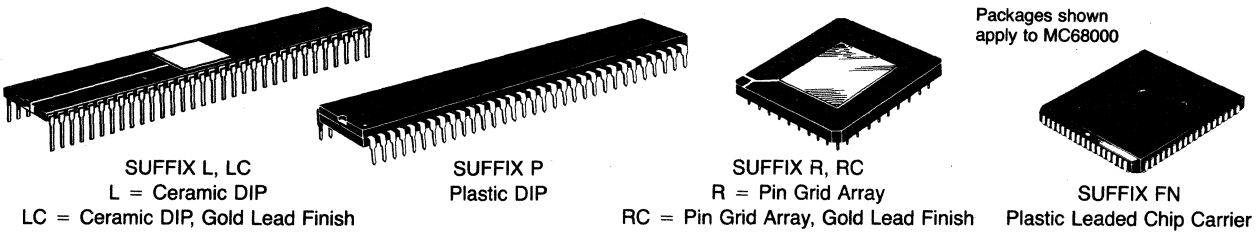

Packages shown apply to MC68000

SUFFIX L, LC
L = Ceramic DIP
LC = Ceramic DIP, Gold Lead Finish

SUFFIX P
Plastic DIP

SUFFIX R, RC
R = Pin Grid Array
RC = Pin Grid Array, Gold Lead Finish

SUFFIX FN
Plastic Leaded Chip Carrier

MC68020RC
The Original 32-Bit Performance Standard

The MC68020, oh twenty, is the industry's leading 32-bit microprocessor because of high performance, architecture, ease of design-in, and long-range compatible growth path.

The 020 has a full 32-bit internal and 32-bit external, regular, symmetrical architecture designed with the customer in mind. It offers all the functionality of the other M68000 Family MPUs, and maintains software user-code compatibility which controls the expense of your product migration.

Programmers appreciate the large general purpose register set, simple yet powerful instruction set and the many flexible M68000 addressing modes. The unique on-chip instruction cache helps provide burst-mode operation to 12.5 MIPS.

The 020 is the proven leader in high performance systems in office automation, engineering workstations, fault tolerant computers, parallel processors, telephone switching systems, and intelligent controllers.

MC68010L,LC,P,R,RC,FN
A Virtual Memory Enhancement

The MC68010 offers the advantage of Virtual Memory. A high-speed loop mode operation executes tight software loops faster to enhance performance. Its instruction continuation feature has made it the choice for fault-tolerant and parallel processing systems. The MC68010 can support a governing operating system which handles the supervisory chores of any number of subordinate operating systems.

MC68HC000L,LC,P,R,RC,FN
A Micropower Alternative

HCMOS design gives the MC68HC000 all the functions and performance of its MC68000 predecessors . . . at one-tenth of the operating power requirements. With a maximum power dissipation of only 0.175 watts, the MC68HC000 is ideal for high-performance computer peripherals, industrial controllers, instrumentation and communications equipment.

MC68000L,LC,P,R,RC,FN
The 16-Bit Foundations

As the first member of the M68000 family, the state-of-the-art technology and advance circuit design concepts of the MC68000 16-bit MPU started a new trend in microprocessor architecture. Its seventeen 32-bit data and address registers permit rapid internal execution of its powerful yet simple instruction set. It is designed for large multiprocessing systems and realtime applications with vectored interrupts, seven priority levels and a 16 megabyte linear addressing space. It offers mainframe-like performance, supporting high-level languages and sophisticated operating systems.

The MC68000 MPU has been joined by more advanced products with even greater capabilities, yet it satisfies a large segment of the existing applications. It is extremely cost competitive and it remains one of the major growth products in the entire MPU line.

MC68008LC,P,FN
An 8-Bit Compatible Competitor

With an 8-bit data bus and 32-bit internal architecture, the MC68008 offers performance that competes with a number of 16-bit MPUs. It has the same register set, same instructions, and the same functionality as the MC68000 with extensive exception processing. Large modular programs can be developed and executed efficiently because of the large, 1-megabit non-segmented, linear address space. It is the choice for high performance, cost effective, 8-bit designs, particularly those requiring a migration path to 16-bit or full 32-bit operation.

MC682881RC
A Floating Point Coprocessor

Designed specifically for arithmetic expansion of the MC68020 MPU, this powerful coprocessor can also be used as a peripheral to all other M68000 family members, and with non-M68000 processors as well. It performs floating point math calculations in strict conformance to a full implementation of the IEEE Standard for Binary Floating Point Arithmetic (754) and, in addition to the basic add, subtract, multiply and divide functions, it handles full selection of transcendental and non-transcendental operations. These operations include root values, trigonometric functions, exponentials, hyperbolics, and logs. All functions are calculated to 80 bits of extended precision in hardware.

MC68882RC
Enhanced Floating Point Coprocessor

The MC68882 is pin-to-pin hardware and software compatible with the MC68881 Floating Point Coprocessor and implements a variety of performance enhancements including dual-ported registers and an advanced pipeline. Additional circuitry allows execution of multiple instructions in parallel for more than twice the Floating Point performance of the trail-blazing MC68881. Where higher performance requirements indicate, the MC68882 is a drop-in replacement for the MC68881.

M68000 Peripherals

Memory Management & DMA Control

MC68851RC
Paged Memory Management Unit, PMMU

The PMMU is a 32-bit memory manager which provides full support for a demand paged virtual environment with the 68010 or MC68020. It supports a 4-gigabyte addressing space when used as a coprocessor with the MC68020. An on-chip address translation cache minimizes translation delays and maximizes system performance.

MC68451L,LC,R,RC
Memory Management Unit, MMU

The MMU is the basic element of a memory management mechanism in an M68000 based system. The MMU provides address translation and protection for the entire 16 megabyte addressing range of the MC68000 microprocessor. It provides 32 segments of variable memory size and allows for multiple MMU capabilities to expand to any number of segments. Virtual memory support is also provided for the MC68010 MPU, as is full support for the UNIX System V/68 Operating System.

MC68450L,LC,R,RC
DMA Controller, DMAC

The DMAC maintains high-performance data movement for complex M68000 MPU-based systems. While pin compatible with the MC68440 DDMA, the DMAC offers four completely independent DMA channels. In addition to all the features of the DDMA, the DMAC also provides very sophisticated manipulation of data through sequential and linked array-chained addressing capabilities.

MC68442R,RC,FN
Expanded Dual DMA, EDDMA

32-bit DDMA for MC68020 based systems. The EDDMA supports up to 4 gigabytes of addressing range, and is pin compatible with the MC68440 and MC68450.

MC68440L,LC,P,R,RC,FN
Dual Direct Memory Access Controller, DDMA

The DDMA complements the performance capabilities of M68000 microprocessors by moving blocks of data in a quick, efficient manner with a minimum of intervention from the MPU. The DDMA performs memory-to-memory, peripheral-to-memory, and memory-to-peripheral transfers through each of two completely independent DMA channels. The DDMA also offers two interrupt vectors per channel and supports both 8-bit and 16-bit data transfers.

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Network Devices

MC68824RC
Token Bus Controller, TBC

The TBC is the industry's first single-chip VLSI device to implement the IEEE 802.4 Media Access Control Sublayer of the ISO Data Link Layer, as specified by General Motors Manufacturing Automation Protocol, MAP. The TBC supports serial data rates of 1, 5, and 10 Mbps and relieves the host processor of the frame formatting and token management functions. For efficient transfer of data frames, to and from memory, the TBC features an on-chip four-channel DMA with bus master capability, a 32-bit address range, an 8- or 16-bit data bus, and a 40-byte FIFO. The MC68824 also offers support options for network bridges, real-time support and network monitoring services.

MC68184L
Broadband Interface Controller, BIC

The BIC, coupled with rf circuitry, makes up a broadband modem needed in each node of a MAP broadband communications network. The MC68184 implements the digital portion of IEEE 802.4 broadband physical layer of the ISO/OSI (International Standards Organization/Open System Interconnect) communication model for standardized multi-vendor data communications networking. The digital portion implemented by the BIC manipulates data and provides control for the rf transmitter and receiver. The BIC supports high-speed data rates up to 10 Mbps using a duo-binary modulation technique. The IEEE 802.4 recommended standard serial interface is used to connect the BIC to the Token Bus Controller (TBC), MC68824, for implementing both layers one and two of the OSI communication model.

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Data Communications

MC68652P
Multi-Protocol Communication Controller, MPCC

The MPCC is a single-channel, serial data communications device that recognizes byte control and bit oriented protocols. Also included within the device is CRC (programmable error detection) circuitry. The MPCC handles data transfers of 8- or 16-bit widths at a maximum 2-Mbit/second rate.

MC68681, MC2681L,P
Dual Universal Asynchronous Receiver/ Transmitter, DUART

The MC68681 features two completely independent full-duplex asynchronous receiver/transmitter channels that interface directly to the M68000 microprocessor bus. Receiver data registers are quadruple buffered and transmitter data registers are double buffered for minimum MPU intervention. Each has its own independently selectable baud rate. Multifunction 6-bit input port and 8-bit output port, a 16-bit programmable counter/timer, interrupt handling capabilities, and a maximum one-megabyte per second transfer rate make the DUART an extremely powerful device for complex data communication applications. Full device functionality with an M68000 bus interface is provided by the MC2681.

MC68605RC
X.25 Protocol Controller, XPC

The XPC implements the 1984 CCITT X.25 Recommendation Data Link Procedure (level 2) LAPB. In addition to handling the lower level communications functions (HDLC framing, CRC generation/checking, and zero insertion/deletion), the XPC also independently handles higher level communications functions (frame sequencing, retransmission, flow control, retries limit and timeout conditions). This allows the host to operate almost totally isolated from the task of ensuring error-free transmission and reception of data.

MC68606RC,FN
Multi-Link LAPD Controller CCITT Q.920/ Q.921, LAPD

The MC68606 Multi-link LAPD (MLAPD) Protocol Controller fully implements CCITT Recommendation Q.920/ Q.921 Link Layer Access Procedure (LAPD) protocol for ISDN networks. The MLAPD is designed to handle both signalling and data links in high-performance ISDN primary rate applications.

This VLSI device provides a cost-effective solution to ISDN link-level processing with simultaneous support for up to 8K logical links. The MC68606 is an intelligent communications protocol controller compatible with AT&T specifications for ISDN devices and features low power consumption and high performance, with an aggregate data rate in excess of 2.048 Mbps.

MC68661P
Enhanced Peripheral Communication Interface, EPCI

The EPCI is a universal synchronous/asynchronous data communications controller that interfaces to the M68000 Family and most other 8- or 16-bit microprocessors. Its receiver and transmitter are double buffered for efficient full- and half-duplex operation. An internal baud rate clock (with various baud rate sets available) eliminates the need for a system clock. The EPCI converts parallel data characters accepted from the microprocessor data bus into transmit-serial data. Simultaneously, the EPCI can convert receive-serial data to parallel data characters for input to the MPU.

General Purpose I/O

MC68230LC,P
Parallel Interface/Timer, PI/T

The PI/T provides versatile double-buffered parallel interfaces and a system-oriented timer for M68000 systems. The parallel interfaces operate either in a unidirectional or bidirectional mode, either 8- or 16-bit wide. The timer is 24 bits with full programmability and a 5-bit prescaler. The PI/T has a complete M68000 bus interface and is fully compatible with the MC68450 DMAC.

MC68901LC,P
Multifunction Peripheral, MFP

The MFP provides basic microcomputer function requirements as a single companion chip to the M68000 Family of Microprocessors. Features provided via a direct M68000 system bus interface include a full-function, single-channel universal serial asynchronous receiver/transmitter (USART) for data communication, an 8-source interrupt controller, eight parallel I/O lines, and four 8-bit timers.

System Interface

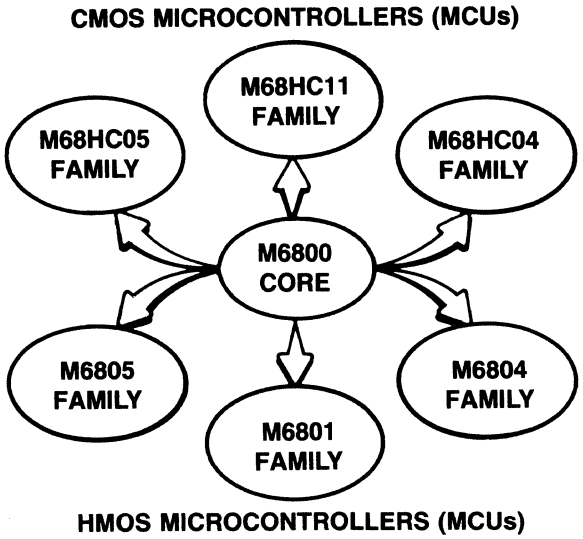
MC68153L,P
Bus Interrupt Module, BIM

The BIM interfaces an M68000 microcomputer system bus to multiple slave devices which require interrupt capabilities. It allows up to four independent sources of interrupt requests to be routed to any of the seven M68000 interrupt levels. The BIM is VMEbus and VERSAbus compatible and fully programmable.

MC68452L,P
Bus Arbitration Module, BAM

The BAM arbitrates the control of an M68000 system bus when multiple bus masters are involved. These bus masters can be processors, DMA controllers, and serial or parallel data communication controllers. Up to eight masters can be handled by each BAM device.

The 8-Bit M6800 Families



Single-Chip Microcontrollers (MCUs)

A Broad Spectrum of Design Solutions

Increased levels of peripheral integration gave rise to the single-chip microcontroller (MCU). Single-chip 8-bit MCUs essentially consist of a basic microprocessor, an on-chip clock oscillator, a timer, user programmable Read-Only Memory (ROM) to handle program routines for a dedicated application, Random Access Memory (RAM) capacity to handle the associated data manipulations, and sufficient input-output capability to interface with a number of parallel and serial oriented external peripherals. These single-chip systems reduce component cost, equipment manufacturing cost, and space requirements.

Motorola MCU families encompass both HCMOS and HMOS technologies. Each family, or core, fills a niche in the price/performance ranges demanded by the vast variety of applications in today's marketplace. Within each family there is the selection of on-chip peripheral functions that most closely fit the requirements of the eventual system.

HCMOS MCU Families

M68HC11, M68HC05, M68HC04

Two of the latest trends in MCU technology are HCMOS processing and on-chip EEPROM. HCMOS (high-speed complementary metal oxide silicon) processing offers several advantages over HMOS (high density NMOS) processing, including lower power consumption, higher throughputs, wider supply voltage ranges, and higher noise immunity.

The M68HC11 Family

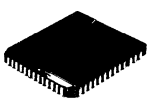
The M68HC11 with on-chip EEPROM is one of the most powerful and most versatile MCU families available in the market today. This family utilizes new high-density CMOS design techniques, and matches the highest nominal bus rate (2.1 MHz) of its fastest HMOS counterpart. Its basic M6800 core was expanded with eleven new instructions that add significant performance improvement without compromising compatibility with other M6800 MPU and peripheral family members.

Among the more significant additions to the instruction set is one that concatenates the two 8-bit accumulators into one double-byte accumulator, permitting 16-bit internal processing with a substantial improvement in throughput. A significant number of instruction enhancements result from the addition of a second 16-bit index register.

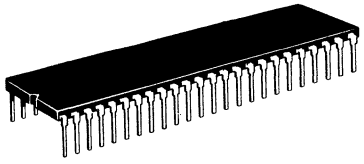
On-chip peripheral capabilities include a full duplex serial communications interface (SCI) with a variety of baud rates, an asynchronous communications interface, a 16-bit free running timer, and 38 I/O lines.

A selection of memory options meets a variety of needs combined with a mix of other functions. This yields cost-effective optimization for specific requirements.

With on-chip EEPROM for nonvolatile storage through power losses, the internal RAM is free for temporary data storage. Calibration tables, data acquisition, software corrections, custom routines, and look-up tables can be programmed into the EEPROM.



52-Lead
PLCC
Case 778
Suffix FN



48-Lead
Plastic
Case 767
Suffix P

Packages shown apply to MC68HC11A8.

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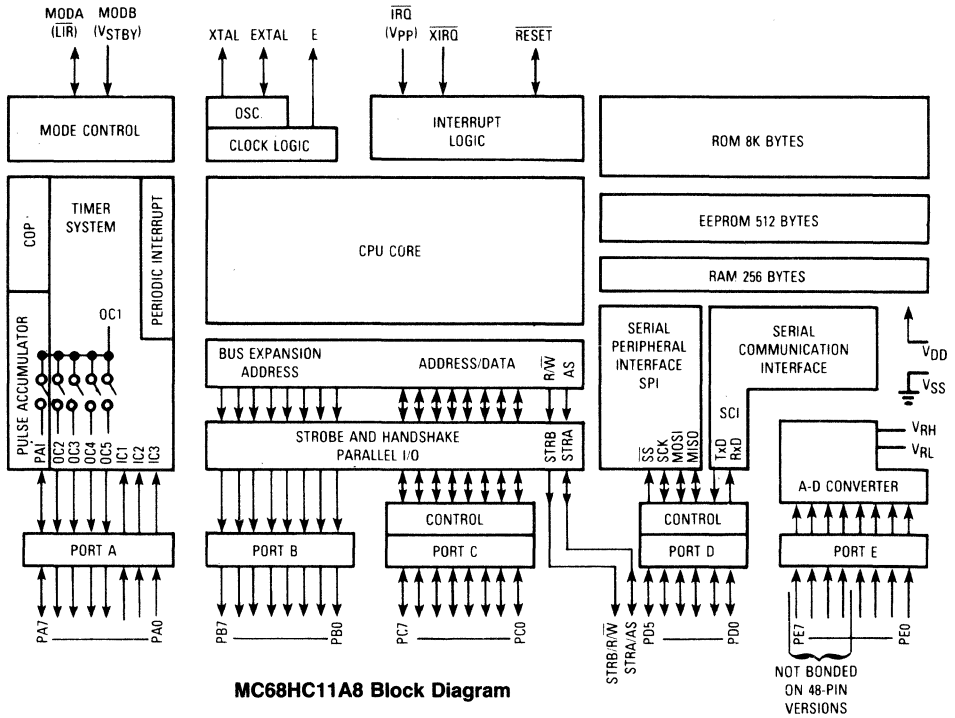

MC68HC11A8 Block Diagram

The M68HC11 Family

	HCMOS MC68HC							
	11A0 FN,P	**11A1 FN,P**	**11A8 FN,P**	**11E1 FN**	**11E9 FN**	**811A2 FN,P**	**99 FN**	**11D3 FN,P**
ROM (Bytes)	0	0	8192	0	12K	0	12K	4K
RAM (Bytes) — All saved during standby	256	256	256	512	512	256	256	128
EEPROM (Bytes)	—	512	512	512	512	2K	—	—
Timer	16-Bit	16-Bit	16-Bit	16-Bit	16-Bit	16-Bit	16-Bit	16-Bit
Serial Peripheral Interface (SPI)	Yes	Yes	Yes	Yes	Yes	Yes	No	Yes
Serial Communications Interface (SCI)	Yes	Yes	Yes	Yes	Yes	Yes	No	Yes
Input Capture Functions	3	3	3	4	4	3	1	2
Output Compare Functions	5	5	5	4	4	5	1	3
A/D Converter	Yes	Yes	Yes	Yes	Yes	Yes	No	No
Real-Time Interrupt	Yes	Yes	Yes	Yes	Yes	Yes	No	Yes
Watchdog (COP)	Yes	Yes	Yes	Yes	Yes	Yes	No	Yes

An M68HC11-Based Hard Disk Controller

The MC68HC99 hard disk controller is a single-chip microcontroller dedicated to disk control. It contains a high speed serial data controller, Reed-Solomon based error detection and correction, two 528 byte data buffers, and a host interface that is completely SCSI compatible. Also on the MC68HC99 are an MC68HC11 microprocessor core, 12K bytes of mask-programmable ROM, 256 bytes of scratchpad RAM, a 16-bit timer, and two 8-bit bidirectional parallel I/O ports (used to select the disk and position the read/write heads). The MC68HC99 replaces the multiple-chip set controller solutions used in current board level and drive embedded controller designs. It interfaces with ST-506, ESDI, and SMD disks and it supports SCSI as well as other popular host computer interfaces. Its command set and functions are user programmable.

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The M68HC05 Family

The M68HC05 Family currently offers the widest variety of on-chip memory and I/O selections to provide users with a system that approximates their "ideal" requirements. This wide selection of functional options in standard, off-the-shelf components, adds the benefits of low cost to highly complex circuits that closely rival the applications-specific advantages of custom designs.

The M68HC05 core brings the high performance and greater chip density of HCMOS to the M6805 single-chip MCU Family. On-chip functions include 176 bytes of RAM, an oscillator with RC or crystal mask options, 24 bidirectional I/O lines, a 16-bit timer, five interrupt vectors, an enhanced UART (SCI), and a synchronous serial system (SPI). The fully static design allows operation down to dc. Stop and wait modes further enhance power savings for ultra low power/ battery applications.

Software capabilities like the 8 x 8 unsigned multiply instruction, true bit manipulation, memory-mapped I/O, and addressing modes with indexed addressing make the M68HC05 core a desirable option for applications between the low cost M68HC04 Family and the highly integrated M68HC11 Family.

The M68HC04 Family

Having somewhat lesser performance than the versatile M68HC05 Family, the M68HC04 Family represents a low-cost means of upgrading earlier 4-bit processor-based equipment to the more powerful world of 8-bit processing. It is ideal for dedicated high volume applications. The objective of minimizing cost led to the development of a self-test scheme in the form of a ROM-driven on-chip signature analysis technique. This attractive alternative to conventional testing utilizes polynomial division to compress lengthy output responses to much smaller results.

The HMOS Families

M6801/M6805/M6804

Today, given equivalent functionality, when low power consumption is not an issue and price is a major consideration, HMOS MCUs may be the best solution for an application. Motorola offers three HMOS MCU families: M6801, M6805, and the M6804.

The M6801 family is manufactured in HMOS providing a high degree of chip complexity with relatively small (low cost) dimensions. On the low end of the scale are the M6803 members intended for use with external ROM or EPROM, with a resultant saving in MPU cost. The 68701 series includes the substitution of EPROM for the more conventional factory-programmed ROM, thereby offering user-programmability.

Based on an M6800 8-bit core, the M6805 Family trims some of the lesser used MC6800 instructions, but includes bit-modify and test instructions as well as powerful indexing modes. The Family consists of a variety of members with various functions ranging from 1 to 3+ K of mask programmable ROM, 64 to 112 bytes of RAM, and on-chip peripherals such as an analog to digital converter and synchronous communication interface. Most part types also offer an EPROM version with the same functions.

The M6804 Family is a low cost line of single-chip microcontrollers designed to be cost competitive with 4-bit machines that are currently on the market, yet the M6804 Family offers more processing power and a streamlined instruction set that is easier to use. A very small die size and an extensive built-in self test written into each chip reduce the cost. A unique application for the M6804, because of its price structure, is to replace TTL logic. That is, the M6804 can perform as an intelligent PLA (programmable logic array). Any time an interface has to be built between some computer and the real world, an M6804 Family device can be a cost effective solution.

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On-Chip I/O

Single-chip MCUs are available in packages ranging in pin configurations from 20 pins to 68 pins. As many as 12 pins are required to serve power and control functions; up to 40 pins in the largest packages may be used as I/O.

Although most digital I/O takes the form of general purpose input/output ports, several of the pins may be used in a number of designs for special serial communications interfaces.

A/D Converters — Members of the M68HC11 and M6805 Families include a multi-channel 8-bit A/D converter. The 6805R and S versions contain four analog input channels and the M68HC11 MCUs feature up to eight channels.

COP — "Computer Operating Properly" reset timer acts as a "watchdog" to automatically reset the CPU if not reset by a program sequence in a given amount of time. All M68HC11 Family members contain this feature.

Interrupts — Every Motorola MCU includes fully automatic interrupts (registers saved). The M68HC11, M6801 and M6805 Families contain programmable vectors for both external pins and internal timers.

SCI (Serial Communications Interface) — The SCI is used for long-range communications, as in data transfer from an MCU to a terminal or modem. This two-line interface is also called a UART (Universal Asynchronous Receiver/Transmitter).

SPI (Serial Peripheral Interface) — The SPI is used primarily for serial communications between chips on the same printed circuit board.

Timers — Timers may generate interrupts to a program at a periodic rate, measure external values, count external events and generate measured output waveforms. The M68HC11, M68HC05, and M6801 Families include a 16-bit timer that may be used to perform three of the above functions simultaneously. The M6804 and M6805 timers consist of a programmable 8-bit counter and a selectable 7-bit prescaler.

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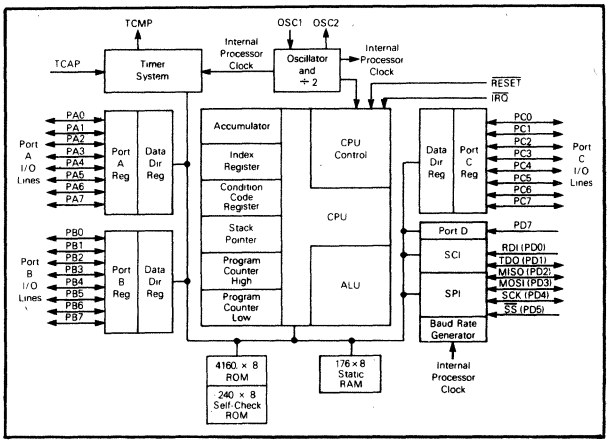
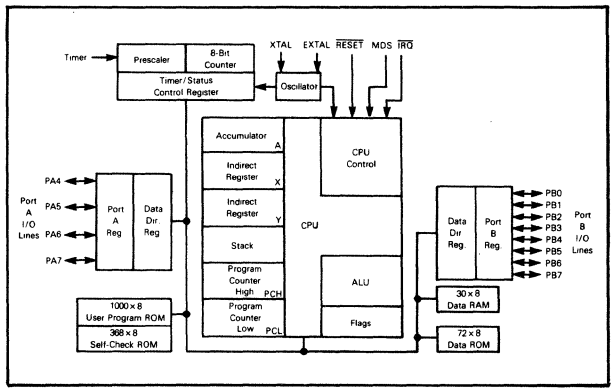


MC68HC05C4 Block Diagram



MC68HC04J2 Block Diagram

The M68HC05 Family (HCMOS)

MC68HC05									
	C2	**C3**	**C4**	**C8**	**A6**	**B4**	**B6**	**L6**	**M4**
ROM	2K	2K	4K	8K	4160	4K	6K	6208	4K
RAM	176	176	176	176	176	176	176	176	128
EEPROM	0	0	0	0	2096	0	256	0	0
Timer	16-Bit	16-Bit	16-Bit	16-Bit	16-Bit	16-Bit	16-Bit	16-Bit	8-Bit 16-Bit
SPI	No	Yes	Yes	Yes	Yes	No	No	Yes	No
SCI	No	Yes	Yes	Yes	Yes	Yes	Yes	No	No
A/D	No	No	No	No	No	Yes	Yes	No	Yes
I/O	24	24	24	24	24	32	32	24	32
PKG	40-DIP	40-DIP	40-DIP 44-PLCC	40-DIP 44-PLCC	40-DIP 44-PLCC	52-PLCC	52-PLCC	68-FPPLCC	
EPROM or EEPROM Version			MC68HC 805C4	MC68HC 705C8			MC68HC 805B6		

The M68HC04 Family (HCMOS)

MC68HC04			
	J2	**J3**	**P3**
ROM	1008	1672	1688
RAM	32	124	124
Timer	8-Bit	8-Bit	8-Bit
I/O	12	12	20

The M6804 Family (HMOS)

MC6804			
	J1	**J2**	**P2**
ROM	512	1008	1024
RAM	32	32	32
Timer	8-Bit	8-Bit	8-Bit
I/O	12	12	20
EPROM Version			MC68 704P2

The M6805 Family (HMOS)

MC6805								
	R2	**R3**	**S2**	**S3**	**U2**	**U3**	**P2**	**P6**
ROM	2048	3776	1480	3720	2048	3776	1110	1804
RAM	64	112	64	104	64	112	64	64
SPI	—	—	Yes	Yes	—	—	—	—
A/D	Yes	Yes	Yes	Yes	—	—	—	—
I/O Bi-directional	24	24	21	14	24	24	20	20
I/O Uni-directional	8	8	7	7	8	8	—	—
PKG	40-DIP	40-DIP	28-DIP	28-DIP	40-DIP	40-DIP	28-DIP	28-DIP
EPROM Version	MC68 705R3	MC68 705R3	MC68 705S3	MC68 705S3	MC68 705U3	MC68 705U3	MC68 705P3	MC68 705P3

The M6801 Family (HMOS)

	MC 6801	**MC 6803**	**MC 6801U4**	**MC 6803U4**
RAM	128	128	192	192
Standby RAM	64	64	64	64
ROM	2048	—	4096	—
Timer	16-Bit	16-Bit	16-Bit	16-Bit
Input Capture Functions	1	1	1	1
Output Compare Functions	1	1	2	2
Serial Comm.	Yes	Yes	Yes	Yes
Parallel I/O	29	13	29	13
EPROM	MC 68701	—	MC 68701U4	—

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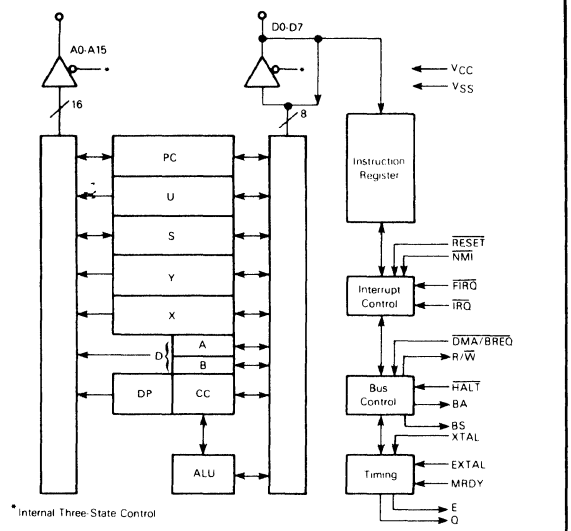
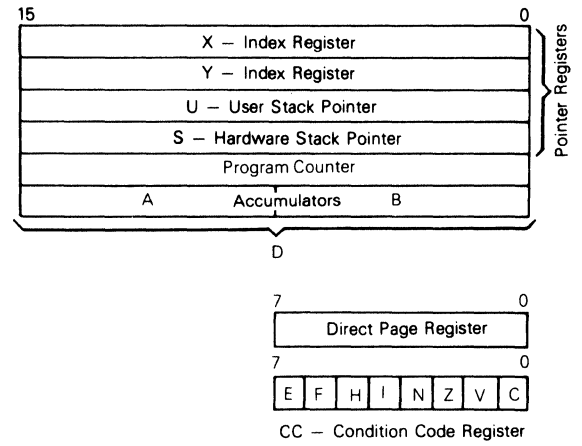


Block Diagram of MC6809 — the most powerful Motorola 8-bit MPU



MC6809 Programming Model

Large-scale integration permits combining a basic microprocessor with a variety of peripheral functions on a single chip. This has led to a series of single-chip MCUs that can represent significant cost savings in many applications. Yet, in some instances, the basic MPU has some advantages:

- Being a non-dedicated device, it can be combined with a number of peripheral chips to provide a nearly ideal circuit configuration;
- Having reached a high degree of maturity, it is cost effective and easy to implement;
- With a long history of utilization, it is supported by a wide selection of peripheral chips that maximizes system flexibility.
- Motorola provides two proven NMOS MPUs and an unexcelled list of peripherals that still bears investigation for new designs where the more elaborate MCUs don't quite fill the bill.

The M6800 Families

M6800/6802

The M6800 Family has earned an enviable reputation as one of the easiest to use lines of microprocessors. The basic M6800 Family consists of:

MC6800 — Basic processor with external clock.

MC6802 — Adds on-chip clock and 128 x 8-bit RAM. Has 32-byte RAM retainability through V_{CC} standby function.

Seventy-two powerful instructions and six different addressing modes give these microprocessors unexcelled capabilities. These capabilities are enhanced by a single 5.0 V supply requirement that reduces system complexity and cost, a 16-bit address system that permits selective addressing of more than 65,000 memory locations, and inherent design that treats each peripheral as a memory location, thereby reducing programming complexity.

MC6809/6809E

Today, there is controversy about where a microcomputer turns into a "mini". While a number of benchmarks have been suggested, it is generally conceded that 16-bit processing capability constitutes a minimum "mini" requirement. From this standpoint alone, the M6809 Family at least borders on minicomputer capabilities.

The M6809 Family has two members:

MC6809 — Processor with on-chip clock.

MC6809E — Has external clock inputs for multi-processor operations.

Both units are available with operating frequencies of 1, 1.5, and 2 MHz; and at operating temperatures of 0 to 70°C and −40 to 85°C.

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8-Bit Peripheral Support

The following list of 8-bit peripherals includes both NMOS and CMOS units that support both the MPU line and selected members of Motorola's MCU families.

Memory and Memory Control

M6800-Compatible Memory — 28 x 8-Bit Static RAM **MCM6810**

Dual-Port RAM Unit — permits two MPUs to exchange data via 256 bytes of RAM. Low-power HCMOS technology **MC68HC34**

Direct Memory Access Controller — bypasses MPU during data transfer between memory and peripherals. . **MC6844**

I/O Peripherals

Real-Time Clock Plus RAM — CMOS for low-power battery operation; includes 50 bytes of CMOS RAM **MC146818,A**

Real-Time Clock plus RAM — with serial interface **MC68HC68T1**

Peripheral Interface Adapter — two I/O ports, each controlling an independent 8-bit data bus **MC6821**

CMOS Parallel Interface — 24 independently programmable I/O lines. **MC146823**

Port Replacement Unit — replaces ports B and C of MC68HC11 MCU when these are unavailable because of expanded or test mode operation **MC68HC24**

Programmable Timer — three 16-bit binary counters **MC6840**

Interface Adapter — operates to IEEE-488 standards. **MC68488**

Asynchronous Communications Interface Adapter — formats serial data to interface with bus-organized systems. **MC6850**

Advanced Data Link Controller — provides serial-to-parallel and parallel-to-serial conversion of data . . . **MC6854**

Synchronous Serial Data Adapter — interfaces between M6800 MPU system and data terminals at speeds up to 600 kbps **MC6852**

Graphics/Display Peripherals

CRT Controller — interfaces between a terminal and an M6800 MPU to simplify the development of intelligent terminals, word processing and information display devices **MC6845**

Video Display Generator — interfaces the M6800 family (or similar product) to a standard color or black and white NTSC television receiver **MC6847**

System Enhancement

Data Security Device — MOS circuit protects data by employment of cryptographic measures. **MC6859**

Serial Peripheral Interface

MPUs and some MCUs can be used in expandable multichip systems using Serial Peripheral Interface. SPI is a simple 2-3 wire interconnect method to allow MPUs, MCUs, and peripherals to communicate with each other, even in multimaster CPU configurations. To satisfy these system requirements, Motorola supplies a broad line of CMOS SPI peripherals.

PLL Frequency Synthesizers — Typical applications include the areas of televisions, CATV, radios, scanners, cordless telephones, and personal computers.

- **MC145155** — Single modulus; ÷ R = 14 stages, ÷ N = 14 stages
- **MC145156** — Dual modulus; ÷ R = 12 stages, ÷ A = 7 stages, ÷ N = 10 stages
- **MC145157** — Single modulus; ÷ R = 14 stages, ÷ N = 14 stages
- **MC145158** — Dual modulus; ÷ R = 14 stages, ÷ A = 7 stages, ÷ N = 10 stages
- **MC145159** — Sample and hold detector, dual modulus; ÷ R = 14 stages, ÷ A = 7 stages, ÷ N = 10 stages

Data Converters — These parts may be applied to instrumentation, automotive uses, industrial controls and home electronics.

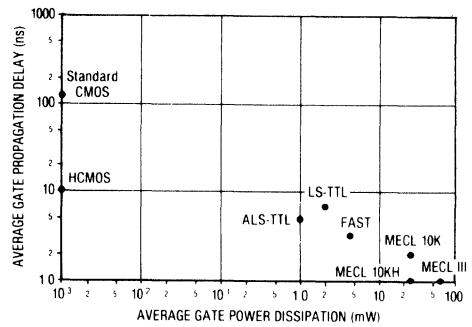
- **MC145040** — ADC; 11 inputs, SAR, external clock
- **MC145041** — ADC; 11 inputs, SAR, internal clock
- **MC144110** — DAC; six 6-bit converters
- **MC144111** — DAC; four 6-bit converters

Display Decoders/Drivers — These products find applications over a wide range of equipments such as automotive dash boards, home computers, appliances, radios and clocks.

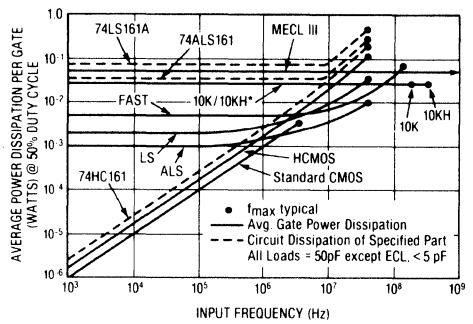
- **MC14499** — 4-digit 7-segment LED driver
- **MC145000** — 48-segment LCD driver (master); multiplexed-by-four
- **MC145001** — 44-segment LCD driver (slave); multiplexed-by-four
- **MC145453** — LCD driver; 33 nonmultiplexed segments (for 4½-digit, 7-segment-plus-decimal display); may be paralleled for more digits.

Standard Logic Families

LSTTL:	SN54/74LS Series	**MECL10K:**	MC10000 Series	**Standard CMOS:**	MC14000 Series
FAST:	MC54/74F Series	**MECL10KH:**	MC10H000 Series	**High-Speed CMOS:**	MC54/74HC Series
		ECLinPS:	MC10E/100E Series	**FACT:**	MC74AC(T) Series
		MECL III:	MC1600 Series		



Graph 1 — General Comparison of Speed/ Power Characteristics



Graph 2 — Variations in Power Dissipation as a Function of Operating Frequency

The variety of established and newly introduced logic families challenges the system designer with choosing the best available technology for each design. Each family offers distinct advantages and limitations.

The three most often used characteristics for determining family selection are propagation delay, operating frequency, and power consumption. For Motorola logic families, these characteristics are displayed and compared in the graphs above.

Technical Comparisons

Schottky TTL

Since its introduction, TTL has become the most popular form of digital logic. It has evolved from the original gold-doped saturated 7400 logic, to Schottky-Clamped logic, and finally to the modern advanced families of TTL logic. The popularity of these TTL families stems from their ease of use, low cost, medium-to-high speed operation, and good output drive capability.

Motorola offers two modern TTL logic families — LS and FAST*. They are pin and functionally compatible and can easily be combined in a system to achieve maximum performance at minimum cost.

LS (Low Power Schottky) is currently the more popular and commands by far the largest share of the total TTL logic market. It is low-cost and provides moderate performance at low power.

FAST, the state-of-the-art, high-performance TTL family, is growing rapidly and gaining a significant share of the total TTL logic market. FAST offers a 20-to-30 percent improvement in performance over the older Standard Schottky family (74S) with a 75-to-80 percent reduction in power. When compared with the Advanced Schottky family (74AS), FAST offers nearly equal performance at a 25-to-50 percent savings in power.

FAST is manufactured on Motorola's MOSAIC (oxide-isolated) process. This process provides FAST with inherent speed/power advantages over the older junction-isolated 74S and 74LS families, allowing the FAST family to be designed and specified with improved noise margins, reduced input currents, and superior line driving capabilities. Additionally, FAST designs incorporate power-down circuitry on all three-state outputs, and buffered outputs on all storage devices.

Two further advantages of FAST are the load specifications and power supply specifications. FAST ac characteristics are specified at a heavier capacitive load than the earlier families (50 pF versus 15 pF) to more accurately reflect actual in-circuit performance. And Motorola's dc and ac characteristics for FAST are specified over a full 10% supply voltage range — a significant improvement over earlier families (5% for dc, 0% for ac) and a considerable improvement over the prevalent FAST standards covering only a 5% range for both dc and ac.

SPEED/POWER CHARACTERISTICS FOR SCHOTTKY TTL LOGIC
(ALL TYPICAL RATINGS)

Characteristic	Symbol	LS	FAST	Units
Quiescent Supply Current/Gate	I_G	0.4	1.1	mA
Power/Gate (Quiescent)	P_G	2.0	5.5	mW
Propagation Delay	t_p	9.0	3.7	ns

Characteristic	Symbol	LS	FAST	Units
Speed Power Product	—	18	19.2	pJ
Clock Frequency (D-F/F)	f_{max}	33	125	MHz
Clock Frequency (Counter)	f_{max}	40	125	MHz

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MECL (ECL)

Motorola's Emitter Coupled Logic (MECL) is a nonsaturating form of digital logic which eliminates transistor storage time as a speed limiting characteristic, permitting very high speed operation.

Motorola offers four versions of MECL: MECL 10K, MECL 10KH, MECL III and the recently introduced ECLinPS (ECL in picoseconds) family.

The *MECL 10K* series has become the industry standard for high-speed applications. In order to make the circuits comparatively easy to use, edge speed was slowed to 2.0 ns while the important propagation delay was held to 2.0 ns. The slow edge speed permits use of wire-wrap and standard printed circuit lines; however, the circuits are specified to drive transmission lines for optimum performance.

The newer *MECL 10KH* family features 100% improvement in propagation delay and clock speeds while maintaining power supply current equal to MECL 10K. This new MECL family is voltage compensated which allows guaranteed dc and switching parameters over a ±5% power supply range. Noise margins of MECL 10KH are 75% better than the MECL 10K series. MECL 10KH is compatible with MECL 10K and MECL III, a key element in allowing users to enhance existing systems by increasing the speed in critical timing areas.

ECLinPS is the latest ECL family to enter the competition and represents a major advance in high-speed logic capabilities. With a gate propagation delay of only 0.33 ns and a flip-flop toggle frequency at least 600 MHz it literally eclipses the performance of the earlier ECL lines while maintaining signal and power-supply compatibility with MECL 10H and with ECL 100K (not manufactured by Motorola).

MECL III, with its 1.0 ns gate propagation delays and greater than 1.0 GHz flip-flop toggle rates, remains the industry speed leader. The 1.0 ns rise and fall times require a transmission line environment for all but the smallest systems. For this reason, all circuit outputs are designed to drive transmission lines and all output logic levels are specified when driving 50-ohm loads. Because of MECL III's fast edge speeds, multi-layer boards are recommended above 200 MHz. MECL III's popularity is with high-speed test and communications equipment.

Speed/power comparisons for Motorola ECL families are as follows:

SPEED/POWER CHARACTERISTICS FOR MECL

(ALL TYPICAL RATINGS)		MECL 10K		MECL/10KH	ECLinPS	MECL III	
Characteristic	**Symbol**	**MC101xx**	**MC102xx**	**MC10H1xx**		**MC16xx**	**Units**
Quiescent Supply Current/Gate	I_G	5.0	5.0	5.0	5.0	10	mA
Power/Gate (Quiescent)	P_G	26	26	26	26	54	mW
Propagation Delay	t_p	2.0	1.5	1.0	0.33	1.1	ns
Speed Power Product	—	52	39	26	8.6	59	pJ
Clock Frequency (D-F/F)	f_{max}	125	200	250	600	550	MHz
Clock Frequency (Counter)	f_{max}	125	—	250	500	1000	MHz

ECLinPS INTRODUCTION SCHEDULE

MC10/ MC100	Function	Features	Output Type	XC Prodn	MC Prodn
E111	1:9 Differential Clock Driver	Low Skew, Enable, V_{BB}	Diff.	Now	3Q88
E142	9-Bit Shift Register, 500 MHz	Async. Reset	SE	Now	3Q88
E155	6-Bit 2:1 Mux-Latch	Common Enable, Reset	SE	Now	3Q88
E167	6-Bit 2:1 Mux-Register	Common CLK, Reset	SE	Now	3Q88
E143	9-Bit Hold Register, 500 MHz	Async. Reset	SE	Now	3Q88
E336	3-Bit Registered Cutoff Bus XCVR	25 Ohm Cutoff Outputs	Diff.	Now	3Q88
E151	6-Bit D Register	Common CLK, Reset	Diff.	Now	3Q88
E158	5-Bit 2:1 Multiplexer	Common Select	Diff.	Now	4Q88
E154	5-Bit 2:1 Mux-Latch	Common Enable, Reset	Diff.	Now	4Q88
E131	4-Bit D Flip-Flop	Individual CLK, Reset	Diff.	Now	4Q88
E171	3-Bit 4:1 Multiplexer	Split Select	Diff.	Now	4Q88
E156	3-Bit 4:1 Mux-Latch	Common Enable, Reset	Diff.	Now	4Q88
E160	12-Bit Parity Generator/Checker	Register — Shiftable	Diff.	3Q88	4Q88
E451	6-Bit D Reg., Diff. Data & CLK Inputs	V_{BB}, Common Reset	SE	3Q88	4Q88

All resets are asynchronous. Diff. = Differential, SE = Single Ended.
XC = Non reliability qualified production. MC = Fully qualified production.
Schedule dates subject to change. Contact sales office for verification.

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CMOS

Complementary MOS (CMOS) technology provides the lowest power consumption logic circuits available.

Motorola currently offers three versions of CMOS logic: Standard (MC14000 Series) CMOS in metal gate technology, High-Speed (HC) CMOS in silicon-gate technology, and the latest sub-two micron (FACT) silicon-gate technology.

Standard CMOS logic is best suited for systems which require low power, medium speed operation. It offers a wide operating voltage range (3 to 18 V) and the highest noise immunity of any logic family. Standard CMOS circuits are classified as B or UB series devices, in accordance with JEDEC Standard 13-B. UB series gates and inverters are constructed with a single inverting stage between input and output, as opposed to multiple gain stages in the B series. The subsequent decreased gain in the UB series results in less noise immunity; however, these UB devices exhibit higher speed since only a single stage is involved.

A full line of High Speed CMOS devices (54/74 HC) was developed to be both pinout and functionally equivalent to the most popular LSTTL parts. The HC family also contains devices that are pinout and functionally equivalent to some of the more popular MC14000B series CMOS parts.

The silicon-gate processing technology allows the HC family to combine the fast switching speeds of LSTTL with the low power-consumption advantages and the high noise immunity.

High-Speed CMOS logic circuits can directly interface with LSTTL/NMOS inputs; with pullup resistors HC devices can be driven by LSTTL/NMOS outputs. An alternative method is to use an HCT interface device which accepts LSTTL input levels without the aid of pullup resistors.

FACT devices are faster than any previous CMOS technology, approaching even the speed of advanced bipolar products. In addition, they provide wide logic fanout and higher noise margins than most of its competitors. They are designed to be directly interchangeable with slower-speed CMOS and equivalent bipolar products.

Motorola's initial FACT introductions are given in the table below. They are directly interchangeable with FACT devices from National Semiconductor Corporation, and the Motorola product family is expected to expand rapidly into a full-function line of over 100 devices.

SPEED/POWER CHARACTERISTICS FOR CMOS LOGIC

(ALL TYPICAL RATINGS)

Characteristic	Symbol	Standard CMOS (15 V)	Hi-Speed CMOS (6 V)	FACT	Units
Quiescent Supply Current/Gate	I_G	0.0001	0.0003	0.0002	mA
Power/Gate (Quiescent)	P_G	0.0006	0.001	0.001	mW
Propagation Delay	t_p	50	8.0	5.0	ns
Speed Power Product	—	0.030	0.01	0.01	pJ
Clock Frequency (D-F/F)	f_{max}	14	40	160	MHz
Clock Frequency (Counter)	f_{max}	8.0	40	125	MHz

MOTOROLA FACT FUNCTIONS

MC74AC(T★)00 Series, (−40 to +85°C)
(Available in plastic dual-in-line and SOIC packages.)

Gates — NAND

AC/ACT00	Quad 2-Input
AC10	Triple 3-Input

Gates — OR/NOR/Exclusive-OR

AC32/ACT32	Quad 2-Input OR
AC02/ACT02	Quad 2-Input NOR

Inverters/Non-Inverters

AC04/ACT04	Hex Inverter

Schmitt Triggers

AC14/ACT14	Hex Inverter

★ ACT devices have TTL-compatible inputs.

Flip-Flops

AC/ACT74	Dual D w/Set & Clear
AC174	Hex D w/Set & Clear
AC273	Octal D w/Set & Clear
AC/ACT374	Octal D

AND Gates

AC/ACT08	Quad 2-Input
AC/ACT11	Triple 3-Input

Latches

AC/ACT373	Octal D

Counters

AC163	4-Bit Binary
AC4020	14-Stage Binary
AC4040	12-Stage Binary

Multiplexers

AC/ACT151	8-Input
AC153	Dual 4-Input
AC157	Quad 2-Input

Decoders/Demultiplexers

AC/ACT138	1-of-8
AC139	Dual 1-of-4

Buffers/Line Drivers

AC/ACT240	Octal
AC/ACT244	Octal
AC541	Octal

Transceivers/Registered Transceivers

AC/ACT245	Octal

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HTL/DTL Circuits

Motorola still supplies a large selection of HTL (High-Threshold Logic) and DTL (Diode-Transistor Logic) circuits. These are recommended primarily for replacement purposes. A list of available type numbers is given below.

DTL

Device Number	Function
MC830	Expandable NAND Gate
MC832	Expandable Buffer
MC833	Dual Expander
MC834	Hex Inverter
MC835	Hex Inverter (without output resistors)
MC836	Hex Inverter
MC837	Hex Inverter
MC838	Decade Counter
MC839	Divide-by-Sixteen Counter
MC840	Hex Inverter (without input diodes)
MC841	Hex Inverter (without output resistors and input diodes)
MC843	4 Input AND Driver with NOR Strobe
MC844	Expandable Dual Power Gate
MC845	Clocked Flip-Flop
MC846	Quad 2-Input NAND Gate
MC848	Clocked Flip-Flop
MC849	Quad 2-Input NAND Gate
MC936	Hex Inverter
MC937	Hex Inverter
MC938	Decade Counter
MC939	Divide-by-Sixteen Counter
MC940	Hex Inverter (without input diodes)
MC941	Hex Inverter (without output resistors and input diodes)
MC944	Expandable Dual Power Gate
MC945	Clocked Flip-Flop
MC946	Quad 2-Input NAND Gate
MC948	Clocked Flip-Flop
MC949	Quad NAND Gate
MC950	Pulse Triggered Binary
MC951	Monostable Multivibrator
MC952	Dual J-K Flip-Flop (common clock and CD Separate SD)
MC953	Dual J-K Flip-Flop (separate clock and SD, No CD)
MC955	Dual J-K Flip-Flop (common clock and CD, separate SD, 2 k pullup resistor)

HTL

Device Number	Function
MC660	Expandable Dual 4-Input Gate (active pullup)
MC661	Expandable Dual 4-Input Gate (passive pullup)
MC662	Expandable Dual 4-Input Line Driver
MC663	Dual J-K Flip-Flop
MC664	Master-Slave R-S Flip-Flop
MC665	Triple Level Translator
MC666	Triple Level Transistor
MC667	Dual Monostable Multivibrator
MC668	Quad 2-Input Gate (passive pullup)
MC669	Dual 4-Input Expander
MC670	Triple 3-Input Gate (passive pullup)
MC671	Triple 3-Input Gate (active pullup)
MC672	Quad 2-Input Gate (active pullup)
MC673	Dual 2-Input AND-OR-INVERT Gate
MC674	Dual 2-Input AND-OR-INVERT Gate
MC675	Dual Pulse Stretcher
MC677	Hex Inverter With Strobe (active pullup)
MC678	Hex Inverter With Strobe (without output resistors)

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Available Functions

Functionally Comparable Logic Integrated Circuits

The following table offers a quick guide to logic circuits in the various families available from Motorola. Devices within a single (horizontal) row perform similar functions. Pinout configuration are generally identical when the numbers in a row correspond, although there may be exceptions. Consult the appropriate data book for specific details.

The numbers in the (vertical) columns are suffixes that follow the basic line prefixes associated with each specific logic family. These prefixes are as follows:

TTL		CMOS		MECL		
LS	FAST	STD	HC ★	10K	10KH	III
PREFIXES						
SN54/74LS	MC54/74F	MC14	MC54/74HC	MC10	MC10H	MC

Thus, the TTL LS Quad 2-input gate (item 1 in the table) can be ordered under the part number SN54LS08 (or SN74LS08). Similarly, the MECL 10KH Quad 2-input gate can be ordered as MC10H104.

Function	TTL LS	TTL FAST	CMOS STD	CMOS HC★	Package*	MECL 10K	MECL 10KH	MECL III	Package*
AND Gates									
Quad 2-Input	08	08	081	08	632	104	104		620
Quad 2-Input, Open-Collector	09				646				648
Triple 3-Input	11	11	073	11					
Triple 3-Input, Open-Collector	15								
Dual 4-Input	21	21	082						
Hex						197			
NAND Gates									
Quad 2-Input	00	00	011	**00**	632				
Quad 2-Input, Open-Collector	01				648				
Quad 2-Input, Open-Collector	03			**03**					
Quad 2-Input, High-Voltage	26								
Quad 2-Input Buffer	37								
Quad 2-Input Buffer, Open-Collector	38								
13-Input	133			133	620,648				
Triple 3-Input	10	10	023	10	632				
Triple 3-Input, Open-Collector	12				648				
Dual 4-Input	20	20	012	20					
Dual 4-Input, Open-Collector	22								
Dual 4-Input Buffer	40								
8-Input	30		068	30					
Quad 2-Input NAND with Schmitt Trigger Inputs	132		093	132					
OR Gates									
Quad 2-Input	32	32	071	32	632	103	103	1664	620
Dual 3-Input 3-Output					646	110			648
High-Speed Dual 3-Input 3-Output						210	210		
Triple 3-Input			075	4075					
Dual 4-Input			072						

(continued)

Temperature Ranges:
TTL 54 Series: −55 to +125°C
TTL 74 Series: 0 to +70°C
CMOS 54/74 Series: −55 to +125°C
CMOS MC14...A Series: −55 to +125°C
CMOS MC14...C Series: −40 to +85°C
MECL 10K/MECL III: −30 to +85°C
MECL 10KH: 0 to 75°C

*See Surface Mount section for SO and PLCC packages.

★ **Bold face type numbers are available in both HC and HCT versions.**

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Function	TTL		CMOS		Package*	MECL			Package*
	LS	FAST	STD	HC★		10K	10KH	III	
NOR Gates									
Quad 2-Input	02	02	001	02(36)	632	102	102	1662	620
Quad 2-Input Buffer	28				646				648
Quad 2-Input Buffer, Open-Collector	33								
Dual 5-Input	260								
Triple 3-Input	27		025	27					
Quad 2-Input with Strobe						100	100		
Triple 4-3-3 Input						106	106		
Dual 3-Input 3-Output						111			
High-Speed Dual 3-Input 3-Output						211	211		
Dual 3-Input, plus Inverter			000						
Dual 4-Input			002	4002					
8-Input			078	4078					
Exclusive OR Gates									
Quad 2-Input	86	86	070	86	632	113	113		620
Quad 2-Input	386				646				648
Quad, Open-Collector	136								
Triple 2-Input								1672	620
Exclusive NOR Gates									
Quad, 2-Input Open Drain Output	266		077		632				
Triple 2-Input					646			1674	620
Quad, 2-Input				7266					
Complex Gates									
Quad OR/NOR					632	101	101		620
Triple 2-3-2 Input OR/NOR					646	105	105	1688	648
Triple 2-Input Exclusive OR/Exclusive NOR						107	107		
Dual 4-5 Input OR/NOR						109	109		
Dual 4-5 Input OR/NOR							209		
Dual 2-Wide 2-3 Input OR-AND/OR-AND-Invert						117	117		
Dual 2-Wide 3-Input OR-AND						118	118		
4-Wide 4-3-3-3 Input OR-AND Gate						119	119		
OR-AND/OR-AND-INVERT Gate						121	121		
High-Speed Dual 3-Input 3-Output OR/NOR						212			
Dual 4-Input OR/NOR								1660	
Dual AND-OR-INVERT Gate	51	51	506	51					
3-2-2-3 Input AND-OR-INVERT Gate	54								
2-Wide and 4-Input AND-OR-INVERT Gate	55								
4-2-2-3 Input AND-OR-INVERT Gate		64							
Triple Gate (Dual 4-Input NAND Gate and 2-Input NOR/OR Gate or 8-Input AND/NAND Gate)			501						
4-Bit AND/OR Selector (Quad 2-Channel Data Selector or Quad Exclusive NOR Gate)			519						
Dual 5-Input Majority Logic Gate			530						
Hex Gate (Quad Inverter plus 2-Input NOR Gate plus 2-Input NAND Gate)			572						
2-Wide, 2-Input/2-Wide, 3-Input AND-OR Gate				58					

*See Surface Mount section for SO and PLCC packages.

(continued)

★ **Bold face type numbers are available in both HC and HCT versions.**

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FUNCTIONALLY COMPARABLE LOGIC INTEGRATED CIRCUITS (continued)

Function	TTL		CMOS		Package*	MECL			Package*
	LS	FAST	STD	HC★		10K	10KH	III	
Inverters/Buffers (Non 3-State)									
Hex Inverter	04	04	069	**04**	632				620
Hex Inverter, Open-Collector	05	05		05	646				648
Dual Complementary Pair plus Inverter			007		620				
Hex Buffer			050	4050	648				
Strobed Hex Inverter/Buffer			502						
Hex Buffer with Enable						188	188		
Hex Inverter with Enable						189	189		
Hex Inverter/Buffer			049	4049		195			
Hex Unbuffered Inverter				U04					
Translators									
Quad MTTL to MECL, ECL Strobe					620	124	124		620
Quad TTL to MECL, TTL Strobe					648		424		648
Quad MECL to MTTL						125	125		
Quad MECL to TTL, Single Supply							350		
Triple MECL to NMOS						177			
TTL or CMOS to CMOS Hex Level Shifter			504						
Quad MST-to-MECL 10,000						190			
Hex MECL 10,000 to MST						191			
Bus-Oriented 3-State Circuits									
Quad Buffer, Low Enable, 3-State	125A			**125**	632				
Quad Buffer, High Enable, 3-State	126A			**126**	646				
Octal Bus/Line Driver, Inverting, 3-State	240	240		**240**	732				
Octal Bus/Line Driver, 3-State	241	241		**241**	738				
Quad Bus Transceiver, Inverting 3-State	242	242		242	632				
Quad Bus Transceiver, Noninverting, 3-State	243	243		243	646				
Octal Driver, Noninverting, 3-State	244	244		**244**	732				
Octal Bus Transceiver, Noninverting, 3-State	245	245		**245**	738				
Hex Buffer, Common Enable, 3-State	365A			365	620				
Hex Inverter, Common Enable, 3-State	366A			366	648				
Hex Buffer, 4-Bit and 2-Bit, 3-State	367A		503	367					
Hex Inverter, 4-Bit and 2-Bit, 3-State	368A			368					

(continued)

Temperature Ranges:
TTL 54 Series: −55 to +125°C
TTL 74 Series: 0 to +70°C
CMOS 54/74 Series: −55 to +125°C
CMOS MC14...A Series: −55 to +125°C
CMOS MC14...C Series: −40 to +85°C
MECL 10K/MECL III: −30 to +85°C
MECL 10KH: 0 to 75°C

*See Surface Mount section for SO and PLCC packages.

★ **Bold face type numbers are available in both HC and HCT versions.**

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Function	TTL		CMOS			MECL			
	LS	FAST	STD	HC★	Package*	10K	10KH	III	Package*
Bus-Oriented 3-State Circuits (continued)									
Octal Buffer (81LS95), 3-State	795				732				620
Octal Buffer (81LS96), 3-State	796				738				
Octal Buffer (81LS97), 3-State	797								
Octal Buffer (81LS98), 3-State	798								
Octal Buffer/Line Driver, 3-State	540			**540**					
Octal Buffer/Line Driver, 3-State	541			**541**					
Octal Bus Transceiver, Inverting, 3-State	640			**640**					
Octal Bus Transceiver, True, Inverting, 3-State									
Octal Bus Transceiver, Noninverting, 3-State	645								
Octal Transceiver with Storage, 3-State	623								
Octal Transceiver/Latch/Multiplexer, Noninverting, 3-State				646	724				
Octal Transceiver/Latch/Multiplexer, Inverting, 3-State				**648**	758				
Dual Latching Bus Driver						128			
Bus Driver (25 ohm outputs)									
Triple 4-3-3 Input						123	123		620,648
Quad Driver/Receiver with 2-1 Output Multiplexer							330		724,758
Dual Driver/Receiver with 4-to-1 Output Multiplexers							332		732
Quad Driver/Receiver with Transmit and Receiver Latches							334		738
Triple 3-Input Driver with Enable							423		
Open-Collector Bus Transceivers									
Octal Bus, Noninverting, Open-Collector	641				732				
Octal Bus, Inverting, Open-Collector	642				738				
Schmitt Triggers									
Quad 2-Input NAND	132	132	093	132	632,646				
Dual			583		620,648				
Dual 4-Input	13	13			632				
Hex	14	14	584 106	14	646				

*See Surface Mount section for SO and PLCC packages.

(continued)

★ **Bold face type numbers are available in both HC and HCT versions.**

FUNCTIONALLY COMPARABLE LOGIC INTEGRATED CIRCUITS (continued)

Function	TTL		CMOS			MECL			
	LS	FAST	STD	HC★	Package*	10K	10KH	III	Package*
Latches									
4-Bit Bi-Stable Latch with Q and Q	75		042	75	620,648				620
4-Bit Bi-Stable Latch	77				632,646				648
Octal Transparent Latch, 3-State, Noninverting	373	373		**373**	620				
Quad Latch	375				648	168			
Quad NAND R-S Latch	279		044						
8-Bit Addressable Latch (9334)	259	259	099	259					
Dual 4-Bit Addressable Latch	256	256							
Octal Transparent Latch, 3-State				**573**	732				
Octal Transparent Latch, 3-State, Inverting		533		**533**	738				
Dual Latch						130	130		620
Quad (negative transition) Latch					620	133			648
Quad (positive transition) Latch					648	153			
Quint Latch						175	175		
Quad NOR R-S Latch			043						
Dual 4-Bit Latch			508		623,709				
8-Bit, Bus-Compatible, 3-State Latches — Internal Counter			597						
8-Bit, Bus-Compatible, 3-State Latches — Binary Address			598						
8-Bit Addressable Latch with Bidirectional Port			599		707,726				
Octal D-Type Transparent Latch, 3-State				**373**	732,738				
Octal D-Type Latch w/Readback, 3-State				793					
Flip-Flops/Registers									
Dual JK	73A		027	73	620,648	135	135		620
Dual D	74A	74	013	74	632,646	131	131		648
Dual JK	76A			76	620,648				
Dual JK with Preset	109A	109		109	620,648				
Dual JK with Clear	107A			107	632,646				
Dual JK Edge-Triggered	112A			112	620,648				
Dual JK Edge-Triggered	113A			113	632,646				

(continued)

Temperature Ranges:
TTL 54 Series: −55 to +125°C
TTL 74 Series: 0 to +70°C
CMOS 54/74 Series: −55 to +125°C
CMOS MC14...A Series: −55 to +125°C
CMOS MC14...C Series: −40 to +85°C
MECL 10K/MECL III: −30 to +85°C
MECL 10KH: 0 to 75°C

*See Surface Mount section for SO and PLCC packages.

★ **Bold face type numbers are available in both HC and HCT versions.**

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Function	TTL		CMOS		Package*	MECL			Package*
	LS	FAST	STD	HC★		10K	10KH	III	
Flip-Flops/Registers (continued)									
Dual JK Edge-Triggered	114A								620
4-Bit D Register, 3-State	173		076	173	620				648
Hex D with Clear	174	174	174	174	648				
Hex D with Enable	378	378			732,738				
Quad D with Clear	175	175	175	175	620,648				
Octal D with Clear	273			273	620				
Octal D, 3-State	374	374		**374**	648				
Octal D with Enable	377								
4-Bit D with Enable	379	379							
Hex D						176	176		
Hex "D" Master-Slave/with Reset						186	186		
Octal D, Inverting, 3-State				**564**	732				
Octal D					738				
Octal D, Inverting									
Octal D, 3-State				**574**					
High-Speed Dual Type D Master-Slave						231			
Dual Clocked R-S								1666	
Dual Clocked Latch								1668	
Master-Slave Type D								1670	
UHF Prescaler Type D								1690	
Octal D Flip-Flop, 3-State		534		**534**					
Counters									
Decade	90				632				620
Divide-By-12	92				646				648
4-Bit Binary	93					154			
Decade, Asynchronously Presettable	196								
4-Bit Binary, Asynchronously Presettable	197								
BCD Decade, Asynchronously Reset	160A	160A	160	160	620				
4-Bit Binary, Asynchronous Reset	161A	161A	161	161	648	178	016	1654	
BCD Decade, Synchronous Reset	162A	162A	162	162					
4-Bit Binary, Synchronous Reset	163A	163A	163	163					
Up/Down Decade, with Clear	192	192	510						
Up/Down Binary, with Clear	193	193	516						
Up/Down Decade	190	190				137			
Up/Down Binary	191	191	029			136	136		
Decade (Divide By 2 and 5)	290				632	138		1678	
4-Bit Binary	293				646				
Dual Decade	390		518	390	620,648				
Dual 4-Bit Binary	393		520	393	632,646				
Dual Decade	490				620,648				
Decade Up/Down, 3-State		568			732				
Binary Up/Down, 3-State	569	569			738				

*See Surface Mount section for SO and PLCC packages.

(continued)

★ **Bold face type numbers are available in both HC and HCT versions.**

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FUNCTIONALLY COMPARABLE LOGIC INTEGRATED CIRCUITS (continued)

Function	TTL		CMOS		Package*	MECL			Package*
	LS	FAST	STD	HC ★		10K	10KH	III	
Counters (continued)									
Synchronous 4-Bit Up/Down Binary	669				648				693
Up/Down Decade	168	168		168					
Up/Down Binary	169	169		169					
Programmable Decade			522						
Programmable Binary			526						
Seven-Stage Ripple Counter			024	4024	632,646				
Decade Counter/Divider			017	4017	620				
Presettable Divide-by-N			018		648				
14-Bit Binary Counter/Divider			060	4060					
12-Bit Binary			040	4040					
14-Bit Binary			020	4020					
Octal Counter/Divider			022						
Dual Programmable BCD/Binary			569						
Three-Digit BCD			553						
Real Time 5-Decade			534		623				
1 GHz Divide-by-Four Prescaler					709			1697	
1 GHz Divide-by-Four								1699	620,648
Register Files									
4 x 4 Register File, Open-Collector	170				620				620
4 x 4 Register File, 3-State	670				648				648
16 x 4 Bit Register File							145		
Shift Registers									
8-Bit Serial-In/Parallel-Out Shift Register	164		034	164	632,646				
8-Bit Parallel-In/Serial-Out Shift Register	165		021	165	620,648				

(continued)

Temperature Ranges:
TTL 54 Series: −55 to +125°C
TTL 74 Series: 0 to +70°C
CMOS 54/74 Series: −55 to +125°C
CMOS MC14...A Series: −55 to +125°C
CMOS MC14...C Series: −40 to +85°C
MECL 10K/MECL III: −30 to +85°C
MECL 10KH: 0 to 75°C

*See Surface Mount section for SO and PLCC packages.

★ Bold face type numbers are available in both HC and HCT versions.

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Function	TTL		CMOS		Package*	MECL			Package*
	LS	FAST	STD	HC ★		10K	10KH	III	
Shift Registers (continued)									
4-Bit Shift Register	95B				632,646				620
8-Bit Parallel-In/Serial-Out Shift Register	166		014		620,648				648
4-Bit Shift Register	195A	195		195				1694	
4-Bit Universal Shift Register	194A	194	194	194		141	141		
8-Bit Shift/Storage Register, 3-State	299		094	299	732,738				
8-Bit Shift Register with Sign Extend, 3-State	322A								
8-Bit Shift/Storage Register, 3-State	323	323							
4-Bit Shift Register, 3-State	395				620,648				
16-Bit Serial-In/Serial-Out Shift Register, 3-State	673				623,649				
16-Bit Parallel-In/Serial-Out Register, 3-State	674								
18-Bit Static Shift Register			006		632,646				
1-to-64 Bit Variable Length Shift Register			557		620,648				
Dual 64-Bit Static Shift Register			517		648,690				
4-Bit Parallel-In/Parallel-Out Shift Register			035		620,648				
Dual 4-Bit Static Shift Register			015						
128-Bit Static Shift Register			562		632,646				
8-Bit Parallel to Serial S.R. w/Input Latches, 3-State				589	620,648				
8-Bit Serial to Parallel S.R. 3-State				595					
8-Bit Parallel to Serial S.R. w/Input Latches				597					
Multiplexers/Data Selectors									
Quad 2-Input Multiplexer, Noninverting	157	157,A	519	**157**	620	158	158		620
Quad 2-Input Multiplexer, Inverting	158	158,A		**158**	648	159	159		648
Quad 2-Input Multiplexer, Noninverting, 3-State	257A	257,A		**257**					
Quad 2-Input Multiplexer, Inverting, 3-State	258A	258,A							
Quad 2-Multiplexer, with Output Register	298					173	173		
Dual 4-Input Multiplexer	153	153	539	153		174	174		
Dual 4-Input Multiplexer, 3-State	253	253		253					
8-Input Multiplexer	151	151		151		164	164		
8-Input Multiplexer, 3-State	251	251	512	251					
Dual 4-Input Multiplexer (Inverting LS153)	352	352							
Dual 4-Input Multiplexer (3-State LS352)	353	353							
QUAD 2-Input Multiplexer with Output Register	398	398			732,738				
Quad 2-Input Multiplexer with Output Register	399	399			620,648				
Synchronous Address Multiplexer (MC6883)	783				711				
Dual Multiplexer with Latch and Common Reset					734	132			

*See Surface Mount section for SO and PLCC packages.

(continued)

★ **Bold face type numbers are available in both HC and HCT versions.**

FUNCTIONALLY COMPARABLE LOGIC INTEGRATED CIRCUITS (continued)

Function	TTL		CMOS			MECL			
	LS	FAST	STD	HC★	Package*	10K	10KH	III	Package*
Multiplexers/Data Selectors (continued)									
Dual Multiplexer with Latch					632	134			620
Quad Analog Switch/Quad Multiplexer			016	4016 4316	646				648
Quad Analog Switch/Quad Multiplexer			066	4066					
Triple 2-Channel Analog Multiplexer/Demultiplexer			053	4053 4353	620				
Dual 4-Channel Analog Multiplexer/Demultiplexer			052	4052 4352					
Dual 4-Channel Analog Data Selector			529						
Quad 2-Input Analog Multiplexer/Demultiplexer			551						
8-Channel Analog Multiplexer/Demultiplexer			051	4051 4351					
4-to-16 Decoder				154	724,758				
8-Input Multiplexer, 3-State				354	732				
8-Input Multiplexer, 3-State				356	738				
Decoders/Demultiplexers									
Dual 1-of-4 Decoder/Demultiplexer	139	139		139	620				620
Dual 1-of-4 Decoder (Low)	155		556		648	171	171		648
Dual 1-of-4 Decoder, Open-Collector	156								
1-of-10 Decoder	42			42					
1-of-10 Decoder/Driver, Open-Collector	145								
1-of-8 Decoder/Demultiplexer (Low)	138	138		**138**		161	161		
3-Line to 8-Line Decoder/Demultiplexer	137			137					
1-of-10 Decoder, 3-State		537							
1-of-8 Decoder, 3-State		538							
Dual 1-of-4 Decoder, 3-State		539							
Binary to 1-8 (High)						162	162		
Dual Binary 1-4 (High)			555			172	172		
BCD-to-Decimal/Binary-to-Octal Decoder			028						
4-Bit Latch/4-to-16 Line Decoder (High)			514	4514	724,758,				
4-Bit Latch/4-to-16 Line Decoder (Low)			515		709,623				
1-of-8 Decoder/Demultiplexer w/Latched Inputs				237					
Display Decoder/Drivers									
BCD to 7-Segment Decoder/Driver, Open-Collector	47				620				
BCD to 7-Segment Decoder/Driver with Pull-Ups	48		558		648				
BCD to 7-Segment Decoder/Driver, Open-Collector	247				620				
BCD to 7-Segment Decoder/Driver with Pull-Ups	248				648				

(continued)

Temperature Ranges:
TTL 54 Series: −55 to +125°C
TTL 74 Series: 0 to +70°C
CMOS 54/74 Series: −55 to +125°C
CMOS MC14...A Series: −55 to +125°C
CMOS MC14...C Series: −40 to +85°C
MECL 10K/MECL III: −30 to +85°C
MECL 10KH: 0 to 75°C

*See Surface Mount section for SO and PLCC packages.

★ **Bold face type numbers are available in both HC and HCT versions.**

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Function	TTL		CMOS		Package*	MECL			Package*
	LS	FAST	STD	HC★		10K	10KH	III	
Display Decoder/Drivers (continued)									
Hex-to-Seven Segment Decoder/Driver/Latch			495		620				
BCD-to-Seven Segment Latch/Decoder/Driver			511	4511	648				
BCD-to-Seven Segment Latch/Decoder/Driver — Ripple Blanking			513		707,726				
BCD-to-Seven Segment Latch/Decoder/Driver			543	4543	620,648				
BCD-to-Seven Segment Latch/Decoder/Driver — Ripple Blanking			544		707,726				
BCD-to-Seven Segment Decoder/Driver — High Current			547		620,648				
48-Segment Multiplexed LCD Driver (Master)			5000		623,709				
48-Segment Multiplexed LCD Driver (Slave)			5001		707,726				
Priority Encoders									
10-Line Decimal to 4-Line Priority Encoder	147				620				620
8-Input to 3-Line Priority Encoder	148	148	532		648	165	165		648
8-Input to 3-Line Priority Encoder	748								
8-Input to 3-Line Priority Encoder, 3-State	348								
8-Input to 3-Line Priority Encoder, 3-State	848								
Multivibrators									
Retriggerable Monostable Multivibrator	122				632,646	198			620
Dual Retriggerable Monostable Multivibrator	123				620				648
Dual One-Shot (Very Stable)	221				648				
Dual Precision Retriggerable/Resettable Monostable Multivibrator			538						
Oscillators/Timers									
Voltage Controlled Oscillator					626,693			1658	620
25-Stage Frequency Divider			521		620				648
Programmable Timer			536		648				607
Programmable Oscillator/Timer			541		632,646				632
Emitter Coupled Oscillator								1648	646
Receivers									
Triple Line						114			620,648
Quad Line						115	115	1692	620,650
Triple Line						116	116		620,648
High-Speed Triple Line						216			
Quad Bus						129			
Comparators									
4-Bit Magnitude Comparator	85		585	85	620,648				620
8-Bit Magnitude Comparator		521			732				648
8-Bit Magnitude Comparator, 3-State	682				738				
8-Bit Magnitude Comparator, 3-State	684								
8-Bit Magnitude Comparator	688			**688**					
5-Bit Magnitude Comparator						166	166		

*See Surface Mount section for SO and PLCC packages.

(continued)

★ **Bold face type numbers are available in both HC and HCT versions.**

FUNCTIONALLY COMPARABLE LOGIC INTEGRATED CIRCUITS (continued)

Function	TTL		CMOS			MECL			
	LS	FAST	STD	HC★	Package*	10K	10KH	III	Package*
Arithmetic Operators									
4-Bit Full Adder	83A		008		620				620
4-Bit Full Adder (Rotated LS83A)	283	283			648				648
4-Bit ALU	181	181	581		623	181	181		
4-Bit ALU	181	181 381 382			709 649 624,758				
4-Bit Barrel Shifter		350			620,648				620
Quad 4-Bit Adder Subtractor	385				732,738				648
Look Ahead Carry Generator		182	582		620,648	179	179		
Dual High-Speed Adder/Subtractor						180	180		
2-Bit Logic Unit/Function Generator						182			
4 x 2 Multiplier						183			623
2 x 1 Array Multiplier, High-Speed						287			620
BCD Rate Multiplier			527		620				648
2 x 2 Bit Parallel Binary Multiplier			554		648				
Triple Serial Adder (Positive Logic)			032						
Triple Serial Adder (Negative Logic)			038						
NBCD Adder			560						
9's Complementer			561		632,646				
Parity Generators/Checkers									
9-Bit Odd/Even Parity Generator/Checker	280	280		280	632,646	170			620
12-Bit Parity Generator/Checker			531		620,648	160	160		648
Error Detection-Correction									
IBM Code						163			620
Motorola Code						193			648
Hamming Code		2960			740				

Temperature Ranges:
TTL 54 Series: −55 to +125°C
TTL 74 Series: 0 to +70°C
CMOS 54/74 Series: −55 to +125°C
CMOS MC14...A Series: −55 to +125°C
CMOS MC14...C Series: −40 to +85°C
MECL 10K/MECL III: −30 to +85°C
MECL 10KH: 0 to 75°C

*See Surface Mount section for SO and PLCC packages.

★ **Bold face type numbers are available in both HC and HCT versions.**

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Bipolar Memories

ECL RAMs

Emitter-coupled logic (ECL) represents today's fastest logic form; ECL memories complement this characteristic. Motorola ECL RAMs are available to match the speed capabilities of the ECL10K and 10KH logic families, the two most pervasive ECL lines available.

ECL10K/10KH

Organization	Device Type	Suffix	Access Time (ns Max)	Power Dissipation (mW Typ)	Package	Comments
8 x 2	MCM10143	L	15	610	L-Case 623	Multiport Register File
16 x 4	MC10H145	P,L,FN	6	700	P-Case 648 L-Case 620 FN-Case 775	Register File
	MCM10145	L	15	463	L-Case 620	Register File
64 x 1	MCM10148	L	15	420	L-Case 620	
128 x 1	MCM10147	L	15	415		
256 x 1	MCM10144	L	26	468		
1K x 1	MCM10146	L	29	600		

ECL — PROMs

High-speed PROMs fully compatible with MECL 10K and 10KH logic families.

Organization	Device Type	Suffix	Access Time (ns Max)	Power Dissipation (mW Typ)	Package
32 x 8	MCM10139	L	20	520	L-Case 620
256 x 4	MCM10149	L10 L25	10 25	540	

Motorola Semiconductor

Consumer Electronic Circuits

Entertainment Radio Receiver Circuits

C-QUAM® AM Stereo Decoders

Function	Features	Suffix/Case	Device
Basic AM Stereo Decoder	Monaural/Stereo AM Detector, Indicator, 6–10 V Operation	P/738	MC13020
Advanced AM Stereo Decoder	Medium Voltage 2–8 V, Decoder and IF Amp	DW/751F	MC13022
AM Front End	Tuning Stabilizer for MC13022	P/738	MC13023
AM Stereo Personal Radio	Complete Low Voltage AM Stereo Receiver	P/724	MC13024
Tuning Stabilizer	Companion for MC13020 for Manual Tuned Receivers	P/648	MC13021
AM Broadcast Receiver	AM Receiver Subsystem — Ideal Companion for MC13020	P/738	MC13041

FM Stereo Decoder

Function	Channel Separation dB Typ	THD % Typ	Stereo/Indicator Lamp Driver mA Max	Features	Suffix/Case	Device
FM Multiplex Stereo Decoder	62	0.1	100	Low Signal Blend for Noise Reduction	—/648	TCA4500A

Audio Amplifiers

Function	P_O Watts	V_{CC} Vdc Max	V_{in} @ rated P_O mV Typ	I_D mA Typ	R_L Ohms	Suffix/Case	Type
Mini Watt SOIC Audio Amp	1.0 W	35	80	11	16	D/751	MC13060
Low Power Audio Amp	400 mW	16	—	2.5 mA	8–100	D/751 P/626	MC34119

Audio Attenuators/Controls

Function	V_{CC} Range Vdc	THD %	Tone Control Range dB Typ	Attenuation Range dB Typ	Suffix/Case	Device
Stereo, Volume, Bass, Treble, Balance	8.5–18	0.1 Typ	±14	80	P/707	TCA5550
Stereo, Volume, Bass, Treble, Balance	3–18	0.5 Max	±15	80	P/707	TDA1524

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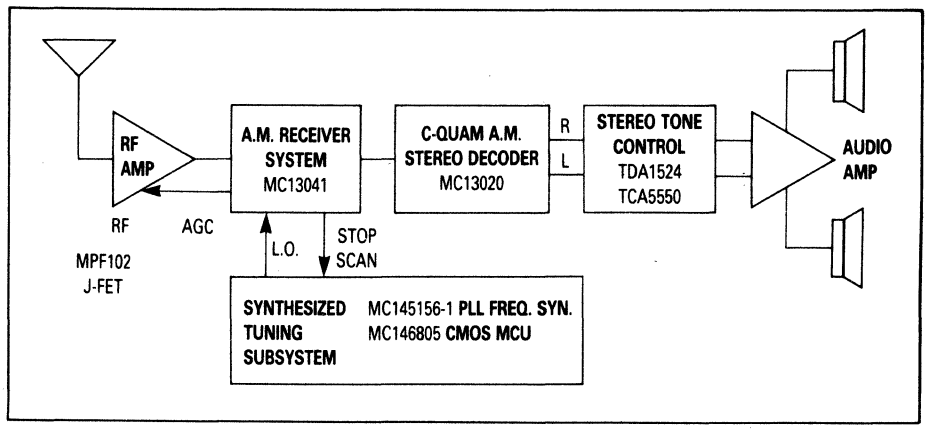

When AM stereo broadcasting was sanctioned by the F.C.C. in 1982, there were five different systems vying for user approval. Since then C-QUAM® has become the defacto standard in the U.S.A., as the market and broadcasters recognize its performance advantages. It is the legal standard in Canada, Australia and Brazil where A.M. is the dominant radio medium. C-QUAM is available from nearly 50 automobile radio makers and a dozen home receiver builders (for as little as $60 in a basic tuner).

Based on the field-proven C-Quam performance, Motorola has developed a low-cost, high performance C-Quam AM Stereo Decoder chip, with fully compatible, no-compromise mono performance, as the basis for both broadcast and receiving equipment. Additional IC components from Motorola's inventory offer a single supply source for state-of-the-art radio receiver designs. New products cover virtually every type of receiver — home, auto, and personal portable.

Radio Circuits (See Communications Section)

Video Circuits

Modulators

Function	Features	Suffix/Case	Device
TV Modulator (Hi Quality)	RF Oscillator/Modulator, and FM Sound Oscillator/Modulator	P/646	MC1374
Video RGB to PAL/NTSC Encoder	RGB and Sync Inputs, Composite Video Out — PAL/NTSC Switch Selectable	P/738	MC1377
Video Synchronizer	Complete Color TV Video Overlay Synchronizer	P/711	MC1378

Demodulators

Color Processor	PAL/NTSC Input, RGB Output, also RGB Inputs, Plus Fast Blanking Input. Ideal for Text, Graphics, Overlays	P/711	TDA3301 TDA3303
Color Processor	PAL/NTSC Input, RGB Outputs, On-Chip Hue Control	P/724	TDA3330
Color Processor	PAL/NTSC Input, Color Difference Outputs On-Chip Hue Control	P/707	TDA3333

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Tuning System

Function	Features	Suffix/Case	Device
Remote Control Amplifier	Infrared Diode Signal Amplifier Shaper	P/626	MC3373
PLL-Tuning Circuit	TV Tuning System — Prescaler — M-Bus Control	DW/751C	MC44802

Deflection

Horizontal Processor	Linear Balanced Phase Detector, Oscillator and Predriver, Adjustable dc Loop Gain, Adjustable Duty Cycle	P/626	MC1391

Sound

Sound IF Detector, dc Volume Control, Preamplifier	30 μV, 3.0 dB Limiting, Excellent AMR	—/646	TBA120C
Sound IF, Low Pass Filter, Detector, dc Volume Control, Preamplifier	Complete TV Sound System; 100 μV, 3 dB Limiting Sensitivity; 4 Watts Output; V_{CC} = 24 V; R_L = 16 Ω	P/648C	TDA3190
	750 mW Output	P/648C	TDA1190
Stereo Sound Control System	Stereo Balance, Volume, Bass, Treble Control	P/707	TCA5550

Transistor Arrays

Function	$I_{C(max)}$ mA	V_{CEO} Volts Max	V_{CBO} Volts Max	V_{EBO} Volts Max	Suffix/Case	Device
One Differentially Connected Pair and Three Isolated Transistors	50	15	20	5.0	P/646 D/751A	MC3346
Dual Independent Differential Amplifiers with Associated Constant Current Transistors	50	15	20	5.0	P/646	CA3054

Television Subsystems

Function	Features	Suffix/Case	Device
MONOMAX — 1-Chip Black and White TV Subsystem	Video IF, Detector, AGC, Video Amplifier, Horizontal Processor, Vertical Processor, and Sync For 525 Line Systems	P/710	MC13001X
	Same as Above Except For 625 Line Systems	P/710	MC13002X
Sound IF, Low Pass Filter, Detector, dc Volume Control, Preamplifier, Power Amplifier	Complete TV Sound System; 100 μV, 3 dB Limiting Sensitivity; 4 Watts Output; V_{CC} = 24 V; R_L = 16 Ω	P/648C	TDA3190
	Same as TDA1190Z Except for 750 mW Output	P/648C	TDA1190
MONOMAX Audio/Vertical Output	High Level 750 mW Audio Output — Vertical Yoke Driver	P/648C	MC13014

Video IF Amplifiers

Function	Features	Suffix/Case	Device
1st and 2nd Video IF Amplifier	IF Gain @ 45 MHz = 50 dB typ, AGC Range = 60 dB min	P/626	MC1350
3rd IF, Video Detector, Video Buffer, and AFC Buffer	Low Level Detection, Low Harmonic Generation, Zero Signal dc Output Voltage of 7.0 to 8.2 V	P/626	MC1330A1P
	Same as MC1330A1 Except Zero Signal dc Output Voltage of 7.8 to 9.0 V	P/626	MC1330A2P
SAW Preamp, IF Amplifier, Detector, AGC, AFC	Complete Video IF or Parallel Sound IF System Complete AFT System with Simple Quadrature Detector	P/707	MC13010P
Advanced Video IF	Complete Video/Audio IF System for High Performance Analog TV Receivers	DW/751F	MC44301

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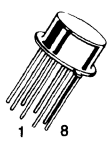
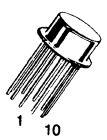
Amplifiers and Comparators

Operational Amplifiers

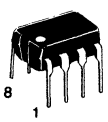
Motorola offers a broad line of bipolar operational amplifiers to meet a wide range of applications. From low-cost industry-standard types to high precision circuits, the span encompasses a large range of performance capabilities. These linear integrated circuits are available as single, dual, and quad monolithic devices in a variety of temperature ranges and package styles. Most devices may be obtained in unencapsulated "chip" form as well. For price and delivery information on chips, please contact your Motorola Sales Representative or Distributor.



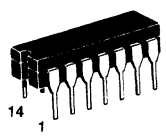
CASE 601
METAL
H, G SUFFIX



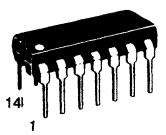
CASE 603
METAL
G SUFFIX



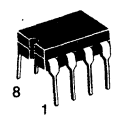
CASE 626
PLASTIC
N, P OR P1 SUFFIX



CASE 632
CERAMIC
J, L SUFFIX



CASE 646
PLASTIC
N, N-14, P OR P2 SUFFIX



CASE 693
CERAMIC
J OR J-8, U, Z, JG SUFFIX

Single Operational Amplifiers

Device	I_{IB} μA Max	V_{IO} mV Max	TC_{VIO} μV/°C Typ	I_{IO} nA Max	A_{vol} V/mV Min	BW (A_V=1) MHz Typ	SR (A_V=1) V/μs Typ	Supply Voltage V Min	Supply Voltage V Max	Description	Package Suffix
Noncompensated											
Commercial Temperature Range (0°C to +70°C)											
LM301A	0.25	7.5	10	50	25	1.0	0.5	±3.0	±18	General Purpose	H, N/626, J/693
LM308	7.0	7.5	15	1.0	25	1.0	0.3	±3.0	±18	Precision	H, N/626
LM308A	7.0	0.5	5.0	1.0	80	1.0	0.3	±3.0	±18	Precision	H, N/626
MC1439	1.0	7.5	15	100	15	2.0	4.2	±6.0	±18	High Slew Rate	G/601, P1
MC1709C	1.5	7.5	15	500	15	1.0	0.3	±3.0	±18	General Purpose	G/601, P1, U
MC1748C	0.5	6.0	15	200	20	1.0	0.5	±3.0	±18	General Purpose	G/601, P1, U
Industrial Temperature Range (−25°C to +85°C)											
LM201A	0.075	2.0	10	10	50	1.0	0.5	±3.0	±22	General Purpose	H, N/626, J/693
LM208	0.002	2.0	3.0	0.2	50	1.0	0.3	±3.0	±20	Precision	H, N/626, J/632, J-8
LM208A	0.002	0.5	1.0	0.2	80	1.0	0.3	±3.0	±20	Precision	H, N/626, J/632, J-8
Military Temperature Range (−55°C to +125°C)											
LM101A	0.075	2.0	10	10	50	1.0	0.5	±3.0	±22	General Purpose	H, J/693
LM108	0.002	2.0	3.0	0.2	50	1.0	0.3	±3.0	±20	Precision	H, J, J-8/693
LM108A	0.002	0.5	1.0	0.2	80	1.0	0.3	±3.0	±20	Precision	H, J, J-8/693
MC1539	0.5	3.0	15	60	50	2.0	4.2	±4.0	±18	High Slew Rate	G/601
MC1709	0.5	5.0	15	200	25	1.0	0.3	±3.0	±18	General Purpose	G/601, U
MC1709A	0.6	3.0	5.0	100	25	1.0	0.5	±3.0	±18	High Performance MC1709	G/601
MC1748	0.5	5.0	15	200	50	1.0	0.5	±3.0	±22	General Purpose	G/601, U

Motorola Semiconductor

Device	I_{IB} μA Max	V_{IO} mV Max	TC_{VIO} μV/°C Typ	I_{IO} nA Max	A_{vol} V/mV Min	BW (A_V=1) MHz Typ	SR (A_V=1) V/μs Typ	Supply Voltage V Min	Supply Voltage V Max	Description	Package Suffix
Internally Compensated											
Commercial Temperature Range (0°C to +70°C)											
LF351	200 pA	10	10	100 pA	25	4.0	13	±5.0	±18	JFET Input	N/626
LF355	200 pA	10	5.0	50 pA	50	1.0	5.0	±5.0	±18	JFET Input	H/601, J/693
LF355B	100 pA	5.0	5.0	20 pA	50	2.5	5.0	±5.0	±22	JFET Input	H/601, J/693
LF356	200 pA	10	5.0	50 pA	50	2.0	15	±5.0	±18	JFET Input	H/601, J/693
LF356B	100 pA	5.0	5.0	20 pA	50	5.0	12	±5.0	±22	JFET Input	H/601, J/693
LF357	200 pA	10	5.0	50 pA	50	3.0	75	±5.0	±18	Wideband FET Input	H/601, J/693
LF357B	100 pA	5.0	5.0	20 pA	50	20	50	±5.0	±22	JFET Input	H/601, J/693
LF441C	100 pA	5.0	10	50 pA	25	2.0	6.0	±5.0	±18	Low Power JFET Input	N/626
LM11C	100 pA	0.6	2.0	10 pA	250	1.0	0.3	±3.0	±20	Precision	H, N/626, J/632, J-8/693
LM11CL	200 pA	5.0	3.0	25 pA	50	1.0	0.3	±3.0	±20	Precision	H, N/626, J/632, J-8/693
LM307	0.25	7.5	10	50	25	1.0	0.5	±3.0	±18	General Purpose	N/626
MC1436	0.04	10	12	10	70	1.0	2.0	±15	±34	High Voltage	G/601, U
MC1456	0.03	10	12	10	70	1.0	2.5	±3.0	±18	High Performance	G/601, P1, U
MC1733C	30	—	—	5.0 μA	80	90	—	±4.0	±8.0	Differential Wideband Video Amp	G/601, L, P/646
MC1741C	0.5	6.0	15	200	20	1.0	0.5	±3.0	±18	General Purpose	G/601, P1, U
MC1741SC	0.5	6.0	15	200	20	1.0	10	±3.0	±18	High Slew Rate	G/601, P1
MC1776C	0.003	6.0	15	3.0	100	1.0	0.2	±1.2	±18	μPower, Programmable	G/601, P1, U
MC3476	0.05	6.0	15	25	50	1.0	0.2	±1.5	±18	Low Cost μPower, Programmable	G/601, P1, U
MC34001	200 pA	10	10	100 pA	25	4.0	13	±5.0	±18	JFET Input	G/601, P/626, U
MC34001A	100 pA	2.0	10	50 pA	50	4.0	13	±5.0	±18	JFET Input	G/601, P/626, U
MC34001B	200 pA	5.0	10	100 pA	50	4.0	13	±5.0	±18	JFET Input	G/601, P/626, U
MC34071	0.50	5.0	10	75	25	4.5	10	+3.0	+44	High Performance,	P/626, U
MC34071A	500 nA	3.0	10	50	50	4.5	10	+3.0	+44	Single Supply	P/626, U
MC34080	200 pA	1.0	10	100 pA	25	16	55	±5.0	±22	Decompensated	P/626, U
MC34080A	200 pA	0.5	10	100 pA	50	16	55	±5.0	±22	MC34081 for $A_V \geq 2$	P/626, U
MC34081	200 pA	1.0	10	100 pA	25	8.0	30	±5.0	±22	High Speed, JFET Input	P/626, U
MC34081A	200 pA	0.5	10	100 pA	50	8.0	30	±5.0	±22	High Speed, JFET Input	P/626, U
MC34181	0.1 nA	2.0	10	0.05	25	4.0	10	±2.5	±18	Low Power JFET Input	P/626
OP-27E	0.040	0.025	0.2	35	1000	8.0	2.8	±4.0	±22	Low Noise, Precision	P/626
OP-27F	0.055	0.060	0.3	50	1000	8.0	2.8	±4.0	±22	Low Noise, Precision	P/626
OP-27G	0.080	0.100	0.4	75	700	8.0	2.8	±4.0	±22	Low Noise, Precision	P/626
TL061AC	200 pA	6.0	10	100 pA	4.0	2.0	6.0	±2.5	±18	Low Power JFET Input	P/626
TL061BC	200 pA	3.0	10	100 pA	4.0	2.0	6.0	±2.5	±18	Low Power JFET Input	P/626
TL061C	200 pA	15	10	200 pA	4.0	2.0	6.0	±2.5	±18	Low Power JFET Input	P/626
TL071AC	200 pA	6.0	10	50 pA	50	4.0	13	±5.0	±18	Low Noise, JFET Input	P/626, JG
TL071BC	200 pA	3.0	10	50 pA	50	4.0	13	±5.0	±18	Low Noise, JFET Input	P/626, JG
TL071C	200 pA	10	10	50 pA	25	4.0	13	±5.0	±18	Low Noise, JFET Input	P/626, JG
TL081AC	200 pA	6.0	10	100 pA	50	4.0	13	±5.0	±18	JFET Input	P/626, JG
TL081BC	200 pA	3.0	10	100 pA	50	4.0	13	±5.0	±18	JFET Input	P/626, JG
TL081C	400 pA	15	10	200 pA	25	4.0	13	±5.0	±18	JFET Input	P/626, JG
Industrial Temperature Range (−25°C to +85°C)											
OP-27E	0.040	0.025	0.2	35	1000	8.0	2.8	±4.0	±22	Low Noise, Precision	Z
OP-27F	0.055	0.060	0.3	50	1000	8.0	2.8	±4.0	±22	Low Noise, Precision	Z
OP-27G	0.080	0.100	0.4	75	700	8.0	2.8	±4.0	±22	Low Noise, Precision	Z
Automotive Temperature Range (−40°C to +85°C)											
MC33071	0.50	5.0	10	75	25	4.5	10	+3.0	+44	High Performance,	P/626, U
MC33071A	500 nA	3.0	10	50	50	4.5	10	+3.0	+44	Single Supply	P/626, U
MC33171	0.10	4.5	10	20	50	1.8	2.1	+3.0	+44	Low Power, Single Supply	P/626
MC33181	0.1 nA	2.0	10	0.05	25	4.0	10	±2.5	±18	Low Power JFET Input	P/626
TL061V	200 pA	6.0	10	100 pA	4.0	2.0	6.0	±2.5	±18	Low Power JFET Input	P/626

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Single Operational Amplifiers (continued)

Device	I_{IB} μA Max	V_{IO} mV Max	TC_{VIO} μV/°C Typ	I_{IO} nA Max	A_{vol} V/mV Min	BW (A_V = 1) MHz Typ	SR (A_V = 1) V/μs Typ	Supply Voltage V Min	Supply Voltage V Max	Description	Package Suffix
Internally Compensated											
Military Temperature Range (−55°C to +125°C)											
LM11	50 pA	0.3	1.0	10 pA	250	1.0	0.3	±3.0	±20	Precision	H, J/632, J-8/693
MC1536	0.02	5.0	10	3.0	100	1.0	2.0	±15	±40	High Voltage	G/601, U
MC1556	0.015	4.0	10	2.0	100	1.0	2.5	±3.0	±22	High Performance	G/601, 693, U
MC1733	0.20	—	—	3.0 μA	90	90	—	±4.0	±8.0	Differential Wideband Video Amp	G/603, L
MC1741	0.5	5.0	15	200	50	1.0	0.5	±3.0	±22	General Purpose	G/601, U
MC1741S	0.5	5.0	15	200	50	1.0	10	±3.0	±22	High Slew Rate	G/601, U
MC1776	0.0075	5.0	15	3.0	200	1.0	0.2	±1.2	±18	μPower, Programmable	G/601, L
MC35001	100 pA	10	10	100 pA	25	4.0	13	±5.0	±22	JFET Input	G/601, U
MC35001A	75 pA	2.0	10	25 pA	50	4.0	13	±5.0	±22	JFET Input	G/601, U
MC35001B	100 pA	5.0	10	50 pA	50	4.0	13	±5.0	±22	JFET Input	G/601, U
MC35071	0.50	5.0	10	75	25	4.5	10	+3.0	+44	High Performance,	U
MC35071A	500 nA	3.0	10	50	50	4.5	10	+3.0	+44	Single Supply	U
MC35080	200 pA	1.0	10	100 pA	25	16	55	±5.0	±22	Decompensated	U
MC35080A	200 pA	0.5	10	100 pA	50	16	55	±5.0	±22	MC35081 for $A_V \geq 2$	U
MC35081	200 pA	1.0	10	100 pA	25	8.0	30	±5.0	±22	High Speed, JFET Input	U
MC35081A	200 pA	0.5	10	100 pA	50	8.0	30	±5.0	±22	High Speed, JFET Input	U
MC35171	0.10	4.5	10	20	50	1.8	2.1	+3.0	+44	Low Power, Single Supply	U
MC35181	0.1 nA	2.0	10	0.05	25	4.0	10	±2.5	±18	Low Power JFET Input	U
OP-27A	0.040	0.025	0.2	35	1000	8.0	2.8	±4.0	±22	Low Noise, Precision	Z
OP-27B	0.055	0.060	0.3	50	1000	8.0	2.8	±4.0	±22	Low Noise, Precision	Z
OP-27C	0.080	0.100	0.4	75	700	8.0	2.8	±4.0	±22	Low Noise, Precision	Z
TL061M	200 pA	6.0	10	100 pA	4.0	2.0	6.0	±2.5	±18	Low Power JFET Input	JG
TL071M	200 pA	6.0	10	50 pA	35	4.0	13	±5.0	±18	Low Noise, JFET Input	JG
TL081M	200 pA	9.0	10	100 pA	25	4.0	13	±5.0	±18	JFET Input	JG

Dual Operational Amplifiers

Device	I_{IB} μA Max	V_{IO} mV Max	TC_{VIO} μV/°C Typ	I_{IO} nA Max	A_{vol} V/mV Min	BW (A_V = 1) MHz Typ	SR (A_V = 1) V/μs Typ	Supply Voltage V Min	Supply Voltage V Max	Description	Package Suffix
Noncompensated											
Commercial Temperature Range (0°C to +70°C)											
MC1437	1.5	7.5	10	500	15	1.0	0.25	±3.0	±18	Dual MC1709	L, P/646
Military Temperature Range (−55°C to +125°C)											
MC1537	0.5	5.0	10	200	25	1.0	0.25	±3.0	±18	Dual MC1709	L
Internally Compensated											
Commercial Temperature Range (0°C to +70°C)											
LF353	200 pA	10	10	100 pA	25	4.0	13	±5.0	±18	JFET Input	N/626
LF442C	100 pA	5.0	10	50 pA	25	2.0	6.0	±5.0	±18	Low Power JFET Input	N/626
LM358	0.25	6.0	7.0	50	25	1.0	0.6	±1.5	±18	Single Supply	H, N/626, J/693
								+3.0	+36	(Low Power Consumption)	
LM833	1.0	5.0	2.0	200	31.6	15	7.0	±2.5	±18	Dual, Low Noise, Audio	P/626
MC1458	0.5	6.0	10	200	20	1.1	0.8	±3.0	±18	Dual MC1741	G/601, P1, U
MC1458C	0.70	10	10	300	20	1.1	0.8	±3.0	±18	Dual General Purpose	G/601, P1
MC1458S	0.5	6.0	10	200	20	1.0	10	±3.0	±18	High Slew Rate	G/601, P1, U
MC1747C	0.5	6.0	10	200	25	1.0	0.5	±3.0	±18	Dual MC1741	G/603, L, P2
MC3458	0.5	10	7.0	50	20	1.0	0.6	±1.5	±18	Split Supplies	G/601, P1, U
								+3.0	+36	Single Supply (Low Crossover Distortion)	

Device	I_{IB} μA Max	V_{IO} mV Max	TC_{VIO} μV/°C Typ	I_{IO} nA Max	A_{vol} V/mV Min	BW (A_V=1) MHz Typ	SR (A_V=1) V/μs Typ	Supply Voltage V Min	Supply Voltage V Max	Description	Package Suffix
Commercial Temperature Range (0°C to +70°C) (continued)											
MC4558AC	0.5	5.0	10	200	50	2.8	1.6	±3.0	±22	High Frequency	P1
MC4558C	0.5	6.0	10	200	20	2.8	1.6	±3.0	±18	High Frequency	G/601, P1, U
MC34002	100 pA	10	10	100 pA	25	4.0	13	±5.0	±18	JFET Input	G/601, P/626, U
MC34002A	75 pA	2.0	10	50 pA	50	4.0	13	±5.0	±18	JFET Input	G/601, P/626, U
MC34002B	100 pA	5.0	10	70 pA	25	4.0	13	±5.0	±18	JFET Input	G/601, P/626, U
MC34072	0.50	5.0	10	75	25	4.5	10	+3.0	+44	High Performance,	P/626, U
MC34072A	500 nA	3.0	10	50	50	4.5	10	+3.0	+44	Single Supply	P/626, U
MC34082	200 pA	3.0	10	100 pA	25	8.0	30	±5.0	±22	High Speed, JFET Input	P/626, U
MC34082A	200 pA	1.0	10	100 pA	50	8.0	30	±5.0	±22	High Speed, JFET Input	P/626, U
MC34083	200 pA	3.0	10	100 pA	25	16	55	±5.0	±22	Decompensated	P/626, U
MC34083A	200 pA	1.0	10	100 pA	50	16	55	±5.0	±22	MC34082 for $A_V \geq 2$	P/626, U
MC34182	0.1 nA	3.0	10	0.05	25	4.0	10	±2.5	±18	Low Power JFET Input	P/626
TL062AC	200 pA	6.0	10	100 pA	4.0	2.0	6.0	±2.5	±18	Low Power JFET Input	P/626
TL062BC	200 pA	3.0	10	100 pA	4.0	2.0	6.0	±2.5	±18	Low Power JFET Input	P/626
TL062C	200 pA	15	10	200 pA	4.0	2.0	6.0	±2.5	±18	Low Power JFET Input	P/626
TL072AC	200 pA	6.0	10	50 pA	50	4.0	13	±5.0	±18	Low Noise, JFET Input	P/626, JG/693
TL072BC	200 pA	3.0	10	50 pA	50	4.0	13	±5.0	±18	Low Noise, JFET Input	P/626, JG/693
TL072C	200 pA	10	10	50 pA	25	4.0	13	±5.0	±18	Low Noise, JFET Input	P/626, JG/693
TL082AC	200 pA	6.0	10	100 pA	50	4.0	13	±5.0	±18	JFET Input	P/626, JG/693
TL082BC	200 pA	3.0	10	100 pA	50	4.0	13	±5.0	±18	JFET Input	P/626, JG/693
TL082C	400 pA	15	10	200 pA	25	4.0	13	±5.0	±18	JFET Input	P/626, JG/693
Industrial Temperature Range (−25°C to +85°C)											
LM258	0.15	5.0	10	30	50	1.0	0.6	±1.5 ±3.0	±18 ±36	Split or Single Supply Op Amp	H, N/626, J/693
Automotive Temperature Range (−40°C to +85°C)											
LM2904	0.25	7.0	7.0	50	100 typ	1.0	0.6	±1.5 ±3.0	±13 ±26	Split or Single Supply Op Amp	H, N/626, J/693
MC3358	5.0	8.0	10	75	20	1.0	0.6	±1.5 ±3.0	±18 ±36	Split Supplies Single Supply	P1/626
MC33072	0.50	5.0	10	75	25	4.5	10	+3.0	+44	High Performance,	P/626, U
MC33072A	500 nA	3.0	10	50	50	4.5	10	+3.0	+44	Single Supply	P/626, U
MC33077	1.0	1.0	2.0	180	150	37	11	±2.5	±18	Dual, Low Noise	P/626
MC33078	750 nA	2.0	2.0	150	31.6	16	7.0	±5.0	±18	Low Noise	N/626
MC33172	0.10	4.5	10	20	50	1.8	2.1	+3.0	+44	Low Power, Single Supply	P/626
MC33182	0.1 nA	3.0	10	0.05	25	4.0	10	±2.5	±18	Low Power JFET Input	P/626
MC33282	100 pA	200μV	5.0	50 pA	50	30	12	±2.5	±18	Low Input Offset JFET	P/646
TL062V	200 pA	6.0	10	100 pA	4.0	2.0	6.0	±2.5	±18	Low Power JFET Input	P/626
Military Temperature Range (−55°C to +125°C)											
LM158	0.15	5.0	10	30	50	1.0	0.6	±1.5 +3.0	±18 +36	Split Supplies Single Supply (Low Power Consumption)	H, J/693
MC1558	0.5	5.0	10	200	50	1.1	0.8	±3.0	±22	Dual MC1741	G/601, U
MC1558S	0.5	5.0	10	200	50	1.0	10	±3.0	±22	High Slew Rate	G/601, U
MC1747	0.5	5.0	10	200	50	1.0	0.5	±3.0	±22	Dual MC1741	G/601, L
MC3558	0.5	5.0	10	50	50	1.0	0.6	±1.5 +3.0	±18 +36	Split Supplies Single Supply	G/601, U
MC4558	0.5	5.0	10	200	50	2.8	1.6	±3.0	±22	High Frequency	G/601, U
MC35002	100 pA	10	10	100 pA	25	4.0	13	±5.0	±22	JFET Input	G/601, U
MC35002A	75 pA	2.0	10	25 pA	50	4.0	13	±5.0	±22	JFET Input	G/601, U
MC35002B	100 pA	5.0	10	50 pA	50	4.0	13	±5.0	±22	JFET Input	G/601, U
MC35072	0.50	5.0	10	75	25	4.5	10	+3.0	+44	High Performance,	U
MC35072A	500 nA	3.0	10	50	50	4.5	10	+3.0	+44	Single Supply	U
MC35082	200 pA	3.0	10	100 pA	25	8.0	30	±5.0	±22	High Speed, JFET Input	U
MC35082A	200 pA	1.0	10	100 pA	50	8.0	30	±5.0	±22	High Speed, JFET Input	U

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Dual Operational Amplifiers (continued)

Device	I_{IB} μA Max	V_{IO} mV Max	TC_{VIO} μV/°C Typ	I_{IO} nA Max	A_{vol} V/mV Min	BW ($A_V=1$) MHz Typ	SR ($A_V=1$) V/μs Typ	Supply Voltage V Min	Supply Voltage V Max	Description	Package Suffix
Military Temperature Range (−55°C to +125°C)											
MC35083	200 pA	3.0	10	100 pA	25	16	55	±5.0	±22	Decompensated	U
MC35083A	200 pA	1.0	10	100 pA	50	16	55	±5.0	±22	MC35082 for $A_V \geq 2$	U
MC35172	0.10	4.5	10	20	50	1.8	2.1	+3.0	+44	Low Power, Single Supply	U
MC35182	0.1 nA	3.0	10	0.05	25	4.0	10	±2.5	±18	Low Power JFET Input	U
TL062M	200 pA	6.0	10	100 pA	4.0	2.0	6.0	±2.5	±18	Low Power JFET Input	JG
TL072M	200 pA	6.0	10	50 pA	35	4.0	13	±5.0	±18	Low Noise JFET Input	JG
TL082M	200 pA	6.0	10	100 pA	25	4.0	13	±5.0	±18	JFET Input	JG

Quad Operational Amplifiers

Device	I_{IB} μA Max	V_{IO} mV Max	TC_{VIO} μV/°C Typ	I_{IO} nA Max	A_{vol} V/mV Min	BW ($A_V=1$) MHz Typ	SR ($A_V=1$) V/μs Typ	Supply Voltage V Min	Supply Voltage V Max	Description	Package Suffix
Internally Compensated											
Commercial Temperature Range (0°C to +70°C)											
LF347	200 pA	10	10	100 pA	25	4.0	13	±5.0	±18	JFET Input	N/646
LF347B	200 pA	5.0	10	100 pA	50	4.0	13	±5.0	±18	JFET Input	N/646
LF444C	100 pA	10	10	50 pA	25	2.0	6.0	±5.0	±18	Low Power JFET Input	N/646
LM324	0.25	6.0	7.0	50	25	1.0	0.6	±1.5 +3.0	±16 +32	Low Power Consumption	J/632, N/646
LM348	0.20	6.0	—	50	25	1.0	0.5	±3.0	±18	Quad MC1741	J/632, N/646
MC3401/ LM3900	0.3	—	—	—	1.0	5.0	0.6	±1.5 +3.0	±18 +36	Norton Input	J/632, N/646
MC3403	0.5	10	7.0	50	20	1.0	0.6	±1.5 +3.0	±18 +36	No Crossover Distortion	L, P/646
MC4741C	0.5	6.0	15	200	20	1.0	0.5	±3.0	±18	Quad MC1741	L, P/646
MC34004	200 pA	10	10	100 pA	25	4.0	13	±5.0	±18	JFET Input	L, P/646
MC34004B	200 pA	5.0	10	100 pA	50	4.0	13	±5.0	±18	JFET Input	L, P/646
MC34074	0.50	5.0	10	75	25	4.5	10	+3.0	+44	High Performance,	L, P/646
MC34074A	500 nA	3.0	10	50	50	4.5	10	+3.0	+44	Single Supply	L, P/646
MC34084	200 pA	12	10	100 pA	25	8.0	30	±5.0	±22	High-Speed, JFET Input	P/646
MC34084A	200 pA	6.0	10	100 pA	50	8.0	30	±5.0	±22	High-Speed, JFET Input	P/646
MC34085	200 pA	12	10	100 pA	25	16	55	±5.0	±22	Decompensated	P/646
MC34085A	200 pA	6.0	10	100 pA	50	16	55	±5.0	±22	MC34084 for $A_V \geq 2$	P/646
MC34184	0.1 nA	10	10	0.05	25	4.0	10	±2.5	±18	Low Power JFET Input	P/646
TL064AC	200 pA	6.0	10	100 pA	4.0	2.0	6.0	±2.5	±18	Low Power JFET Input	N/646
TL064BC	200 pA	3.0	10	100 pA	4.0	2.0	6.0	±2.5	±18	Low Power JFET Input	N/646
TL064C	200 pA	15	10	200 pA	4.0	2.0	6.0	±2.5	±18	Low Power JFET Input	N/646
TL074AC	200 pA	6.0	10	50 pA	50	4.0	13	±5.0	±18	Low Noise JFET Input	J/632, N/646
TL074C	200 pA	10	10	50 pA	25	4.0	13	±5.0	±18	Low Noise JFET Input	J/632, N/646
TL084AC	200 pA	6.0	10	100 pA	50	4.0	13	±5.0	±18	JFET Input	J/632, N/646
TL084BC	200 pA	3.0	10	100 pA	50	4.0	13	±5.0	±18	JFET Input	J/632, N/646
TL084C	400 pA	15	10	200 pA	25	4.0	13	±5.0	±18	JFET Input	J/632, N/646
Industrial Temperature Range (−25°C to +85°C)											
LM224	0.15	5.0	7.0	30	50	1.0	0.6	±1.5 ±3.0	±16 ±32	Split or Single Supply Op Amp	J/632, N/646
LM248	0.20	6.0	—	50	25	1.0	0.5	±3.0	±18	Quad MC1741	J/632, N/646
Automotive Temperature Range (−40°C to +85°C)											
LM2902	0.5	10	—	50	—	1.0	0.6	±1.5 +3.0	±13 +26	Differential Low Power	N/646

Quad Operational Amplifiers (continued)

Device	I_{IB} μA Max	V_{IO} mV Max	TC_{VIO} μV/°C Typ	I_{IO} nA Max	A_{vol} V/mV Min	BW (A_V = 1) MHz Typ	SR (A_V = 1) V/μs Typ	Supply Voltage V Min	Supply Voltage V Max	Description	Package Suffix
Automotive Temperature Range (−40°C to +85°C) (continued)											
MC3301/ LM2900	0.3	—	—	—	1.0	4.0	0.6	±2.0 +4.0	±15 +28	Norton Input	P/646 N/646
MC3303	0.5	8.0	10	75	20	1.0	0.6	±1.5 +3.0	±18 +36	Differential General Purpose	P/646
MC33074	0.50	5.0	10	75	25	4.5	10	+3.0	+44	High Performance, Single Supply	L, P/646
MC33074A	500 nA	3.0	10	50	50	4.5	10	+3.0	+44	Quad High Performance	L, P/646
MC33079	750 nA	2.5	2.0	150	31.6	16	7.0	±5.0	±18	Quad Low Noise	N/646
MC33174	0.10	4.5	10	20	50	1.8	2.1	+3.0	+44	Low Power, Single Supply	P/646
MC33184	0.1 nA	10	10	0.05	25	4.0	10	±2.5	±18	Low Power JFET Input	P/646
MC33284	100pA	200μV	5.0	50pA	50	30	12	±2.5	±18	Low Input Offset JFET	P/646
TL064V	200 pA	9.0	10	100 pA	4.0	2.0	6.0	±2.5	±18	Low Power JFET Input	N/646
Telecommunications Temperature Range (−40°C to +85°C)											
MC143403	1.0 nA	30	—	200 pA	45 dB	0.8	1.5	4.75	12.6	CMOS, Low Power, Drives Low-Impedance Loads	L, P/646
MC143404	1.0 nA	30	—	200 pA	60 dB	0.8	1.0	4.75	12.6	CMOS, Very Low Power	L, P/646
Military Temperature Range (−55°C to +125°C)											
LM124	0.15	5.0	7.0	30	50	1.0	0.6	±1.5 +3.0	±16 +32	Low Power Consumption	J/632, N/646
LM148	0.10	5.0	—	25	50	1.0	0.5	±3.0	±18	Quad MC1741	J/632
MC3503	0.5	5.0	7.0	50	50	1.0	0.6	±1.5 +3.0	±18 +36	General Purpose Low Power	L, P/646
MC4741	0.5	5.0	15	200	50	1.0	0.5	±3.0	±22	Quad MC1741	L
MC35004	100 pA	10	10	100 pA	25	4.0	13	±5.0	±22	JFET Input	L
MC35004B	100 pA	5.0	10	50 pA	50	4.0	13	±5.0	±22	JFET Input	L
MC35074	0.50	5.0	10	75	25	4.5	10	+3.0	+44	High Performance, Single Supply	L
MC35074A	500 nA	3.0	10	50	50	4.5	10	+3.0	+44	Quad High Performance	L
MC35084	200 pA	12	10	100 pA	25	8.0	30	±5.0	±22	High Speed, JFET Input	L
MC35084A	200 pA	6.0	10	100 pA	50	8.0	30	±5.0	±22	High Speed, JFET Input	L
MC35085	200 pA	12	10	100 pA	25	16	55	±5.0	±22	Decompensated	L
MC35085A	200 pA	6.0	10	100 pA	50	16	55	±5.0	±22	MC35084 for $A_V \geq 2$	L
MC35174	0.10	4.5	10	20	50	1.8	2.1	+3.0	+44	Low Power, Single Supply	L
MC35184	0.1 nA	10	10	0.05	25	4.0	10	±2.5	±18	Low Power JFET Input	L
TL064M	200 pA	9.0	10	100 pA	4.0	2.0	6.0	±2.5	±18	Low Power JFET Input	J/632
TL074M	200 pA	9.0	10	50 pA	35	4.0	13	±5.0	±18	Low Noise JFET Input	J/632
TL084M	200 pA	9.0	10	100 pA	25	4.0	13	±5.0	±18	JFET Input	J/632

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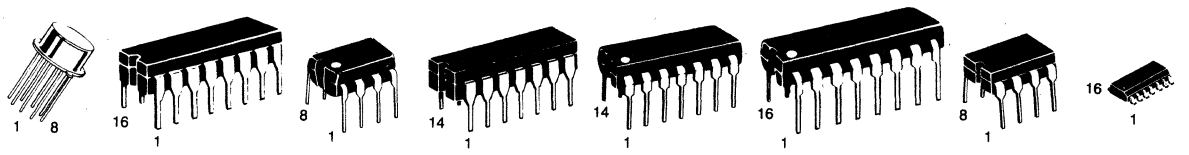
Comparators



CASE 601 METAL **H SUFFIX** | CASE 620 CERAMIC **L SUFFIX** | CASE 626 PLASTIC **N SUFFIX** | CASE 632 CERAMIC **J SUFFIX** | CASE 646 PLASTIC **N SUFFIX** | CASE 648 PLASTIC **P SUFFIX** | CASE 693 CERAMIC **J-8 SUFFIX** | CASE 751B PLASTIC **D SUFFIX**

Device	I_{IB} μA Max	V_{IO} mV Max	I_{IO} μA Max	A_V V/V Typ	I_O mA Min	Response Time ns	Supply Voltage V	Description	Temperature Range (°C)	Package Suffix
Single										
BIPOLAR										
LM111	0.10	3.0	0.01	200K	8.0	200	+15, −15	With strobe, will operate from single supply	−55 to +125	H, J-8
LM211	0.10	3.0	0.01	200K	8.0	200	+15, −15		−25 to +85	H, J-8
LM311	0.25	7.5	0.05	200K	8.0	200	+15, −15		0 to +70	H, N/626, J-8
CMOS										
MC14578	1.0 pA	50	—	—	1.1	—	+3.5 to +14	Requires only 10 μA from single-ended supply	−30 to +70	D/751B, P/648
Dual										
BIPOLAR										
LM193	0.10	5.0	0.025	200K	6.0	1300	±1.5 to ±18 or +3.0 to +36	Designed for single or split supply operation, input common mode includes ground (negative supply)	−55 to +125	H
LM193A	0.10	2.0	0.025	200K	6.0	1300			−55 to +125	H
LM293	0.25	5.0	0.050	200K	6.0	1300			−25 to +85	H
LM293A	0.25	2.0	0.050	200K	6.0	1300			−25 to +85	H
LM393	0.25	5.0	0.050	200K	6.0	1300			0 to +70	H, N/626
LM393A	0.25	2.0	0.050	200K	6.0	1300			0 to +70	H, N/626
LM2903	0.25	7.0	0.050	200K	6.0	1500			−40 to +85	N/626
MC3405	0.5	10	0.050	200K	6.0	1300	±1.5 to ±7.5 or +3.0 to 15	This device contains two op amps and two comparators in a single package	0 to +70	L/632, P/646
MC3505	0.5	5.0	0.050	200K	6.0	1300			−55 to +125	L/632
CMOS										
MC14575	0.001	30	0.0001	20K	3.0	1000	±1.5 to ±7.5 or +3.0 to 15	This device contains two op amps and two comparators in a single package	−40 to +85	P/648 D/751B
Quad										
BIPOLAR										
LM139	0.10	5.0	0.025	200K	6.0	1300	±1.5 to ±18 or +3.0 to +36	Designed for single or split supply operation, input common mode includes ground (negative supply)	−55 to +125	J
LM139A	0.10	2.0	0.025	200K	6.0	1300			−55 to +125	J
LM239	0.25	5.0	0.050	200K	6.0	1300			−25 to +85	J, N/646
LM239A	0.25	2.0	0.050	200K	6.0	1300			−25 to +85	J, N/646
LM339	0.25	5.0	0.050	200K	6.0	1300			0 to +70	J, N/646
LM339A	0.25	2.0	0.050	200K	6.0	1300			0 to +70	J, N/646
LM2901	0.25	7.0	0.050	100K	6.0	1300			−40 to +85	N/646
MC3302	0.50	20	0.500	30K	6.0	1300			−40 to +85	N/646
MC3430	40	6.0	1.0 Typ	1.2K	16	33	+5.0, −5.0	High speed comparator/ sense-amplifier	0 to +70	L, P
MC3431	40	10	1.0 Typ	1.2K	16	33	+5.0, −5.0		0 to +70	L, P
MC3432	40	6.0	1.0 Typ	1.2K	16	40	+5.0, −5.0		0 to +70	L, P
MC3433	40	10	1.0 Typ	1.2K	16	40	+5.0, −5.0		0 to +70	L, P
CMOS										
MC14574	0.001	30	0.0001	20K	3.0	1000	±1.5 to ±7.5 or +3.0 to +15	Externally programmable power dissipation with one or two resistors	−40 to +85	P/648 D/751B

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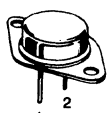
Power Supply Circuits

Linear Voltage Regulators

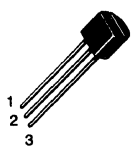
Fixed Output

These low cost monolithic circuits provide positive and/or negative regulation at currents from 100 mA to 3.0 A. They are ideal for on-card regulation employing current limiting and thermal shutdown. Low V_{diff} devices are offered for battery powered systems.

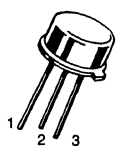
Although designed primarily as fixed voltage regulators, these devices can be used with external components to obtain adjustable voltages and currents.



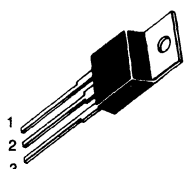
CASE 1
METAL
K SUFFIX



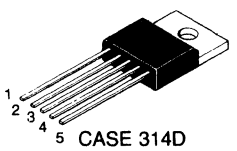
CASE 29
PLASTIC
P, Z SUFFIX



CASE 79
METAL
G, H SUFFIX



CASE 221A
PLASTIC POWER
T, KC SUFFIX



CASE 314D
PLASTIC
T SUFFIX

Fixed-Voltage, 3-Terminal Regulators for Positive or Negative Polarity Power Supplies

V_{out} Volts	Tol.† Volts	I_O mA Max	Device Positive Output	Device Negative Output	V_{in} Min/Max	Reg_{line} mV	Reg_{load} mV	$\Delta V_O/\Delta T$ mV/°C Typ	Case Suffix
5	±0.5	100	LM2931-5.0	—	5.6/40	30	50	1.0	Z, T
	±0.25		MC78L05C	MC79L05C	6.7/30	200	60		P, G
			LM2931A-5.0	—	5.6/40	30	50		Z, T
			MC78L05AC	MC79L05AC	6.7/30	150	60		P, G
		500	MC78M05C	MC79M05C	7/35	100	100	1.0	G, T
	±0.4	1500	LM109	—				1.1	K, H
			LM209	—					
	±0.25		LM309	—		50		1.0	
	±0.35		MC7805*	—	8.0/35			0.6	K
	±0.25		MC7805B#	—	8/35	100		1.0	T
			MC7805C	MC7905C	7/35				K, T
	±0.2		MC7805A*	—	7.5/35	10	50	0.6	K
			MC7805AC	MC7905AC			100		K, T
	±0.25		LM140-5*	—	7.0/35	50	50		K
	±0.2		LM140A-5*	—		10	25		
	±0.25		LM340-5	—		50	50		K, T
	±0.2		LM340A-5	—		10	25		
	±0.1		TL780-05C	—	7.0/35	5.0	25	0.06	KC
	±0.25	3000	MC78T05C	—	7.3/35	25	30	0.1	K, T
	±0.2		MC78T05AC	—		10	25		

#T_J = −40° to +125°C †Output Voltage Tolerance for Worst Case *T_J = −55° to +150°C (continued)

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Fixed Output Voltage Regulators (continued)

V_{out} Volts	Tol.† Volts	I_O mA Max	Device Positive Output	Device Negative Output	V_{in} Min/Max	Reg_{line} mV	Reg_{load} mV	$\Delta V_O/\Delta T$ mV/°C Typ	Case Suffix
5	±0.4	3000	LM123*	—	7.5/20	25	100	0.1	K
			LM223	—					
	±0.25		LM323	—					T
	±0.2		LM123A	—					K
			LM223A	—		15	50		
			LM323A	—					T
5.2	±0.26	1500	—	MC7905.2C	7.2/35	105	105	1.0	T
6	±0.3	500	MC78M06C	—	8/35	100	120	1.0	T
	±0.35	1500	MC7806*	—	9/35	60	100	0.7	K
	±0.3		MC7806B#	—		120	120		T
			MC7806C	MC7906C	8/35				K, T
	±0.24		MC7806AC	—	8.6/35	11	100		T
			LM140-6*	—	8/35	60	60		K
	±0.3		LM340-6	—					K, T
8	±0.8	100	MC78L08C	—	9.7/30	200	80	—	P, G
			MC78L08AC	—		175			
	±0.4	500	MC78M08C	—	10/35	100	160	1.0	G, T
		1500	MC7808*	—	11.5/35	80	100		K
			MC7808B#	—		160	160		T
			MC7808C	MC7908C	10.5/35				K, T
	±0.3		MC7808AC	—	10.6/35	13	100		T
	±0.4		LM140-8*	—	10.5/35	80	80		K
			LM340-8	—					K, T
		3000	MC78T08C	—	10.4/35	35	30	0.16	
12	±1.2	100	MC78L12C	MC79L12C	13.7/35	250	100	—	P, G
	±0.6		MC78L12AC	MC79L12AC					
		500	MC78M12C	MC79M12C	14/35	100	240	1.0	G, T
		1500	MC7812*	—	15.5/35	120	120	1.5	K
			MC7812B#	—		240	240		T
			MC7812C	MC7912C	14.5/35				K, T
	±0.5		MC7812A*	—	14.8/35	18	50		K
			MC7812AC	—			100		T
	±0.6		LM140-12*	—	14.5/35	120	120	1.5	K
	±0.5		LM140A-12*	—		18	32		
	±0.6		LM340-12	—		120	120		K, T
	±0.5		LM340A-12	—		18	32		
	±0.24		TL780-12C	—		5.0		0.15	KC
	±0.6	3000	MC78T12C	—	14.5/35	45	30	0.24	K, T
	±0.5		MC78T12AC	—		18	25		

#T_J = −40° to +125°C †Output Voltage Tolerance for Worst Case *T_J = −55° to +150°C

(continued)

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Fixed Output Voltage Regulators (continued)

V_{out} Volts	Tol.† Volts	I_O mA Max	Device Positive Output	Device Negative Output	V_{in} Min/Max	Reg_{line} mV	Reg_{load} mV	$\Delta V_O/\Delta T$ mV/°C Typ	Case Suffix
15	±1.5	100	MC78L15C	MC79L15C	16.7/35	300	150	—	P, G
	±0.75		MC78L15AC	MC79L15A					
		500	MC78M15C	MC79M15C	17/35	100	300	1.0	G, T
		1500	MC7815*	—	18.5/35	150	150	1.8	K
			MC7815B#	—		300	300		T
			MC7815C	MC7915C	17.5/35				K, T
	±0.6		MC7815A*	—	17.9/35	22	50		K
			MC7815AC	—			100		K, T
	±0.75		LM140-15*	—	17.5/35	150	150		K
	±0.6		LM140A-15*	—		22	35		
	±0.75		LM340-15	—		150	150		K, T
	±0.6		LM340A-15	—		22	35		
	±0.3		TL780-15C	—		15	60	0.18	KC
	±0.75	3000	MC78T15C	—	17.5/40	55	30	0.3	K, T
	±0.6		MC78T15AC	—		22	25		
18	±1.8	100	MC78L18C	MC79L18C	19.7/35	325	170	—	P
	±0.9		MC78L18AC	MC79L18AC					
		500	MC78M18C	—	20/35	100	360	1.0	G, T
		1500	MC7818*	—	22/35	180	180	2.3	K
			MC7818B#	—		360	360		T
	±0.7		MC7818C	MC7918C	21/35				K, T
			MC7818AC	—		31	100		T
	±0.9		LM340-18	—		180	180		T
20	±1.0	500	MC78M20C	—	22/40	10	400	1.1	G, T
24	±2.4	100	MC78L24C	MC79L24C	25.7/40	350	200	—	P
	±1.2		MC78L24AC	MC79L24AC		300			
		500	MC78M24C	—	26/40	100	480	1.2	G, T
		1500	MC7824*	—	28/40	240	240	3.0	K
			MC7824B#	—		480	480		T
			MC7824C	MC7924C	27/40				K, T
	±1.0		MC7824AC	—	27.3/40	36	100		T
	±1.2		LM340-24	—		240	240		T

#T_J = −40° to +125°C †Output Voltage Tolerance for Worst Case *T_J = −55° to +150°C

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Adjustable Output Voltage Regulators

Motorola offers a broad line of adjustable output voltage regulators with a variety of output current capabilities. Adjustable voltage regulators provide users the capability of stocking a single integrated circuit providing a wide range of output voltages for industrial and communications applications. The three-terminal devices require only two external resistors to set the output voltage.

Positive Output Regulators

I_O mA Max	Device	Suffix	V_{out} Volts Min	V_{out} Volts Max	V_{in} Volts Min	V_{in} Volts Max	$V_{in}-V_{out}$ Differential Volts Min	P_D Watts Max T_A = 25°C	P_D Watts Max T_C = 25°C	Regulation % V_{out} @ T_A = 25°C Max Line	Regulation % V_{out} @ T_A = 25°C Max Load	TC V_{out} Typ %/°C	T_J = °C Max	Case
100	LM317L	H,Z	1.2	37	5.0	40	3.0	Internally Limited		0.04	0.5	0.006	125	29,79
	LM217L#									0.02	0.3	0.004	150	
	LM117L*											0.003		
	LM2931C	T	3.0	24	3.16		0.6			0.15	1.0	—	125	314D
150	MC1723	CP	2.0	37	9.5	40	3.0	1.25	—	0.1	0.3	0.003	150	646
		CG						1.0	2.1			0.003		603C
		G										0.002		
		CL						1.5	—			0.003	175	632
		L							—			0.002		
500	LM317M	T	1.2	37	5.0	40	3.0	Internally Limited		0.04	0.5	0.0056	125	221A
1500	LM317	T	1.2	37	5.0	40	3.0	Internally Limited		0.04	0.5	0.006	125	221A
	LM317	H, K												79, 1
	LM217#											0.004		
	LM117*									0.02	0.3	0.003	150	
3000	LM350	T	1.2	33	5.0	36	3.0	Internally Limited		0.03	0.5	0.008	125	221A
	LM350	K												1
	LM250#									0.01	0.3	0.0057	150	
	LM150*											0.0051		

Negative Output Regulators

I_O mA Max	Device	Suffix	V_{out} Volts Min	V_{out} Volts Max	V_{in} Volts Min	V_{in} Volts Max	$V_{in}-V_{out}$ Differential Volts Min	P_D Watts Max T_A = 25°C	P_D Watts Max T_C = 25°C	Regulation % V_{out} @ T_A = 25°C Max Line	Regulation % V_{out} @ T_A = 25°C Max Load	TC V_{out} Typ %/°C	T_J = °C Max	Case
500	LM337M	T	−1.2	−37	5.0	40	3.0	Internally Limited		0.04	1.0	0.0048	125	221A
1500	LM337	T	−1.2	−37	5.0	40	3.0	Internally Limited		0.04	1.0	0.0048	125	221A
	LM337	H, K												79, 1
	LM237#									0.02	0.5	0.0034	150	
	LM137*											0.0031		

#T_J = −25° to +150°C *T_J = −55° to +150°C

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Switching Regulators

Used as a control circuit in PWM, push-pull, bridge and series type Switchmode supplies, the devices include a voltage reference, oscillator, pulse-width modulator, phase splitter and output drive sections. Frequency and duty cycle are independently adjustable. Most of these devices also include one or two on-chip error amplifiers for voltage or current error signal feedback.

Single-Ended Controllers

These single-ended voltage- and current-mode controllers are designed for use in buck, boost, flyback, and forward converters. They are cost effective in applications that range from 0.1 to 200 watts power output.

I_O mA Max	V_{CC} Volts		V/I Operating Mode	Ref. Volts	Max Osc. Freq. (kHz)	Device	Suffix	T_A °C	Case
	Min	Max							
250	7.0	40	V	5.0 ± 5.0%	200	MC34060	P	0 to +70	646
							L		632
						MC35060	L	−55 to +125	
500				5.0 ± 1.5%		MC34060A	D	0 to +70	751A
							P		646
						MC33060A	D	−40 to +85	751A
							P		646
						MC35060A	L	−55 to +125	632
1000	4.2	12	I	1.25 ± 2.0%	300	MC34129	D	0 to +70	751A
							P		646
						MC33129	D	−40 to +85	751A
							P		646
	11.5	30		5.0 ± 2.0%	500	UC3842A	D	0 to +70	751A
							N		626
	11			5.0 ± 1.0%		UC2842A	D	−25 to +85	751A
							J		693
							N		626
	8.2			5.0 ± 2.0%		UC3843A	D	0 to +70	751A
							N		626
				5.0 ± 1.0%		UC2843A	D	−25 to +85	751A
							J		693
							N		626
1500	2.5	40	V	1.24 ± 5.2%#	100	μA78S40	PC	0 to +70	648
							DC		620
							PV	−40 to +85	648
							DM	−55 to +125	620
				1.25 ± 5.6%#		MC34063	P1	0 to +70	626
							U		693
						MC33063	P1	−40 to +85	626
							U		693
						MC35063	U	−55 to +125	
				1.25 ± 2.0%		MC34063A	D	0 to +70	751
							P1		626
						MC33063A	D	−40 to +85	751
							P1		626
						MC35063A	U	−55 to +125	693

Tolerance applies over the specified operating temperature range.

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Double-Ended Controllers

These double-ended voltage-mode controllers are designed for use in push-pull, half-bridge, and full-bridge converters. They are cost effective in applications that range from 100 to 2000 watts power output.

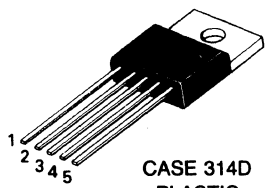
I_O mA Max	V_{CC} Volts Min	V_{CC} Volts Max	V/I Operating Mode	Ref. Volts	Max Osc. Freq. (kHz)	Device	Suffix	T_A °C	Case
500	7.0	40	V	5.0 ± 5.0%#	200	TL494	CN	0 to +70	648
							CJ		620
							IN	−25 to +85	648
							IJ		620
							MJ	−55 to +125	
				5.0 ± 1.5%	300	TL594	CN	0 to +70	648
							IN	−25 to +85	
							MJ	−55 to +125	620
±500	8.0			5.1 ± 2.0%	400	SG3525A	N	0 to +70	648
							J		620
				5.1 ± 1.0%		SG2525A	N	−25 to +85	648
							J		620
						SG1525A	J	−55 to +125	
				5.1 ± 2.0%		SG3527A	N	0 to +70	648
							J		620
				5.1 ± 1.0%		SG2527A	N	−25 to +85	648
							J		620
						SG1527A	J	−55 to +125	
±200				5.0 ± 2.0%	350	SG3526	N	0 to +125*	707
							J		726
				5.0 ± 1.0%		SG2526	N	−25 to +150*	707
							J		726
						SG1526	J	−55 to +150*	

*Junction Temperature Range
#Tolerance applies over the specified operating temperature range.

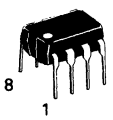
Motorola Semiconductor

Power Controllers

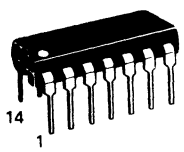
An assortment of battery and ac line-operated control ICs for specific applications are shown. They are designed to enhance system performance and reduce complexity in a wide variety of control applications.



CASE 314D
PLASTIC
T SUFFIX



CASE 626
PLASTIC



CASE 646
PLASTIC
P SUFFIX

Zero Voltage Switches

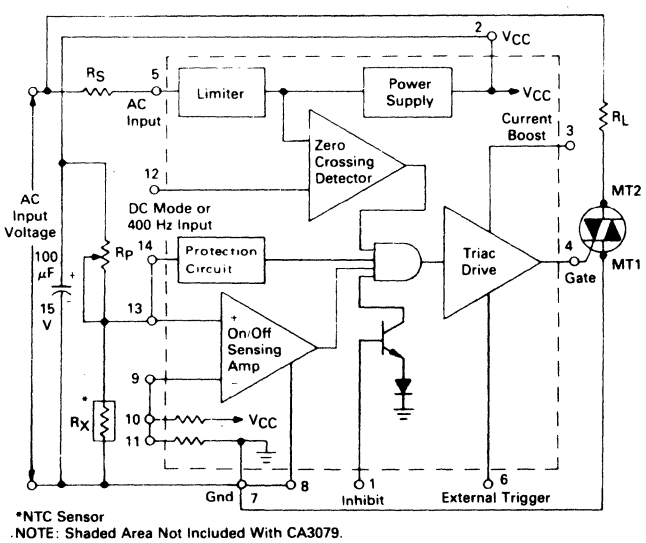
CA3079P/CA3059P

T_A = −40° to +85°C, Case 646

. . . designed for thyristor control in a variety of ac power switching applications for ac input voltages of 24 V, 120 V, 208/230 V, and 227 V @ 50/60 Hz. Features include:

- Limiter-Power Supply — Allows operation directly from an ac line.
- Differential On/Off Sensing Amplifier — Tests for condition of external sensors or input command signals. Proportional control capability or hysteresis may be implemented.
- Zero-Crossing Detector — Synchronizes the output pulses to the zero voltage point of the ac cycle. Eliminates RFI when used with resistive loads.
- Triac Drive — Supplies high-current pulses to the external power controlling thyristor.
- Protection Circuit (CA3059 only) — A built-in circuit may be actuated, if the sensor opens or shorts, to remove the drive circuit from the external triac.
- Inhibit Capability (CA3059 only) — Thyristor firing may be inhibited by the action of an internal diode gate.
- High Power DC Comparator Operation (CA3059 only) — Operation in this mode is accomplished by connecting Pin 7 to Pin 12 (thus overriding the action of the zero-crossing detector).

CA3079



*NTC Sensor
NOTE: Shaded Area Not Included With CA3079.

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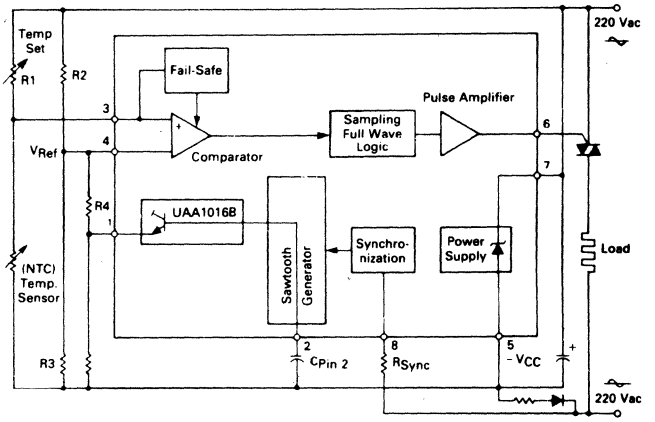
Zero Voltage Controller

UAA1016B — T_A = −20° to +100°C, Case 626

. . . designed to drive triacs with the Zero Voltage technique which allows RFI free power regulation of resistive loads. They provide the following features:

- Proportional Temperature Control Over an Adjustable Band
- Adjustable Burst Frequency (to Comply with Standards)
- Sensor Fail-Safe
- No dc Current Component Through the Main Line (to Comply with Standards)
- Negative Output Current Pulses (Triacs Quadrants 2 and 3)
- Direct ac Line Operation
- Low External Components Count

UAA1016B

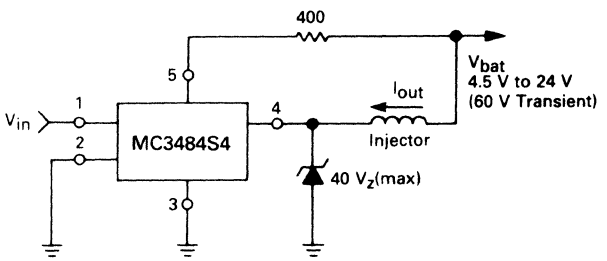


Integrated Solenoid Driver

MC3484S2,S4 — T_J = −40° to +125°C, Case 314D

The MC3484 is an integrated monolithic solenoid driver. Its typical function is to apply full battery voltage to fuel injector(s) for rapid current rise, in order to produce positive injector opening. When load current reaches a preset level (4.0 A in MC3484S4 or 2.4 A in MC3484S2) the injector driver reduces the load current by a 4-to-1 ratio and operates as a constant current supply. This condition holds the injector open and reduces system dissipation.

MC3484



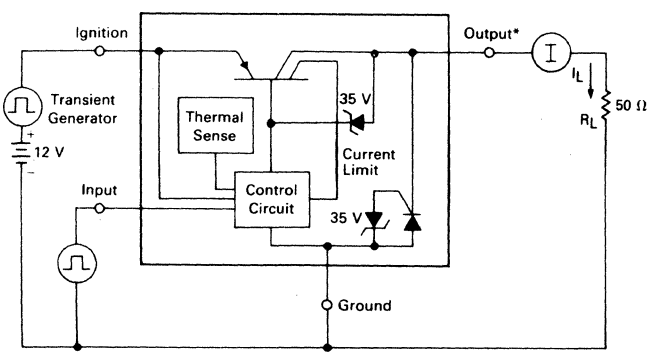
High-Side Driver Switch

MC3399T — T_J = −40° to +150°C, Case 314D

The MC3399T is a High-Side Driver Switch that is designed to drive loads from the positive side of the power supply. The output is controlled by a TTL compatible Enable pin. In the ON state, the device exhibits very low saturation voltages for load currents in excess of 750 mA. The device also protects the load from positive- or negative-going high voltage transients by becoming an open circuit and isolating the transient for its duration from the load.

The MC3399T is fabricated on a power BIMOS process which combines the best features of Bipolar and MOS technologies. The mixed technology provides higher gain PNP output devices and results in Power Integrated Circuits with reduced quiescent current.

MC3399T



NOTE:
*Depending on Load Current and Transient Duration, an Output Capacitor (C_O) of sufficient value may be used to hold up Output Voltage during the Transient, and absorb Turn-off Delay Voltage Overshoot.

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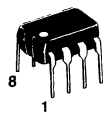
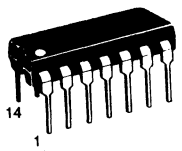
Motor Controllers

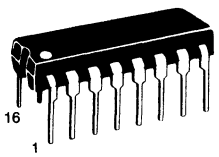
This section contains integrated circuits designed for cost effective control of specific motor-families. Included are controllers for dc servo, stepper, brushless, and universal type motors.



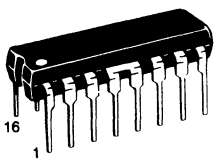
CASE 626
PLASTIC
P SUFFIX



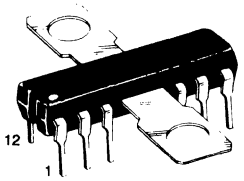
CASE 646
PLASTIC
P SUFFIX



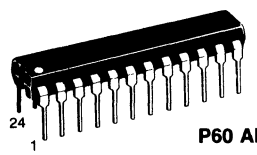
CASE 648
PLASTIC
P SUFFIX



CASE 648C
PLASTIC
P SUFFIX



CASE 721
PLASTIC



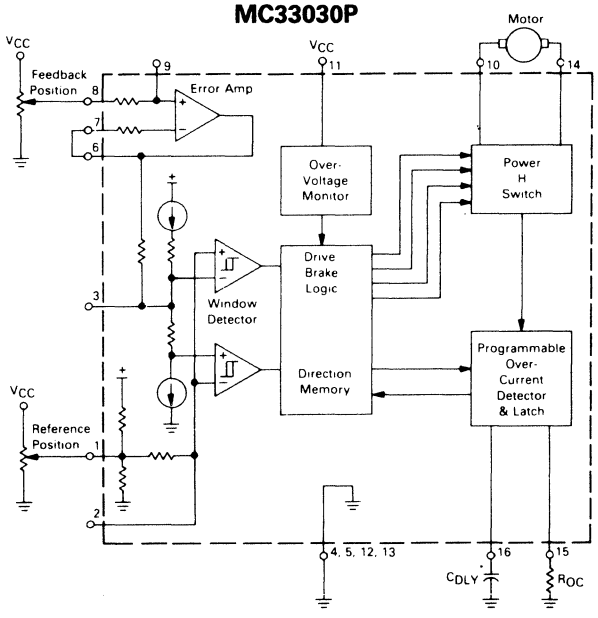
CASE 724
PLASTIC
P60 AND P120 SUFFIX

DC Servo Motor Controller/Driver

MC33030P — T_A = −40° to +85°C, Case 648C

A monolithic dc servo motor controller providing all active functions necessary for a complete closed loop system. This device consists of an on-chip op amp and window comparator with wide input common-mode range, drive and brake logic with direction memory, power H switch driver capable of 1.0 A, independently programmable over-current monitor and shutdown delay, and over-voltage monitor. This part is ideally suited for almost any servo positioning application that requires sensing of temperature, pressure, light, magnetic flux, or any other means that can be converted to a voltage.

MC33030P

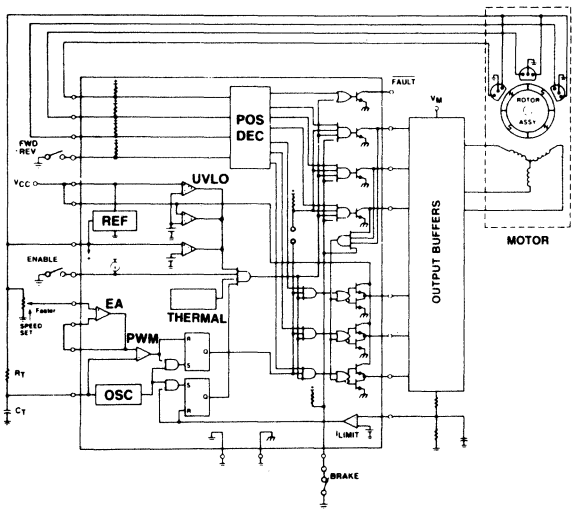


DC Brushless Motor Controller

MC33034P60,P120 — T_A = −40° to +85°C, Case 724

The MC33034 Series is a high performance monolithic brushless motor controller containing all of the active functions required to implement a full featured open-loop three or four phase motor control system. These devices consist of a rotor position decoder for proper commutation sequencing, temperature compensated reference capable of supplying sensor power, frequency programmable sawtooth oscillator, fully accessible error amplifier, pulse width modulator comparator, three open collector top drivers, and three high current totem pole bottom drivers ideally suited for driving power MOSFETs.

MC33034



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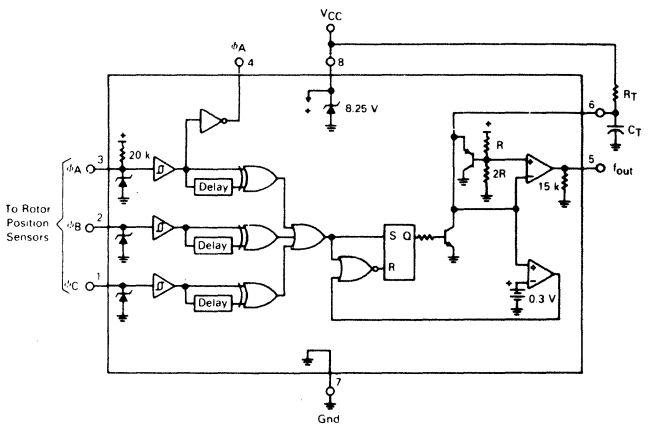
Closed-Loop Brushless Motor Adapter

MC33039P — T_A = −40° to +85°C, Case 626

The MC33039P is a high performance closed-loop speed control adapter specifically designed for use in dc brushless motor control systems. Implementation will allow precise speed regulation without the need for a magnetic or optical tachometer. This device contains three input buffers each with hysteresis for noise immunity, three digital edge detectors, a programmable monostable, and an internal shunt regulator. Also included is an inverter output for use in systems that require conversion of sensor phasing. Although this device is primarily intended for use with the MC33034 brushless motor controller, it can be used cost effectively in many other closed-loop speed control applications.

MC33039

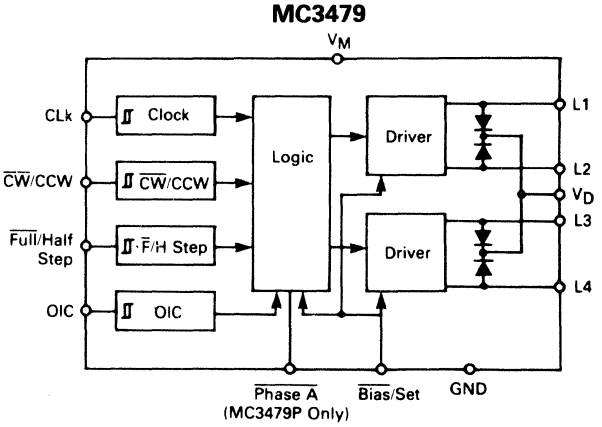


Stepper Motor Drivers

MC3479P — T_A = 0° to +70°C, Case 648C
SAA1042,A — T_A = 0° to +70°C, Case 721

Stepper Motor Drivers provide up to 500 mA of drive per coil for two phase 6.0 V to 24 V stepper motors. Control logic is provided to accept commands for clockwise, counter clockwise and half or full step operation. MC3479P has added Output Impedance Control (OIC) and Phase A drive state indicator (not available on SAA1042 devices).

MC3479



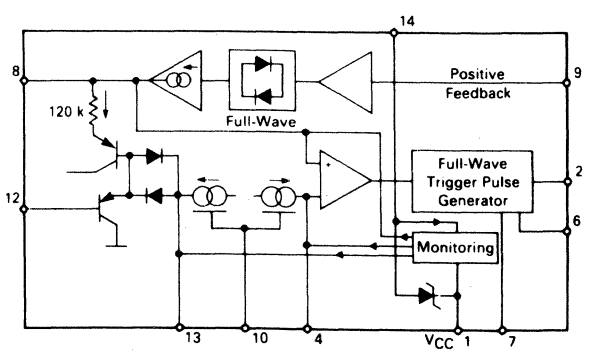
Triac Phase Angle Controller

TDA1185A T_A = 0° to +70°C, Case 646

. . . generates controlled triac triggering pulses and allows tacholess speed stabilization of universal motors by an integrated positive feedback function.

- Low Cost External Components Count
- Optimum Triac Firing (2nd and 3rd Quadrants)
- Repetitive Trigger Pulses When Triac Current is Interrupted by Motor Brush Bounce
- Triac Current Sensed to Allow Inductive Loads
- Soft Start
- Power Failure Detection and General Circuit Reset
- Low Power Consumption: 1.0 mA

TDA1185A



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Universal Motor Speed Controllers

TDA1085A T_A = 0° to +70°C, Case 648

. . . all the necessary functions for the speed control of universal (ac/dc) motors in an open or closed loop configuration. Facility for defining the initial speed/time characteristic. The circuits provide a phase angle varied trigger pulse to the motor control triac

- Guaranteed Full Wave Triac Drive
- Soft Start from Power-up
- On-Chip Frequency/Voltage Converter and Ramp Generator
- Current Limiting Incorporated
- Direct Drive from ac Line

TDA1085C T_A = −10° to +120°C, Case 648

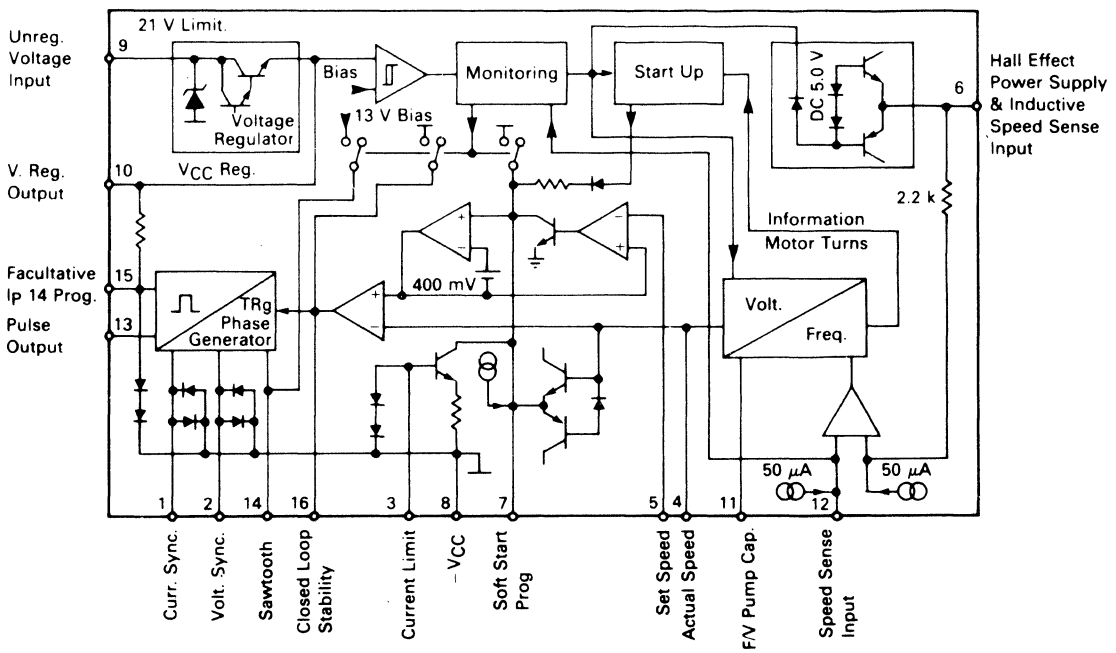
Similar to TDA1085A, but designed for commercial washing machine service.

TDA1285A T_A = 0° to +70°C, Case 648

Similar to TDA1085A, plus:

- Repeated Trigger Pulse if Triac Fails to Latch
- Over 65 mA Output Pulse Current
- Automatic Adaptation to Inductive or Hall Effect Sensors
- Sensor Circuit Continuity Detection

TDA1285A



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Data Conversion

The line of data conversion products which Motorola offers spans a wide spectrum of speed and resolution/accuracy. Features, including bus compatibility, minimize external parts count and provide easy interface to microprocessor systems. Various technologies, such as Bipolar and CMOS, are utilized to achieve functional capability, accuracy and production repeatability. Bipolar technology generally results in higher speed, while CMOS devices offer greatly reduced power consumption.

A-D Converters

CMOS

Resolution (Bits)	Device	Nonlinearity (Max)	Conversion Time	Input Voltage Range	Supplies (V)	Temperature Range	Package	Comments
8	MC145040	±1/2 LSB	10 μs	0 to V_{DD}	+5.0 ±10%	−40°C to +85°C	P/738 FN/775	Requires External Clock, 11-Ch MUX
	MC145041		20 μs					Includes Internal Clock, 11-Ch MUX
	MC14442		20 μs				P/710 FN/776	μP Compatible 11-Channel MUX S.A.R.
	MC14549B MC14559B	successive approximation registers			+3.0 to +18	−55°C to +125°C −40°C to +85°C	L/620 P/648	Compatible with MC1408 S.A.R. 8-bit D-A Converter
8–10	MC14443/47	±0.5% Full Scale	300 μs	Variable w/Supply	+5.0 to +18	−40°C to +85°C	P/648 DW/751G	μP Compatible, Single Slope, 6-Channel MUX
3-1/2 Digit	MC14433	±0.05% ±1 Count	40 ms	±2.0 V ±200 mV	+5.0 to +8.0 −2.8 to −8.0		P/709	Dual Slope

Bipolar

7	MC10321	±1/2 LSB	40 ns	0 to 2.0 V_{p-p} Max	+5.0 V and −3.0 V to −6.0 V	0°C to +70°C	P/738 DW/751D	Video Speed, Grey Code
8	MC10319	±1 LSB					L/623 P/709 DW/751F Die Form	Video Speed Flash Converter, Internal Grey Code
	MC6108	±1/2 LSB	1.8 μs	±5.0 V 0 to 5.0 V 0 to 10 V	+5.0, −5.2		P/710	μP Compatible, Three-State Outputs, includes Reference

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D-A Converters

CMOS

Resolution (Bits)	Device	Suffix	Accuracy @ 25°C (Max)	Max Settling Time (±1/2 LSB)	Supplies (V)	Temperature Range	Package	Comments
6	MC144110	P DW	—	—	+5.0 to +15	0°C to +85°C	707 751G	Serial input, Hex DAC, 6 outputs
	MC144111	P DW					646 751G	Serial input, Quad DAC, 4 outputs

Bipolar

8	DAC-08	Q	±1/2 LSB	150 ns	±4.5 to ±18	−55°C to +125°C	620	High-Speed Multiplying
		AQ	±1/4 LSB	135 ns				
		C	±1 LSB	150 ns		0°C to +70°C	620 648 D/751B	
		E	±1/2 LSB					
		H	±1/4 LSB	135 ns				
	MC1408	L6/P6	±2 LSB	300 ns Typ	+5.0, −5.0 to −15	0°C to +75°C	620 648	Multiplying
		L7/P7	±1 LSB					
		L8/P8	±1/2 LSB					
	MC1508	L8				−55°C to +125°C	620	
	MC10318	CL6	±2 LSB	10 ns Typ	−5.2	0°C to +70°C	620	ECL input Logic Levels Video Applications
		CL7	±1 LSB					
		L	±1/2 LSB				690	
		L9	±1/4 LSB					
4 x 3	MC10320	L		3 ns	+5.0, or ±5.0		733	125 MHz Color Graphics Triple DAC
	MC10320-1							90 MHz Color

A-D/D-A Converters

CMOS — For Telecommunications

Resolution (Bits)	Device	Monotonicity (Bits)	Conversion Time	Input Voltage Range	Supplies (V)	Temperature Range	Package	Comments
13	MC145402	13	62.5 μs	±3.28 V peak	±5.0 to 6.0	−40°C to +85°C	L/620	Digital signal processing (e.g., echo cancelling, high-speed modems, phone systems with conferencing)

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Communication Circuits

RF Communications

Narrowband Dual Conversion Receivers — FM/FSK — VHF

Type	V_{CC}	I_{CC}	Sensitivity	RF Input (Max)	IF1 (Max)	IF2 (limiter in)	Mute	RSSI	Max Data Rate	Notes	Package	Case Suffix
MC3362	2–7 V	3 mA	<1 μV	180 MHz	10.7 MHz	455 kHz	—	√	1.2 kb	Includes buffered VCO output	24 Pin DIP, SOIC	P/724 DW/751E
MC3363	2–7 V	4 mA	<1 μV	180 MHz	10.7 MHz	455 kHz	√	√	1.2 kb	Includes RF amp, mute	28 Pin SOIC	DW/751F

AM Receiver Medium/Short Wave

MC13041	6.5–16.5 V	25 mA	6 μV	10 MHz	455 kHz	—	—	√	—	Includes scan stop	20 Pin DIP	P/738 DW/751D

Wideband Data (FM/FSK) Receiver — VHF

Type	V_{CC}	I_{CC}	Sensitivity	IF1 (Max)	IF2 (limiter in)	Mute	RSSI	Max Data Rate	Notes	Package	Case Suffix
MC3356	3–9 V	25 mA	30 μV	200 MHz	10.7 MHz	√	√	500 kb	Includes front end mixer/L.O.	20 Pin DIP/PLCC	P/738 FN/775

Narrowband IF's — Wideband (FM/FSK) IF

MC3357	4–8 V	5 mA	5 μV	45 MHz	455 kHz	√	—	—		16 Pin DIP/SOIC	P/648 D/751B
MC3359	4–9 V	7 mA	2 μV	45 MHz	455 kHz	√	—	—		18 Pin DIP/SOIC	P/707 DW/751C
MC3361	2–8 V	6 mA	2 μV	60 MHz	455 kHz	√	—	—		16 Pin DIP/SOIC	P/648 D/751B
MC3367	1–5 V	1 mA	<1 μV	75 MHz	455 kHz	√	—	1.2 kb	1 Cell Operation	28 Pin SOIC	DW/751F
MC3371	2–8 V	6 mA	2 μV	60 MHz	455 kHz	√	√	—	(3Q88 Intro)	16 Pin DIP/SOIC	P/648 D/751B
MC13055	3–12 V	25 mA	20 μV	—	40 MHz	√	√	2 Mb	Wideband Data IF	16 Pin DIP/SOIC	P/648 D/751B

Transmitters — FM/FSK

Type	V_{CC}	I_{CC}	P_{out}	Max RF Freq. Out	Battery Check	Tone OSC	Max Mod. Freq.	Notes	Package	Case Suffix
MC2831A	3–8 Vdc	5 mA	−30 dBm	50 MHz	√	√	5.0 kHz (xtal ctl)	Includes low battery checker, tone osc.	16 Pin DIP/SOIC	P/648 D/751B
MC2833	3–8 Vdc	3 mA	−30 dBm to +10 dBm	150 MHz	—	—	5.0 kHz (xtal ctl)	Includes two frequency multiplier/amplifier transistors	16 Pin DIP/SOIC	P/648 D/751B

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Balanced Modulator/Demodulator

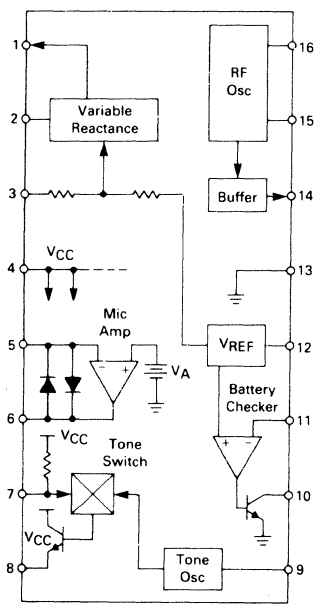
Type	V_{CC}	I_{CC}	Function	Package	Case Suffix
MC1596	5–30 V	10 mA	Carrier Balance >50 dB General purpose balanced modulator/ demodulator for AM, SSB, FM Detection	10 Pin Metal	G/603
MC1496	5–30 V	10 mA		14 Pin Ceramic DIL, DIP, SOIC	L/632 P/646 D/751A

Low Power FM Transmitter System

MC2831A — T_A = −30° to +75°C, Case 648, 751B

- Complete VHF FM Transmitter/Exciter
- Mike Preamp with Limiting
- Tone Generator for CTSS or AFSK
- Crystal or L-C VCO Operation
- Buffer/Multiplier Output Stage
- Low Voltage (internal reference) Warning Circuit
- Easily Partitioned for Semicustom Applications

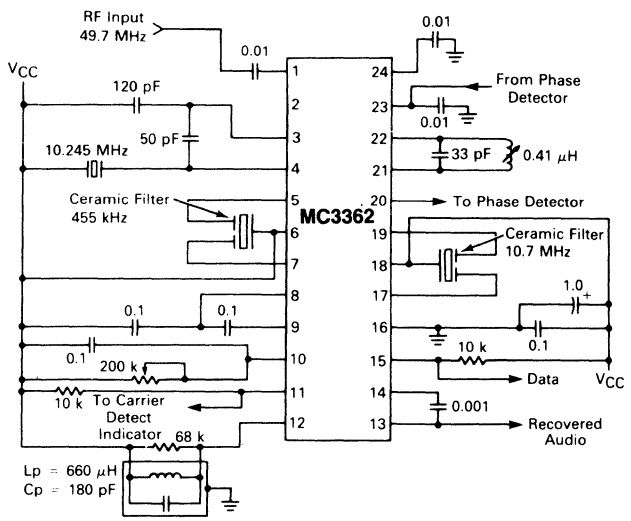
MC2831A



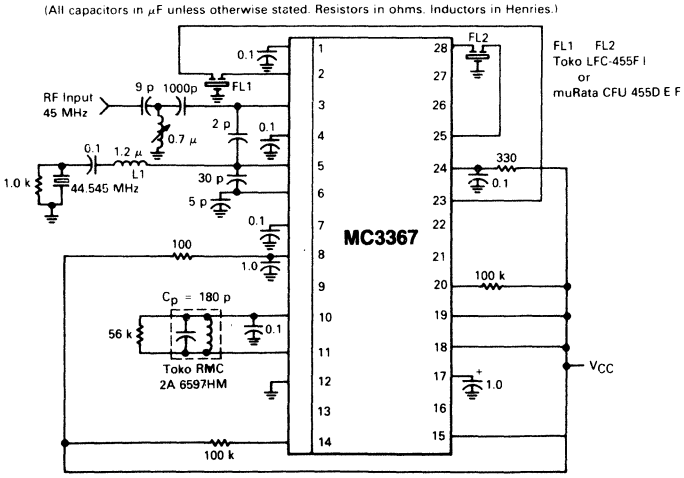
MOSAIC® 1.5 VHF Narrowband Dual-Conversion Receivers

MC3362/MC3363 — T_A = −40°C to +85°C, Case 724, 751A

- Operation to 180 MHz
- 2–8 V dc Supply
- >1 μV for 20 dB Quieting Sensitivity
- Analog and Data Modulation Recovery
- >60 dB Dynamic Range RSSI
- Crystal or VCO First L.O. Operation
- On-Chip RF Amp/MC3363



(All capacitors in μF unless otherwise stated. Resistors in ohms. Inductors in Henries.)



Low Voltage FM Narrowband Receiver

MC3367 — T_A = 0°C to +70°C, Case 751F

- Single Cell Operation to 0.9 V_{CC}
- Single Conversion Operation to 75 MHz
- Current Drain of 1 mA
- Split I.F. Amplifier for Single or Dual Filters
- Analog and Data Outputs
- Sensitivity of 0.7 μV Typ for 20 dB Quieting
- Low Battery Voltage Indicator

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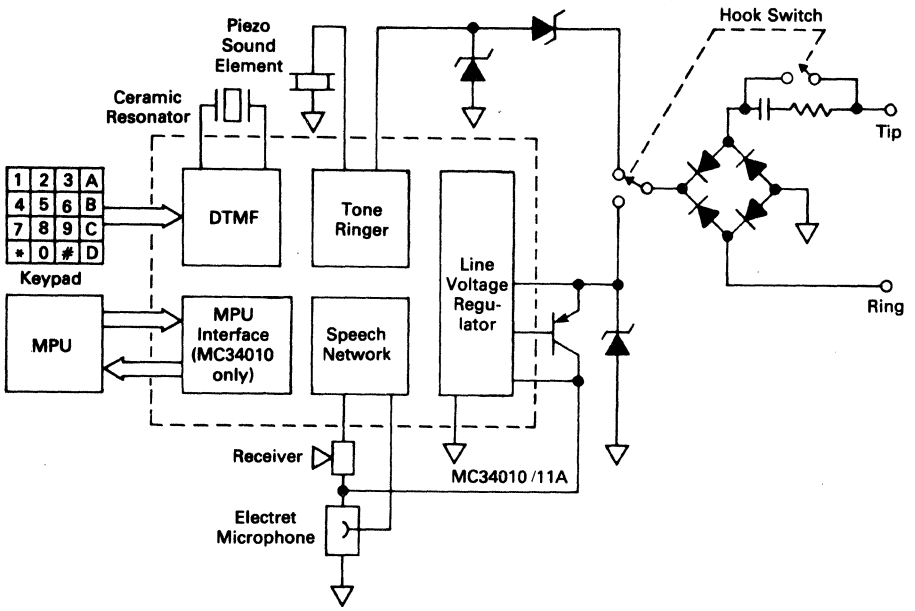
Electronic Telephone

The Complete Electronic Telephone Circuit

MC34010/11A — T_A = −20° to +60°C, Case 711, 777



The conventional transformer-driven telephone handset is undergoing major innovations. The bulky transformer is disappearing. So are many of its discrete components, including the familiar telephone bell. They are being replaced with integrated circuits that perform all the major handset functions simply, reliably and inexpensively . . . functions such as 2-to-4 wire conversion, DTMF dialing, tone ringing, and a variety of related activities.

The culmination of these capabilities is the Electronic Telephone Circuit, the MC34010/11A. These IC's place all of the above mentioned functions on a single monolithic chip.

These telephone circuits utilize advanced bipolar linear (I^2L) technology and provide all the necessary elements of a modern tone-dialing telephone. The MC34010 even incorporates an MPU interface circuit for the inclusion of automatic dialing in the final system.

Features

- Provides All Basic Telephone Functions, Including DTMF Dialer, Tone Ringer, Speech Network and Line Voltage Regulator
- DTMF Generator Uses Low-Cost Ceramic Resonator with Accurate Frequency Synthesis Technique
- Tone Ringer Drives Piezoelectric Transducer and Satisfies EIA-470 Requirements
- Speech Network Provides Two–Four Wire Conversion with Adjustable Sidetone Utilizing an Electret Transmitter
- On-Chip Regulator Insures Stable Operation Over Wide Range of Loop Lengths
- I^2L Technology Provides Low 1.4 Volt Operation and High Static Discharge Immunity
- MC34010P Provides Microprocessor Interface Port for Automatic Dialing Features

Also Available — a broad line of additional telephone components for customizing systems design.

Audio Control Circuit

MC145429 Telset audio interface circuit for MPU-controlled independent adjustment of earpiece, speaker and ringer volume.

Dialer Circuits

MC14408/9 Binary-to-phone pulse converter changes 4-bit binary input code to corresponding serial output pulses.

MC14410 2-of-8 tone encoder converts digital input code to corresponding high- and low-band sine waves.

MC14419 2-of-8 key pad-to-binary encoder accepts inputs from 16-key switches arranged in a 4 x 4 matrix. Contains illegal-state detector to eliminate false data outputs.

MC145410 Integrated tone/pulse dialer with 18-digit redial. Operates at 2.5 to 6 volt range.

MC145412/13 Integrated Tone/Pulse 10-number Repertory Dialer.

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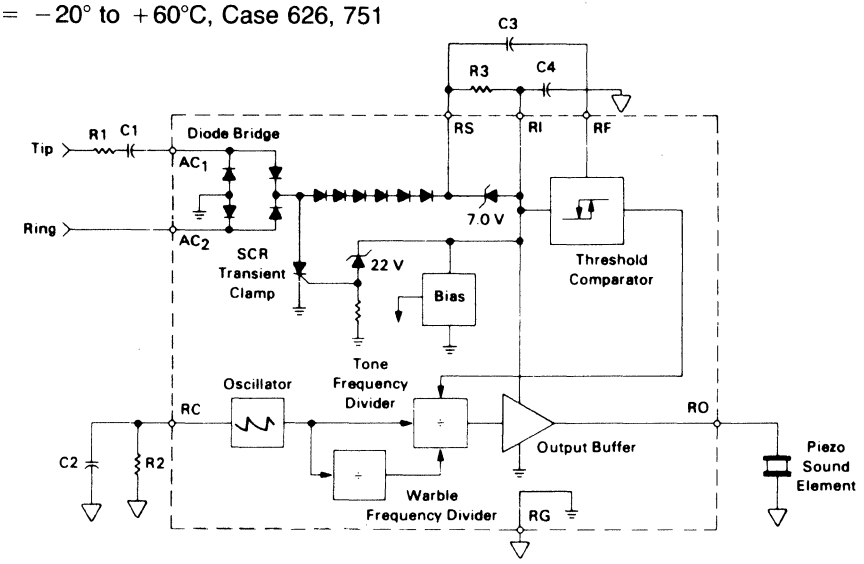
Tone Ringers

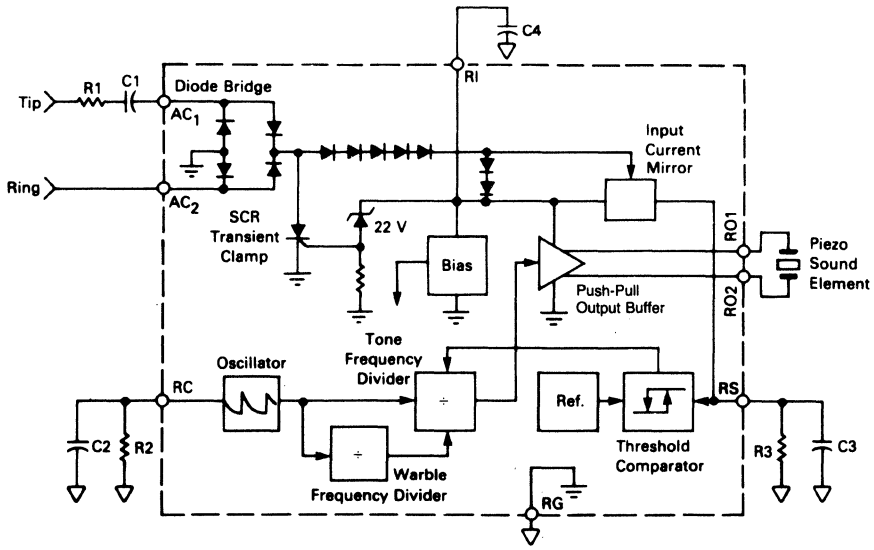
The MC34012 and MC34017 Tone Ringers are designed to replace the bulky bell assembly of a telephone, while providing the same function and performance under a variety of conditions. The operational requirements spelled out by the FCC and the EIA, simply stated, are that a ringer circuit MUST function when a ringing signal is provided, and MUST NOT ring when other signals (speech, dialing signals, noise) are on the line. The MC34012 series and the MC34017 series were designed to meet those requirements.

MC34012 — T_A = −20° to +60°C, Case 626, 751



- Complete Telephone Bell Replacement Circuit with Minimum External Components
- On-Chip Diode Bridge and Transient Protection
- Direct Drive for Piezoelectric Transducers
- Base Frequency Options — MC34012-1: 1.0 kHz
  MC34012-2: 2.0 kHz
  MC34012-3: 500 Hz
- Push-Pull Output Stage for Greater Output Power Capability (MC34017)
- Base Frequency Options — MC34017-1: 1.0 kHz
  MC34017-2: 2.0 kHz
  MC34017-3: 500 Hz
- Input Impedance Signature Meets Bell and EIA Standards
- Rejects Rotary Dial Transients

MC34017 — T_A = −20° to +60°C, Case 626, 751



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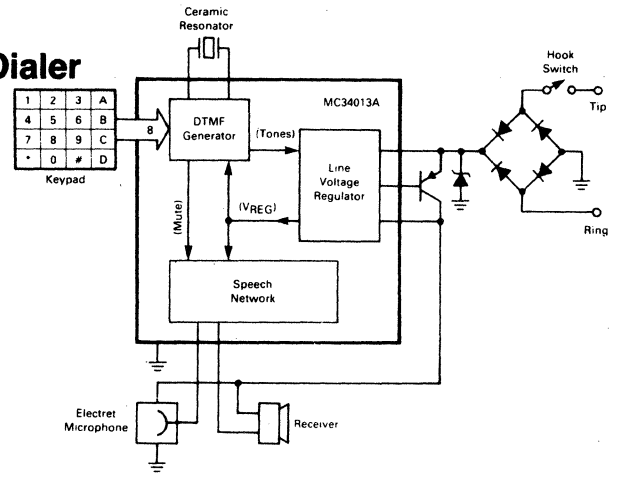
Telephone Speech Network and Tone Dialer

MC34013A — T_A = −20° to +60°C, Case 710,776

- Linear/I^2L Technology Provides Low 1.4 Volt Operation in Both Speech and Dialing Modes
- Speech Network Provides 2–4 Wire Conversion with Adjustable Sidetone Utilizing an Electret Microphone
- DTMF Generator Uses Low-Cost Ceramic Resonator with Accurate Frequency Synthesis Technique
- On-Chip Regulator Insures Stable Operation Over Wide Range of Loop Lengths
- Dialer Mutes Speech Network with Internal Delay for Click Suppression on DTMF Key Release

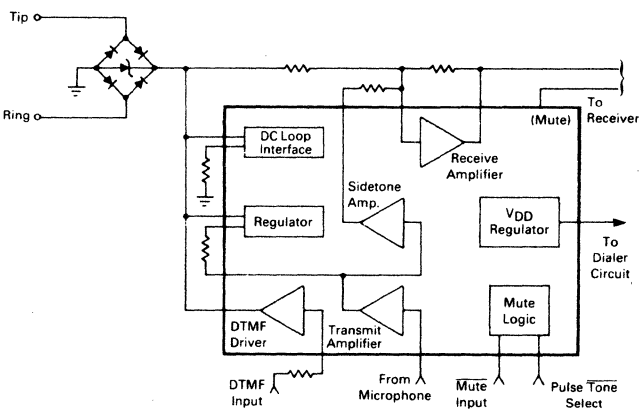


Speech Network with Dialer Interface

MC34014 — T_A = −20° to +60°C, Case 707, 775

The MC34014 is a Telephone Speech Network integrated circuit which incorporates adjustable transmit, receive, and sidetone functions, line interface circuit, dialer interface, and a regulated output voltage for a dialer circuit. It includes an equalization circuit to compensate for various line lengths and the conversion from 2-to-4 wire is accomplished with supply voltages as low as 1.5 volts.

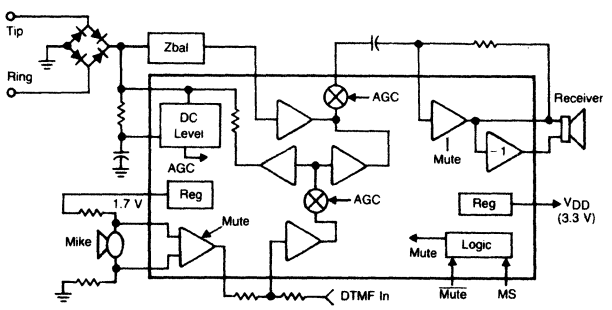
- Transmit, Receive, and Sidetone Gains Set By External Resistors
- Loop Length Equalization for Transmit, Receive, and Sidetone Functions
- Operates Down to 1.5 Volts (V+) in Speech Mode
- Provides Regulated Voltage for CMOS Dialer
- Speech Amplifiers Muted During Pulse and Tone Dialing
- DTMF Output Level Adjustable with a Single Resistor
- Compatible with 2-Terminal Electret Microphones
- Compatible with Receiver Impedances of 150 Ω and Higher



Telephone Speech Network with Dialer Interface

MC34114 — T_A = −20° to +70°C, Case 707, 751D

- Operation Down to 1.2 Volts
- Externally Adjustable Transmit, Receive, and Sidetone Gains
- Differential Microphone Amplifier Input Minimizes RFI
- Transmit, Receive, and Sidetone Equalization on both Voice and DTMF Signals
- Regulated 1.7 Volts Output for Biasing Microphone
- Regulated 3.3 Volts Output for Powering External Dialer
- Microphone and Receive Amplifiers Muted During Dialing
- Differential Receive Amplifier Output Eliminates Coupling Capacitor
- Operates with Receiver Impedances of 150 Ω and Higher
- MC34114 Complies with Bell Telephone and BT Standards



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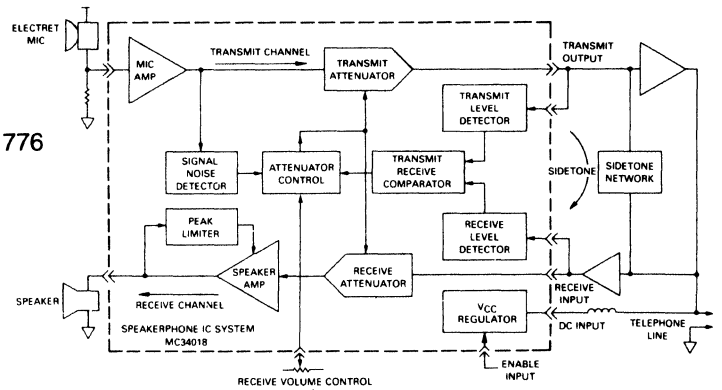
Voice Switched Speakerphone Circuit

MC34018 — T_A = −20° to +60°C, Case 710, 776

The MC34018 Speakerphone integrated circuit incorporates the necessary amplifiers, attenuators, and control functions to produce a high quality hands-free speakerphone system. Included are a microphone amplifier, a power audio amplifier for the speaker, transmit and receive attenuators, a monitoring system for background sound level, and an attenuation control system which responds to the relative transmit and receive levels as well as the background level. Also included are all necessary regulated voltages for both internal and external circuitry, allowing line-powered operation (no additional power supplies required). A Chip Select pin allows the chip to be powered down when not in use. A volume control function may be implemented with an external potentiometer. MC34018 applications include speakerphones for household and business use, intercom systems, automotive telephones, and others.



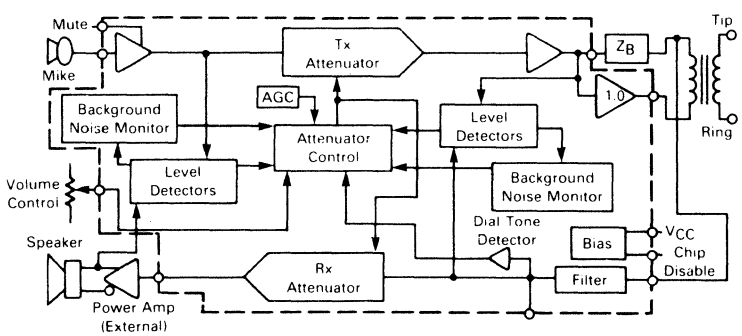
- All Necessary Level Detection and Attenuation Controls for a Hands-Free Telephone in a Single Integrated Circuit
- Background Noise Level Monitoring with Long Time Constant
- Wide Operating Dynamic Range Through Signal Compression
- On-chip Supply and Reference Voltage Regulation
- Typical 100 mW Output Power (into 25 Ω) with Peak Limiting to Minimize Distortion
- Chip Select Pin for Active/Standby Operation
- Linear Volume Control Function

Voice Switched Speakerphone Circuit

MC34118 — T_A = −20° to +60°C, Case 710, 751F

The MC34118 Voice Switched Speakerphone Circuit incorporates the necessary amplifiers, attenuators, level detectors, and control algorithm to form the heart of a high quality hands-free speakerphone system. Included are a microphone amplifier with adjustable gain and MUTE control, Transmit and Receive attenuators which operate in a complementary manner, level detectors at both input and output of both attenuators, and background noise monitors for both the transmit and receive channels. A Dial Tone Detector prevents the dial tone from being attenuated by the Receive background noise monitor circuit. Also included are two line driver amplifiers which can be used to form a hybrid network in conjunction with an external coupling transformer. A high-pass filter can be used to filter out 60 Hz noise in the receive channel, or for other filtering functions. A Chip Disable pin permits powering down the entire circuit to conserve power on long loops where loop current is at a minimum.

The MC34118 may be operated from a power supply, or it can be powered from the telephone line, requiring typically 5.0 mA. The MC34118 can be interfaced directly to Tip and Ring (through a coupling transformer) for stand-alone operation, or it can be used in conjunction with a handset speech network and/or other features of a featurephone.



- Improved Attenuator Gain Range: 52 dB Between Transmit and Receive
- Low Voltage Operation for Line-Powered Applications (3.0–6.5 V)
- 4-Point Signal Sensing for Improved Sensitivity
- Background Noise Monitors for Both Transmit and Receive Paths
- Microphone Amplifier Gain Set by External Resistors — Mute Function Included
- Chip Disable for Active/Standby Operation
- On Board Filter Pinned-Out for User Defined Function
- Dial Tone Detector to Inhibit Receive Idle Mode During Dial Tone Presence
- Compatible with MC34119 Speaker Amplifier

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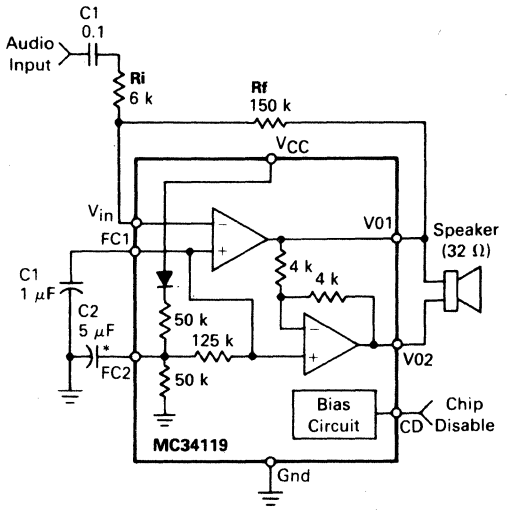
Audio Amplifier

MC34119 — T_A = 0° to +70°C, Case 626, 751

A low power audio amplifier circuit intended (primarily) for telephone applications, such as speakerphones. Provides differential speaker outputs to maximize output swing at low supply voltages (2 volt min.). Coupling capacitors to the speaker, and snubbers, are not required. Overall gain is externally adjustable from 0 to 46 dB. A Chip Disable pin permits powering-down to mute the audio signal and reduce power consumption.

- Drives a Wide Range of Speaker Loads (16–100 Ω)
- Output Power Exceeds 250 mW with 32 Ω Speaker
- Low Distortion (THD = 0.4% Typical)
- Wide Operating Supply Voltage (2–16 Volts) — Allows Telephone Line Powered Applications.
- Low Quiescent Supply Current (2.5 mA Typical)
- Low Power-Down Quiescent Current (60 μA Typical)



* = Optional

Differential Gain = $2 \times \frac{Rf}{Ri}$

Current Mode Switching Regulator

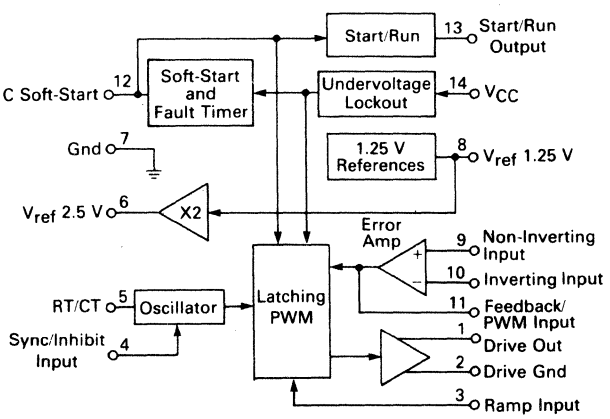
MC34129 — T_A = 0° to +70°C, Case 646, 751A

High performance current mode switching regulator for low-power digital telephones. Unique internal fault timer provides automatic restart for overload recovery. A start/run comparator is included to implement bootstrapped operation of V_{CC}.

Although primarily intended for digital telephone systems, these devices can be used cost effectively in many other applications.

On-chip functions and features include:

- Current Mode Operation to 300 kHz
- Automatic Feed Forward Compensation
- Latching PWM for Cycle-By-Cycle Current Limiting
- Latched-Off or Continuous Retry after Fault Timeout
- Soft-Start with Maximum Peak Switch Current Clamp
- Internally Trimmed 2% Bandgap Reference
- Input Undervoltage Lockout



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Memory Interface and Control

Motorola's line of circuits in this category have well established industry standards for reading and writing in a floppy disk system. The write circuits are designed for both straddle erase and tunnel erase heads, and provide both the writing and erasing functions. The read circuits include all the circuitry for peak detection, filtering, wave shaping, and guaranteed peak shift specifications.

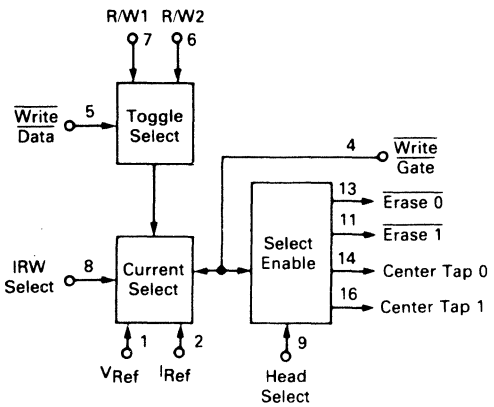
Floppy Disk Write Controllers

Straddle Erase Controller

MC3469P — T_A = 0° to +70°C, Case 648

Designed to provide the entire interface between floppy disk heads and the head control and write data signals for straddle-erase heads.

Provisions are made for selecting a range of accurately controlled write currents and for head selection during both read and write operation. Additionally, provisions are included for externally adjusting degauss period and inner/outer track compensation.

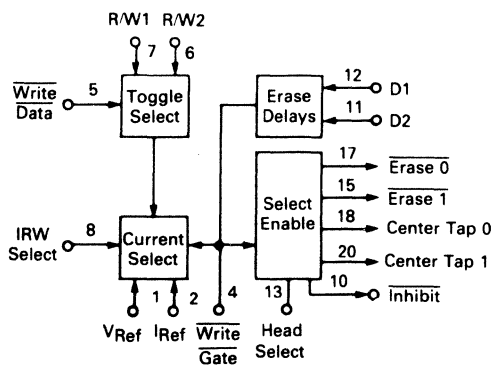


Tunnel/Straddle Erase Controller

MC3471P — T_A = 0° to +70°C, Case 738

Provides the entire interface between the write data and head control signals and the heads (write and erase) for either tunnel or straddle-erase floppy disk systems.

Has provisions for external adjustment of degauss period, inner/outer track compensation, and the delay from write gate to erase turn-on and turn-off.



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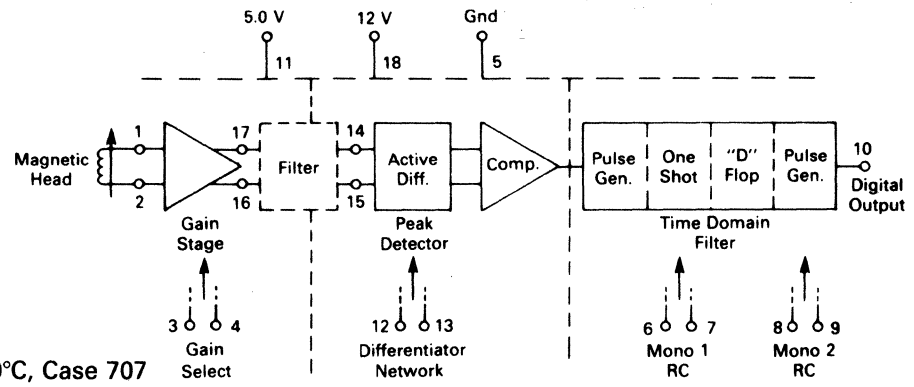
Floppy Disk Read Amplifier System



MC3470,A — T_A = 0° to +70°C, Case 707

Designed as monolithic Read Amplifier System for obtaining digital information from floppy disk storage. These devices accept differential ac signals produced by the magnetic head and provides a digital output pulse that corresponds to each peak of the input signal. A gain stage amplifies the input waveform and applies it to an external filter network, enabling the active differentiator and time domain filter to produce the desired output. These devices provide all the active circuitry to perform the floppy disk Read amplifier function, and guarantee to have a maximum peak shift of 5.0%, adjustable to zero, for the MC3470P and 2.0%, adjustable to zero, for the MC3470AP.

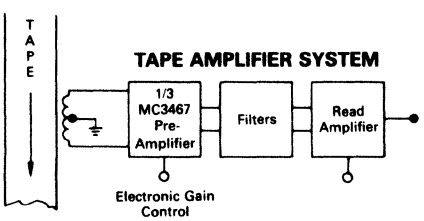
Device Number	Peak Shift (f = 250 kHz, V_{ID} = 1.0 V_{pp})	Differential Input Voltage Gain (f = 200 kHz, V_{ID} = 5.0 mV [RMS])		Input Common Mode Range (5% Max THD)	
		V/V		V	
	% Max	Min	Max	Min	Max
MC3470	5.0	80	130	−0.1	1.5
MC3470A	2.0	100	130		

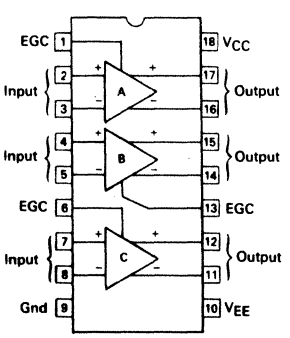
Magnetic Tape Sense Amplifier

MC3467L,P — T_A = 0° to +70°C, Case 726, 707

The MC3467 provides three independent preamplifiers with individual electronic gain control, optimized for use in 9-track magnetic tape memory systems where low noise and low distortion are paramount objectives.

The electronic gain control allows each amplifier's gain to be set anywhere from essentially zero to a maximum of approximately 100 V/V. Minimum small-signal bandwidth is 10 MHz, and Common-Mode Input Voltage range is 1.5 V min.



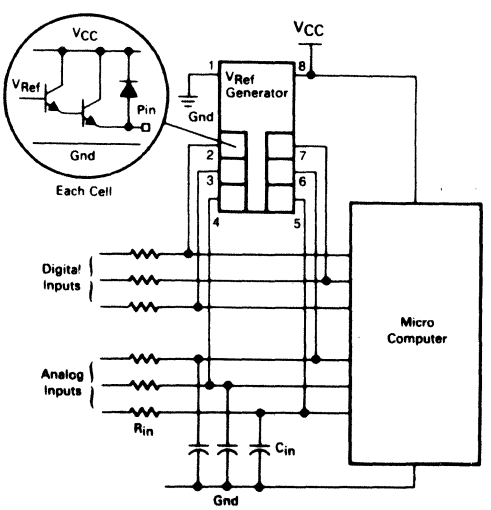


Peripheral Clamping Array

TCF6000P1,D — T_A = −40° to +85°C, Case 626, 751

. . . designed to protect input/output lines of microprocessor systems against voltage transients.

- Optimized for HMOS System
- Minimal Component Count
- Low Board Space Requirement
- No P.C.B. Track Crossovers Required
- Applications Areas Include Automotive, Industrial, Telecommunications and Consumer Goods



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Microprocessor Bus Interface

Motorola offers a spectrum of line drivers and receivers which provide interfaces to many industry standard specifications. Many of the devices add key operational features, such as hysteresis, short circuit protection, clamp diode protection, or special control functions.

Address and Control Bus Extenders

These devices are designed to extend the drive capabilities of today's standard microprocessors. All devices are fabricated with Schottky TTL technology for high speed.

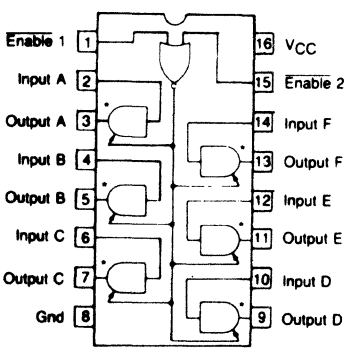
$V_{OL(max)}$ @ 48 mA	$V_{OH(min)}$ @ −5.2 mA	Propagation Delay Max (ns)	Buffers Per Package	Device	Package	Comments
0.5	2.4	13	6	MC8T95/ MC6885	L/620 P/648	Noninverting
0.5	2.4	11	6	MC8T96/ MC6886	L/620 P/648	Inverting
0.5	2.4	13	6	MC8T97/ MC6887	L/620 P/648	Noninverting
0.5	2.4	11	6	MC8T98/ MC6888	L/620 P/648	Inverting

Hex 3-State Buffers/Inverters — T_A = 0° to +75°C

These devices differ in that the non-inverting MC8T95/ MC6885 and inverting MC8T96/MC6886 provide a two-input Enable which controls all six buffers, while the noninverting MC8T97/MC6887 and inverting MC8T98/ MC6888 provide two Enable inputs — one controlling four buffers and the other controlling the remaining two buffers.

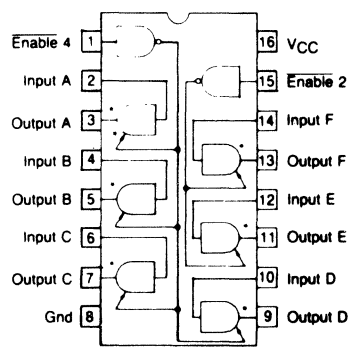
#These devices may be ordered by either of the paired numbers.

MC8T95/MC6885# — Noninverting
MC8T96/MC6886# — Inverting
Two-input Enable controls all six buffers



*Add inverter for MC6886/MC8T96.

MC8T97/MC6887# — Noninverting
MC8T98/MC6888# — Inverting
Two Enable inputs, one controlling four buffers and the other controlling the remaining two buffers.



*Add inverter for MC6888/MC8T98.

Microprocessor Data Bus Extenders

Driver Characteristics		Receiver Characteristics				
Output Current (mA)	Propagation Delay Max (ns)	Propagation Delay Max (ns)	Transceivers Per Package	Device	Package/ Suffix	Comments
48	14	14	4	MC8T26A (MC6880A)	P/648 L/620	Inverting Logic
48	17	17	4	MC8T28 (MC6889)	P/648 L/620	Noninverting Logic

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Single-Ended Bus Transceivers

For Instrumentation Bus, Meets GPIB/IEEE Standard 488

Driver Characteristics		Receiver Characteristics				
Output Current (mA)	Propagation Delay Max (ns)	Propagation Delay Max (ns)	Transceivers Per Package	Device	Package/ Suffix	Comments
48	50	50	4	MC3446A	P/648	MOS Compatible, Input Hysteresis
48	30	50	8	MC3447	P3/724 L/623	Input Hysteresis, Open Collector, 3-State Outputs with Terminations
48	17	25	4	MC3448A	P/648 L/620	Input Hysteresis, Open Collector 3-State Outputs with Terminations
100	30	30	4	MC3440A	P/648	Input Hysteresis, Enable for 3 Drivers
				MC3441A		Common Enable, Input Hysteresis

For High-Current Party-Line Bus for Industrial and Data Communications

100	15	15	4	MC26S10	P/648 L/620	Open Collector Outputs, Common Enable

Line Receivers

General Purpose

S = Single Ended D = Differential	Type* Of Output	t_{prop} Delay Time Max (ns)	Party-Line Operation	Strobe Or Enable	Power Supplies (V)	Device	Package/ Suffix	Receivers Per Package	Companion Drivers	Comments
D D	TP OC	25 25	Yes Yes	Yes Yes	±5 ±5	MC3450 MC3452	P/648 L/620	4 4	MC3453	Quad version of MC75107/8
D D	TP OC	25 25	Yes Yes	Yes Yes	±5 ±5	MC75107 MC75108	P/646 L/632	2 2	MC75S110	Dual version of MC3450/2
S	TP	30	Yes	Yes	+5	MC3437	P/648 L/620	6		Input Hysteresis

360/370 I/O Interface

S	TP	30	Yes	No	+5	MC75125 MC75127	P/648 L/620	7	MC3481 MC3485	Schottky Circuitry
S	TP	30	Yes	Yes	+5	MC75128 MC75129	P/738 L/732	8	MC3481 MC3485	Active high strobe Active low strobe

*OC = Open Collector, TP = Totem-pole output

EIA Standard

S = Single Ended D = Differential	Type* Of Output	t_{prop} Delay Time Max (ns)	Party-Line Operation	Strobe Or Enable	Power Supplies (V)	Device	Package/ Suffix	Receivers Per Package	Companion Drivers	EIA Standard
S	R	85	No	No	+5	MC1489 MC1489A	P/646 L/632	4	MC1488	(RS-232) EIA-232-D
S, D S, D	TP TP	30 30	Yes Yes	Yes Yes	+5 +5	AM26LS32 MC3486	P/648 L/620	4 4	AM26LS31 MC3487	(RS-422/423) EIA-422/423
S, D S, D	TP TP	35 35	Yes Yes	Yes Yes	+5 +5	SN75173 SN75175	N/648 J/620	4 4	SN75172 SN75174	(RS-422/423/485) EIA-422/423/485

*R = Resistor Pull-up, TP = Totem-pole output

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Line Drivers

General Purpose

Output Current Capability (mA)	t_{prop} Delay Time Max (ns)	S = Single Ended D = Differential	Party-Line Operation	Strobe Or Enable	Power Supplies (V)	Device	Package/ Suffix	Drivers Per package	Companion Receivers	Comments
15	15	D	Yes	Yes	±5	MC3453	P/648 L/620	4	MC3450 MC3452	Quad version of MC75S110
15	15	D	Yes	Yes	±5	MC75S110	P/646 L/632	2	MC75107 MC75108	Dual version of MC3453

360/370 I/O Interface

60	45	S	Yes	Yes	+5	MC3481	P/648 L/620	4	MC75125 MC75127	Short Circuit Fault Flag
60	45	S	Yes	Yes	+5	MC3485	P/648 L/620	4	MC75128 MC75129	Short Circuit Fault Flag

EIA Standard

Output Current Capability (mA)	t_{prop} Delay Time Max (ns)	S = Single Ended D = Differential	Party-Line Operation	Strobe Or Enable	Power Supplies (V)	Device	Package/ Suffix	Drivers Per Package	Companion Receivers	EIA Standard
85 85	35 35	D D	Yes Yes	Yes Yes	+5 +5	SN75172 SN75174	N/648 J/620	4 4	SN75173 SN75175	(RS-485) EIA-485
48	20	D	Yes	Yes	+5	MC3487	P/648 L/620	4	MC3486	(RS-422) EIA-422 with 3-State Outputs
48	20	D	Yes	Yes	+5	AM26LS31	P/648 D/620	4	AM26LS32	
20	—	S	No	No	±12	MC3488A (μA9636A)	P1/626 U/693	2	MC3486 AM26LS32	(RS-423/232) EIA-423/232-D
10	350	S	No	Yes	±9 to ±12	MC1488	P/646 L/632	4	MC1489 MC1489A	(RS-232) EIA-232-D

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Line Transceivers

Driver Prop Delay (Max ns)	Receiver Prop Delay (Max ns)	CE = Common Enable DE = Driver Enable RE = Receiver Enable	Party Line Operation	Power Supply (V)	Device	Package/ Suffix	Drivers Per Package	Receivers Per Package	EIA Standard
20	30	DE, RE	Yes	+5	MC34050	L/620 P/648	2	2	(RS-422) EIA-422
20	30	DE	Yes	+5	MC34051	L/620 P/648	2	2	(RS-422) EIA-422

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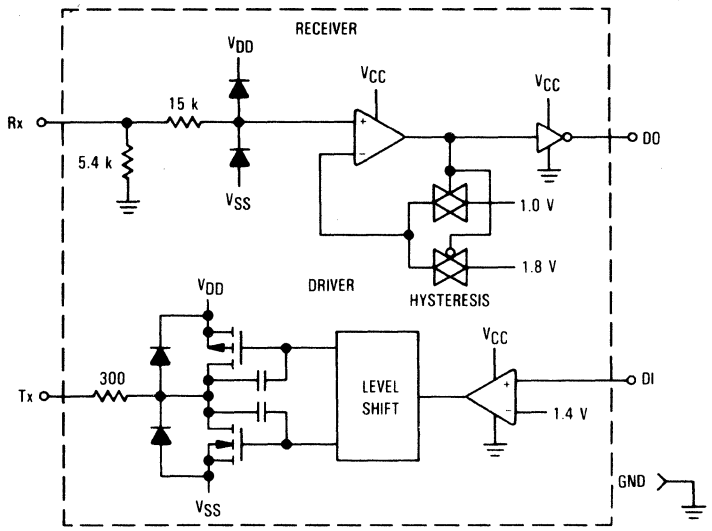
EIA-232-D/V.28 Driver/Receiver

MC145406L,P — T_A = −40° to +85°C, Case 620, 648

The MC145406 is a silicon-gate CMOS IC that combines three drivers and three receivers to fulfill the electrical specifications of EIA-232-D and CCITT V.28. Using ±12 volt supplies and a +5.0 volt supply, this 16-pin device consumes a maximum of 15 mW.



Peripheral Drivers

Output Current Capability (mA)	Input Capability	Propagation Delay Time Max (μs)	Output Clamp Diode	Off State Voltage Max (V)	Device	Drivers Per Package	Package/ Suffix	Logic Function
300	TTL, DTL	1.0	Yes	70	MC1472	2	P1/626 U/693	NAND
500	TTL, CMOS, PMOS	1.0	Yes	50	ULN2801	8	A/707	Invert
500	14 V to 25 V PMOS	1.0	Yes	50	ULN2802	8	A/707	Invert
500	TTL, CMOS	1.0	Yes	50	ULN2803	8	A/707	Invert
500	6.0 V to 15 V MOS	1.0	Yes	50	ULN2804	8	A/707	Invert
500	TTL, CMOS PMOS	1.0	Yes	50	MC1411,B	7	P/648	Invert
500	14 V to 25 V PMOS	1.0	Yes	50	MC1412,B	7	P/648	Invert
500	TTL, 5.0 V CMOS	1.0	Yes	50	MC1413,B	7	P/648	Invert
500	8.0 V to 18 V MOS	1.0	Yes	50	MC1416,B	7	P/648	Invert
1500	TTL, 5.0 V CMOS	1.0	Yes	50	ULN2068B	4	B/648	Invert
1500	TTL, 5.0 V CMOS	1.0	No	50	ULN2074	4	B/648	Collector, Emitter available at Pins

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Display Drivers/Decoders, CMOS

These CMOS devices include digit as well as matrix drivers for LEDs, LCDs, and VFDs. They find applications over a wide range of end equipment, such as instruments, automotive dash boards, home computers, appliances, radios and clocks.

Display Drivers

Display Type	Input Format	Drive Capability Per Package	On-Chip Latch	Display Control	Segment Drive Current	Device Number
LCD (Direct Drive)	Parallel BCD	7 Segments	✓	Blank	~1 mA	MC14543B
			✓	Blank, Ripple Blank	~1 mA	MC14544B
	Serial Binary [Compatible with the Serial Peripheral Interface (SPI) on CMOS MCUs]	33 Segments or Dots	✓		20 μA	MC145453
Muxed LCD (1/4 Mux)	Serial Binary [Compatible with the Serial Peripheral Interface (SPI) on CMOS MCUs]	48 Segments or Dots	✓		~200 μA	MC145000
		44 Segments or Dots	✓		~200 μA	MC145001
LED, Incandescent, Fluorescent*	Parallel BCD	7 Segments	✓	Blank, Lamp Test	25 mA	MC14511B
			✓	Blank, Ripple Blank, Lamp Test	25 mA	MC14513B
				Blank	65 mA	MC14547B
Muxed LED	Serial Binary [Compatible with the Serial Peripheral Interface (SPI) on CMOS MCUs]	4 Digits + Decimals	✓	Oscillator (Scanner)	50 mA (Peak)	MC14499
		5 Characters + Decimals or 25 Lamps	✓	Oscillator (Scanner), Low-Power Mode, Dimming	25 mA (Peak)	MC14489
LED	Parallel Hex	7 Segments + A thru F Indicator	✓		10 mA**	MC14495★1
(Interfaces to Display Drivers)	Parallel BCD	7 Segments		Ripple Blank, Enable		MC14558B

*Absolute maximum working voltage = 18 V
**On-chip current-limiting resistor
★Replace ★ with package identifier (see product data).

Functions

Device Number	Function	Package
MC14495★1	Hexadecimal-to-7-Segment Latch/Decoder ROM/Driver	648
MC14489	Multi-Character LED Display/Lamp Driver	738, 751D
MC14499	4-Digit 7-Segment LED Display Decoder/Driver with Serial Interface	707
MC14511B	BCD-to-7-Segment Latch/Decoder/Driver	620, 648
MC14513B	BCD-to-7-Segment Latch/Decoder/Driver with Ripple Blanking	726, 707
MC14543B	BCD-to-7-Segment Latch/Decoder/Driver for Liquid Crystals	620, 648
MC14544B	BCD-to-7-Segment Latch/Decoder/Driver with Ripple Blanking	726, 707
MC14547B	High-Current BCD-to-7-Segment Decoder/Driver	620, 648
MC14558B	BCD-to-7-Segment Decoder	620, 648
MC145000	48-Segment Serial Input Multiplexed LCD Driver (Master)	709, 776
MC145001	44-Segment Serial Input Multiplexed LCD Driver (Slave)	707, 776
MC145453	33-Segment, Non-Multiplexed LCD Driver with Serial Interface	711, 777

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STANDARD MILITARY PRODUCT FLOWS

TABLE I details the screening and quality conformance inspection procedures for Motorola's standard military flows. Motorola has established two distinct product flows which are designed to meet the following applications:

1. **MOTOROLA SMD/883 CLASS B FLOW:** Motorola SMD/883 Class B products are offered for use in airborne or ground system applications. SMD/883 product is screened and tested per the applicable requirements of MIL-M-38510, MIL-STD-883 including general provision paragraph 1.2 (and subordinate paragraphs), and applicable SMD/DESC drawing. Marking shall be in accordance with JEDEC Publication No. 101. Fabrication, screening and testing are not restricted to U.S.A. facilities.
2. **MIL-M-38510 JAN CLASS B FLOW:** JAN Class B products are offered for use in airborne or ground system applications. Fabrication, screening and testing are restricted to DESC certified lines.

CLASS B FLOW(S): The Class B flow has become the "Industry standard flow." This product receives all the 100% screening tests specified by Method 5004, MIL-STD-883. These tests include *visual inspection* to the requirements of Condition B of Method 2010 (and Method 5004 paragraph 3.3), *burn-in,* Condition A, B, C, D or E per Method 1015, for 160 hours at +125° (or equivalent per Table I or Method 1015), and *static electrical testing at high and low rated temperatures.*

TABLE I

	MIL-STD-883 and SMD		MIL-M-38510 JAN	
SCREEN	**METHOD**	**REQM'T.**	**METHOD**	**REQM'T.**
Internal Visual (Precap)	2010 Condition B and 38510	100%	2010 Cond. B and 38510	100%
Stabilization Bake	1008 24 hours min. Condition C or equivalent.	100%	1008 24 hours min. Condition C or equivalent.	100%
Temperature Cycling	1010 Condition C	100%	1010 Condition C	100%
Constant Acceleration	2001 Condition E (min.) in Y_1 Plane	100%	2001 Conditon E (min.) in Y_1 Plane	100%
Seal Fine & Gross	1014, Conditions B & C	100%	1014, Conditions B & C	100%
Interim Electrical	Per applicable device specification	Optional	JAN slash sheet electrical specification	Optional
Burn-In Test	1015 160 hours @ 125°C or equivalent	100%	1015 160 hours @ 125°C or equivalent	100%
Final Electrical Tests (A) Static Tests (1) 25°C (Subgroup 1, Table 1, 5005) (2) Max & min rated op temperature (Subgroups 2 & 3, Table 1, 5005) (B) Dynamic Test or Switching Tests 25°C (Subgroup 4 or 9, Table 1, 5005) (C) Functional Test 25°C (Subgroup 7, Table 1, 5005)	Standard military drawing specification	 100% 100% 100% 100%	JAN slash sheet electrical specifications	 100% 100% 100% 100%
Quality Conformance Inspection: Group A (A) Static (1) 25°C (Subgroup 1) (2) Temp. (Subgroup 2 & 3) (B) Dynamic & Switching Tests (1) 25°C (Subgroup 4 or 9) (2) Temp. (Subgroup 5 & 6 or 10 & 11 (C) Functional (1) 25°C (Subgroup 7)	5005 Class B		5005 Class B	
Group B	5005 Class B		5005 Class B	
Group C	5005 Class B		5005 Class B	26 wks. prod.
Group D	5005 Class B		5005 Class B	36 wks. pkg. prod.
External Visual	2009	100%	2009	100%

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Military IC Numbering Systems

MIL-STD-883 — Example; 54LS00M/B2CJC

54LS00	M(1)	/B	X	X	JC
Device Number	LCC Package	Class B	Case	Lead Finish	JEDEC Marking

DESC STANDARD MILITARY DRAWING (SMD) — Example; 5962-8671001RA

5962(2)	XXXXX	01	X	X
DESC Desig.	Device Number	Device Detail	Case	Lead Finish

MIL-M-38510 (JAN) — Example; JM38510/30908BEA

JM38510	/XXX	XX	B	X	X
MIL Desig.	Device Number	Device Detail	Class B	Case	Lead Finish

Notes:
(1) Suffix M must be added to the Device Number when ordering a circuit in the Chip Carrier Package. For other packages, the M Suffix should be omitted.
(2) The DESC Designation number need not be used for ordering purposes since each device identification number uniquely associates the device with the DESC classification.

MIL-M-38510 Case Outlines

Letter	Description	Letter	Description
A	14-lead FP (1/4″ x 1/4″)	L	24-lead DIP (1/4″ x 1-1/4″)
B	14-lead FP (3/16″ x 1/4″)	M	12-lead Can
C	14-lead DIP (1/4″ x 3/4″)	P	8-lead DIP (1/4″ x 3/8″)
D	14-lead FP (1/4″ x 3/8″)	Q	40-lead DIP (9/16″ x 2-1/16″)
E	16-lead DIP (1/4″ x 7/8″)	R	20-lead DIP (1/4″ x 1-1/16″)
F	16-lead FP (1/4″ x 3/8″)	S	20-lead FP (1/4″ x 1/2″)
G	8-lead Can	V	18-lead DIP (1/4″ x 15/16″)
H	10-lead FP (1/4″ x 1/4″)	W	22-lead DIP (3/8″ x 1-1/8″)
I	10-lead Can	2	20-Terminal SQ. LCC (.350″ x .350″)
J	24-lead DIP (1/2″ x 1-1/4″)	3	28-Terminal SQ. LCC (.450″ x .450″)
K	24-lead FP (3/8″ x 5/8″)		

JEDEC Case Outlines

Undesignated package letters in the MIL-M-38510 Case Outlines Table (above) have the following definitions. Pin count is determined by circuit requirements.

U = Leadless Chip Carrier
X = DIP
Y = Flat Pack
Z = All other configurations

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STANDARD MILITARY PRODUCT MARKING

MINIMUM MARKING REQUIREMENT: All Motorola standard military product receives the following marking:

1. Motorola Symbol (logo): Example — Ⓜ
2. Seal Date Code (per MIL-M-38510): Example — 8511
3. ESD Identifier, Equilateral Triangle: Example — Δ
4. Device Part Number.
5. Index Point (defines starting point for numbering leads and/or mechanical orientation and shall consist of either a pin 1 dot, package notch or a dog-leg on pin 1 terminal).
6. Motorola's manufacturer's designating symbol CGG per NAV-SHIPS 0967-190-4010.*
7. If package material contains beryllium oxide, the part is marked with the designator "BeO."

*CGG not marked on can packages

ADDITIONAL MARKING:
JEDEC product also receives the following marking:

a. Multiple part numbers (when applicable) as defined below:
   — MOTOROLA JEDEC part number
   — DESC DRAWING part number (if applicable).
b. Country of Origin (marked on backside of CERDIP, CERFLAT, and LCCC package types and on the side or bottom of "Metal Can" packages).
   NOTE: A unique prefix code may be added to the Inspection Lot Identification Code (seal date) which identifies the country of origin for both assembly and test. See table below.
c. "883" MIL-STD-883 General Provisions paragraph 1.2.1 compliance marking.

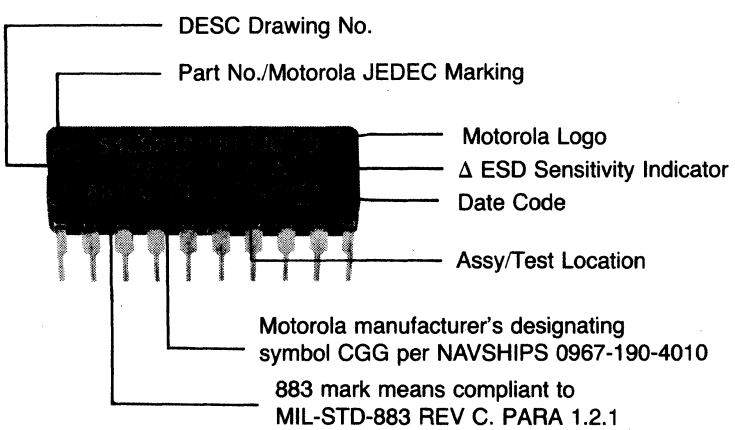
LOCATOR CODES FOR ASSEMBLY OR TEST

D — Austin, TX
E — Oakhill, TX
I — Anam, Korea (Contractor)
K — Seoul, Korea (MKL)
L — Hong Kong
M — Mesa, AZ
Q — Kuala Lumpur, Malaysia (KLM)
R — Seremban, Malaysia
T — France
W — Guadalajara, Mexico
Y — Tempe, AZ
Z — Scotland

The prefix letter closest to the date code is the Test Location Code. The letter to the left of the Test Location Code is the Assembly Location Code.

Example:

K **Y** **85XX** **B**
— Lot Designator
— Seal Date Code
— Test Location — Tempe, Arizona
— Assembly Location — Seoul, Korea



Surface Mount Technology

Linear and Interface

Bipolar

All the major bipolar analog families are now represented in surface mount packaging. Standard SOIC and PLCC packages are augmented by SOP-8 and DPAK for Linear regulators. In addition, tape and reel shipping to the updated EIA-481A is now on line for the industry's largest array of op-amps, regulators, interface, data conversion, consumer, telecom and automotive Linear ICs.

Device	Function	Package
DAC-08CD,ED	High Speed 8-Bit Multiplying D-to-A Converter	SO-16
LF347D	Quad BIFET Operational Amplifiers	SO-14
LF351D	Single BIFET Operational Amplifier	SO-8
LF353D	Dual BIFET Operational Amplifiers	SO-8
LF412CD	Dual BIFET High Power Operational Amplifiers	SO-8
LF441CD	Single BIFET Low Power Operational Amplifier	SO-8
LF442CD	Dual BIFET Low Power Operational Amplifiers	SO-8
LF444CD	Quad BIFET Low Power Operational Amplifiers	SO-14
LM201AD	General Purpose Adjustable Operational Amplifier	SO-8
LM208D,AD	Precision Operational Amplifier	SO-8
LM211D	High Performance Voltage Comparator	SO-8
LM224D	Quad Low Power Operational Amplifiers	SO-14
LM239D,AD	Quad Single Supply Comparators	SO-14
LM258D	Dual Low Power Operational Amplifiers	SO-8
LM293D	Dual Comparators	SO-8
LM301AD	General Purpose Adjustable Operational Amplifier	SO-8
LM308D,AD	Precision Operational Amplifier	SO-8
LM311D	High Performance Voltage Comparator	SO-8
LM317LD	Positive Adjustable 100 mA Voltage Regulator	SOP-8
LM324D,AD	Quad Low Power Operational Amplifiers	SO-14
LM339D,AD	Quad Single Supply Comparators	SO-14
LM348D	Quad MC1741 Operational Amplifiers	SO-14
LM358D	Dual Low Power Operational Amplifiers	SO-8
LM385D-1.2	Micropower Voltage Reference Diodes	SO-8
LM385D-2.5	Micropower Voltage Reference Diodes	SO-8
LM393D	Dual Comparators	SO-8
LM833D	Dual Audio Amplifiers	SO-8
LM2901D	Quad Single Supply Comparators	SO-14
LM2902D	Quad Low Power Operational Amplifiers	SO-14
LM2903D	Dual Comparators	SO-8
LM2904D	Dual Low Power Operational Amplifiers	SO-8
LM2931AD-5.0,D-5.0	Low Dropout Voltage Regulator	SOP-8
LM2931CD*	Adjustable Low Dropout Voltage Regulator	SOP-8
LM3900D	Quad Single Supply Operational Amplifiers	SO-14
MC1377DW*	Color Television RGB to PAL/NTSC Encoder	SO-20
MC1378FN	Video Overlay Synchronizer	PLCC-44
MC1403D	Precision Low Voltage Reference	SO-8
MC1413D	Peripheral Driver Array	SO-16
MC1436D,CD	High Voltage Operational Amplifier	SO-8
MC1455D	Timing Circuit	SO-8
MC1458D,CD	Dual Operational Amplifiers	SO-8
MC1458SD	High Slew Rate Dual Operational Amplifiers	SO-8
MC1488D	Quad EIA-232C Drivers	SO-14
MC1489D	Quad EIA-232C Receivers	SO-14
MC1496D	Balanced Modulator-Demodulator	SO-14
MC1723CD	Adjustable Positive Or Negative Voltage Regulator	SO-14
MC1733CD	Differential Video Amplifier	SO-14
MC1741CD	General Purpose Operational Amplifier	SO-8
MC1741SCD	High Slew Rate Operational Amplifier	SO-8
MC1747CD	Dual MC1741 Operational Amplifiers	SO-14
MC1776CD	Programmable Operational Amplifier	SO-8
MC26LS31D	Quad EIA-422/3 Drivers	SO-16

*To Be Introduced.

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Bipolar (continued)

Device	Function	Package
MC26LS32D	Quad EIA-422 Receivers	SO-16
MC2831AD	FM Transmitter	SO-16
MC3346D	General Purpose Transistor Array	SO-14
MC3356FN	FSK Receiver	PLCC-20
MC3357D	Low Power FM IF Amplifier	SO-16
MC3359DW	Low Power Narrowband FM IF Amplifier	SO-20
MC3361D	Low Voltage Narrowband FM IF Amplifier	SO-16
MC3362DW	Dual Conversion Receivers	SO-28
MC3363DW*	Dual Conversion Receivers	SO-28
MC3367DW	Low Voltage VHF Receiver	SO-28
MC3371D*	Low Voltage FM Receiver with RSSI	SO-16
MC3401D	Quad Operational Amplifiers	SO-14
MC3403D	Quad Differential-Input Operational Amplifiers	SO-14
MC3423D	Overvoltage Sensing Circuit	SO-8
MC3448AD	Quad GPIB Transceivers	SO-16
MC3450D	Quad Line Receivers	SO-16
MC3452D	Quad Line Receivers	SO-16
MC3458D	Dual Low Power Operational Amplifiers	SO-8
MC3486D	Quad EIA-422/3 Receivers	SO-16
MC3487D	Quad EIA-422 Drivers	SO-16
MC4558CD	Dual High Frequency Operational Amplifiers	SO-8
MC4741CD	Quad MC1741 Operational Amplifiers	SO-14
MC78L05ACD	Positive Voltage Regulator, 5 V, 100 mA	SOP-8
MC78L08ACD	Positive Voltage Regulator, 8 V, 100 mA	SOP-8
MC78L12ACD	Positive Voltage Regulator, 12 V, 100 mA	SOP-8
MC78L15ACD	Positive Voltage Regulator, 15 V, 100 mA	SOP-8
MC78M05CDT*	Positive Voltage Regulator, 5 V, 500 mA	DPAK
MC78M12CDT*	Positive Voltage Regulator, 12 V, 500 mA	DPAK
MC78M15CDT*	Positive Voltage Regulator, 15 V, 500 mA	DPAK
MC79L05ACD	3-Terminal Negative Fixed Voltage Regulator, −5 V, 100 mA	SOP-8
MC79L12ACD	3-Terminal Negative Fixed Voltage Regulator, −12 V, 100 mA	SOP-8
MC79L15ACD	3-Terminal Negative Fixed Voltage Regulator, −15 V, 100 mA	SOP-8
MC79M05CDT*	3-Terminal Negative Fixed Voltage Regulator, −5 V, 500 mA	DPAK
MC79M12CDT*	3-Terminal Negative Fixed Voltage Regulator, −12 V, 500 mA	DPAK
MC79M15CDT*	3-Terminal Negative Fixed Voltage Regulator, −15 V, 500 mA	DPAK
MC13022DW*	Medium Voltage AM Stereo C-QUAM Decoder	SO-28
MC13024DW*	Low Voltage C-QUAM Receiver	SO-24
MC13041DW*	AM Receiver Subsystem	SO-20
MC13055D	VHF LAN Receiver — FSK	SO-16
MC13060D	1 Watt Audio Amp	SOP-8
MC33077D	Dual, Low Noise High Frequency Operational Amplifiers	SO-8
MC33078D	Dual Audio, Low Noise Operational Amplifiers	SO-8
MC33079D	Low Power, Single Supply Operational Amplifier	SO-14
MC33171D	Single, Low Power, Single Supply Operational Amplifier	SO-8
MC33172D*	Dual, Low Power, Single Supply Operational Amplifiers	SO-8
MC33174D*	Quad, Low Power, Single Supply Operational Amplifiers	SO-14
MC33282D*	Dual Precision Low Input JFET Operational Amplifiers	SO-14
MC33284D*	Quad Precision JFET Operational Amplifiers (Trim-in-the-Package)	SO-14
MC34001D,AD,BD	Single JFET Input Operational Amplifier	SO-8
MC34002D,AD,BD	Dual JFET Input Operational Amplifiers	SO-8
MC34004D,BD	Quad JFET Input Operational Amplifiers	SO-14
MC34011AFN	Electronic Telephone Circuit	PLCC-44
MC34012-1D	Telephone Tone Ringer	SO-8
MC34012-2D	Telephone Tone Ringer	SO-8
MC34012-3D	Telephone Tone Ringer	SO-8
MC34013AFN	Speech Network and Tone Dialer	PLCC-28
MC34014FN	Telephone Speech Network with Dialer Interface	PLCC-20
MC34017-1D	Telephone Tone Dialer	SO-8
MC34017-2D	Telephone Tone Dialer	SO-8
MC34017-3D	Telephone Tone Dialer	SO-8
MC34018DW	Voice Switched Speakerphone Circuit	SO-28

*To Be Introduced.

Bipolar (continued)

Device	Function	Package
MC34018FN	Voice Switched Speakerphone Circuit	PLCC-28
MC34060AD*	Switchmode Pulse Width Modulation Control Circuit	SO-14
MC34063AD	Precision DC-to-DC Converter Control Circuit	SO-8
MC34071D	Single, High Speed, Single Supply Operational Amplifier	SO-8
MC34072D*	Dual, High Speed, Single Supply Operational Amplifiers	SO-8
MC34074D*	Quad, High Performance, Single Supply Operational Amplifiers	SO-14
MC34080D	High Speed Decompensated ($A_{VCL} \geq 2$) JFET Input Operational Amplifier	SO-8
MC34081D	High Speed JFET Input Operational Amplifier	SO-8
MC34114DW	Speech Network II	SO-18
MC34118DW	Speakerphone II	SO-28
MC34119D	Telephone Speaker Amplifier	SO-8
MC34129D	Power Supply Controller	SO-14
MC34181D	Single, Low Power, High Speed JFET Operational Amplifier	SO-8
MC34182D	Dual, Low Power, High Speed JFET Operational Amplifiers	SO-8
MC34184D	Quad, Low Power, High Speed JFET Operational Amplifiers	SO-14
MC44301DW*†	High Performance Video IF	SO-28
NE592D	Video Amplifier	SO-14
TL061CD	Single BIFET Low Power Operational Amplifier	SO-8
TL062CD	Dual BIFET Low Power Operational Amplifiers	SO-8
TL064CD	Quad BIFET Low Power Operational Amplifiers	SO-14
TL071CD,ACD,BCD	Single, Low Noise JFET Input Operational Amplifier	SO-8
TL072CD,ACD,BCD	Dual, Low Noise JFET Input Operational Amplifiers	SO-8
TL074CD,ACD,BCD	Quad, Low Noise JFET Input Operational Amplifiers	SO-14
TL081CD,ACD,BCD	Single, JFET Input Operational Amplifier	SO-8
TL082CD,ACD,BCD	Dual, JFET Input Operational Amplifiers	SO-8
TL084CD,ACD,BCD*	Quad, JFET Input Operational Amplifiers	SO-14
TL431CD	Programmable Precision Reference	SOP-8
TYA1350D	IF Amplifier (M1350D)	SO-8
UAA1041D	Automotive Direction Indicator	SO-8
UC2842AD	Off-Line Current Mode PWM Controller	SO-14
UC2843AD	Current Mode PWM Controller	SO-14
UC3842AD	Off-Line Current Mode PWM Controller	SO-14
UC3843AD	Current Mode PWM Controller	SO-14

*To Be Introduced.
†Formerly MC13011DW

CMOS

Both the SOIC and PLCC packages are offered by Motorola for these CMOS products. The SOIC packages are denoted by a common suffix of "D" or "DW." This package identifier is added to the end of each standard part number. In the case of PLCC packages, the "FN" suffix is utilized — again after the standard device part number.

SOIC packages with a suffix "L" in the Package column indicate wide-body version (e.g., SO-24L).

Device	Function	Package
MC14433DW	3-1/2 Digit A/D Converter	SO-24
MC14442FN	11-Channel, 8-Bit A/D Converter with Parallel Interface	PLCC-28
MC14443DW	6-Channel A/D Converter Subsystem	SO-16L
MC14447*	6-Channel A/D Converter Subsystem	
MC14469FN	Addressable Asynchronous Receiver/Transmitter	PLCC-44
MC14495DW1**	Hex-to-7 Segment Latch/Decoder ROM/Driver	SO-16L
MC14497*	PCM Remote Control Transmitter	
MC14499DW	7-Segment LED Display Decoder/Driver with Serial Interface	SO-20L
MC14573D	Quad Programmable Operational Amplifier	SO-16
MC14574D	Quad Programmable Comparator	SO-16
MC14575D	Dual/Dual Programmable Amplifier-Comparator	SO-16
MC14578D	Micro-Power Comparator plus Voltage Follower	SO-16
MC144110DW	Hex D/A Converter with Serial Interface	SO-20L
MC144111DW	Quad D/A Converter with Serial Interface	SO-16L
MC145000FN	48-Segment Multiplexed LCD Driver (Master)	PLCC-28
MC145001FN	44-Segment Multiplexed LCD Driver (Slave)	PLCC-28
MC145026D	Remote Control Encoder	SO-16
MC145027DW	Remote Control Decoder	SO-16L
MC145028DW	Remote Control Decoder	SO-16L

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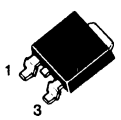
CMOS — continued

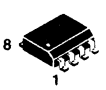
Device	Function	Package
MC145030DW	Remote Control Encoder/Decoder	SO-20L
MC145040FN1**	A/D Converter with Serial Interface	PLCC-20
MC145040FN2**	A/D Converter with Serial Interface	PLCC-20
MC145041FN1**	A/D Converter with Serial Interface	PLCC-20
MC145041FN2**	A/D Converter with Serial Interface	PLCC-20
MC145106FN	PLL Frequency Synthesizer	PLCC-20
MC145145FN★	4-Bit Data Bus Input PLL Frequency Synthesizer	PLCC-20
MC145146FN★	4-Bit Data Bus Input PLL Frequency Synthesizer	PLCC-20
MC145151FN★	Parallel Input PLL Frequency Synthesizer	PLCC-28
MC145152FN★	Parallel Input PLL Frequency Synthesizer	PLCC-28
MC145155FN★	Serial Input PLL Frequency Synthesizer	PLCC-20
MC145155DW★	Serial Input PLL Frequency Synthesizer	SO-20L
MC145156FN★	Serial Input PLL Frequency Synthesizer	PLCC-20
MC145156DW★	Serial Input PLL Frequency Synthesizer	SO-20L
MC145157FN★	Serial Input PLL Frequency Synthesizer	PLCC-20
MC145157DW★	Serial Input PLL Frequency Synthesizer	SO-16L
MC145158FN★	Serial Input PLL Frequency Synthesizer	PLCC-20
MC145158DW★	Serial Input PLL Frequency Synthesizer	SO-16L
MC145159FN★	Serial Input PLL Frequency Synthesizer with Analog Phase Detector	PLCC-20
MC145453FN	33-Segment LCD Driver with Serial Interface	PLCC-44

*Introduction of these devices in surface mount packages is dependent on market demand.
**The digit 1 or 2 after the package designator is not a part of the package definition but describes electrical capability of the device.
★Electrical variations may require a numerical suffix after the package suffix. Contact your Motorola representative for details.

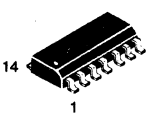
Surface Mount Technology Package Overview



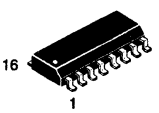
CASE 369A
PLASTIC
DPAK
DT SUFFIX



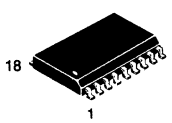
CASE 751
PLASTIC
SO-8, SOP-8
D SUFFIX



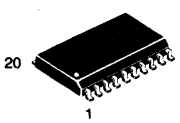
CASE 751A
PLASTIC
SO-14
D SUFFIX



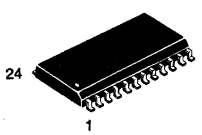
CASE 751B
PLASTIC
SO-16
D SUFFIX



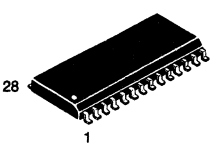
CASE 751C
PLASTIC
SO-18
DW SUFFIX



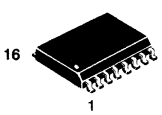
CASE 751D
PLASTIC
SO-20
DW SUFFIX



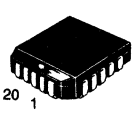
CASE 751E
PLASTIC
SO-24
DW SUFFIX



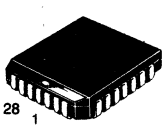
CASE 751F
PLASTIC
SO-28
DW SUFFIX



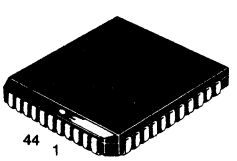
CASE 751G
PLASTIC
SO-16L
DW SUFFIX



CASE 775
PLASTIC
PLCC-20
FN SUFFIX



CASE 776
PLASTIC
PLCC-28
FN SUFFIX



CASE 777
PLASTIC
PLCC 44
FN SUFFIX

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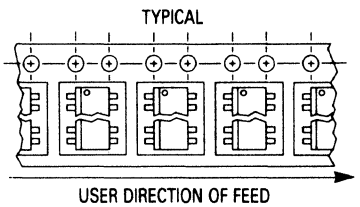
Tape and Reel

Standard Bipolar Logic, Bipolar Analog and MOS Integrated Circuits

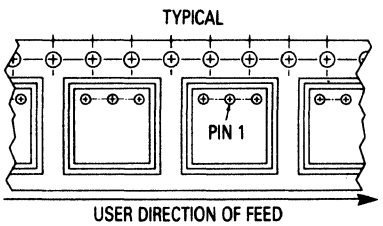
Motorola has now added the convenience of Tape and Reel packaging for our growing family of standard Integrated Circuit products. Two reel sizes are available, for all but the largest types, to support the requirements of both first and second generation pick-and-place equipment. The packaging fully conforms to the latest EIA-481A specification. The anti-static embossed tape provides a secure cavity, sealed with a peel-back cover tape.

Mechanical Polarization

SOIC DEVICES



PLCC DEVICES



Package	Tape Width (mm)	Device per Reel	Reel Size* (inch)	Tape & Reel Lot Size(1) (Min)	Device Suffix
SO-8, SOP-8	12 12	750 2,500	7 13	5,000 5,000	R1 R2
SO-14	16 16	750 2,500	7 13	5,000 5,000	R1 R2
SO-16	16 16	750 2,500	7 13	5,000 5,000	R1 R2
SO-16L (WIDE)	16 16	250 1,000	7 13	5,000 5,000	R1 R2
SO-20L (WIDE)	24 24	250 1,000	7 13	5,000 5,000	R1 R2
SO-24L (WIDE)	24 24	250 1,000	7 13	5,000 5,000	R1 R2
SO-28L (WIDE)	24 24	200 1,000	7 13	3,000 3,000	R1 R2
PLCC-20	16 16	200 1,000	7 13	3,000 3,000	R1 R2
PLCC-28	24 24	200 500	7 13	2,400 2,500	R1 R2
PLCC-44	32 32	200 500	7 13	2,000 2,000	R1 R2
PLCC-52 PLCC-68 PLCC-84	32 44 44	500 250 250	13 13 13	2,000 2,000 2,000	R2 R2 R2
TO-226AA	18	1800	13	10,000	RA, RB or RP only

Notes: 1. Minimum lot size information applies to OEM customers. Distributors may break lots or reels at their option, however broken reels may not be returned.
2. Integrated Circuits in TO-226AA packages are available in Styles A and B only, with optional "Ammo Pack" (Suffix RP).

For ordering information please contact your local Motorola Semiconductor Sales Office.
Distribution minimum order quantity is 1 reel.
*Reel size: 7"/178 mm, 13"/330 mm.

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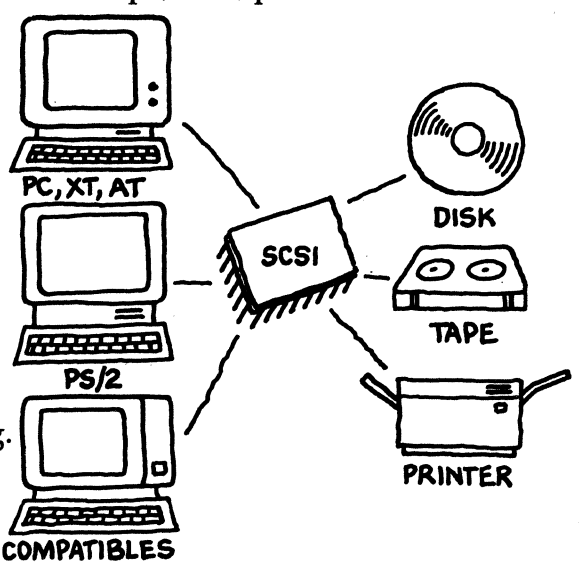
Merger Candidates.

NCR

The merger maker is NCR's 53C400 host adapter.

With it, you can connect any SCSI-based tape, disk, printer or other peripheral to the full range of IBM PC, XT, AT and compatible personal computers and the IBM Personal System/2 Model 30.



A 53C400 engineered merger is beneficial to both sides of the bus. On the peripheral side, it provides high throughput — supporting asynchronous data transfer rates up to 2.0 MBytes/sec. All the while assuring the highest data integrity with parity generation and checking. And with on-chip single-ended transceivers, it helps minimize board space.

The host side of the bus benefits, too. Through the use of Programmed Input/Output, the memory MOVE BLOCK instruction and two rotating 128-byte buffers, the chip matches speed between the SCSI bus and host bus and allows bursts up to 1 MByte/sec.

The NCR53C400 has virtually everything you need. All you add is external ROM and optional static RAM to the controller board to create a complete solution. The 53C400 will also be offered with a ROM BIOS and installable driver at no additional cost.

And the 53C400 has a memory mapped interface that makes it easier to program than I/O mapped devices.

Let NCR help you manage PC/peripheral mergers. For more information write to NCR Microelectronics, 1635 Aeroplaza Drive, Colorado Springs, CO 80916. Or call 1-800-525-2252.

Creating value

NCR Corp.

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Hue Betcha.

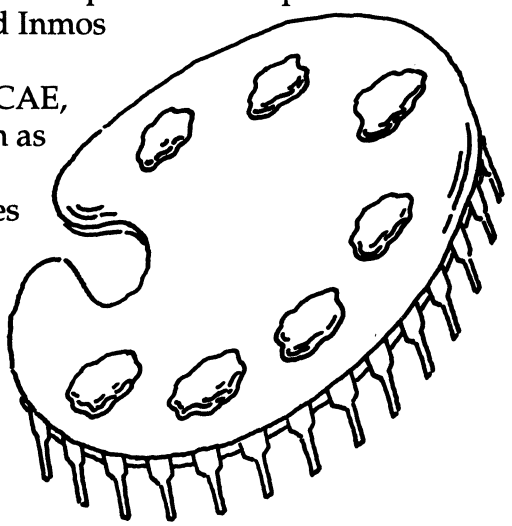
NCR

Hue better believe NCR has the color chip for your next VGA solution.

Palette DAC is an integrated Color Lookup Table that's pin compatible with the industry standard Inmos CLUT used in IBM PS/2 computers.

But hue can use it for CAD/CAM/CAE, image processing and instrumentation as well as personal computers.

The NCR 77C171 Palette DAC comes in two versions. The 36 MHZ version is what hue want for standard VGA and enhanced VGA controllers supporting 132 column displays and 800 X 600 formats. The 50 MHZ version supports 8514A format display controllers.



NCR Corp.

The chip displays 256 colors (from a universe of 262,144) via its 256 X 18 palette RAM and three six-bit DACs.

And the 77C171 provides full blanking capability — blanking both display data and microprocessor palette access. This allows the palette to be updated during active displays without producing snow.

The chip includes a bidirectional microprocessor interface for loading and reading the palette RAM. And a pixel word mask register can be logically ANDed with the incoming display pixel addresses to produce hidden figures, animation and blinking — without rewriting palette RAM values.

Are hue interested enough to find out more? Would hue like a sample? Then write to NCR Microelectronics Division, 1635 Aeroplaza Drive, Colorado Springs, CO 80916. Or call 1-800-525-2252.

Creating value

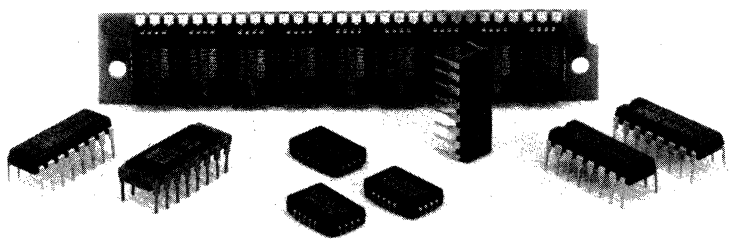
HIGH SPEED DRAMS

NEW

NMB TECHNOLOGIES

Now – Highest speed AND production – 60/70/80ns 1Mb and 256K FutureFast™ DRAMS.

FEATURES



- CMOS Technology
- Variety of Packages and Modes
- Wide Operating Margins
- Advanced Processing and Testing
- Very High Speed
- Volume Production
- State-of-the-art Design

NMB Semiconductor

AAA2800 256K DRAM

- **Access Time:** 60, 70, 80 ns
- **Organization:** 256K×1
- **Modes:** Fast Page, Static Column
- **Packages:** P-DIP, C-DIP, PLCC, SIMM
- **Status:** Production: Now

PARAMETER	SYMBOL	256K × 1		
Max. $\overline{RAS}$ Access Time	^tRAC	60 ns	70 ns	80 ns
Max. Column Address Access Time	^tCAA	32	35	40
Min. Read/Write Cycle Time	^tRC	121	136	151
Static Column Mode Read Cycle Time	^tSRC	35	40	45
Static Column Mode Write Cycle Time	^tSWC	35	38	40
Fast Page Mode Cycle Time	^tPC	37	41	46

AAA1M100 1Mb DRAM

- **Access Time:** 100, 120 ns
- **Organization:** 256K×4; 1Mb×1
- **Modes:** Fast Page, Static Column
- **Packages:** P-DIP, C-DIP, ZIP, SOJ, SIMM
- **Status:** Production: 4Q1988

PARAMETER	SYMBOL	1Mb × 1		256K × 4	
Max. $\overline{RAS}$ Access Time	^tRAC	100 ns	120 ns	100 ns	120 ns
Max. Column Address Access Time	^tCAA	50	60	50	60
Min. Read/Write Cycle Time	^tRC	190	220	190	220
Static Column Mode Cycle Time	^tSRC, ^tSWC	55	65	55	65
Fast Page Mode Cycle Time	^tPC	55	55	55	65

AAA1M200 1Mb DRAM

- **Access Time:** 60, 70, 80 ns
- **Organization:** 256K×4; 1Mb×1
- **Modes:** Fast Page, Static Column
- **Packages:** P-DIP, C-DIP, ZIP, SOJ, SIMM
- **Status:** Production: 1Q1989

PARAMETER	SYMBOL	1Mb × 1			256K × 4		
Max. $\overline{RAS}$ Access Time	^tRAC	60 ns	70 ns	80 ns	60 ns	70 ns	80 ns
Max. Column Address Access Time	^tCAA	30	35	40	30	35	40
Min. Read/Write Cycle Time	^tRC	100	115	130	100	115	130
Static Column Mode Cycle Time	^tSRC, ^tSWC	35	40	45	35	40	45
Fast Page Mode Cycle Time	^tPC	40	45	50	40	45	50

* Specificiations subject to change without notice.

NMB TECHNOLOGIES INCORPORATED

SEMICONDUCTOR DIVISION

For complete specifications and pricing, contact

NMB TECHNOLOGIES INCORPORATED

9730 Independence Ave., Chatsworth, CA 91311 • Telephone: (818) 341-3355

FAX: (818) 341-8207 • TWX: (910) 494-1232 • Telex Number: 651340

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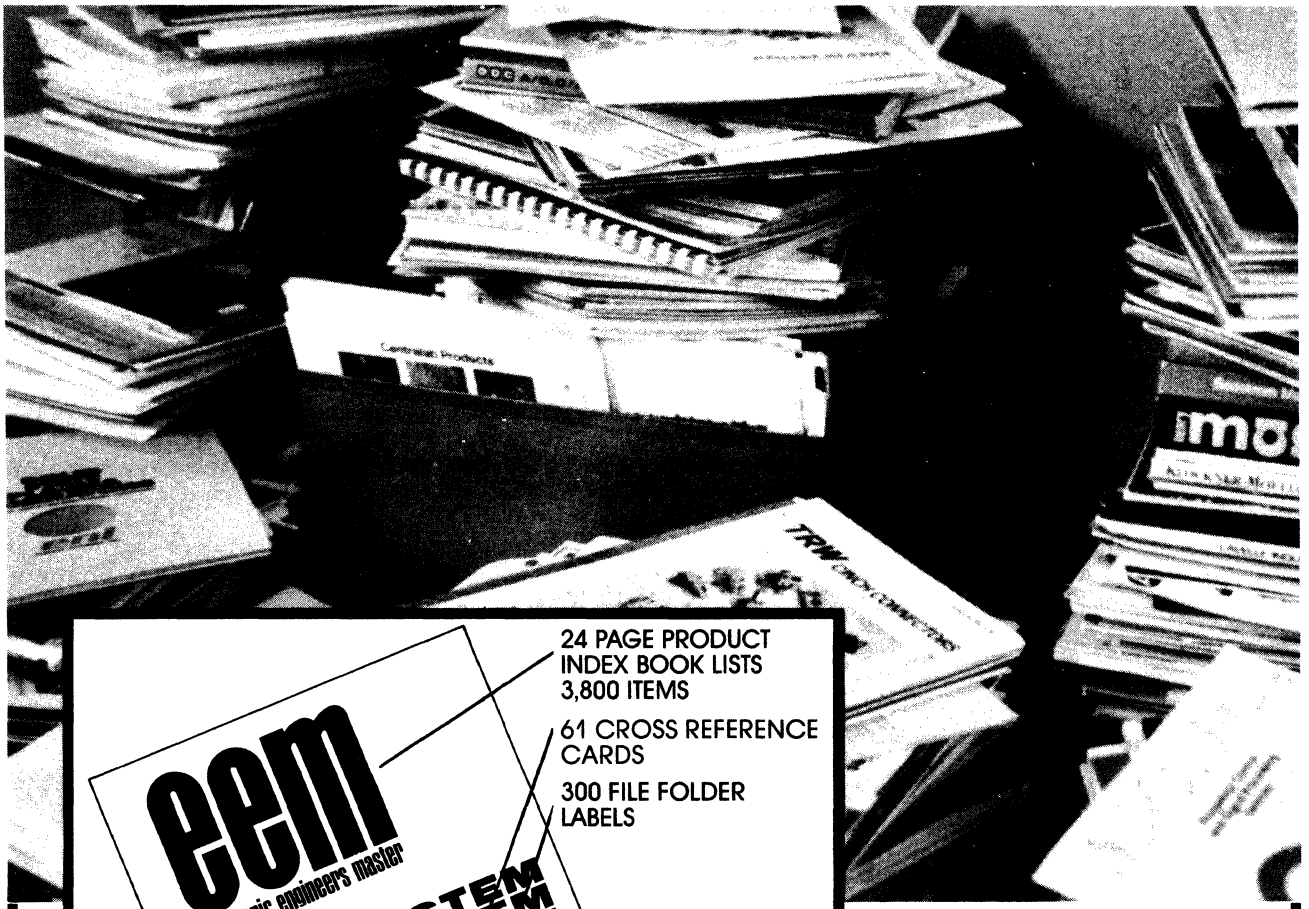

ALL NEW with this edition of EEM

GET ORGANIZED!

Are your catalog files organized? Can you find any given catalog in a matter of seconds? If your answer is "Yes," you probably already have the EEM File System. But, if you said "No," you really ought to look into this simple system. It will save hours of time and tons of aggravation.

The EEM File System was invented over twenty-five years ago to help people who specify, buy, or work with electronic products and equipment. It is upgraded on a constant basis to reflect the current state of the art. It's easy to use and easy to customize to your particular needs.

You say you want to file catalogs by type of product? That's easy to do with The System. But, what are you going to do when there are multiple products in one catalog? Take Mallory for example. There are all kinds of products in the Mallory Short Form Catalog. With the EEM File System all you do is file the catalog under "M" for Mallory and refer to it on all of the cross reference cards that apply.

There are thousands of EEM File Systems in everyday use in engineering and procurement offices all over the world. Shouldn't you be using this proven system?

The EEM File System is shipped in one neat package. The package contains everything you need to set up your very own filing system. Best of all, it's easy to get and very affordable. Send a check or money order for $25.00 and EEM will pay the postage and sales tax. If you must use a purchase order, please add $2.00 for postage and handling. An invoice will be mailed to you under separate cover.

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EEM FILE SYSTEM,
645 stewart ave., garden city, ny 11530

OXFORD COMPUTER

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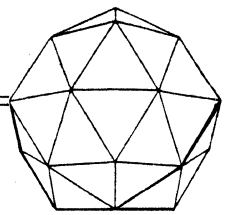

INTELLIGENT MEMORY CHIPS

Steven G. Morton,
Founder and Chief Technical Officer

INTELLIGENT MEMORY CHIPS PROVIDE A LEAPFROG IN PERFORMANCE ACROSS THE SPECTRUM OF ULTRA HIGH PERFORMANCE NUMERICAL COMPUTING

In most computers, large amounts of data are stored in memory chips. This data must be moved to a separate processor, only to have the results returned to memory. This is like taking the mountain (of data) to Mohammed (the processor). We take Mohammed to the mountain, breaking the Von Neumann bottleneck.

Our "Intelligent Memory Chips" are matrix-vector multipliers. We place multiple, simple, serial processor slices within custom-designed, CMOS memory chips. Multiple chips work together in a small module to provide any matrix or vector precision desired. Inherently parallel, as more modules are used in a system, not only does the storage capacity increase, but the amount of processing power directly increases as well. By eliminating inefficiencies in the movement and processing of data, these chips and modules provide systems that are 10-times or more cost-effective than previously available. Systems performing BILLIONS to TRILLIONS of multiply-and-add operations per second are readily achieved.

A full family of Intelligent Memory Chips, support chips, multi-chip modules, evaluation boards and software tools is planned. Joint ventures are invited.

Oxford Computer

APPLICATIONS

Digital Signal Processing
- Image Processing
- Large, Multi-window Convolution
- 2-D and 3-D FFTs
- Adaptive Filters

Matrix Multiplication
- 3-D Graphics
- Fixed- and Floating-Point Supercomputing
- Pattern Recognition
- Artificial Neural Networks

SHORT-FORM SPECIFICATIONS (Advance Information)

Intelligent Convolution Memory		Intelligent Graphics Memory
♦64K * 1-bit Chip (64K1-ICMC)		♦256K * 4-bits Chip (256K4-IGMC)
•256 rows * 256 columns SRAM	:Matrix Memory:	•64K rows * 4 columns DRAM
•1	:Matrix Bits/Element/Chip:	•4
•1 element @ 1b	:Matrix I/O:	•1 element @ 4b
•256 rows * 2 columns @ 16b	:Vector Memory:	•4 * 4 transform matrix @ 32b
•1	:Vector Bits/Element/Cycle:	•8
•1 element @ 8b	:Vector I/O:	•4 elem @ 4b via Matrix Memory
•256 @ 1b * 1b	:Processor Slices:	•4 @ 4b (matrix) * 8b (vector)
•fixed-point	:Data Format:	•fixed-point (flt.-pt. in '90)
•256-point, 2-D convolution	:Other:	•dual-port Matrix Memory
♦64KB @ 8-bits Module (64K8-ICMM)		♦1MB @ 32-bits Module (1MB32-IGMM)
•locally cascadable for very large matrices and convolution windows		•lighting calculations
		•memory mapped matrix I/O
•globally cascadable for hierarchical networks		•internal read/compute/write
•10.24B 1b * 8b mul&add/S (1b-matrix, 8b-vector)		•40M 32b * 32b mul&add/S
•1.28B 8b * 8b mul&add/S (8b-matrix, 8b-vector)		•256 * 256, 2-D, complex FFT @ 32-bits in 200mS
•256 * 256 8b-matrix * 8b-vector in 51.2 uS		•transform 64K, 32-bit 3-D vectors @ 38 Hz (2.4M t/S)
•4b * 8b 256-point convolution @ 10M pixels/S		
•1b * 8b 1K-point convolution @ 10M pixels/S		

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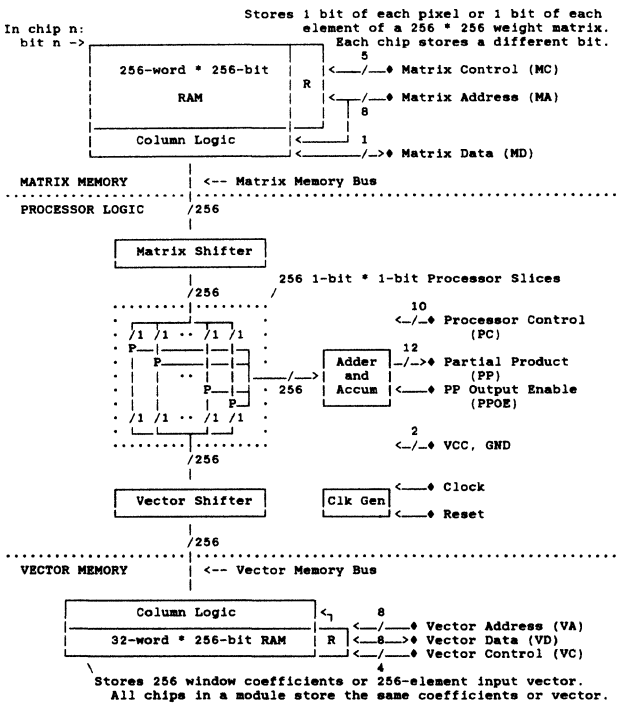
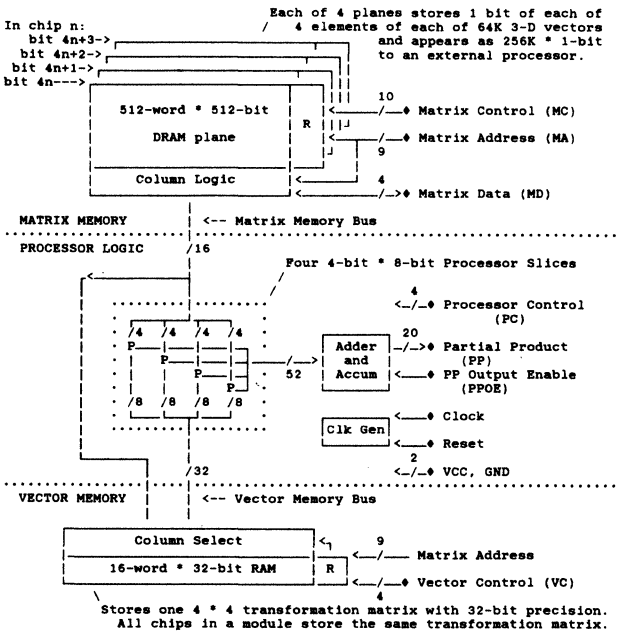
INTELLIGENT MEMORY CHIPS

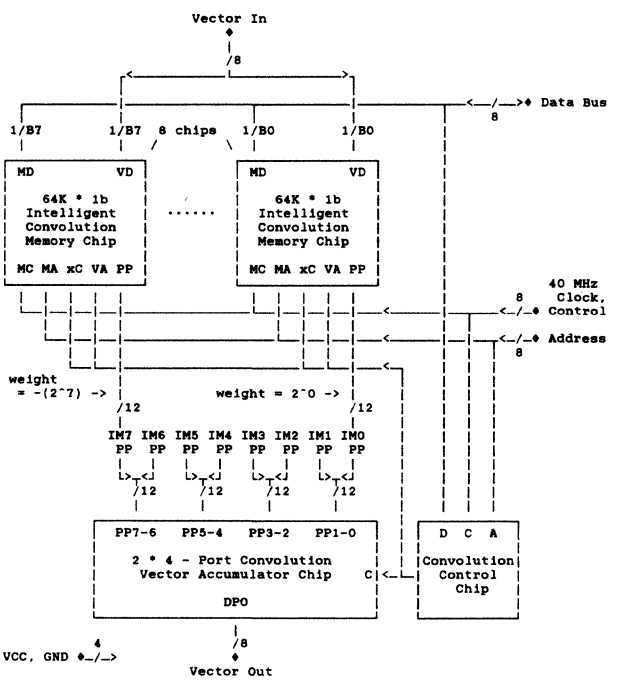
64K * 1-BIT INTELLIGENT CONVOLUTION MEMORY CHIP (64K1-ICMC)



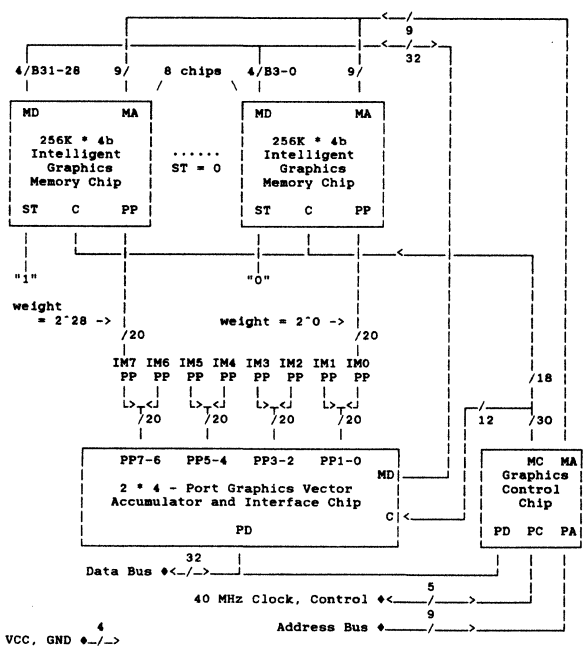
256K * 4-BITS INTELLIGENT GRAPHICS MEMORY CHIP (256K4-IGMC)



64KB @ 8-BITS INTELLIGENT CONVOLUTION MEMORY MODULE (64K8-ICMM)



1MB @ 32-BITS INTELLIGENT GRAPHICS MEMORY MODULE (1MB32-IGMM)



U. S. and Foreign Patents Pending

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PERFORMANCE ELECTRONIC PACKAGING SERVICES, INC.

6354-B CORTE DEL ABETO ☐ CARLSBAD, CALIFORNIA 92009 ☐ 619•931•7824 ☐ FAX 619•931•6557

DRAM MEMORY MODULES

PART NUMBER	ORGANIZATION	DIMENSIONS	PKG.
64 K DRAM BASED MODULES SPEEDS—120, 150, 200 nS.			
PEP4064EC4	64K × 4	2.2 × 0.42 × 0.180	22 PIN SIP
PEP4064EC5	64K × 5	2.9 × 0.42 × 0.180	24 PIN SIP
PEP4064EL8*	64K × 8	3.0 × 0.60 × 0.180	30 PIN SIP
PEP4064EL9*	64K × 9	3.0 × 0.60 × 0.180	30 PIN SIP
256 K DRAM BASED MODULES—60, 70, 80, 100, 120, 150 nS.			
PEP4256EC4	256K × 4	2.2 × 0.42 × 0.180	22 PIN SIP
PEP4256EC5	256K × 5	2.9 × 0.42 × 0.180	24 PIN SIP
PEP4256EL8*	256K × 8	3.0 × 0.60 × 0.180	30 PIN SIP
PEP4256EL9*	256K × 9	3.0 × 0.60 × 0.180	30 PIN SIP
PEP4256EL8-LP	256K × 8	3.0 × 0.45 × 0.320	30 PIN SIP
PEP4256EL9-LP	256K × 9	3.0 × 0.45 × 0.320	30 PIN SIP
1M BIT DRAM BASED MODULES—80, 100, 120 nS.			
PEP1MX4	1M × 4	2.8 × 0.42 × 0.180	24 PIN SIP
PEP1MX5	1M × 5	3.5 × 0.42 × 0.180	26 PIN SIP
PEP4MX1	4M × 1	2.8 × 0.42 × 0.180	26 PIN SIP
PEP1MX4Z	1M × 4	1.5 × 0.350 × 0.440	26 PIN ZIP
PEP4MX1Z	4M × 1	1.5 × 0.35 × 0.44	23 PIN ZIP
PEP1MX8*	1M × 8	3.2 × 0.775 × 0.190	30 PIN SIP
PEP1MX9*	1M × 9	3.2 × 0.775 × 0.190	30 PIN SIP
PEP1MX8-LP	1M × 8	3.5 × 0.435 × 0.320	30 PIN SIP
PEP1MX9-LP	1M × 9	3.5 × 0.435 × 0.320	30 PIN SIP
PEP1MX16	1M × 16	3.3 × 1.50 × 0.320	64 PIN DIP
PEP2MX8	2M × 8	3.3 × 1.50 × 0.320	64 PIN DIP
STATIC RAM MODULES—30, 45, 55, 70, 100, 120 nS.			
S128KX8	128K × 8	1.80 × 0.70	32 PIN DIP
S64KX9	64K × 9	3.3 × 0.80 × 0.200	33 PIN SIP

MEMORY EXPANSION MODULES FOR THE FOLLOWING COMPUTER SYSTEMS:

1. AST PREMIUM 286, 386, ADVANTAGE SERIES BOARDS
2. COMPAQ 286, 386 (20MHZ, 25MHZ), PORTABLE
3. CAMBRIDGE DATA SYSTEMS 286, 386 SX
4. APPLE MACINTOSH SE, MACII, MACIIE
5. SUN MICRO SYSTEMS 386i, SUN 4/110, SUN 3/60

NOTES:

1. *Also available in SIMM package.
2. Call us for your custom module requirements.

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ADC-912

CMOS MICROPROCESSOR-COMPATIBLE
12-BIT A/D CONVERTER

Precision Monolithics Inc.

FEATURES

- **Low Cost**
- **Low Transition Noise Between Codes**
- **12-Bit Accurate**
  - **±1/2 LSB Nonlinearity Error Over Temperature**
  - **No Missing Codes at All Temperatures**
- **12 Microsecond Conversion Time**
- **Internal or External Clock**
- **Fast 90ns Bus Access and Disconnect Time**
- **8 or 16-Bit Data Bus Compatible**
- **Improved ESD Resistant Design**
- **Low 95mW Power Consumption**
- **Space Saving 24-Pin 0.3" DIP, or 24-Lead SOL**

APPLICATIONS

- **Data Acquisition Systems**
- **DSP System Front End**
- **Process Control Systems**
- **Portable Instrumentation**

ORDERING INFORMATION†

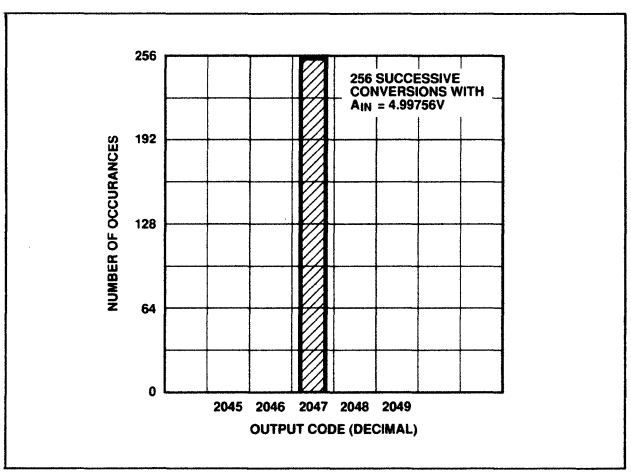
INL (LSB)	MILITARY*†† TEMPERATURE −55°C TO +125°C	EXTENDED INDUSTRIAL†† TEMPERATURE −40°C TO +85°C	COMMERCIAL TEMPERATURE 0°C TO +70°C
±1/2	ADC912BW	ADC912EP	—
±1	—	ADC912FW	—
±1	—	ADC912FP	ADC912HP
±1	—	ADC912FS	ADC912HS††

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic dip, and TO-can packages. For ordering information, see 1988 Data Book, Section 2.

†† For availability and burn-in information, contact your local sales office.

CODE REPETITION



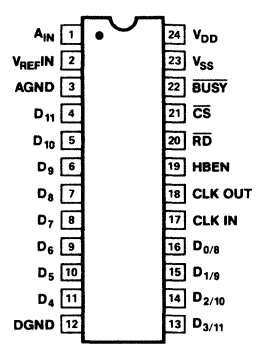
GENERAL DESCRIPTION

The ADC-912 is a monolithic 12-bit accurate CMOS A/D converter. It contains a complete successive approximation A/D converter built with a high accuracy D/A converter, a precision bipolar transistor high-speed comparator, and successive approximation logic including three-state bus interface for logic compatibility. The accuracy of the ADC-912 results from the addition of precision bipolar transistors to PMI's advanced-oxide isolated silicon-gate CMOS process. Particular attention was paid to the reduction of transition noise between adjacent codes achieving a 1/6 LSB uncertainty. The low noise design produces the same digital output for DC analog inputs not located at a transition voltage, see the Code Repetition and Transition Noise plots below. NPN transistors also provide excellent bus interface timing, 90ns access and bus disconnect time which results in faster data transfer without the need for wait states. An external 1MHz clock provides a 12μs conversion time.

In stand-alone applications an internal clock can be used with an external crystal.

An external negative five-volt reference sets the 0 to +10 volt input range. Plus five and minus 12 volt power supplies result in 95mW of total power consumption.

PIN CONNECTIONS

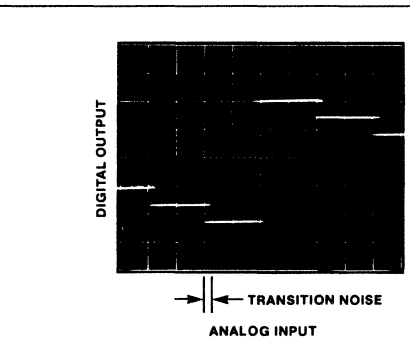


24-LEAD SOL
(S-Suffix)

24-PIN 0.3" EPOXY DIP
(P-Suffix)

24-PIN 0.3" CERDIP
(W-Suffix)

TRANSITION NOISE CROSS PLOT



9/88, Rev. C

Precision Monolithics

DAC-8043

12-BIT SERIAL INPUT
MULTIPLYING CMOS D/A CONVERTER IN 8-PIN PACKAGE

Precision Monolithics Inc.

ADVANCE PRODUCT INFORMATION

FEATURES

- **12-Bit Accuracy in an 8-Pin Mini-Dip**
- **Fast Serial Data Input**
- **Double Data Buffers**
- **Low ±1/2 LSB Max INL and DNL**
- **Max Gain Error—±1 LSB**
- **Low 5ppm/°C Max Tempco**
- **ESD Resistant**

APPLICATIONS

- **Auto-Calibration Systems**
- **Process Control and Industrial Automation**
- **Programmable Amplifiers and Attenuators**
- **Digitally-Controlled Filters**

GENERAL DESCRIPTION

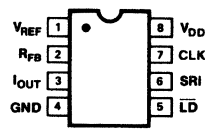
The DAC-8043 is a high accuracy 12-bit CMOS multiplying DAC in a space-saving 8-pin mini-DIP package. Featuring serial data input, double buffering, and excellent analog performance, the DAC-8043 is ideal for applications where PC board space is at a premium. Separate input strobe and load-DAC control lines allow full user control of data loading and analog output.

The circuit consists of a 12-bit serial-in, parallel-out shift register, a 12-bit DAC register, a 12-bit CMOS DAC, and control logic. Serial data is clocked into the input register on the rising edge of the CLOCK pulse. When the new data word has been clocked in, it is loaded into the DAC register with the $\overline{LD}$ input pin.

Operating from a single +5V power supply, the DAC-8043 is the ideal low power, small size, high performance solution to many applications problems.

For applications requiring an asynchronous CLEAR function or more versatile microprocessor interface logic, refer to the PM-7543.

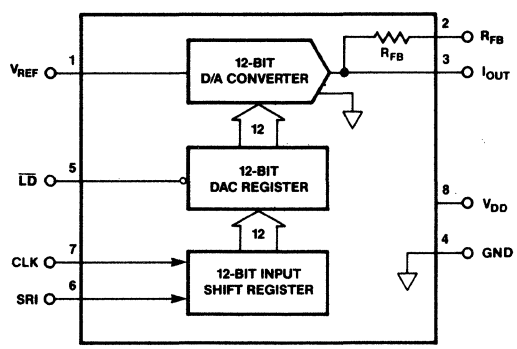
PIN CONNECTIONS



8-PIN EPOXY DIP
(P-Suffix)

8-PIN CERDIP
(Z-Suffix)

FUNCTIONAL BLOCK DIAGRAM



This advance product information describes a product in development at the time of this printing. Final specifications may vary. Please contact local sales office or distributor for final data sheet.

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DAC-8221

DUAL 12-BIT BUFFERED
MULTIPLYING CMOS D/A CONVERTER

Precision Monolithics Inc.

FEATURES

- **Two Matched 12-Bit DACs on One Chip**
- **Packaged in a Narrow 0.3" 24-Pin DIP**
- **Direct Parallel Load of All 12 Bits for High Data Throughput**
- **On-Chip Latches for Both DACs**
- **12-Bit Endpoint Linearity (±1/2 LSB) Over Temperature**
- **+5V to +15V Single Supply Operation**
- **DACs Matched to 0.2% Typically**
- **Four-Quadrant Multiplication**
- **Improved ESD Resistance**

APPLICATIONS

- **Automatic Test Equipment**
- **Industrial Automation**
- **Robotics/Process Control**
- **Programmable Instrumentation Equipment**
- **Programmable Gain/Attenuation Control**
- **Ideal for Battery-Operated Equipment**

ORDERING INFORMATION†

RELATIVE ACCURACY (+5V or +15V)	GAIN ERROR	PACKAGE: MILITARY* TEMPERATURE −55°C to +125°C	PACKAGE: INDUSTRIAL TEMPERATURE −40°C to +85°C	PACKAGE: COMMERCIAL TEMPERATURE 0°C to +70°C
±1/2 LSB	±1 LSB	DAC8221AW	DAC8221EW	—
±1/2 LSB	±2 LSB	—	—	DAC8221GP
±1 LSB	±4 LSB	—	DAC8221FW	DAC8221HP
±1 LSB	±4 LSB	—	DAC8221FP	DAC8221HS††

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic dip, and TO-can packages. For ordering information, see 1988 Data Book, Section 2.

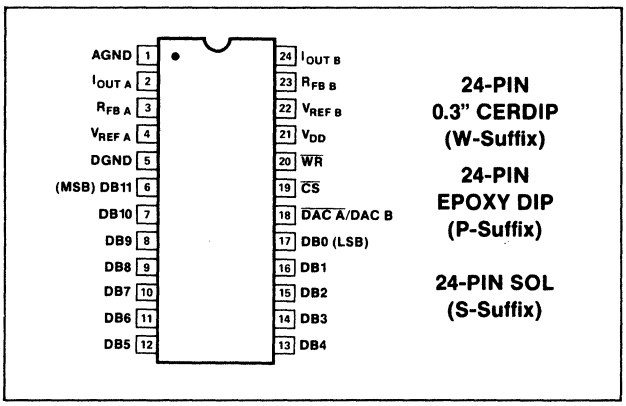
†† For availability and burn-in information on SO and PLCC packages, contact your local sales office.

GENERAL DESCRIPTION

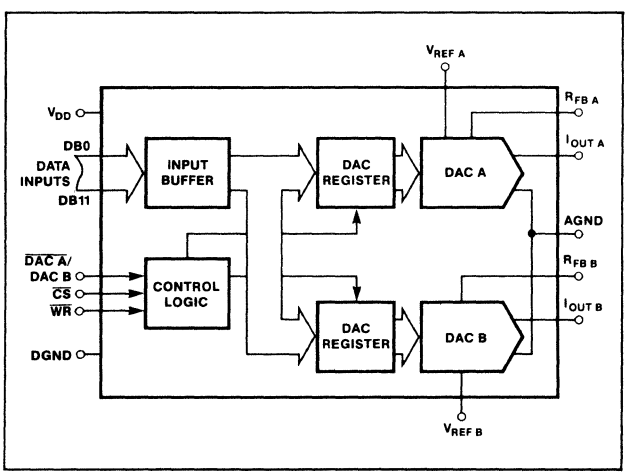
The DAC-8221 combines two identical 12-bit, multiplying, digital-to-analog converters into a single CMOS chip. This device is electrically similar to DAC-8212 with improved microprocessor interface timing and is packaged in a narrow 0.300" DIP. Monolithic construction offers excellent DAC-to-DAC matching and tracking over the full operating temperature range. The DAC-8221 consists of two thin-film R-2R resistor-ladder networks, two 12-bit data latches, one 12-bit input buffer, and control logic. The DAC-8221 operates on a single supply from +5V to +15V. Maximum power dissipation with 0V and +5V logic levels and a +5V supply is less than 0.5mW. The DAC-8221 is manufactured using PMI's highly-stable, thin-film resistors on an advanced oxide-isolated, silicon-gate, CMOS process. PMI's improved latch-up resistant design eliminates the need for external protective Schottky diodes.

A common 12-bit (TTL/CMOS compatible) input port is used to load a 12-bit-wide word into either of the two DACs. This port, whose data loading is similar to that of a RAM's write cycle, interfaces directly with most 12-bit or wider bus systems. With $\overline{WR}$ and $\overline{CS}$ lines at logic LOW, the input data registers are transparent. This allows direct unbuffered data to flow directly to the DAC output selected by $\overline{DAC\ A}$/DAC B control input. For applications requiring double-buffering, see the DAC-8222.

PIN CONNECTIONS



FUNCTIONAL DIAGRAM



Precision Monolithics

4/88, Rev. A1

DAC-8222

DUAL 12-BIT DOUBLE-BUFFERED MULTIPLYING CMOS D/A CONVERTER

Precision Monolithics Inc.

FEATURES

- **Two Matched 12-Bit DACs on One Chip**
- **Direct Parallel Load of All 12 Bits for High Data Throughput**
- **Double-Buffered Digital Inputs**
- **12-Bit Endpoint Linearity (±1/2 LSB) Over Temperature**
- **+5V to +15V Single Supply Operation**
- **DACs Matched to 1% Max**
- **Four-Quadrant Multiplication**
- **Improved ESD Resistance**
- **Packaged in a Narrow 0.3" 24-Pin DIP and 0.3" 24-Pin SOL package**

APPLICATIONS

- **Automatic Test Equipment**
- **Robotics/Process Control/Automation**
- **Programmable Gain/Attenuation Control**
- **Ideal for Battery-Operated Equipment**

ORDERING INFORMATION†

RELATIVE ACCURACY (+5V or +15V)	GAIN ERROR	PACKAGE: MILITARY* TEMPERATURE −55°C to +125°C	PACKAGE: INDUSTRIAL TEMPERATURE −40°C to +85°C	PACKAGE: COMMERCIAL TEMPERATURE 0°C to +70°C
±1/2 LSB	±1 LSB	DAC8222AW	DAC8222EW	—
±1/2 LSB	±2 LSB	—	—	DAC8222GP
±1 LSB	±4 LSB	—	DAC8222FW	DAC8222HP
±1 LSB	±4 LSB	—	DAC8222FP	DAC8222HS††

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic dip, and TO-can packages. For ordering information, see 1988 Data Book, Section 2.

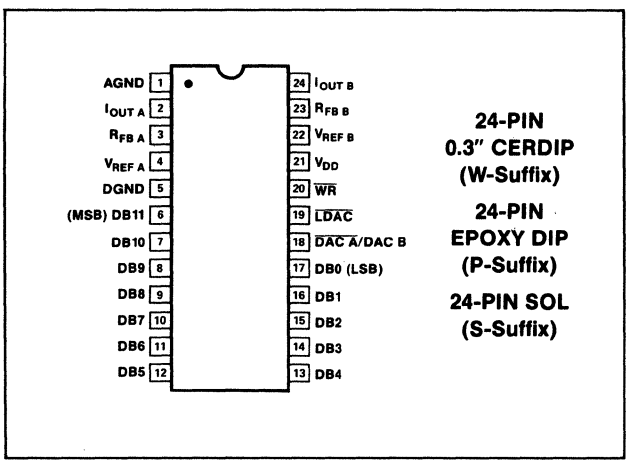
†† For availability and burn-in information on SO and PLCC packages, contact your local sales office.

GENERAL DESCRIPTION

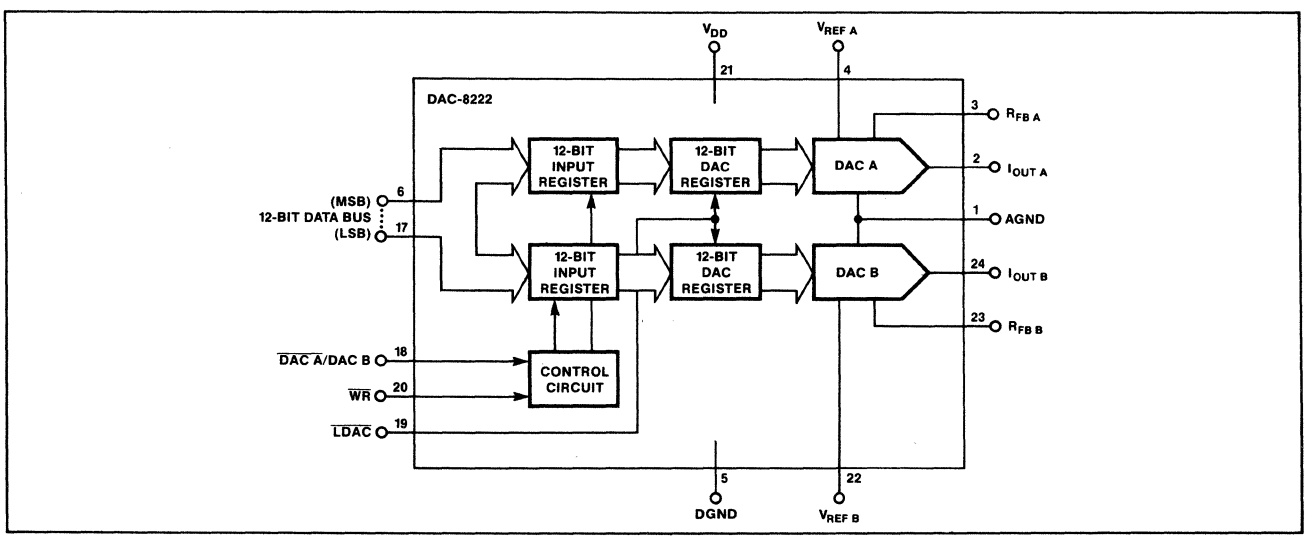
The DAC-8222 is a dual 12-bit, double-buffered, CMOS digital-to-analog converter. It has a 12-bit wide data port that allows a 12-bit word to be loaded directly. This achieves faster throughput time in stand-alone systems or when interfacing to a 16-bit processor. A common 12-bit input TTL/CMOS compatible data port is used to load the 12-bit word into either of the two DACs. This port, whose data loading is similar to that of a RAM's write cycle, interfaces directly with most 12-bit and 16-bit bus systems. (See PMI's DAC-8248 for a complete 8-bit data bus interface product.) A common bus allows the DAC-8222 to be packaged in a narrow 24-pin 0.3" DIP and save PCB space.

The DAC is controlled with two signals, $\overline{WR}$ and $\overline{LDAC}$. With logic low at these inputs, the DAC registers become transparent.

PIN CONNECTIONS



FUNCTIONAL DIAGRAM



3/88, Rev. A1

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DAC-8248

DUAL 12-BIT (8-BIT BYTE)
DOUBLE-BUFFERED CMOS D/A CONVERTER

Precision Monolithics Inc.

FEATURES

- **Two matched 12-bit DACs on One Chip**
- **12-Bit Resolution with an 8-Bit Data Bus**
- **Direct Interface with 8-Bit Microprocessors**
- **Double-Buffered Digital Inputs**
- **$\overline{\text{RESET}}$ to Zero Pin**
- **12-Bit Endpoint Linearity (±1/2 LSB) Over Temperature**
- **Single +5V to +15V Supply Operation**
- **Latch-Up Resistant**
- **Improved ESD Resistance**
- **Packaged in a Narrow 0.3" 24-Pin DIP and 0.3" 24-Pin SOL Package**

APPLICATIONS

- **Multi-Channel Microprocessor-Controlled Systems**
- **Robotics/Process Control/Automation**
- **Automatic Test Equipment**
- **Programmable Attenuator, Power Supplies, Window Comparators**
- **Instrumentation Equipment**
- **Battery Operated Equipment**

GENERAL DESCRIPTION

The DAC-8248 is a dual 12-bit, double-buffered, CMOS digital-to-analog converter. It has an 8-bit wide input data port that interfaces directly with 8-bit microprocessors. It loads a 12-bit word in two bytes using a single control; it can accept either a least significant byte or most significant byte first. For designs with a 12-bit or 16-bit wide data path, choose the DAC-8222 or DAC-8221.

The DAC-8248's double-buffered digital inputs allow both DAC's analog output to be updated simultaneously. This is particularly useful in multiple DAC systems where a common $\overline{\text{LDAC}}$ signal updates all DACs at the same time. A single $\overline{\text{RESET}}$ pin resets both outputs to zero.

ORDERING INFORMATION†

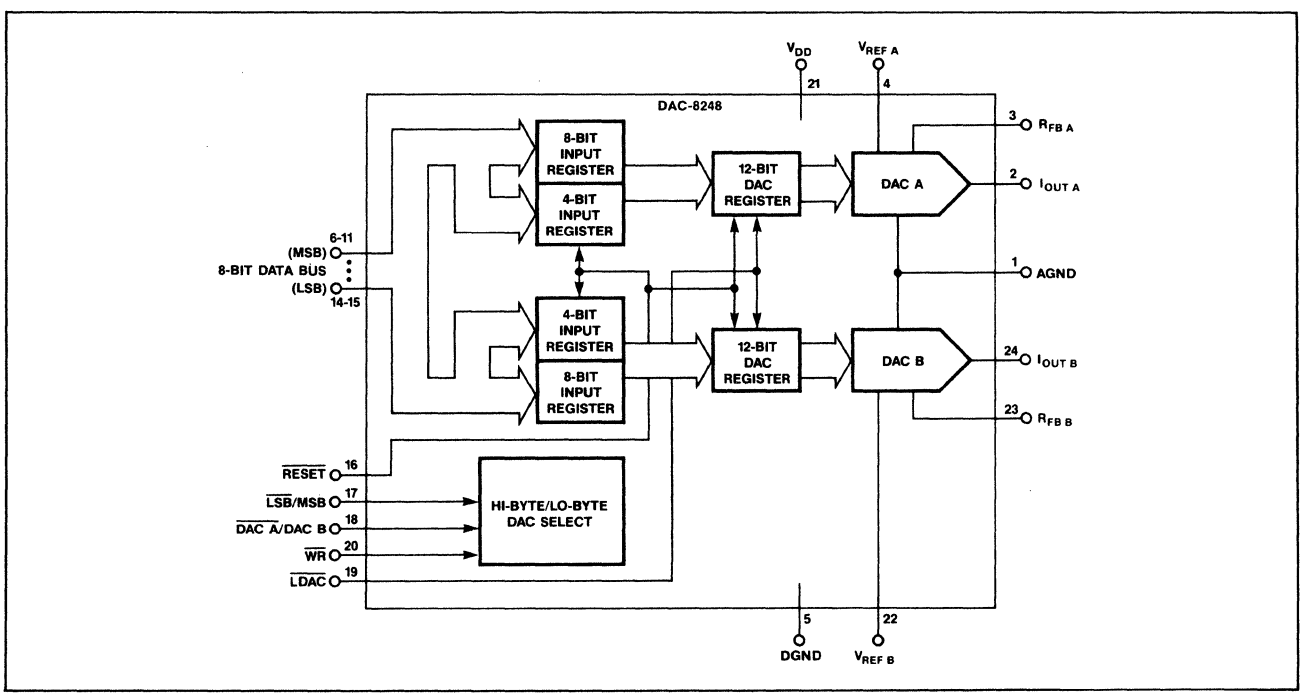
RELATIVE ACCURACY (+5V or +15V)	GAIN ERROR	PACKAGE: MILITARY* TEMPERATURE −55°C to +125°C	PACKAGE: INDUSTRIAL TEMPERATURE −40°C to +85°C	PACKAGE: COMMERCIAL TEMPERATURE 0°C to +70°C
±1/2 LSB	±1 LSB	DAC8248AW	DAC8248EW	—
±1/2 LSB	±2 LSB	—	—	DAC8248GP
±1 LSB	±4 LSB	—	DAC8248FW	DAC8248HP
±1 LSB	±4 LSB	—	DAC8248FP	DAC8248HS††

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for /883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic dip, and TO-can packages. For ordering information, see 1988 Data Book, Section 2.

†† For availability and burn-in information on SO and PLCC packages, contact your local sales office.

FUNCTIONAL DIAGRAM



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FEATURES

- **Recovers Data From Lines Varying From 0 ft. to Over 6000 ft.**
- **Wide Data Rate Range, Under 64kbps to Over 4Mbps**
- **Accepts RZ and NRZ Data Formats**
- **Accepts Unipolar and Bipolar Transmission Formats**
- **Single +5 Volt Operation**
- **Automatic Gain/Equalization Control; Dynamic Range >60dB**
- **TTL/CMOS Compatible Clock and Data Outputs**
- **Provides LOSS-OF-CARRIER Output**
- **Suitable for T1, T148, T1C, and LAN Applications**
- **Meets CCITT and ATT Specifications for ISDN Compatibility**

APPLICATIONS

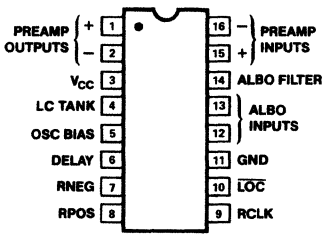
- **PBXs and LANs Using Twisted-Pair, Coax, or Fiber Optic Cable**
- **ISDN Compatible Equipment: Computers, FAX Machines, Test Equipment**
- **Industrial Communications/Process Control**
- **Digital Multiplexers, CSUs, and Switching Equipment**

GENERAL DESCRIPTION

The LIU-01 is a versatile monolithic receiver for use in serial data transmission networks. It allows the recovery of data transmitted in both RZ and NRZ formats over lines from 0 ft. to over 6000 ft. The LIU-01 separates the clock from data and presents both clock and data as TTL/CMOS compatible outputs. A LOSS-OF-CARRIER output is also provided to indicate that the incoming signal has fallen below a usable level. The LIU-01 incorporates a high gain preamplifier and dual ALBO ports enabling it to automatically adjust for the signal attenuation and frequency distortion encountered at varying lengths of twisted-pair, coax, or fiber optic transmission lines. It will tolerate an input signal range of over 60dB and can handle data rates ranging from less than 64kbps to greater than 4Mbps.

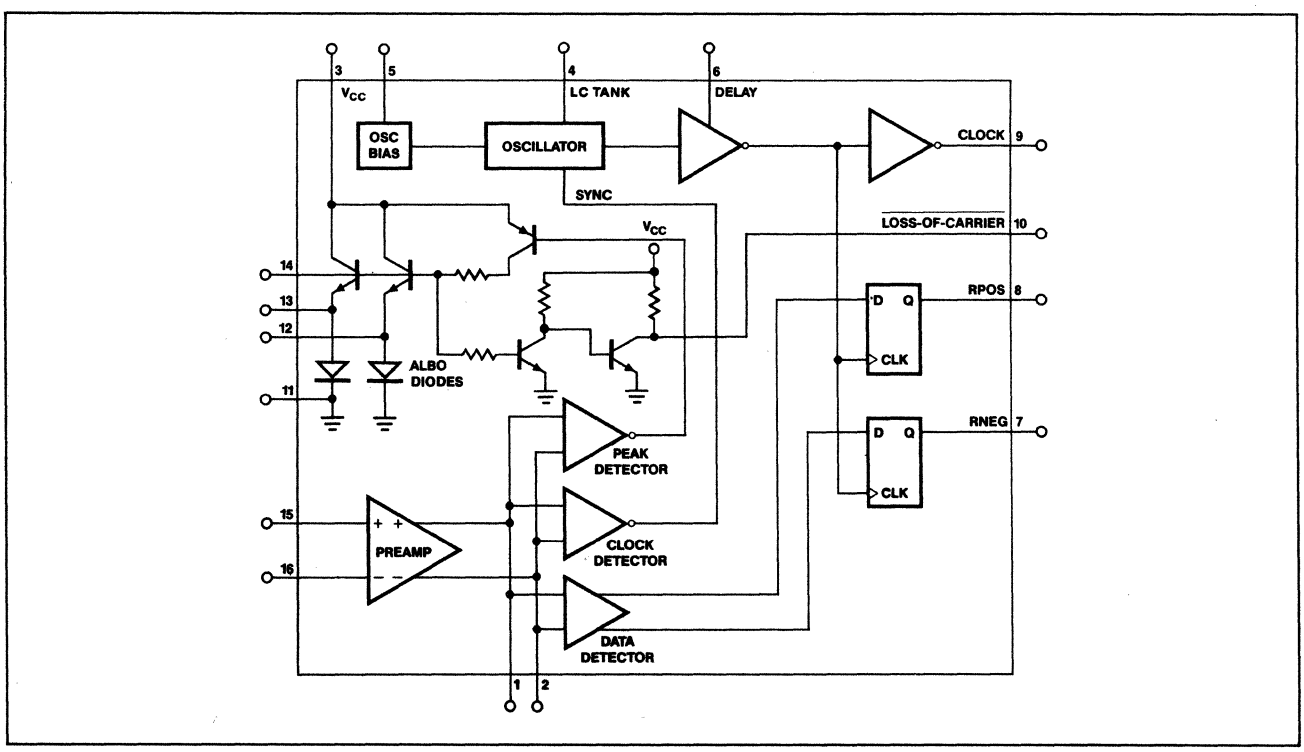
The LIU-01 meets all CCITT and ATT specifications for an ISDN compatible receiver interface. Additionally, it is directly compatible with the R8070 and, with one additional inverter gate, the DS2180 digital T1 transceivers.

PIN CONNECTIONS



16-PIN CERDIP (Q-Suffix)
16-PIN SOL (S-Suffix)
16-PIN PLASTIC DIP (P-Suffix)

FUNCTIONAL BLOCK DIAGRAM



7/88, Rev. B

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MAT-03

LOW NOISE, MATCHED, DUAL PNP TRANSISTOR

Precision Monolithics Inc.

FEATURES

- **Low Offset Voltage** ..... **100μV Max**
- **Low Noise** ..... **1nV/√Hz @ 1kHz Max**
- **High Gain** ..... **100 Min**
- **High Gain Bandwidth** ..... **190MHz Typ**
- **Tight Gain Matching** ..... **3% Max**
- **Excellent Logarithmic Conformance** ..... **$r_{BE} \simeq 0.3\Omega$ Typ**

ORDERING INFORMATION†

$T_A = +25°C$ V_{OS} MAX (μV)	PACKAGE		OPERATING TEMPERATURE RANGE
	TO-78	LCC	
100	MAT03AH*	MAT03ARC/883	MIL
100	MAT03EH	—	XIND
200	MAT03FH	—	XIND

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

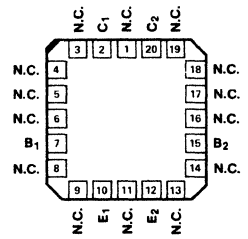
† Burn-in is available on industrial temperature range parts. For ordering information, see 1988 Data Book, Section 2.

GENERAL DESCRIPTION

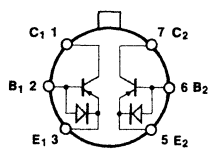
The MAT-03 dual monolithic PNP transistor offers excellent parametric matching and high frequency performance. Low noise characteristics (1nV/√Hz Max @ 1kHz), high bandwidth (190MHz typical), and low offset voltage (100μV Max), makes the MAT-03 an excellent choice for demanding preamplifier applications. In addition to tight current gain matching (3% Max mismatch), between the individual transistors, the MAT-03 also maintains high current gain (100 Min) over a wide collector current range. This tends to reduce errors in current mirrors, resulting from the current gain rolling off over extended current ranges. A low value of bulk resistance (typically 0.3Ω) also makes the MAT-03 an ideal component for applications requiring accurate logarithmic conformance.

Each transistor is individually tested to data sheet specifications. Device performance is guaranteed at 25°C and over the extended industrial and military temperature ranges. To insure the long-term stability of the matching parameters, internal protection diodes across the base-emitter junction clamp any reverse base-emitter breakdown condition which can result in degradation of gain and matching performance due to excessive breakdown current.

PIN CONNECTIONS



MAT-03ARC/883
20-CONTACT LCC
(RC-Suffix)



TO-78
(H-Suffix)

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OP-80

ULTRA-LOW BIAS CURRENT
OPERATIONAL AMPLIFIER

Precision Monolithics Inc.

PRELIMINARY

FEATURES

- **Ultra-Low Bias Current (25°C) ..... 60fA Max**
- **High-Temp Bias Current (125°C) ..... 20pA Max**
- **Low Supply Current ..... 300μA Max**
- **True Single-Supply Operation**
  - **— Common-Mode Range Includes Ground**
  - **— Output Swings to Within 400μV of Ground**
- **Extended Industrial Temp Range ..... −40°C to +85°C**

ORDERING INFORMATION†

I_B (pA)	PACKAGE TO-99	PACKAGE PLASTIC	OPERATING TEMPERATURE RANGE
0.150	OP80AJ*	—	MIL
0.060	OP80EJ	—	XIND
0.300	OP80FJ	—	XIND
2.5	OP80GJ	OP80GP	XIND
2.5	—	OP80GS††	XIND

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic dip, and TO-can packages. For ordering information see 1988 Data Book, Section 2.

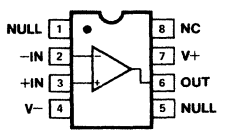
†† For availability and burn-in information on SO and PLCC packages, contact your local sales office.

GENERAL DESCRIPTION

The OP-80 CMOS operational amplifier offers exceptionally low bias currents over its entire operating temperature range. At 125°C, the OP-80 typically has a bias current of only 10pA. During room-temperature operation, the OP-80's bias current is equivalent to a mere 125 electrons per millisecond, only 20fA typical. The OP-80 is capable of operation with either single or dual supplies. Its low cost makes it attractive as a general-purpose amplifier for low-voltage systems, as well as systems demanding the highest level of precision in current-to-voltage conversion.

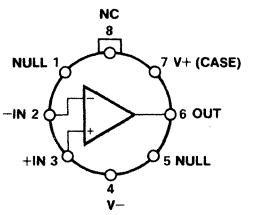
The low supply current minimizes thermal power dissipation, virtually eliminating the effects of chip self-heating. System power-supply demand is reduced as well, resulting in lower overall costs. The OP-80's CMOS design gives a good speed/power ratio, permitting a 0.2V/μs minimum slew rate and a 300kHz gain-bandwidth product with unity-gain stability.

PIN CONNECTIONS



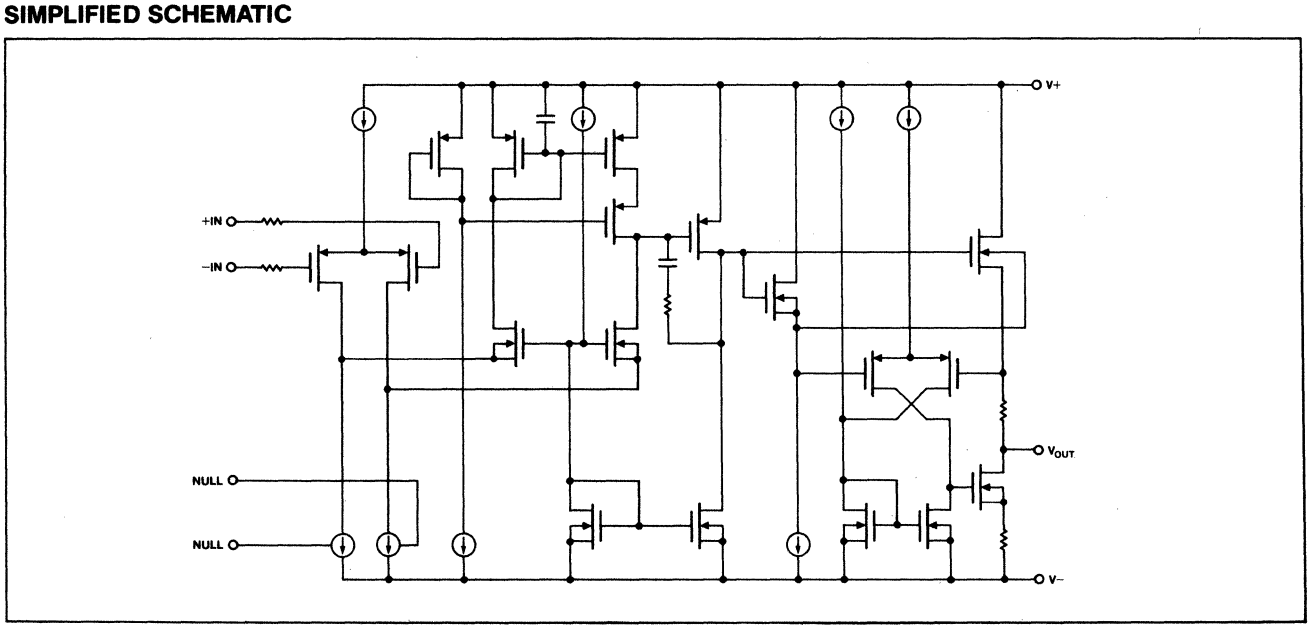
8-PIN PLASTIC DIP
(P-Suffix)

8-PIN SO
(S-Suffix)



TO-99
(J-Suffix)

SIMPLIFIED SCHEMATIC



Manufactured under U.S. Patent Number: 4,675,561.

This preliminary product information is based on testing of a limited number of devices. Final specifications may vary. Please contact local sales office or distributor for final data sheet.

9/87, Rev. A2

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OP-260

DUAL HIGH-SPEED CURRENT-FEEDBACK OPERATIONAL AMPLIFIER

Precision Monolithics Inc.

ADVANCE PRODUCT INFORMATION

FEATURES

- **Slew Rate ..... 200V/μs Min**
- **−3dB Bandwidth (A_V = 1 to 50) ..... 8MHz Min**
- **Output Current Drive ..... 20mA Min**
- **Bandwidth is Independent of Gain**

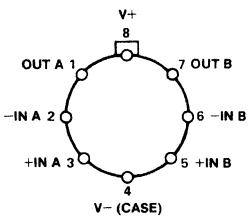
GENERAL DESCRIPTION

The OP-260 represents a new concept in high-speed monolithic operational amplifiers. A dual amplifier, the OP-260 employs current-feedback to provide consistently wideband amplification regardless of gain. A −3dB bandwidth of 8MHz minimum for gains from 1 to 50, and a bandwidth of 5MHz min in a gain of 100 combine with a 200V/μs min slew rate for extremely high-speed operation. Although gain-bandwidth product does not apply to current-feedback amplifiers, the OP-260 rivals op amps with GBWs of ½GHz!

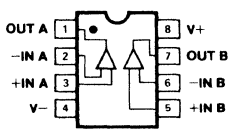
Two independent amplifiers are contained on the OP-260 chip. This allows two-channel amplification with matched AC characteristics between the two amplifiers. High-speed instrumentation front-ends are easily achieved with the OP-260 as well. The OP-260 will output substantial current. 20mA minimum current drive is available, with 40mA minimum during transients. If large loads are being driven, a clip-on heat sink is recommended.

Applications include ultrasound and sonar systems, video blocks, IF amplification and high-speed data acquisition systems.

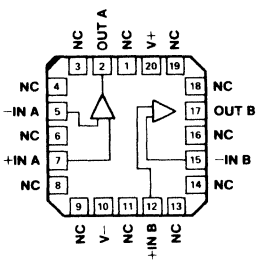
PIN CONNECTIONS



TO-99
(J-Suffix)

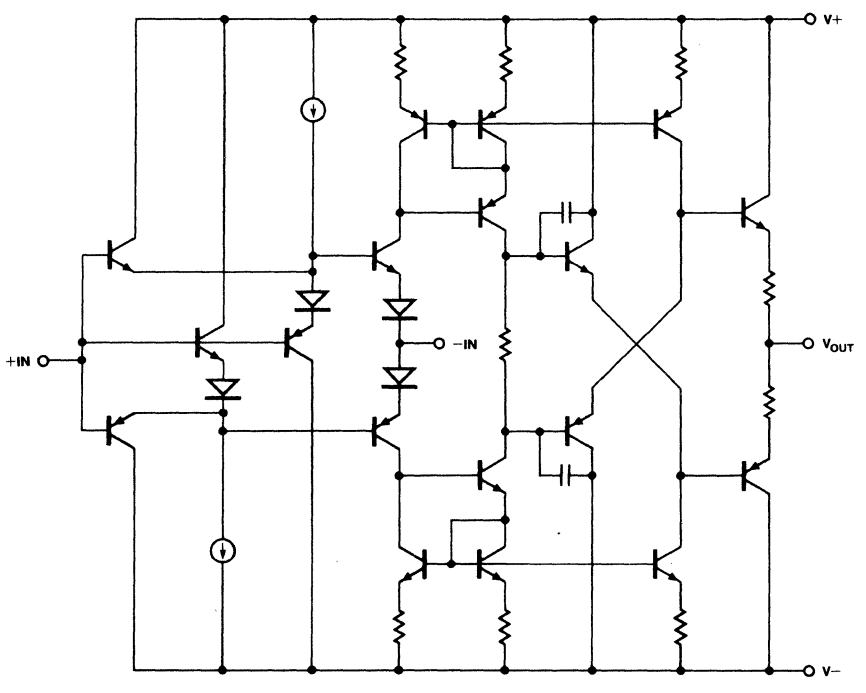


EPOXY MINI-DIP
(P-Suffix)



20-CONTACT
HERMETIC LCC
(RC-Suffix)

SIMPLIFIED SCHEMATIC (One of Two Amplifiers)



This advance product information describes a product in development at the time of this printing. Final specifications may vary. Please contact local sales office or distributor for final data sheet.

10/87, Rev. A

Precision Monolithics

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OP-271

HIGH-SPEED DUAL
OPERATIONAL AMPLIFIER

Precision Monolithics Inc.

FEATURES

- **Excellent Speed** ..... **8.5V/μs Typ**
- **Fast Settling (0.01%)** ..... **2μs Typ**
- **Unity-Gain Stable**
- **High Gain-Bandwidth** ..... **5MHz Typ**
- **Low Input Offset Voltage** ..... **200μV Max**
- **Low Offset Voltage Drift** ..... **2μV/°C Max**
- **High Gain** ..... **400V/mV Min**
- **Outstanding CMR** ..... **106dB Min**
- **Industry Standard 8-Pin Dual Pinout**

ORDERING INFORMATION†

T_A = 25°C V_{OS} MAX (μV)	PACKAGE			OPERATING TEMPERATURE RANGE
	CERDIP	PLASTIC	LCC	
200	OP271AZ*	—	OP271ARC/883	MIL
200	OP271EZ	—	—	XIND
300	OP271FZ	—	—	XIND
TBD	—	OP271GP	—	XIND
TBD	—	OP271GS††	—	XIND

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic dip, and TO-can packages. For ordering information, see 1988 Data Book, Section 2.

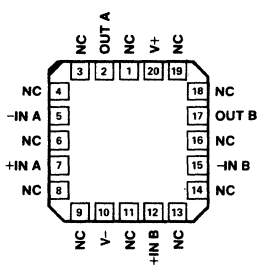
†† For availability and burn-in information on SO and PLCC packages, contact your local sales office.

GENERAL DESCRIPTION

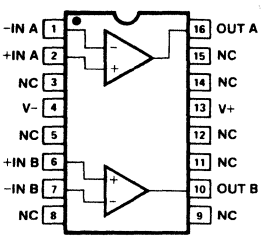
The OP-271 is a unity-gain stable monolithic dual op amp featuring excellent speed, 8.5V/μs typical, and fast settling time, 2μs typical to 0.01%. The OP-271 has a gain-bandwidth of 5MHz with a high phase margin of 62°.

Input offset voltage of the OP-271 is under 200μV with input offset voltage drift below 2μV/°C, guaranteed over the full military temperature range. Open-loop gain exceeds 400,000 into a 10kΩ load insuring outstanding gain accuracy and linearity. The input bias current is under 20nA limiting errors due to source resistance. The OP-271's outstanding CMR, over 106dB, and low PSRR, under 5.6μV/V, reduce errors caused by ground noise and power supply fluctuations. In addition, the OP-271 exhibits high CMR and PSRR over a wide frequency range, further improving system accuracy.

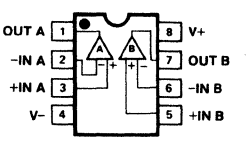
PIN CONNECTIONS



LCC
(RC-Suffix)

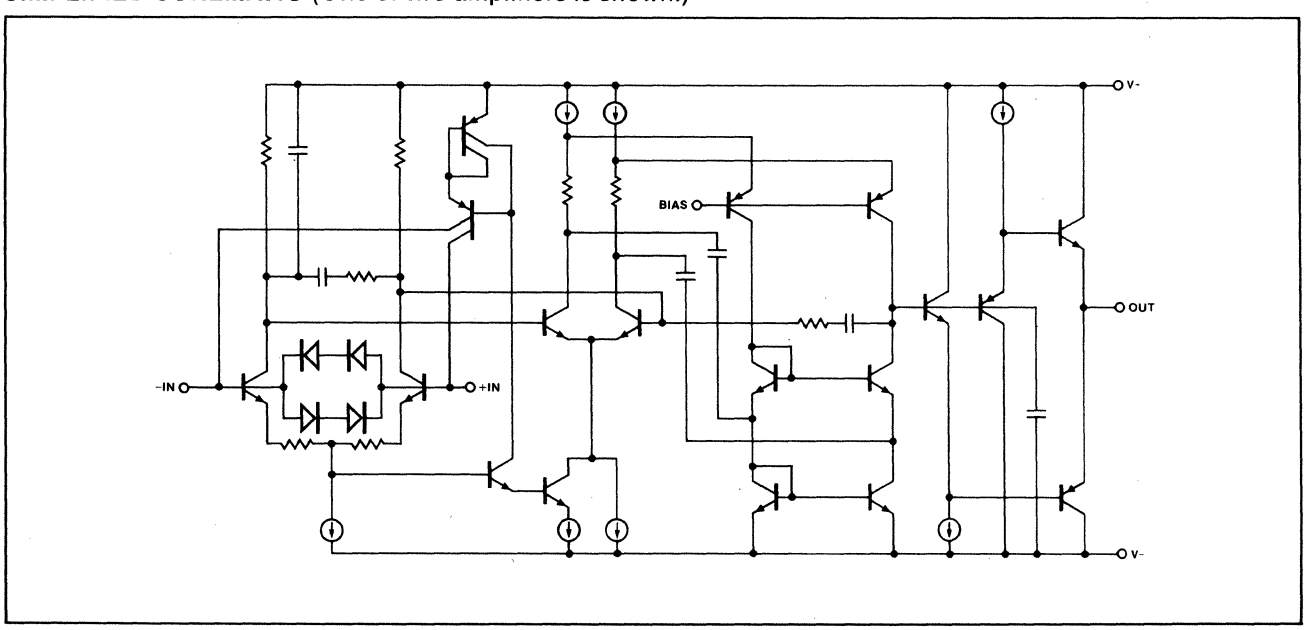


16-PIN SOL
(S-Suffix)



EPOXY MINI-DIP (P-Suffix)
8-PIN HERMETIC DIP
(Z-Suffix)

SIMPLIFIED SCHEMATIC (One of two amplifiers is shown.)



3/88, Rev. B

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OP-290

PRECISION LOW-VOLTAGE MICROPOWER DUAL OPERATIONAL AMPLIFIER

Precision Monolithics Inc.

FEATURES

- **Single/Dual Supply Operation** ..... **+1.6V to +36V**
  ..... **±0.8V to ±18V**
- **True Single-Supply Operation; Input and Output Voltage Ranges Include Ground**
- **Low Supply Current (per amplifier)** ..... **20μA Max**
- **High Output Drive** ..... **5mA Min**
- **Low Input Offset Voltage** ..... **200μV Max**
- **High Open-Loop Gain** ..... **700V/mV Min**
- **Outstanding PSRR** ..... **5.6μV/V Max**
- **Industry Standard 8-Pin Dual Pinout**

ORDERING INFORMATION†

T_A = 25°C V_{OS} MAX (μV)	PACKAGE			OPERATING TEMPERATURE RANGE
	CERDIP	PLASTIC	LCC	
200	OP290AZ*	—	OP290ARC*	MIL
200	OP290EZ	—	—	XIND
300	OP290FZ	—	—	XIND
500	—	OP290GP	—	XIND
500	—	OP290GS††	—	XIND

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic dip, and TO-can packages. For ordering information, see 1988 Data Book, Section 2.

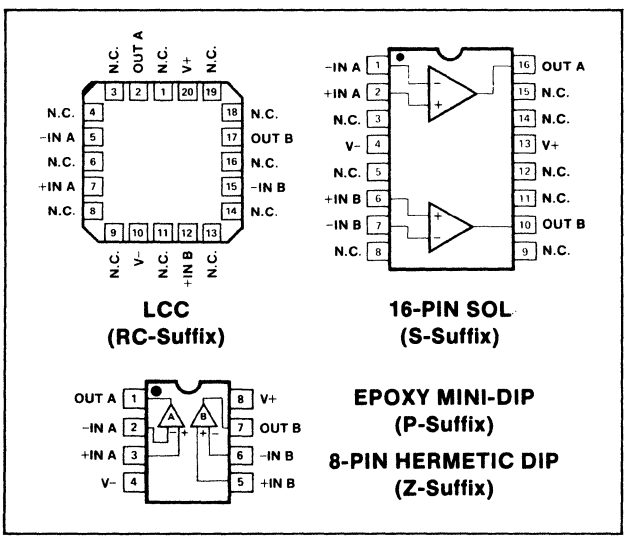
†† For availability and burn-in information on SO and PLCC packages, contact your local sales office.

GENERAL DESCRIPTION

The OP-290 is a high performance micropower dual op amp that operates from a single supply of +1.6V to +36V or from dual supplies of ±0.8V to ±18V. Input voltage range includes the negative rail allowing the OP-290 to accommodate input signals down to ground in single supply operation. The OP-290's output swing also includes ground when operating from a single supply, enabling "zero-in, zero-out" operation.

The OP-290 draws less than 20μA of quiescent supply current per amplifier, while able to deliver over 5mA of output current to a load. Input offset voltage is below 200μV eliminating the need for external nulling. Gain exceeds 700,000 and common-mode rejection is better than 100dB. The power supply rejection ratio of under 5.6μV/V minimizes offset voltage changes experienced in battery powered systems.

PIN CONNECTIONS



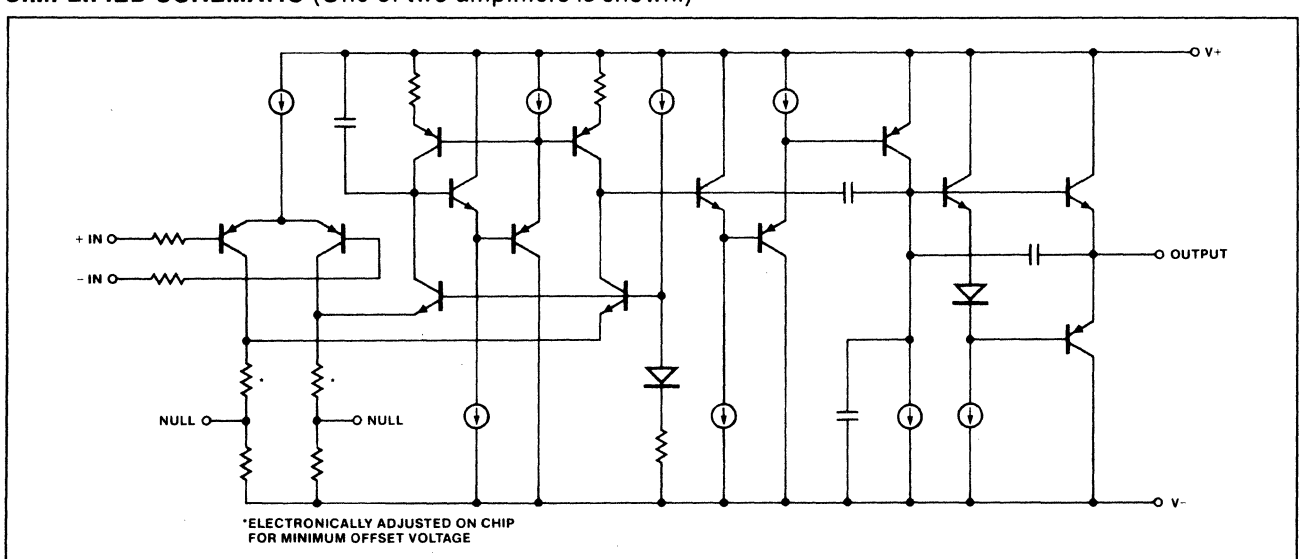
LCC
(RC-Suffix)

16-PIN SOL
(S-Suffix)

EPOXY MINI-DIP
(P-Suffix)

8-PIN HERMETIC DIP
(Z-Suffix)

SIMPLIFIED SCHEMATIC (One of two amplifiers is shown.)



6/88, Rev. B

Precision Monolithics

REF-43

+2.5V LOW-POWER PRECISION VOLTAGE REFERENCE

Precision Monolithics Inc.

FEATURES

- **+2.5 Volt Output** ..... **±0.05% Max**
- **Low Temperature Coefficient** ..... **10ppm/°C Max**
- **Excellent Regulation**
  - **Load Regulation** ..... **20ppm/mA Max**
  - **Line Regulation** ..... **2ppm/V Max**
- **Supply Current** ..... **450μA Max**
- **Temperature Voltage Output** ..... **+1.9mV/°C**
- **Operating Voltage Range** ..... **+4.5V to +40V**
- **Extended Industrial Temp Range** ..... **−40°C to +85°C**

ORDERING INFORMATION†

	PACKAGE				OPERATING TEMPERATURE
TCV_O	TO-99	CERDIP	PLASTIC	LCC	RANGE
10	REF43BJ*	REF43BZ*	—	REF43BRC/883*	MIL
10	REF43FJ	REF43FZ	—	—	XIND
25	REF43GJ	REF43GZ	REF43GP	—	XIND

*For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

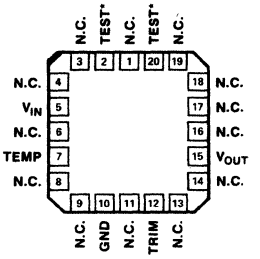
†Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic dip, and TO-can packages. For ordering information see 1988 Data Book, Section 2.

GENERAL DESCRIPTION

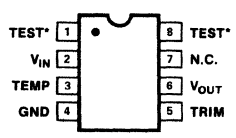
The REF-43 is a low-power precision reference providing a stable +2.5V output independent of variations in supply voltage, load conditions or ambient temperature. It is suitable as a reference level for 8, 10 and 12-bit data acquisition systems, or wherever a stable, known voltage is required.

Tight output tolerances and low thermal drift are assured by zener-zap trimming of both output voltage and its temperature coefficient. A unique curvature correction circuit reduces the thermal curvature which is characteristic of many previous bandgap references.

PIN CONNECTIONS

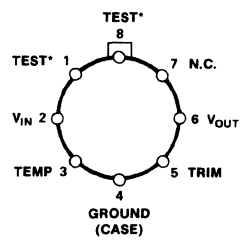


REF-43BRC/883
20-CONTACT LCC
(RC-Suffix)



8-PIN CERDIP
(Z-Suffix)

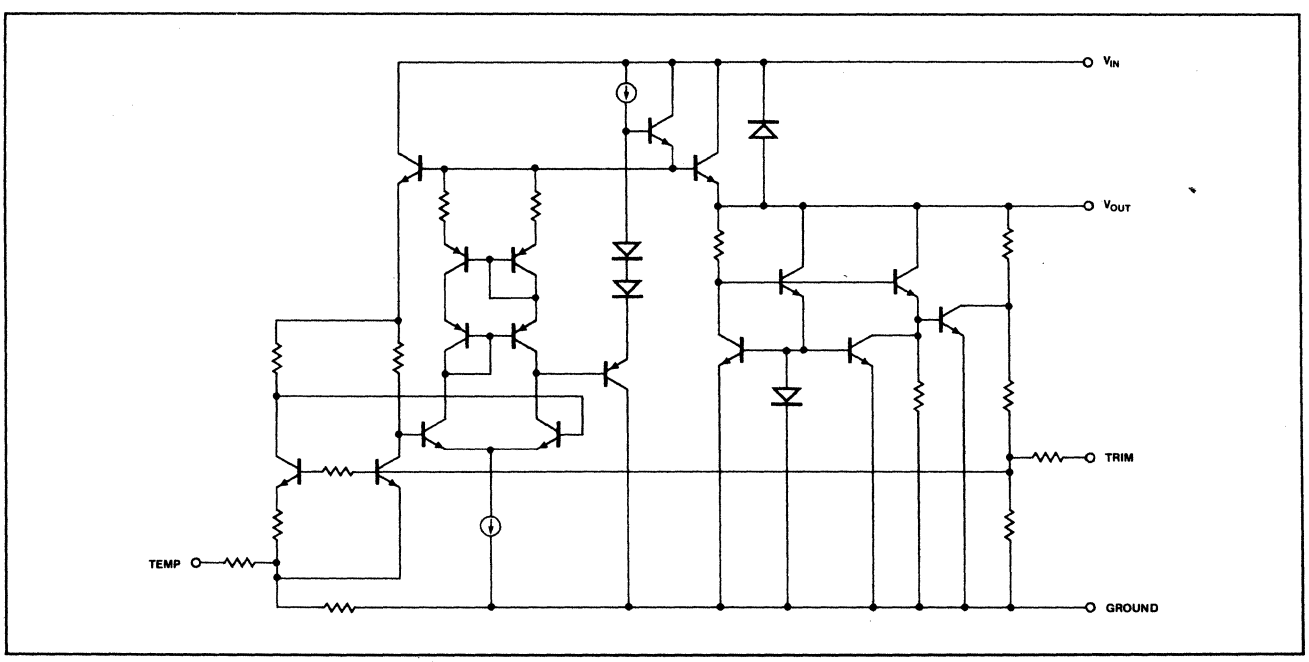
8-PIN PLASTIC DIP
(P-Suffix)



TO-99
(J-Suffix)

*RESERVED FOR FACTORY TESTING.
MAKE NO ELECTRICAL CONNECTION TO THESE PINS.

SIMPLIFIED SCHEMATIC



2/88, Rev. C

Precision Monolithics

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PMI

Audio Silicon Specialists

SSM-2016
DIFFERENTIAL AUDIO PREAMPLIFIER

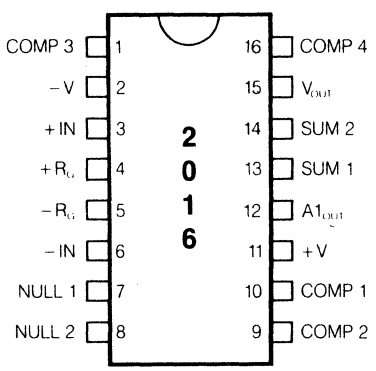
SSM Audio Products

DESCRIPTION

The SSM 2016 is an advanced differential device which can be used not only as a high gain microphone preamplifier, but also for signal summation and as a differential line receiver or low gain balanced input stage. Fabricated on a high voltage process, the 2016 can operate off split supplies from ±9 to ±36 volts. The output stage can source and sink a minimum of 40mA allowing a jack-field to be driven directly. The special package can dissipate 1.5 watts. The input referred noise of the device is 800pV/$\sqrt{Hz}$ yielding a noise figure of 1 dB when operated from a 150Ω source impedance.

FEATURES

- Ultra Low Voltage Noise (800pV/$\sqrt{Hz}$)
- Wide Bandwidth (500kHz @ G = 1000)
- High Slew Rate (10V/μS)
- Very Low Distortion (0.01% @ G = 1000)
- Full D.C. Coupling
- True Differential Inputs
- High Common Mode Rejection (100dB)
- 1/f Noise Corner < 5 Hz
- No Crossover Distortion
- Symmetric Slew Rates



PIN OUT

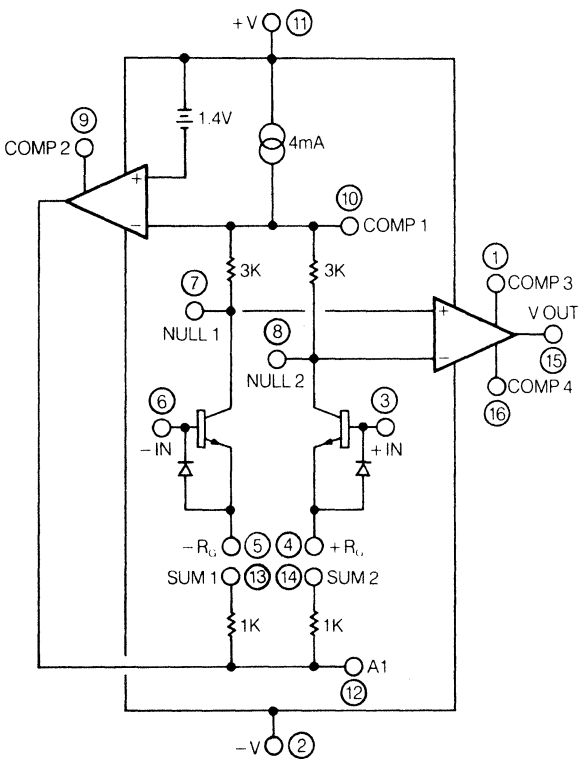


FIGURE 1. BLOCK DIAGRAM

Precision Monolithics

Revised February 1988

The SSM 2016 has been granted mask work protection under the Semiconductor Chip Protection Act of 1983.

PMI

Audio Silicon Specialists™

SSM-2044

4-POLE VOLTAGE CONTROLLED FILTER

SSM Audio Products

DESCRIPTION

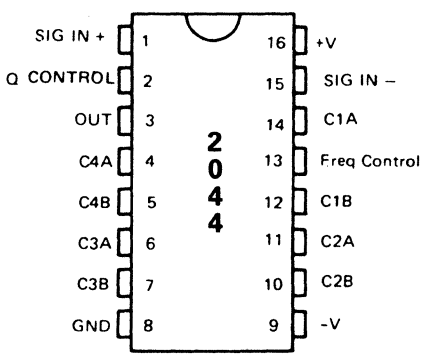
The SSM2044 is a low cost 4-pole voltage controlled filter whose design has been optimized for use as an electronic music lowpass filter. On-chip voltage control of resonance allows direct and easy interfacing with programmers and controllers. A novel filtering technique* provides extended control range, low noise and high control rejection for "pop"-free performance. The filter can also be used as a low distortion sinewave oscillator. No external ladder network is required making the device a real cost and space saver in polyphonic applications.

FEATURES

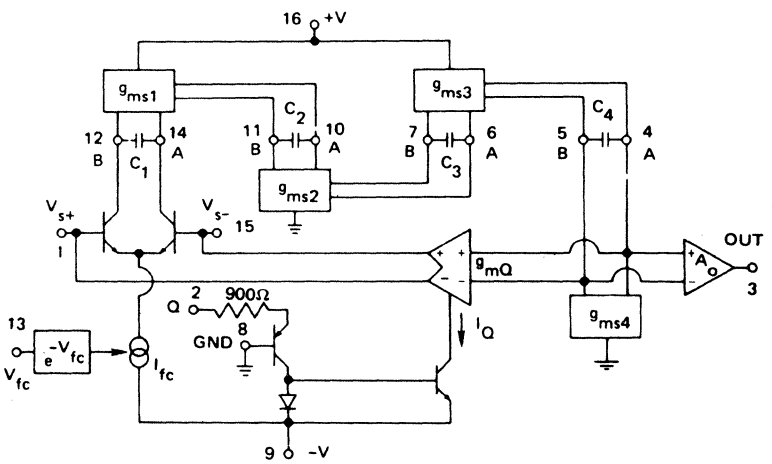
- Low Cost
- High Control Rejection (36db typical for 1000 to 1 sweep)
- ± 18V to ±5V Supplies
- Minimum External Parts Count
- Stable Resonance Over Frequency Sweep
- No Op Amp Required Between Output and VCA
- 90db Dynamic Range
- 10,000 to 1 Minimum Sweep Range
- On-Chip Resonance Control
- Differential Signal Inputs

*U.S. PATENT # 4, 404, 529

Precision Monolithics



Pin Out (Top View)



Functional Block Diagram

Protected under U. S. Patent #4,404,529.

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SSM-2120/2122

DYNAMIC RANGE PROCESSOR/DUAL VCA

SSM Audio Products

DESCRIPTION

The SSM 2120 is a state of the art dynamic range processor integrated circuit designed specifically for use in professional audio systems. The chip, offered in a 22 pin 'skinnydip' package, has two fully independent class A VCA's that exhibit extremely low distortion and offer a 100dB dynamic range. Each VCA has two complementary antilog (dB/volt) control ports to simplify system design. Also included on chip are two independent control side chain circuits, each of which consist of a full wave rectifier, a logging circuit, and a high impedance amplifier. The log/antilog nature of the control paths make possible precisely defined compression/expansion ratios over a 100dB dynamic range.

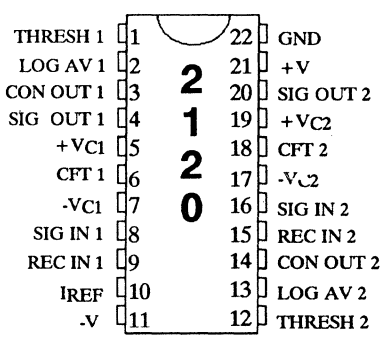
The SSM 2122 is the same die offered in a 16 pin package as a dual VCA without the level detection circuitry accessible.

FEATURES

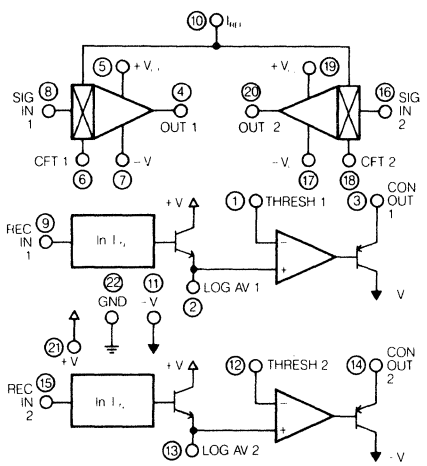
- 0.01% THD @ +10dBV In/Out
- 100dB VCA Dynamic Range
- Low VCA Control Feedthrough
- 100dB Level Detection Range
- Log/Antilog Control Paths
- Low External Component Count

APPLICATIONS

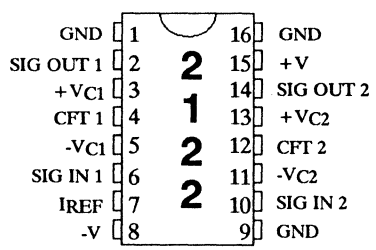
- Compressors
- Expanders
- Limiters
- Dual VCA
- AGC Circuits
- Voltage Controlled Filters
- Noise Reduction Systems
- Stereo Noise Gate



2120 PIN OUT (TOP VIEW)



BLOCK DIAGRAM (2120)



2122 PIN OUT (TOP VIEW)

Revised August 1988

Protected under U. S. Patents #4,471,320 and #4,560,947. Other Patent Pending.

The SSM 2120/2122 has been granted mask work protection under the Semiconductor Chip Protection Act of 1983.

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THE PMI COMMITMENT

PMI is committed to building long-term customer relationships resulting in mutual growth. To be a valued supplier we must provide a useful product, delivered on time, which meets all quality requirements, and is priced to give value to the customer.

To excel in our marketplace, we must always innovate processes, designs, and measurement techniques to provide products of precision and value. To do this, we will provide our people with the necessary resources and tools to do their jobs.

Our Productivity – Dependability – Quality process is a permanent structure for improvement in every area of the organization. We measure our performance, set goals for improvement, implement change, measure results, celebrate success, and set tougher goals. This is an unending process aimed at flawless performance and improving profitability.

Our success depends on the dedication, innovation, and basic productivity of our people. Our culture is one of participation and teamwork. Our approach to each other is firm, fair, and friendly. By these methods we will achieve a leadership position in Quality, Service, and Technology.

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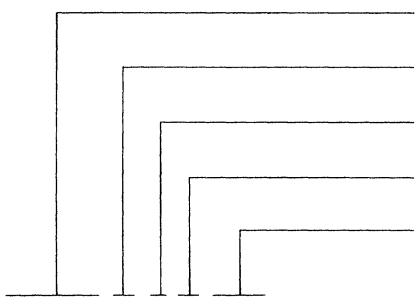
Ordering Information

Packaged Products Part Numbering System



Device Type and Model Number

Burn-In Option

Electrical Grade

Package Suffix

MIL-STD-883, Class B, Revision C Option
PMI -55°C to +125°C devices are available with MIL-STD-883, Class B, Revision C screening as standard products. To order an 883 part, simply add the designation /883 to the part number. For example, the DAC-08AQ, screened to the 883 requirements would be ordered as a DAC-08AQ/883. Contact factory for 883 device specifications.

Package Type

H	= 6-lead TO-78 Can	**S**	= Small Outline Package
J	= 8-lead TO-99 Can	**T**	= 28-lead Ceramic DIP
K	= 10-lead TO-100 Can	**TC**	= 28-position LCC
O	= Not used	**U**	= Not used
P	= Epoxy DIP	**V**	= 24-lead Ceramic DIP
PC	= Plastic Leaded Chip Carrier	**X**	= 18-lead Ceramic DIP
Q	= 16-lead Ceramic DIP	**Y**	= 14-lead Ceramic DIP
R	= 20-lead Ceramic DIP	**Z**	= 8-lead Ceramic DIP
RC	= 20-position LCC		

Select electrical grade from data sheet.

PMI offers all 0°/70°C, –25°/+85°C and –40°/+85°C devices with burn-in. Parts with this option are specified with the letters BI added between the model number and the electrical grade. For example, to order DAC-08EQ with burn-in, the part number is DAC-08BIEQ.

Device Type
Select model number from product listings.

FOR LOCAL STOCK:

PMI Stocking Distributors

Allied Electronics
Anthem Electronics
Bell Industries
Future Electronics
Gerber Electronics
Hall-Mark Electronics
Intek
Newark
Nu-horizons
Pioneer
Semi-Dice

FOR ASSISTANCE, CALL: 1-800-JIT-CMOS

Precision Monolithics Inc. A Bourns Company
HEADQUARTERS:
1500 Space Park Drive
P.O. Box 58020
Santa Clara, CA 95052-8020 USA
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PMI

Precision Monolithics Inc.

A Bourns Company

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Domestic Orders ONLY,
FAX 408-727-1853

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TLX 171189
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TLX 868 722
FAX 042-31 90 17

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FAX 81-32 60 71 00

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TLX 82953 BAPHK HX
FAX 852-56 64 341

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FAX 408-942-0174

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PMI Sales Office
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17871 Santiago Blvd.
Villa Park, CA 92667-4132
TEL (714) 637-9602
FAX 714-974-1589

California-Los Angeles
PMI Sales Office
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18531 Rosco Blvd.
Northridge, CA 91324-4641
TEL (818) 886-6881
FAX 818-886-5015

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TLX 372-7038
FAX 312-250-0925

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FAX 214-783-1219

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FAX 508-794-0970

Pennsylvania-Philadelphia
PMI Sales Office
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130 Buck Rd.
Holland, PA 18966-1743
TEL (215) 953-1070
FAX 215-953-1075

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PMI CMOS Data Converter Cross Reference Guide

ANALOG DEVICES	PRECISION MONOLITHICS	
AD7224	PM7224HP	(Available 3rd Qtr. 1987)
AD7225	DAC8408HP	(Functional replacement with data readback)
AD7226BCHIPS	PM7226GBC	(DICE)
AD7226BQ	PM7226FR	
AD7226KN	PM7226HP	
AD7226KP	PM7226HPC	(PLCC Package available 3rd Qtr. 1987)
AD7226TQ	PM7226BR	
AD7226TQ/883	PM7226BR/883	
AD7226TE/883	PM7226BRC/883	(LCC Package available 3rd Qtr. 1987)
AD7520JD, KD	PM7533FQ	(Improved exact replacements)
AD7520JN, KN	PM7533HP	
AD7520LD	PM7533EQ	
AD7520LN	PM7533GP	
AD7520SD, TD	PM7533BQ	
AD7520SD/, TD/883	PM7533BQ/883	
AD7520UD	PM7533AQ	
AD7520UD/883	PM7533AQ/883	
AD7521JD, KD, LD	PM7541FX	(Improved exact replacements)
AD7521JN, KN, LN	PM7541HP	
AD7521SD, TD, UD	PM7541BX	
AD7521SD/, TD/, UD/883	PM7541BX/883	
AD7523JN, KN	PM7524HP	(Exact replacement when N/C pins 12 & 13 tied to GND)
AD7523LN	PM7524GP	
AD7524ACHIPS	PM7524GBC	(DICE)
AD7524AD, AQ, BD, BQ	PM7524FQ	
AD7524CD, CQ	PM7524EQ	
AD7524JN, KN	PM7524HP	
AD7524LN	PM7524GP	
AD7524JP, KP	PM7524HPC	(PLCC package available 3rd Qtr. 1987)
AD7524SD, TD, TQ	PM7524BQ	
AD7524UD, UQ	PM7524AQ	
AD7524SD/, TD/883	PM7524BQ/883	
AD7524SQ/, TQ/883	PM7524BQ/883	
AD7524UD/883	PM7524AQ/883	
AD7524UQ/883	PM7524AQ/883	
AD7528ACHIPS	PM7528GBC	(DICE)
AD7528AQ, BQ	PM7528FR	
AD7528CQ	PM7528ER	
AD7528JN, KN	PM7528HP	
AD7528JP, KP	PM7528HPC	(PLCC package available 3rd Qtr. 1987)
AD7528LN	PM7528GP	
AD7528SE/, TE/883	PM7528BRC/883	(LCC package available 3rd Qtr. 1987)
AD7528SQ, TQ	PM7528BR	
AD7528UQ	PM7528AR	
AD7528SQ/, TQ/883	PM7528BR/883	
AD7528UQ/883	PM7528AR/883	
AD7530JD, KD	PM7533FQ	(Improved exact replacements)
AD7530JN, KN	PM7533HP	
AD7530LD	PM7533EQ	
AD7530LN	PM7533GP	
AD7531JD, KD	PM7541FX	(Improved exact replacements)
AD7531LD	PM7541EX	
AD7531JN, KN	PM7541HP	
AD7531LN	PM7541GP	
AD7533AQ, BQ	PM7533FQ	
AD7533CQ	PM7533EQ	
AD7533JN, KN	PM7533HP	
AD7533LN	PM7533GP	
AD7533SQ, TQ	PM7533BQ	
AD7533SQ/, TQ/883	PM7533BQ/883	
AD7533UQ	PM7533AQ	
AD7533UQ/883	PM7533AQ/883	

ANALOG DEVICES	PRECISION MONOLITHICS	
AD7537	DAC8248	(Improved functional replacement. Available 4th Qtr. 1987)
AD7541AACHIPS	PM7541AGBC	(DICE)
AD7541AAQ	PM7541AFX	
AD7541ABQ	PM7541AEX	
AD7541AJN	PM7541AHP	
AD7541AKN	PM7541AGP	
AD7541ASD	PM7541ABX	
AD7541ASD/883	PM7541ABX/883	
AD7541ATD	PM7541AAX	
AD7541ATD/883	PM7541AAX/883	
AD7541AD	PM7541FX	
AD7541BD	PM7541EX	
AD7541JN	PM7541HP	
AD7541KN	PM7541GP	
AD7541SD	PM7541BX	
AD7541SD/883	PM7541BX/883	
AD7541TD	PM7541AX	
AD7541TD/883	PM7541AX/883	
AD7542	PM7542	(Available 4th Qtr. 1987)
AD7543	PM7543	(Available 4th Qtr. 1987)
AD7545ACHIPS	PM7545GBC	(DICE)
AD7545AQ, BQ, CQ	PM7545FR	
AD7545GCQ	PM7545ER	
AD7545GLN	PM7545GP	
AD7545GUD, GUQ	PM7545AR	
AD7545GUD/, GUQ/883	PM7545AR/883	
AD7545JN, KN, LN	PM7545HP	
AD7545JP, KP, LP	PM7545HPC	(PLCC package available 3rd Qtr. 1987)
AD7545SD, SQ	PM7545BR	
AD7545SD/, SQ/883	PM7545BR/883	
AD7545TD, TQ	PM7545BR	
AD7545TD/, TQ/883	PM7545BR/883	
AD7545UD, UQ	PM7545BR	
AD7545UD/, UQ/883	PM7545BR/883	
AD7545SE/, TE/, UE/883	PM7545BRC/883	(LCC package available 3rd Qtr. 1987)
AD7547	DAC8212HP	(Improved functional replacement)
AD7548AQ	PM7548FR	
AD7548BQ	PM7548ER	
AD7548JN	PM7548HP	
AD7548KN	PM7548GP	
AD7548SD	PM7548BR	
AD7548SD/883	PM7548BR/883	
AD7548TD	PM7548AR	
AD7548TD/883	PM7548AR/883	

MICROPOWER SYSTEMS	PRECISION MONOLITHICS
MP7623AD	PM7541AFX
MP7623BD	PM7541AEX
MP7623JN	PM7541AHP
MP7623KN	PM7541AGP
MP7623SD	PM7541ABX
MP7623TD	PM7541AAX
MP7628AD	DAC8408FT
MP7628BD	DAC8408ET
MP7628JN	DAC8408HP
MP7628KN	DAC8408GP
MP7628SD	DAC8408BT
MP7628TD	DAC8408AT
MP7645AD	PM7645FR
MP7645BD, CD	PM7645ER
MP7645JN	PM7645HP
MP7645KN, LN	PM7645GP
MP7645SD	PM7645BR
MP7645TD, UD	PM7645AR

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Q2334 DUAL DIRECT DIGITAL SYNTHESIZER

Qual-Comm

FEATURES

- Two Complete Direct Digital Synthesizer Functions On-chip
- Processor Interface for Control of Phase and Frequency
- Synchronous PSK and FSK Modulation Inputs
- Fast Sampling Rate: 2-30MHz
- Frequency Resolution: <0.01Hz
- Amplitude Quantization SNR: 72dB
- Phase Truncation Spurs <76dB
- Double Buffered Registers Allow Synchronous Frequency Change
- Can be Paralleled for Higher Frequencies
- Low Price: $98 (100's)

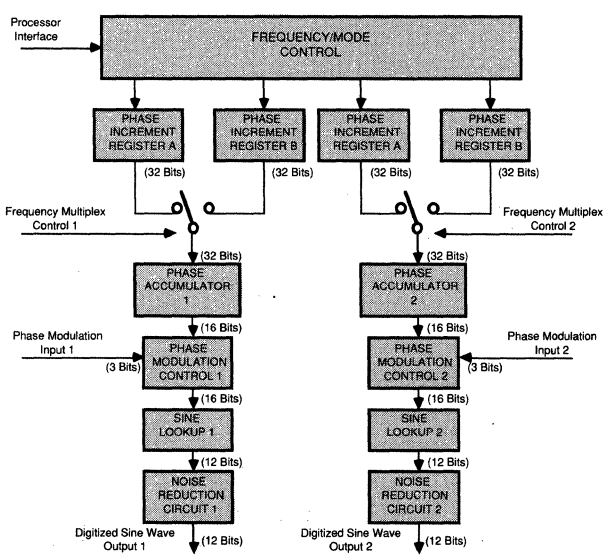
APPLICATIONS

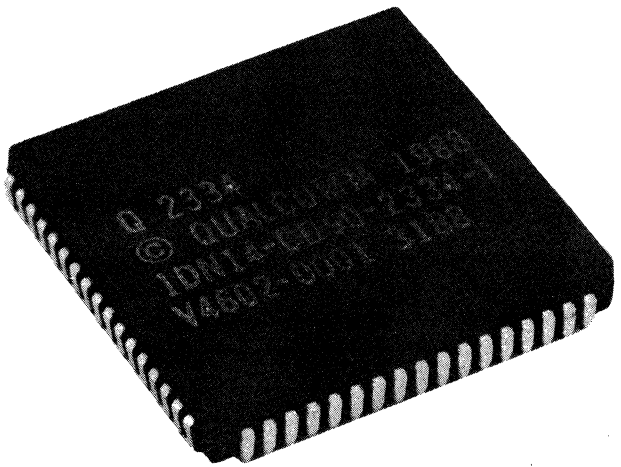
- High Resolution Frequency Synthesis
- Frequency/Phase Modulators
- Quadrature Oscillators

SPECIFICATIONS

- Power Requirements: <160 mA @ 5 VDC
- Process: 1.5 micron CMOS
- Packaging: 68-PLCC
- Operating Temp. Range: -40C to +85C
- MIL-STD-883 Class B Processing Available.

BLOCK DIAGRAM





DESCRIPTION

The *QUALCOMM* Q2334 Dual Direct Digital Synthesizer (DDS) generates high resolution digitized sine wave signals using phase accumulation techniques combined with on-chip sine lookup. The Q2334 contains two independent DDS functions controlled from a single microprocessor interface. This interface provides control for the phase and frequency of the generated sine waves as well as the operating mode of the device. Synchronous inputs are also provided to allow phase and frequency modulation.

The Q2334 provides greater than 76 dB rejection of phase truncation spurs and 72 dB amplitude quantization signal-to-noise ratio. It is ideally suited for applications requiring high resolution sine wave generation, fast phase and frequency switching, and excellent phase/frequency stability.

The two independent on-chip DDS functions provide an efficient technique for implementation of full-duplex systems, quadrature oscillators, and spread spectrum systems. In addition, multiple DDS functions can be paralleled for operation with higher clock rates.

QUALCOMM, Inc.
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Q1401 VITERBI DECODER

FEATURES

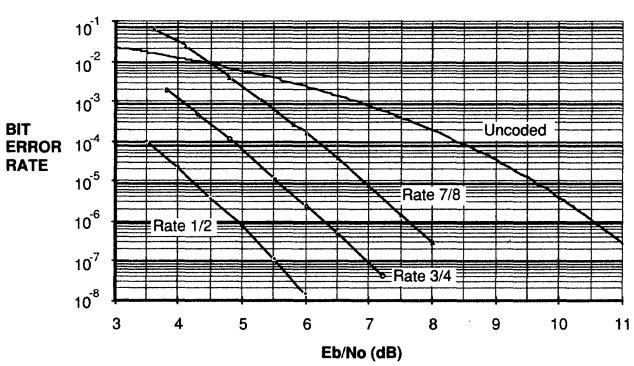
- Stand-alone Full-Duplex Rate 1/2 Encoder/Decoder
- Maximum Data Rate: 17 Mbps
- Implements Optimal K=7 Code
- Hard or Soft Decision (8-level) Decoder Inputs
- Simple Interfacing
- Coding Gain of 5.2 dB at 10^{-5} BER
- Able to Operate at Higher Code Rates using Punctured Coding Techniques
- On-chip Error Monitoring
- Automatic Synchronization to QPSK, BPSK, and OQPSK Modems
- Differential Encoder/Decoder
- CCITT V.35 Scrambler/Descrambler

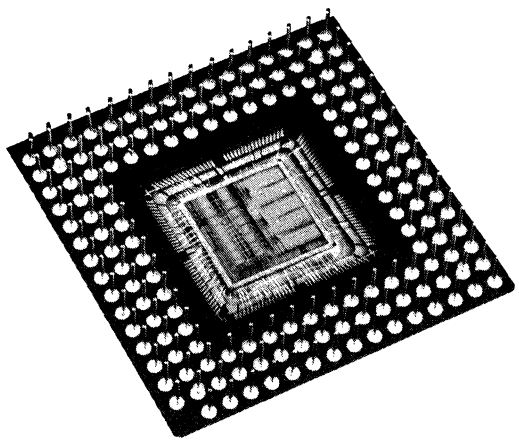
SPECIFICATIONS

- Generating Functions: W0=171 (octal) W1=133 (octal)
- Process: 1.5 micron CMOS
- Power Requirements: <1 mA quiescent. <250 mA at 12 Mbps @ 5V
- Packaging: 155 CPGA
- Operating Temp. Range: 0C to +70C (commercial: Q1401C) -55C to +125C (MIL-STD-883B: Q1401M)

DECODER PERFORMANCE

(With Ideal Soft-Decision PSK Modem, AWGN, Punctured Coding for Rates 3/4 and 7/8)





DESCRIPTION

The *QUALCOMM* Q1401 Viterbi Decoder implements the *de facto* industry and government standard rate 1/2 convolutional code of constraint length 7. The Viterbi Decoder operates with hard-decision or 8-level quantized soft decision symbol inputs, with capability to automatically synchronize to BPSK, QPSK, and OQPSK modem phase ambiguities. Symbol erasure inputs are provided for implementation of higher rate decoders using punctured-coding techniques.

Symbol inputs may be in serial or parallel formats at information rates up to 17 Mbps over full commercial operating conditions (up to 12 Mbps over full military conditions). Two built-in error monitoring techniques provide effective means for determining loss-of-sync, high channel error rate, and fault conditions.

Differential encoding and decoding circuits are included on-chip as well as CCITT V.35 scrambling and descrambling circuits. Combining these features with an on-chip rate 1/2 convolutional encoder, the Q1401 device is a powerful full-duplex Forward Error Correction system on a single VLSI circuit.

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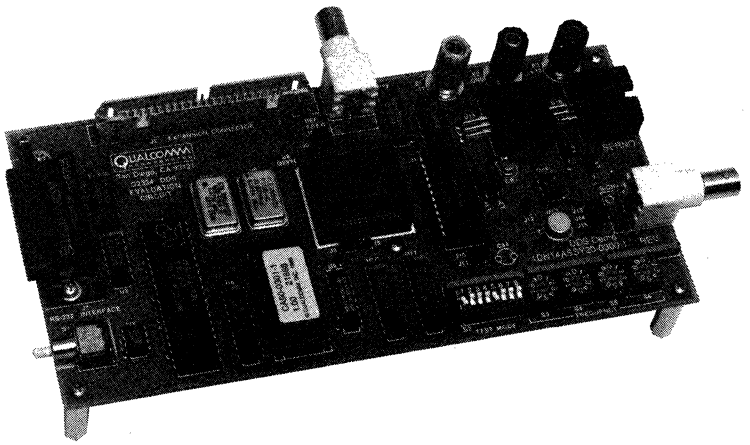
Q2334 DDS EVALUATION KIT



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FEATURES

- A Complete Direct Digital Synthesizer (DDS) System on a single 4x8 inch Circuit Card
- Provides a Rapid, Powerful Approach to Evaluating and Prototyping DDS Systems
- Based on QUALCOMM Q2334 Single-chip Direct Digital Synthesizer
- Includes Pre-programmed microcontroller, High-Speed 12-bit DAC, 20 MHz Frequency Reference, and Low Pass Filter
- DDS Operation is Controlled using on-board Switches or via standard RS-232 Terminal
- Selectable Output Formats: Direct from DAC, Low-pass Filtered Sine Wave Output, or TTL-level Square Wave
- Kit Comes Complete with Full Documentation including User's Guide, Schematics, and Software Listings

SPECIFICATIONS

- Built-in DDS Modes: Basic Oscillator, PSK Modulation, FSK Modulation, Frequency Sweep, Frequency Hopping
- Power Requirements: +12 VDC @ 300 mA, -12 VDC @ 300 mA
- Analog Output: 50 Ohm, DC Coupled
- Digital Controls: ALS TTL Level Compatible
- External Clock Input: 1 Vp-p, 50 Ohm Terminated
- Order Part Number: Q0300

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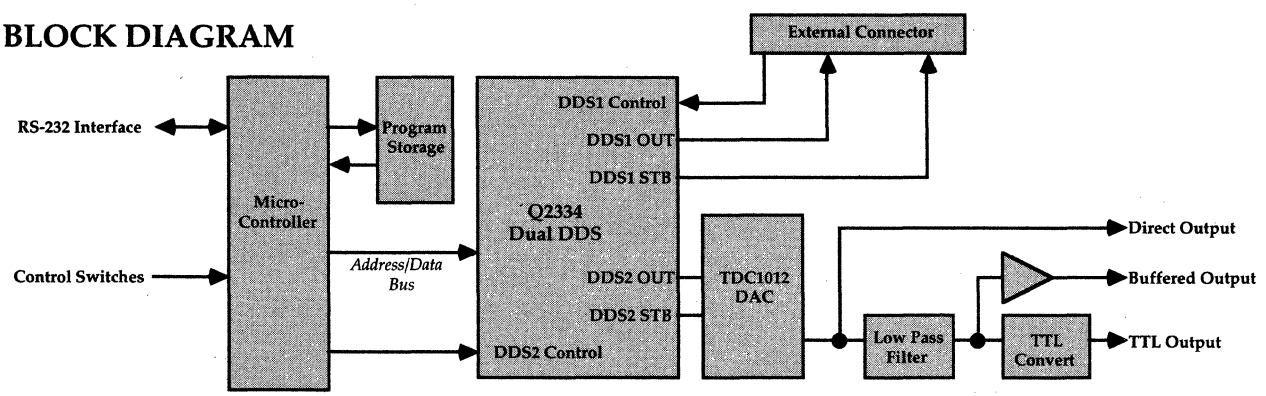
BLOCK DIAGRAM



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COMPANY PROFILE AND CAPABILITIES

QUALCOMM, Inc. is a rapidly-growing San Diego-based systems company specializing in the design, analysis, and manufacture of advanced communications systems and components for commercial and government customers. The company also provides communications message service through its OmniTRACS™ 2-way mobile satellite and position locating service. Two of the founders of ***QUALCOMM,*** Dr. Irwin M. Jacobs and Dr. Andrew J. Viterbi, are internationally recognized leaders in the communications community. ***QUALCOMM*** has production facilities for both military qualified and commercial products as well as fully equipped digital and analog/RF laboratories. ***QUALCOMM*** also maintains a special access facility.

QUALCOMM is dedicated to the *elegant solution* - the solution that provides the most cost effective, reliable answer to today's communication problems. Now, more than ever before, the existing tools of our trade - microprocessors and VLSI, along with advanced information theory and digital signal processing technologies - offer exciting new approaches to elegance and innovation in synthesizing practical solutions to real-world problems. This is characterized by the range of products offered by ***QUALCOMM*** such as:

- **VLSI Products**
  - * Forward Error Correction
  - * Direct Digital Synthesis Products
- **Complete Communication Systems**
  - * Mobile Satellite Systems
  - * Ultra-Small Aperture Satellite Terminals
  - * Government Systems
- **Communication Subsystems**
  - * Satellite and Airborne Modems
  - * Forward Error Correction Systems
  - * Video Processing Equipment
- **Communications Services**
  - * OmniTRACS™ 2-Way Mobile Communication Service
  - * Fixed Service Ku-band Communications

QUALCOMM's staff is an experienced team that produces both theoretical innovation and working, high quality products and systems. This group of people has, for the most part, worked together for the last 15 years and is dedicated to building ***QUALCOMM*** into what its name implies — ***The Quality Communication Company*** of our time.

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Precision Op Amps

Input Offset Voltage Selection Table by Package Type (+25°C limits, in microvolts)

Part Type	Plastic Dip (N)	SOIC (M)	Leadless Ceramic Dip (D)	Metal Chip Carrier (L)	Can TO-99 (T)
RC4077	±10	±25	±10	±10	±10
RC4207*	±75		±75		
RC4227*	±75		±75		
OP-07	±75	±75	±25	±25	±25
OP-27	±25	±25	±25	±25	±25
OP-37	±25	±25	±25	±25	±25
OP-47	±25	±25	±25	±25	±25
OP-77	±25	±60	±25	±25	±25
LT1001	±25	±25	±15	±15	±15
LM108			±500	±500	±500
LH2108*			±500	±500	±500

* Dual

Audio and General Purpose Op Amps

Single Op Amps

Type	Description	Maximum Input Specifications @ 25°C: Offset Voltage (mV)	Offset Current (nA)	Bias Current (nA)	Typ[1] Unity Gain BW (MHz)	Typ. Slew Rate (V/μS)	Temp[2] Range	Available Packages: D	L	M	N	T
LM101A	General Purpose with Improved	2.0	10	75	1.0	0.5	M	X				X
LM301A	Input Characteristics	7.5	50	250	1.0	0.5	C				X	
RC741	General Purpose, Internal Comp	6.0	200	500	1.0	0.5	C	X			X	X
RC5534	High Performance, Low Noise	4.0	300	1500	10	13	C				X	
RM5534		2.0	200	800	10	13	M	X				X
RC5534A[3]		4.0	300	1500	10	13	C				X	
RM5534A[3]		2.0	200	800	10	13	M	X				X

1. Gain bandwidth product for 5534/A series and closed loop bandwidth for OP series.
2. Operating Temperature Range: M = -55°C to +125°C; C = 0°C to +70°C.
3. RM/RC5534A guarantees maximum input noise specification.

Dual Op Amps

Type	Description	Maximum Input Specifications @ 25°C: Offset Voltage (mV)	Offset Current (nA)	Bias Current (nA)	Typ[1] Unity Gain BW (MHz)	Typ. Slew Rate (V/μS)	Temp[2] Range	Available Packages: D	L	M	N	T
LH2101A	High Performance	2	10	75		10		X				
RC747	Dual 741	6	200	500	1	0.5	C				X	
RM747		5	200	500	1	0.5	M	X				X
RC4558	Wideband 741	6	200	500	3	1	C			X	X	
RM4558		5	200	500	3	1	M	X				X
RC4559	High Performance	6	100	250	4 (3)	2 (1,5)	C			X	X	
RM4559		5	100	250	4 (3)	2 (1,5)	M	X				X
RC5532	High Performance, Low Noise	4	150	800	10	8	C				X	
RM5532		2	100	400	10	8	M	X				X
RC5532A[3]		4	150	800	10	8	C				X	
RM5532A[3]		2	100	400	10	8	M	X				X

1. Gain bandwidth product for 5532A series.
2. Operating Temperature Range: M = -55°C to +125°C; C = 0°C to +70°C.
3. RM/RC5532A guarantees maximum input noise specification.

( ) Denotes guaranteed specifications.

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Audio and General Purpose Op Amps

Quad Op Amps

Type	Description	Maximum Input Specifications @ 25°C: Offset Voltage (mV)	Offset Current (nA)	Bias Current (nA)	Typ Unity Gain BW (MHz)	Typ. Slew Rate (V/μS)	Temp[1] Range	Available Packages: D	L	M	N	T
RM4741	741 General Purpose	3	30	200	3.5	1.6	M	X				
RC4741		5	50	300	3.5	1.6	C				X	
LM124	Single Supply	5	±30	150	1	—	M	X				
LM148	Low Power 741	5	±25	100	1	0.5	M	X				
LM324	Single Supply	7	±50	250	1	—	C				X	
LM348	Low Power 741	6	±50	200	1	0.5	C				X	
LM3900	Current Mode, Single Supply	—	—	200	2.5	±.5/-20	C				X	
RC3403A	Ground Sensing	6	50	500	1	1.2	C				X	
RC4136	741 General Purpose	6	200	500	3	1	C			X	X	
RM4136		4	150	400	3	1.5	M	X				
RC4156	High Performance	5	50	300	3.5 (2.8)	1.6 (1.3)	C			X	X	
RM4156		3	30	200	3.5 (2.8)	1.6 (1.3)	M	X				
RC4157	High Speed, Decompensated	5	50	300	19 (15)	8 (6.5)	C				X	
RM4157		3	30	200	19 (15)	8 (6.5)	M	X				

1. Operating Temperature Range: M = -55°C to +125°C; C = 0°C to +70°C.
( ) Denotes guaranteed specification.

Comparators

Type	Description	Maximum Input Specifications @ 25°C: Offset Voltage (mV)	Bias Current (nA)	Offset Current (nA)	Voltage Gain (V/mV Typ)	Max Sat. Voltage	Output Leakage Current (nA Typ)	Available Packages: D	L	M	N	T
LH2111	Dual Precision Voltage	3.0	10	100	200	1.5V	0.2	X				
LM111	Low Input Current	3.0	10	100	200	1.5V	0.2	X	X			X
LM139	Quad Single Supply	±5.0	100	±25	200	400 mV	0.1	X				
LM339	Quad Single Supply	±5.0	250	±50	200	400 mV	0.1			X	X	
LP165	Programmable	3.0	50	20	500	0.4	2	X			X	
RC4805	Precision High Speed	0.6	1800	20	15	0.40	—				X	
RM4805		0.6	1800	150	20	0.40	—	X				X
RM4805A		0.25	1200	80	20	0.40	—	X				X
RC4805E		0.25	1200	80	20	0.40	—				X	

Other Standard Linear Products From Raytheon

D/A Converters
- DAC08 — 8-Bit Current Output
- DAC10 — 10-Bit Current Output
- DAC4881 — 12-Bit Complete
- DAC4888 — 8-Bit Complete
- DAC8565 — 12-Bit with Reference

V/F Converters
- RC4151 — Basic 100 kHz
- RC4152 — Low-drift 100 kHz
- RC4153 — Precision 250 kHz

Voltage References
- REF-01 — 10V Output
- REF-02 — 5V Output

Voltage Regulators
- RC4190 — Low Power Switcher
- RC4191/92/93 — Low Power Switcher
- RC4194 — Dual Tracking Linear
- RC4195 — Dual Tracking Linear
- RC4292 — Negative Input
- RC4391 — Inverting Switcher

Ground Fault Interrupters
- LM1851 — Industry Alternate Source
- RC4143/4144 — Standard GFI
- RC4145 — Low Power GFI

Special Functions
- RC4200 — Analog Multiplier
- RC4444 — Cross-Point Array
- RC4447 — Pin-Diode Driver
- RM3182 — ARINC Bus Driver
- XR2207 — Voltage-Controlled Oscillator
- XR2211 — FSK Demodulator

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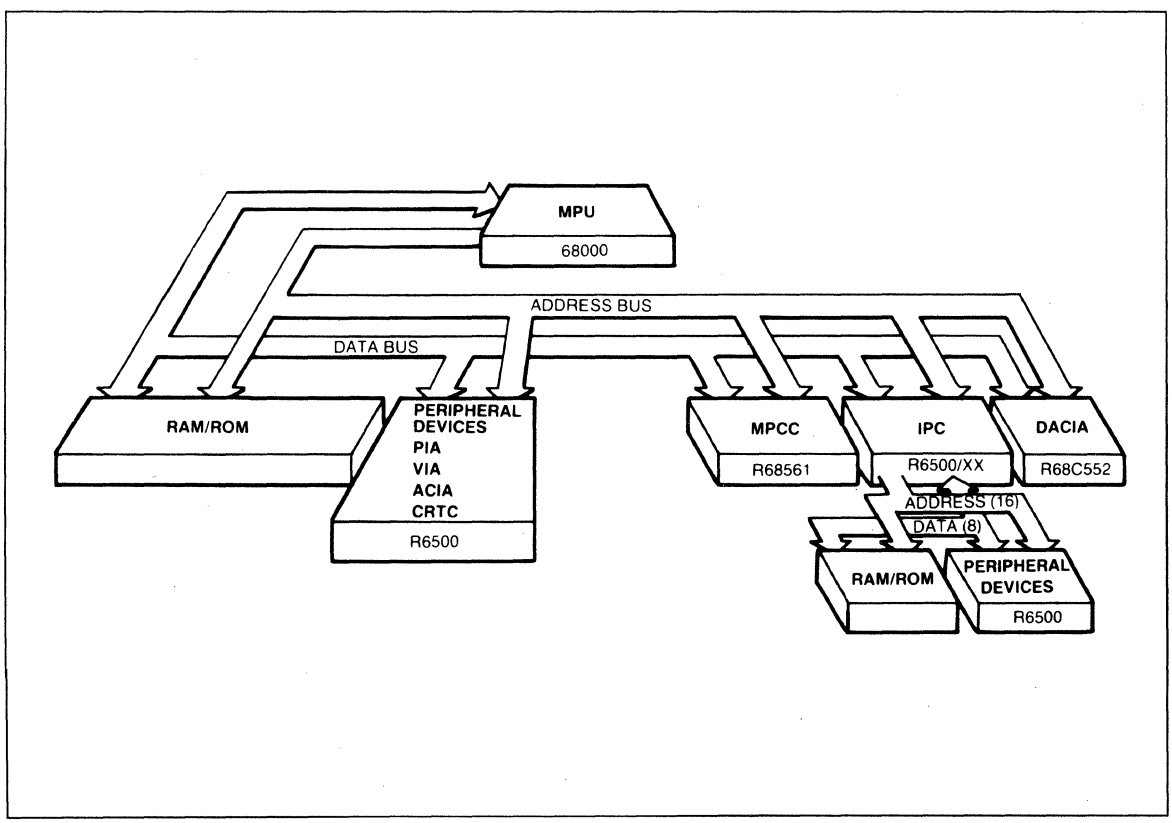
Raytheon Semiconductor

ROCKWELL INTERNATIONAL
SEMICONDUCTOR PRODUCTS DIVISION
Providing Solutions for Your System Requirements

Rockwell International designs and manufactures a family of VLSI products to serve your system requirements. As shown in the diagram below, compatible controller products are available for a wide range of 16-bit and 8-bit applications. Peripheral devices operate on either the 68000 or the 6500 microprocessor bus structure. Many of the peripheral devices are now being used on additional bus structures such as 8085, 80286 and Z80, just to name a few.

These products are produced in high volume at a modern state-of-the-art facility located in Newport Beach, California and are packaged in a newly constructed, fully automated manufacturing facility in Mexicali, Mexico. The class 10,000 clean room environment produces devices to the most stringent industry standards. Rockwell has the organization, systems and support to manufacture products to exisitng and future quality levels.

Rockwell is the first and only semiconductor company to offer a 5 year warranty. You can rely on customer satisfaction and service when choosing a Rockell semiconductor product.



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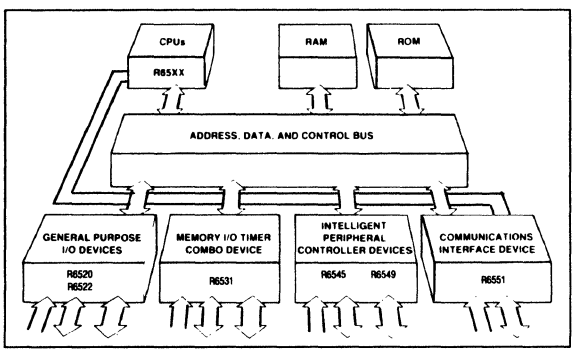
NMOS 8-bit Microprocessors and Peripherals Largest Selling 8-Bit Family

The NMOS R6500 microprocessor family has a wide range of CPUs and peripheral controllers plus versatile memory-I/O timer combinations. It is software compatible with the CMOS microprocessor and peripheral family, as well as, with the family of single-chip microcomputers. Fast instruction execution (1 μs and 2 μs) is available in 1 and 2 MHz versions, respectively.

The entire 8-bit R6500 family is upward compatible with 16-bit bus systems, software compatible with the Rockwell 8-bit microcomputers, and are the building blocks for a wide range of system applications.



NMOS R65XX Microprocessor Family

NMOS

8-Bit Processor

R6502: 8-Bit Microprocessor Unit (MPU) provides high performance (down to 1 μs instruction time) using memory efficient byte-level instructions.

8-Bit Peripherals—6500/6800 bus compatible

R6520: Peripheral Interface Adapter (PIA) interfaces two 8-bit bidirectional parallel data ports with four control lines and an interrupt request output on each port.

R6522: Versatile Interface Adapter (VIA) interfaces two 8-bit bidirectional parallel data ports, two 16-bit timers, and an 8-bit serial port.

R6531: ROM-RAM-I/0 Counter (RRIOC) combines 1K bytes read-only memory, 64 bytes random access memory, a 16-bit counter/latch, and an 8-bit serial channel.

R6545: CRT Controller (CRTC) controls a CRT raster scan video display at a character clock frequency of 2.5 MHz or 3.7 MHz using 19 registers to program display parameters such as number of rows, number of lines, sync positions and widths, row/column or straight binary addressing selection, and interface/non-interlaced scan selection.

R6549: Color Video Display Generator (CVDG) is a color graphics CRT display driver for any application requiring 256 x 210 pixels resolution and a 4096-color palette. Also, special features attractive to videotex and teletext (NAPLPS) applications.

R6551: Asynchronous Communications Adapter (ACIA) with on-board baud generator interfaces an asynchronous channel with 5-8 data bits; 1 or 2 stop bits; and odd, even or no parity; at 1 of 15 selectable rates (to 38,000 baud), or 1/16 external clock rate.

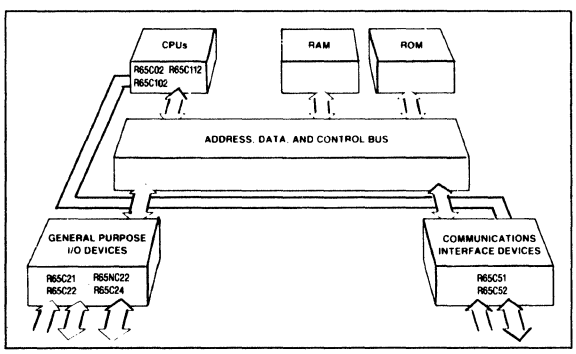
R68560/61: Multi Protocol Communications Controller (MPCC) interfaces to a single high speed serial data channel (up to 4 Mbps), supports popular synchronous or asynchronous formats, and performs protocol handling and checking. Eight and 16 bit host interfaces available.

CMOS 8-bit Microprocessors & Peripherals Fastest Executing — Low Power

There is no CMOS microprocessor family easier to implement than the R65CXX. It is a fast instruction-executing 8-bit family of devices. It's software compatible with a family of single-chip microcomputers and has three powerful CPUs and peripherals for parallel and serial I/O.

In the 8-bit range, nothing gives faster instruction execution (500 μs) with most parts available in 1, 2, 3 and 4 MHz versions.

Because of its inherent characteristics, advanced Rockwell CMOS provides low power consumption, high noise immunity and high speed operation. It's 2 MHz CPU dissipates only 40 mW (compared to 800 mW in NMOS) and requires only 10 μA standby current. Instruction memory requirements are 20% less due to added bit manipulation features.



CMOS R65CSS Microprocessor Family

8-Bit Processor and Peripherals

CMOS

8-Bit Processors – 6500/6800 bus compatible

R65C02/R65C102/R65C112: 8-Bit Microprocessor Units (MPUs) provide high performance (down to 55 ns instruction time) using memory efficient bit and byte-level instructions.

8-Bit Peripherals – 6500/6800 bus compatible

R65C21: Peripheral Interface Adapter (PIA) interfaces two 8-bit bidirectional parallel data ports with four control lines and an interrupt request output on each port.

R65C22: Versatile Interface Adapter (VIA) interfaces two 8-bit bidirectional parallel data ports plus two 16-bit timers and an 8-bit serial port.

R65C24: Peripheral Interface Adapter/Timer (PIAT) interfaces two 8-bit bidirectional parallel data ports and a 16-bit Counter/Timer.

R65C51: Asynchronous Communications Interface Adapter (ACIA) with on-board baud generators interfaces an asynchronous channel with 5-8 data bits; 1 or 2 stop bits; and odd, even or no parity; at 1 of 15 selectable rates (to 38,000 baud) or 1/16 external clock rate.

R65C52: Dual Asynchronous Communications Interface Adapter (DACIA) is a dual channel version of the R65C51 ACIA above.

R68C552: DACIA is a 68000 bus compatible version of the R65C52 DACIA above.

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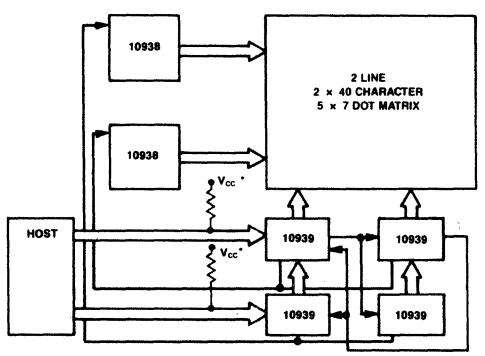
PMOS INTELLIGENT DISPLAY CONTROLLERS

The Rockwell Intelligent Display Controller family of products is designed to interface a host processor to various types of Vacuum Fluorescent Displays (VFD). In addition to providing the display drive signals, these products perform character decoding, grid timing, and display refresh functions. Included in the family are a series of single chip display controllers, a series of anode decoder/drivers, and a grid controller driver.

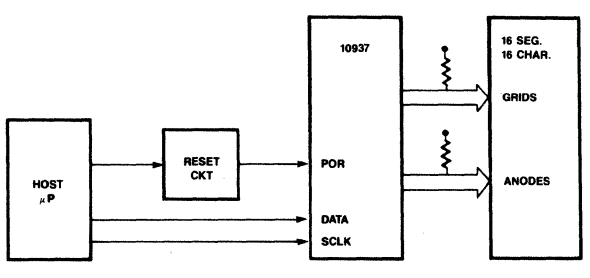
Typical applications for the intelligent display controller family include: automotive instrument clusters, interactive terminals, typewriters, telecommunications products, industrial automation applications, hand-held computers, and instrumentation systems.

By providing a simple interface, both with the host computer and the associated display, the intelligent controller family provides significant advantages over other approaches. The benefits of Rockwell's intelligent display controller approach are: reduction of operation time rquired of the host computer, less display overhead electronics, simplified system design, less board real estate for the display control function, reduced power and cooling, lower overall installed cost and lower maintenance costs.

Features	Grid Drivers	Anode Drivers				Comparison of Single Chip Display Controller Features		
	10939	10938	10941	10942	10943	10937	10951	10957
PLA Size		128	128	128	128	64	64	64
Font		5 × 7 Dot Matrix Alphanumeric	16 Segment Alphanumeric and Bargraph	Top Half 5 × 12 Dot Matrix-Alphanumeric	Bottom Half 5 × 12 Dot Matrix Alphanumeric	16 Segment Alphanumeric Decimal Point Comma	7 Segment Numeric Decimal Point Comma 16 Segment Bargraph	16 Segment Alphanumeric Decimal Point Comma
Grid Dirvers								
Type						Open-Drain	Open-Drain	Open-Drain
Number						16	16	16
Current Limit(mA)						20	20	20
Anode Dirvers	Push-Pull	Push-Pull	Push-Pull	Push-Pull	Push-Pull	Open-Drain	Open-Drain	Open-Drain
Type	20	35	18	23	23	18	18	18
Number	10	2	2	2	2	10	10	10
Current Limit(mA)								
Host Interface	Serial or Parallel	Via 10939	Via 10939	Via 10939	Via 10939	Serial	Serial	Serial
Control Options	Digit Time Duty Cycle Character Count Buffer Pointer Blank Mode Inverse Mode Start Refresh					Duty Cycle Character Count Buffer Pointer Test Mode	Duty Cycle Character Count Buffer Pointer Test Mode	Duty Cycle Character Count Buffer Pointer Test Mode
Power Supply Limits								
VDD(V)	−20 ± 2.0	−20 ± 2.0	−20 ± 2.0	−20 ± 2.0	−20 ± 2.0	−15 ± 1.5	−15 ± 1.5	−15 ± 1.5
VGG(V)	to −50	to −50	to −50	to −50	to −50	to −50	to −50	to −50
Package	40 Pin Dip	40 Pin Dip	24 Pin Dip	28 Pin Dip	28 Pin Dip	40 Pin Dip	40 Pin Dip	40 Pin Dip
Other	Cursor Driver Cascadable		Decimal Point Driver Comma Driver			2 Decimal and Tail Commands	2 Decimal and Tail Commands	4 Decimal and Tail Commands



Driving Two Line Display



Single Chip Display Controller Application

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CMOS and NMOS 8-Bit Microcomputers
Highest Industry Performers

The R6500 single-chip CMOS and NMOS microcomputers provide high-speed and low-power CMOS while being completely software compatible with the 8-bit multi-chip family. They let you move easily from a multi-chip to a single-chip solution when the application warrants. They also function as intelligent peripheral controllers. The R65C10, a CMOS version of the R6500/1, combines the low power of CMOS with advanced pipelining architecture to provide an efficient high-speed single-chip system solution.

We also offer a set of extremely versatile FORTH language devices. The R65F11 and R65F12 contain both the high level language and operating system that can put your product on the market in the shortest possible time.

Feature/Models	R6500/1	R6500/11	R6500/12	R6500/13	R6500/15	R65C10
• INSTRUCTION SPEED	1000ns	1000ns	1000ns	1000ns	1000ns	500ns
• ROM (x8)	2K	3K	3K	256	4K	2K
• RAM (x8)	64	192	192	192	192	64
• I/O LINES	32	32	56	32	32	32
• SERIAL COMM.	—	USART	USART	USART	USART	—
• 16-BIT COUNTERS	ONE	TWO	TWO	TWO	TWO	ONE
• EXPANSION BUS	—	16K	16K	65K	16K	—
• INTERRUPTS						
— EXTERNAL	5	6	6	6	6	5
— INTERNAL	1	4	4	4	4	1
• OPERATING POWER (mW)	750	800	800	800	800	40
• STANDBY (mW)	35*	12*	12*	12*	12*	12
• PACKAGE	40 DIP 44 PLCC	40 DIP 44 PLCC	QUIP 68 PLCC	QUIP 68 PLCC	40 DIP 44 PLCC	40 DIP 44 PLCC

* STANDBY RAM

Rockwell Microcomputers

Feature/Models	R6501Q	R6511Q	R6518
• INSTRUCTION SPEED	1000ns	1000ns	1000ns
• RAM (x8)	192	192	192
• I/O LINES	32	32	16
• SERIAL COMM.	USART	USART	USART
• 16-BIT COUNTERS	TWO	TWO	TWO
• EXTERNAL MEMORY	64K	64K	16K
• INTERRUPTS			
— EXTERNAL	6	6	6
— INTERNAL	4	4	4
• OPERATING POWER (mW)	800	800	800
• STANDBY RAM (mW)	12	12	12
• PACKAGE	64 QUIP 68 PLCC	64 QUIP 68 PLCC	40 DIP 44 PLCC

Rom-less Microcomputers

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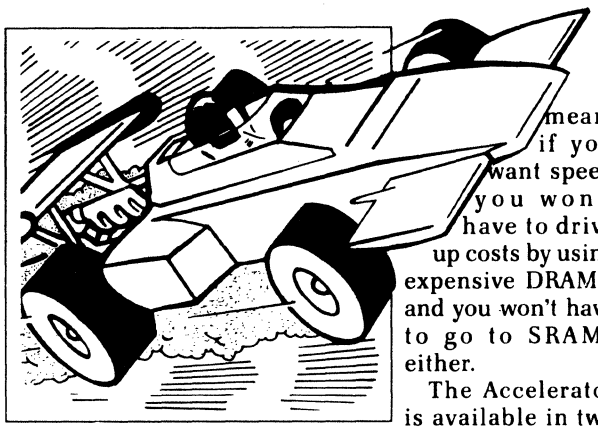
DRAM CONTROLLER

Our new 1- and 4-meg DRAM Controller is also a system accelerator. It can give you

80ns *Performance from* 120ns *DRAMs.*



Our new 1- and 4-meg DRAM Controller does so much for system speed that we've named it *The Accelerator.*

If you're a designer attracted to speed, you're going to want to design it in.

The KS84C21/22 DRAM Controller supports interleaving, and it supports the fastest access modes of the newest DRAMs.

It radically reduces parts count and engineering effort compared to PAL-based designs and interfaces to all major microprocessors.

But above all, it effectively increases the speed of your memory array–giving you performance exceeding 80ns from 120ns DRAMs.* Which means if you want speed, you won't have to drive up costs by using expensive DRAMs, and you won't have to go to SRAMs either.

The Accelerator is available in two versions. One has an externally programmable register, for prototyping and moderate-volume applications. The other version is the first and only mask-programmed DRAM controller ever developed anywhere, and it eliminates still more logic parts.

To make it easier to get started with The Accelerator, we've made up a sample kit.

Request yours today and start designing-in speed!

Samsung's DRAM Controller.

Part	RAMs Supported	Package
KS84C21-25CL	256K, 1 MB	68-pin PLCC
KS84C22-25CL	256K, 1 MB, 4 MB	84-pin PLCC

*System dependent.

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Microprocessor Peripheral Selection Guide

SELECTION GUIDE

DEVICE	PART NUMBER	SPEED	PACKAGE AVAILABILITY		CMOS	ADVANTAGES
			PLASTIC DIP	PLCC		
SCSI Controller	KS53C80-1CP	1 MHz	now	now	Yes	Industry standard
	KS53C80-3CP	3 MHz	now	now	Yes	Higher speed version (3 MHz vs. 1 MHz)
CRT Controller	KS68C45-4CP	4 MHz	now	2H 1989	Yes	Higher speed version (4 MHz vs 1 to 2 MHz), industry standard
	KS68C45-6CP	6 MHz	now	2H 1989	Yes	Higher speed version (6 MHz vs 1 to 2 MHz), industry standard
DMA Controller	KS82C37A-5CP	5 MHz	now	2H 1989	Yes	Typical competitor speeds are 3/4/5 MHz
	KS82C37A-8CP	8 MHz	now	2H 1989	Yes	Higher speed version (8 MHz)
	KS82C37A-10CP	10 MHz	now	2H 1989	Yes	Highest speed version available (10 MHz)
Async Comm Controller	KS82C50-8CP	8 MHz	now	2H 1989	Yes	Industry standard
	KS82C50-10CP	10 MHz	now	2H 1989	Yes	Higher speed version (10 MHz)
Serial Controller	KS82C52-8CP	8 MHz	now	2H 1989	Yes	Industry standard
	KS82C52-10CP	10 MHz	now	2H 1989	Yes	Higher speed version (10 MHz)
Interval Timer	KS82C54-8CP	8 MHz	now	2H 1989	Yes	Industry standard
	KS82C54-10CP	10 MHz	now	2H 1989	Yes	Higher speed version (10MHz)
Peripheral Interface	KS82C55A-8CP	8 MHz	now	2H 1989	Yes	Typical competitor speeds are 3/4/5/8 MHz
	KS82C55A-10CP	10 MHz	now	2H 1989	Yes	Highest speed version available (10 MHz)
Interrupt Controller	KS82C59A-8CP	8 MHz	now	2H 1989	Yes	Typical competitor speeds are 5/8 MHz
	KS82C59A-10CP	10 MHz	now	2H 1989	Yes	Highest speed version available (10 MHz)
Clock Generator	KS82C84A-8CP	8 MHz	now	2H 1989	Yes	Typical competitor speeds are 5/8 MHz
	KS82C84A-10CP	10 MHz	now	2H 1989	Yes	Highest speed version available (10 MHz)
Bus Controller	KS82C88-8CP	8 MHz	now	2H 1989	Yes	Typical competitor speeds are 5/8 MHz
	KS82C88-10CP	10 MHz	now	2H 1989	Yes	Highest speed version available (10 MHz)
286 Clock Generator	KS82C284-10CP	10 MHz	now	2H 1989	Yes	Industry standard
	KS82C284-12CP	12 MHz	now	2H 1989	Yes	High speed version (12 MHz)
	KS82C284-16CP	16 MHz	now	2H 1989	Yes	Highest speed version available (16 MHz)
286 Bus Controller	KS82C288-10CP	10 MHz	now	2H 1989	Yes	Industry standard
	KS82C288-12CP	12 MHz	now	2H 1989	Yes	High speed version (12 MHz)
	KS82C288-16CP	16 MHz	now	2H 1989	Yes	Highest speed version available (16 MHz)
286 Bus Arbiter	KS82C289-10CP	10 MHz	now	2H 1989	Yes	Industry standard
	KS82C289-12CP	12 MHz	now	2H 1989	Yes	High speed version (12 MHz)
	KS82C289-16CP	16 MHz	now	2H 1989	Yes	Highest speed version available (16 MHz)
DRAM Controller	KS84C21-25CL	25 MHz	N/A	now	Yes	For high performance designs, controls 256K, 1M DRAMs
	KS84C22-25CL	25 MHz	N/A	now	Yes	Controls 256K, 1M, 4M DRAMs
DRAM Controller	KS84C21-25CL/XYZ	25 MHz	N/A	now	Yes	Masked version of the DRAM controller, where XYZ is the unique ROM code
	KS84C22-25CL/XYZ	25 MHz	N/A	now	Yes	Masked version of the DRAM controller, where XYZ is the unique ROM code
Serial Comm Controller	KS85C30-8CP	8 MHz	now	2H 1989	Yes	Industry standard (8 MHz)
	KS85C30-10CP	10 MHz	now	2H 1989	Yes	Industry standard (10 MHz)

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CPL
Cross Reference/Selection Guide

CPL CROSS REFERENCE GUIDE

AMD/MMI PART #	SAMSUNG DESCRIPTION	SAMSUNG PART #
PAL12L10	24-Pin ½ Power, 35ns, CMOS PLD	CPL20L10-35
PAL14L8	24-pin ½ Power, 35ns, CMOS PLD	CPL20L8-35
PAL16L6	24-pin ½ Power, 35ns, CMOS PLD	CPL20L8-35
PAL18L4	24-pin ½ Power, 35ns, CMOS PLD	CPL20L8-35
PAL16L8A	20-pin ½ Power, 25ns, CMOS PLD	CPL16L8-25
PAL16L8A-2	20-pin ½ Power, 35ns, CMOS PLD	CPL16L8-35
PAL16L8A-4	20-pin ¼ Power, 35ns, CMOS PLD	CPL16L8L-35
PAL16L8B-2	20-pin ½ Power, 25ns, CMOS PLD	CPL16L8-25
PAL16L8B-4	20-pin ¼ Power, 35ns, CMOS PLD	CPL16L8L-35
PAL16L8	20-pin ½ Power, 35ns, CMOS PLD	CPL16L8-35
PAL16L8D-4	20-pin ¼ Power, 25ns, CMOS PLD	CPL16L8L-25
PAL16R4A	20-pin ½ Power, 25ns, CMOS PLD	CPL16R4-25
PAL16R4A-2	20-pin ½ Power, 35ns, CMOS PLD	CPL16R4-35
PAL16R4A-4	20-pin ¼ Power, 35ns, CMOS PLD	CPL16R4L-35
PAL16R4B-2	20-pin ½ Power, 25ns, CMOS PLD	CPL16R4-25
PAL16R4B-4	20-pin ¼ Power, 35ns, CMOS PLD	CPL16R4L-35
PAL16R4	20-pin ½ Power, 25ns, CMOS PLD	CPL16R4-35
PAL16R4D-4	20-pin ¼ Power, 25ns, CMOS PLD	CPL16R4L-25
PAL16R6A	20-pin ½ Power, 25ns, CMOS PLD	CPL16R6-25
PAL16R6A-2	20-pin ½ Power, 35ns, CMOS PLD	CPL16R6-35
PAL16R6A-4	20-pin ¼ Power, 35ns, CMOS PLD	CPL16R6L-35
PAL16R6B-2	20-pin ½ Power, 25ns, CMOS PLD	CPL16R6-25
PAL16R6B-4	20-pin ¼ Power, 35ns, CMOS PLD	CPL16R6L-35
PAL16R6	20-pin ½ Power, 25ns, CMOS PLD	CPL16R6-35
PAL16R6D-4	20-pin ¼ Power, 25ns, CMOS PLD	CPL16R6L-25
PAL16R8A	20-pin ½ Power, 25ns, CMOS PLD	CPL16R8-25
PAL16R8A-2	20-pin ½ Power, 35ns, CMOS PLD	CPL16R8-35
PAL16R8A-4	20-pin ¼ Power, 35ns, CMOS PLD	CPL16R8L-35
PAL16R8B-2	20-pin ½ Power, 25ns, CMOS PLD	CPL16R8-25
PAL16R8B-4	20-pin ¼ Power, 35ns, CMOS PLD	CPL16R8L-35
PAL16R8	20-pin ½ Power, 35ns, CMOS PLD	CPL16R8-35
PAL16R8D-4	20-pin ¼ Power, 25ns, CMOS PLD	CPL16R8L-25
AmPAL16L8A	20-pin ½ Power, 25ns, CMOS PLD	CPL16L8-25
AmPAL16L8AL	20-pin ½ Power, 25ns, CMOS PLD	CPL16L8-25
AmPAL16L8	20-pin ½ Power, 35ns, CMOS PLD	CPL16L8-35
AmPAL16L8L	20-pin ½ Power, 35ns, CMOS PLD	CPL16L8-35
AmPAL16L8Q	20-pin ¼ Power, 35ns, CMOS PLD	CPL16L8L-35
AmPAL16R4A	20-pin ½ Power, 25ns, CMOS PLD	CPL16R4-25
AmPAL16R4AL	20-pin ½ Power, 25ns, CMOS PLD	CPL16R4-25
AmPAL16R4	20-pin ½ Power, 35ns, CMOS PLD	CPL16R4-35
AmPAL16R4L	20-pin ½ Power, 35ns, CMOS PLD	CPL16R4-35
AmPAL16R4Q	20-pin ¼ Power, 35ns, CMOS PLD	CPL16R4L-35
AmPAL16R6A	20-pin ½ Power, 25ns, CMOS PLD	CPL16R6-25
AmPAL16R6AL	20-pin ½ Power, 25ns, CMOS PLD	CPL16R6-25
AmPAL16R6	20-pin ½ Power, 35ns, CMOS PLD	CPL16R6-35
AmPAL16R6L	20-pin ½ Power, 35ns, CMOS PLD	CPL16R6-35
AmPAL16R6Q	20-pin ¼ Power, 35ns, CMOS PLD	CPL16R6L-35
AmPAL16R8A	20-pin ½ Power, 25ns, CMOS PLD	CPL16R8-25
AmPAL16R8AL	20-pin ½ Power, 25ns, CMOS PLD	CPL16R8-25
AmPAL16R8	20-pin ½ Power, 35ns, CMOS PLD	CPL16R8-35
AmPAL16R8L	20-pin ½ Power, 35ns, CMOS PLD	CPL16R8-35
AmPAL16R8Q	20-pin ¼ Power, 35ns, CMOS PLD	CPL16R8L-35
AmPAL20L10AL	24-pin ½ Power, 25ns, CMOS PLD	CPL20L10-25
AmPAL22V10A	24-pin ½ Power, 25ns, Versatile CMOS PLD	CPL22V10-25
AmPAL22V10	24-pin ½ Power, 35ns, Versatile CMOS PLD	CPL22V10-35

AMD/MMI PART #	DESCRIPTION	SAMSUNG PART #
PAL18L4	24-pin ½ Power, 35ns, CMOS PLD	CPL20L8-35
PAL20L10A	24-pin ½ Power, 25ns, CMOS PLD	CPL20L10-25
PAL20L10	24-pin ½ Power, 35ns, CMOS PLD	CPL20L10-35
PAL20L8A	24-pin ½ Power, 25ns, CMOS PLD	CPL20L8-25
PAL20L8A-2	24-pin ½ Power, 35ns, CMOS PLD	CPL20L8-35
PAL20L8B-2	24-pin ½ Power, 25ns, CMOS PLD	CPL20L8-25
PAL20R4A	24-pin ½ Power, 25ns, CMOS PLD	CPL20R4-25
PAL20R4A-2	24-pin ½ Power, 35ns, CMOS PLD	CPL20R4-35
PAL20R4B-2	24-pin ½ Power, 25ns, CMOS PLD	CPL20R4-25
PAL20R6A	24-pin ½ Power, 25ns, CMOS PLD	CPL20R6-25
PAL20R6A-2	24-pin ½ Power, 35ns, CMOS PLD	CPL20R6-35
PAL20R4B-2	24-pin ½ Power, 25ns, CMOS PLD	CPL20R6-25
PAL20R8A	24-pin ½ Power, 25ns, CMOS PLD	CPL20R8-25
PAL20R8A-2	24-pin ½ Power, 35ns, CMOS PLD	CPL20R8-35
PAL20R8B-2	24-pin ½ Power, 25ns, CMOS PLD	CPL20R8-25
PALC22V10H-25	24-pin ½ Power, 25ns, Versatile CMOS PLD	CPL22V10-25
PALC22V10H-35	24-pin ½ Power, 35ns, Versatile CMOS PLD	CPL22V10-35
PALC16L8Q-25	20-pin ¼ Power, 25ns, CMOS PLD	CPL16L8L-25
PALC16R4Q-25	20-pin ¼ Power, 25ns, CMOS PLD	CPL16R4L-25
PALC16R6Q-25	20-pin ¼ Power, 25ns, CMOS PLD	CPL16R6L-25
PALC16R8Q-25	20-pin ¼ Power, 25ns, CMOS PLD	CPL16R8L-25
ALTERA		
EP310, -2, -3**	20-pin ¼ Power, 35ns, CMOS PLD	CPL16L8L-35 CPL16R4L-35 CPL16R6L-35 CPL16R8L-35
INTEL		
5C031**	20-pin ¼ Power, 35ns, CMOS PLD	CPL16L8L-35 CPL16R4L-35 CPL16R6L-35 CPL16R8L-35
CYPRESS		
PALC16L8-25	20-pin ½ Power, 25ns, CMOS PLD	CPL16L8-25
PALC16L8L-25	20-pin ¼ Power, 25ns, CMOS PLD	CPL16L8L-25
PALC16L8-35	20-pin ½ Power, 35ns, CMOS PLD	CPL16L8-35
PALC16L8L-35	20-pin ¼ Power, 35ns, CMOS PLD	CPL16L8L-35
PALC16R4-25	20-pin ½ Power, 25ns, CMOS PLD	CPL16R4-25
PALC16R4L-25	20-pin ¼ Power, 25ns, CMOS PLD	CPL16R4L-25
PALC16R4-35	20-pin ½ Power, 35ns, CMOS PLD	CPL16R4-35
PALC16R4L-35	20-pin ¼ Power, 35ns, CMOS PLD	CPL16R4L-35
PALC16R6-25	20-pin ½ Power, 25ns, CMOS PLD	CPL16R6-25
PALC16R6L-25	20-pin ¼ Power, 25ns, CMOS PLD	CPL16R6L-25
PALC16R6-35	20-pin ½ Power, 35ns, CMOS PLD	CPL16R6-35
PALC16R6L-35	20-pin ¼ Power, 35ns, CMOS PLD	CPL16R6L-35
PALC16R8-25	20-pin ½ Power, 25ns, CMOS PLD	CPL16R8-25
PALC16R8L-25	20-pin ¼ Power, 25ns, CMOS PLD	CPL16R8L-25
PALC16R8-35	20-pin ½ Power, 35ns, CMOS PLD	CPL16R8-35

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CYPRESS PART #	SAMSUNG DESCRIPTION	SAMSUNG PART #
PALC16R8L-35	20-pin ¼ Power, 35ns, CMOS PLD	CPL16R8L-35
PALC22V10-25	24-pin ½ Power, 25ns, Versatile CMOS PLD	CPL22V10-25
PALC22V10L-25	24-pin ¼ Power, 25ns, Versatile CMOS PLD	CPL22V10L-25
PALC22V10-35	24-pin ½ Power, 35ns, Versatile CMOS PLD	CPL22V10-35
PALC22V10L-35	24-pin ¼ Power, 35ns, Versatile CMOS PLD	CPL22V10L-35
FAIRCHILD		
16L8A	20-pin ½ Power, 25ns, CMOS PLD	CPL16L8-25
16P8A***	20-pin ½ Power, 25ns, CMOS PLD	CPL16L8-25
16R4A	20-pin ½ Power, 25ns, CMOS PLD	CPL16R4-25
16R6A	20-pin ½ Power, 25ns, CMOS PLD	CPL16R6-25
16R8A	20-pin ½ Power, 25ns, CMOS PLD	CPL16R8-25
16RP4A***	20-pin ½ Power, 25ns, CMOS PLD	CPL16R4-25
16RP6A***	20-pin ½ Power, 25ns, CMOS PLD	CPL16R6-25
16RP8A***	20-pin ½ Power, 25ns, CMOS PLD	CPL16R8-25
HARRIS		
HPL16LC8-5***	20-pin ¼ Power, 35ns, CMOS PLD	CPL16L8L-35
HPL16RC4-5***	20-pin ¼ Power, 35ns, CMOS PLD	CPL16R4L-35
HPL16RC6-5***	20-pin ¼ Power, 35ns, CMOS PLD	CPL16R6L-35
HPL16RC8-5***	20-pin ¼ Power, 35ns, CMOS PLD	CPL16R8L-35
LATTICE		
GAL16V8-25Q*	20-pin ¼ Power, 25ns, CMOS PLD	CPL16L8L-25 CPL16R4L-25 CPL16R6L-25 CPL16R8L-25
GAL16V8-25L*	20-pin ½ Power, 25ns, CMOS PLD	CPL16L8-25 CPL16R4-25 CPL16R6-25 CPL16R8-25
GAL20V8-25Q*	24-pin ¼ Power, 25ns, CMOS PLD	CPL20L8L-25 CPL20R4L-25 CPL20R6L-25 CPL20R8L-25
GAL20V8-25L*	24-pin ½ Power, 25ns, CMOS PLD	CPL20L8-25 CPL20R4-25 CPL20R6-25 CPL20R8-25
NATIONAL		
12L10	24-pin ½ Power, 35ns, CMOS PLD	CPL20L10-35
14L8	24-pin ½ Power, 35ns, CMOS PLD	CPL20L8-35
16L6	24-pin ½ Power, 35ns, CMOS PLD	CPL20L8-35
18L4	24-pin ½ Power, 35ns, CMOS PLD	CPL20L8-35
PAL16L8A2	20-pin ½ Power, 35ns, CMOS PLD	CPL16L8-35
PAL16L8A	20-pin ½ Power, 25ns, CMOS PLD	CPL16L8-25
PAL16L8B2	20-pin ½ Power, 25ns, CMOS PLD	CPL16L8-25
PAL16L8B4	20-pin ¼ Power, 35ns, CMOS PLD	CPL16L8L-35
PAL16L8	20-pin ½ Power, 35ns, CMOS PLD	CPL16L8-35

NATIONAL PART #	SAMSUNG DESCRIPTION	SAMSUNG PART #
PAL16R4A2	20-pin ½ Power, 35ns, CMOS PLD	CPL16R4-35
PAL16R4A	20-pin ½ Power, 25ns, CMOS PLD	CPL16R4-25
PAL16R4B2	20-pin ½ Power, 25ns, CMOS PLD	CPL16R4-25
PAL16R4B4	20-pin ¼ Power, 35ns, CMOS PLD	CPL16R4L-35
PAL16R4	20-pin ½ Power, 35ns, CMOS PLD	CPL16R4-35
PAL16R6A2	20-pin ½ Power, 35ns, CMOS PLD	CPL16R6-35
PAL16R6A	20-pin ½ Power, 25ns, CMOS PLD	CPL16R6-25
PAL16R6B2	20-pin ½ Power, 25ns, CMOS PLD	CPL16R6-25
PAL16R6B4	20-pin ¼ Power, 35ns, CMOS PLD	CPL16R6L-35
PAL16R6	20-pin ½ Power, 35ns, CMOS PLD	CPL16R6-35
PAL16R8A2	20-pin ½ Power, 35ns, CMOS PLD	CPL16R8-35
PAL16R8A	20-pin ½ Power, 25ns, CMOS PLD	CPL16R8-25
PAL16R8B2	20-pin ½ Power, 25ns, CMOS PLD	CPL16R8-25
PAL16R8B4	20-pin ¼ Power, 35ns, CMOS PLD	CPL16R8L-35
PAL16R8C	20-pin ½ Power, 35ns, CMOS PLD	CPL16R8-35
PAL20L10	24-pin ½ Power, 35ns, CMOS PLD	CPL20L10-35
PAL20L8A	24-pin ½ Power, 25ns, CMOS PLD	CPL20L8-25
PAL20L8	24-pin ½ Power, 35ns, CMOS PLD	CPL20L8-35
PAL20R4A	24-pin ½ Power, 25ns, CMOS PLD	CPL20R4-25
PAL20R4	24-pin ½ Power, 35ns, CMOS PLD	CPL20R4-35
PAL20R6A	24-pin ½ Power, 25ns, CMOS PLD	CPL20R6-25
PAL20R6	24-pin ½ Power, 35ns, CMOS PLD	CPL20R6-35
PAL20R8A	24-pin ½ Power, 25ns, CMOS PLD	CPL20R8-25
PAL20R8	24-pin ½ Power, 35ns, CMOS PLD	CPL20R8-35
TI		
TIB PAL22V10	20-pin ½ Power, 35ns, Versatile CMOS PLD	CPL22V10-35
TIB PAL22V10A	20-pin ½ Power, 25ns, Versatile CMOS PLD	CPL22V10-25
PAL16L8A	20-pin ½ Power, 25ns, CMOS PLD	CPL16L8-25
PAL16L8A-2	20-pin ½ Power, 35ns, CMOS PLD	CPL16L8-35
TIB PAL16L8-25	20-pin ½ Power, 25ns, CMOS PLD	CPL16L8-25
PAL16R4A	20-pin ½ Power, 25ns, CMOS PLD	CPL16R4-25
PAL16R4A-2	20-pin ½ Power, 35ns, CMOS PLD	CPL16R4-35
TIB PAL16R4-25	20-pin ½ Power, 25ns, CMOS PLD	CPL16R4-25
PAL16R6A	20-pin ½ Power, 25ns, CMOS PLD	CPL16R6-25
PAL16R6A-2	20-pin ½ Power, 35ns, CMOS PLD	CPL16R6-35
TIB PAL16R6-25	20-pin ½ Power, 25ns, CMOS PLD	CPL16R6-25
PAL16R8A	20-pin ½ Power, 25ns, CMOS PLD	CPL16R8-25
PAL16R8A-2	20-pin ½ Power, 35ns, CMOS PLD	CPL16R8-35
TIB PAL16R8-25	20-pin ½ Power, 25ns, CMOS PLD	CPL16R8-25
PAL20L10A	24-pin ½ Power, 25ns, CMOS PLD	CPL20L10-25
PAL20L10A-2	24-pin ½ Power, 35ns, CMOS PLD	CPL20L10-35
TIB PAL20L10-30	24-pin ½ Power, 25ns, CMOS PLD	CPL20L10-25
PAL20L8A	24-pin ½ Power, 25ns, CMOS PLD	CPL20L8-25
PAL20L8A-2	24-pin ½ Power, 35ns, CMOS PLD	CPL20L8-35
TIB PAL20L8-25	24-pin ½ Power, 25ns, CMOS PLD	CPL20L8-25
PAL20R4A	24-pin ½ Power, 25ns, CMOS PLD	CPL20R4-25
PAL20R4A-2	24-pin ½ Power, 35ns, CMOS PLD	CPL20R4-35
TIB PAL20R4-25	24-pin ½ Power, 25ns, CMOS PLD	CPL20R4-25
PAL20R6A	24-pin ½ Power, 25ns, CMOS PLD	CPL20R6-25
PAL20R6A-2	24-pin ½ Power, 35ns, CMOS PLD	CPL20R6-35

* The GAL16V8 and GAL20V8 devices are 20 & 24-pin supersets of Samsung's equivalent devices. Please check output architecture for exact device crossing.

** The EP310 and 5C031 devices are 20-pin supersets of Samsung's equivalent devices. Please check output architecture for exact device crossing.

*** These devices have programmable polarity outputs. Please check output polarity for crossing accuracy.

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CPL CROSS REFERENCE GUIDE (Continued)

TI PART #	SAMSUNG DESCRIPTION	SAMSUNG PART #
TIB PAL20R6-25	24-pin ½ Power, 25ns, CMOS PLD	CPL20R6-25
PAL20R8A	24-pin ½ Power, 25ns, CMOS PLD	CPL20R8-25
PAL20R8A-2	24-pin ½ Power, 35ns, CMOS PLD	CPL20R8-35
TIB PAL20R8-25	24-pin ½ Power, 25ns, CMOS PLD	CPL20R8-25

PRODUCT SELECTION GUIDE

Part #	Pins	Array Inputs	Dedicated Inputs	I/O's	Outputs			Max Speed (ns)[1]		Max I_{CC} (mA)		Available Packages
					Combinatorial	Registered	Total	-25	-35	Low Power	Std. Power	
CPL16L8	20	16	10	6	8	0	8	t_{PD}=25	t_{PD}=35	45	70	N, W
CPL16R4	20	16	8	4	4	4	8	t_{PD}/t_{CO}=25/15	t_{PD}/t_{CO}=35/25	45	70	N, W
CPL16R6	20	16	8	2	2	6	8	t_{PD}/t_{CO}=25/15	t_{PD}/t_{CO}=35/25	45	70	N, W
CPL16R8	20	16	8	0	0	8	8	t_{CO}=15	t_{CO}=25	45	70	N, W
CPL20L10	24	20	12	8	10	0	10	t_{PD}=25	t_{PD}=35	45	70	N, W
CPL20L8	24	20	14	6	8	0	8	t_{PD}=25	t_{PD}=35	45	70	N, W
CPL20R4	24	20	12	4	4	4	8	t_{PD}/t_{CO}=25/15	t_{PD}/t_{CO}=35/25	45	70	N, W
CPL20R6	24	20	12	2	2	6	8	t_{PD}/t_{CO}=25/15	t_{PD}/t_{CO}=35/25	45	70	N, W
CPL20R8	24	20	12	0	0	8	8	t_{CO}=15	t_{CO}=25	45	70	N, W
CPL22V10[2]	24	22	12	10	Programmable Macrocell Outupts		10	t_{PD}/t_{CO}=25/15	t_{PD}/t_{CO}=35/25	55	90	N, W
CPL16V8[2]	20	16	10	8	Programmable Macrocell Outupts		8	t_{PD}/t_{CO}=25/15	t_{PD}/t_{CO}=35/25	55	90	N, W

Package Codes: N = Plastic DIP, W = Windowed CERDIP

Notes:
(1) The above specifications are for the commercial temperature range of 0 to 70°C. All Power supplies are V_{CC} = 5V ± 10%
(2) Contact factory for availability.

CPL STARTER KIT

The Starter Kit includes a software package developed by Personal CAD Systems and based on CUPL™, the most powerful high-level language for designing programmable logic. And it also includes samples of Samsung CPL20 and CPL24 devices, which are supported by the Starter Kit.

The CPL Starter Kit includes:

- CPL20 and CPL24 samples.
- A CPL data book.
- A manual for the CUPL software.
- A Programmable Logic User Guide (PLUG) diskette, which lets you browse interactively through the workings of programmable logic.
- "My First PAL Design," a booklet that leads you step by step through programmable logic design.

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125 Parts

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The entire Samsung AHCT CMOS advanced logic family is in stock, available, ready, and waiting to be shipped—right now. All fast, all very very cool.

KS74AHCT Parts

Gates and Inverters

00	08	20	51
01	09	21	58
02	10	22	86
03	11	27	132
04	12	30	133
05	14	32	266

Buffers and Line Drivers

125	241	367	467
126	244	368	468*
210	365	465*	540
240	366	466	541

Flip-Flops

73	173	534	823
74	174	564	824*
76	175	574	825*
78	273	670	826*
107	374	794	
109	377	821*	
112	399	822*	

Latches

75*	533	841*	845
77*	563	842*	846
259	573	843*	
373	793	844*	

Transceivers/ Registered Transceivers

242*	643	651	664
243*	645	652	665*
245	646	658*	
640	648	659*	

Counters

160	168	192	590*
161	169	193	591*
162	190	390*	592
163	191	393	593*

Decoders/Encoders

42	139	154	238
138	148	155	239

Multivibrators

121*	123*	423*

Logic Level Converters

4049	4050*

Multiplexers

151	158	257	353
153	251	258	
157	253	352	

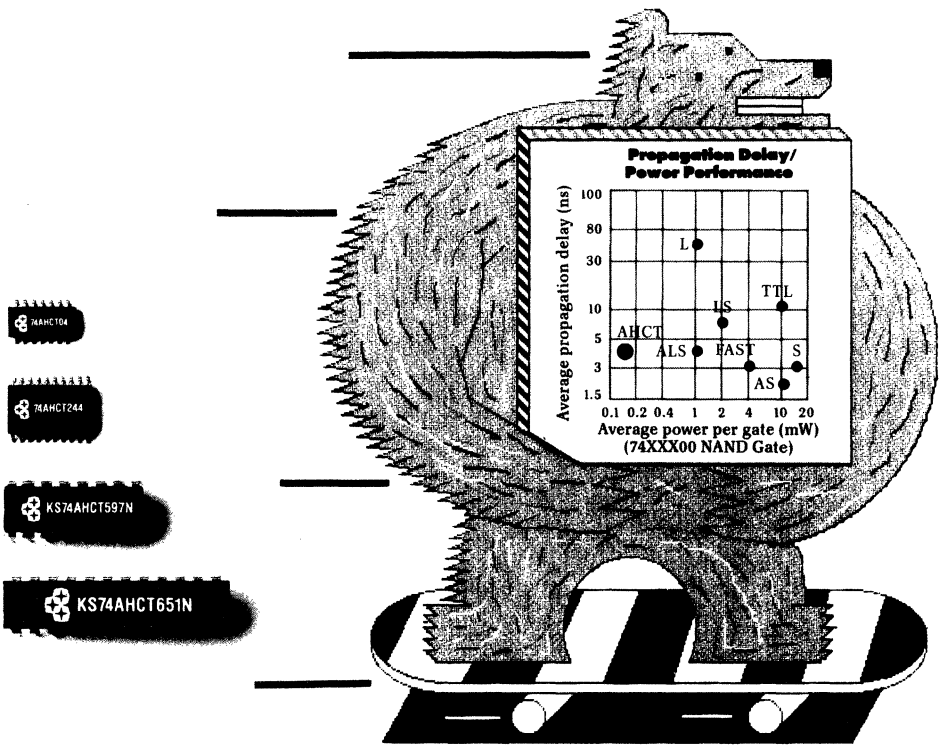
Shift Registers

164	194	299	596*
165	195	595	597
166			

Arithmetic Circuits

181	518	522	684*
182*	519	679	686*
183	520*	680	688
280	521	682	689*

All parts are available in plastic DIP. For SOIC availability, contact the factory.
**Available by end of 1988.*



When you look at both speed and power, you see that Samsung's AHCT family is, simply, unsurpassed.

And unlike other advanced logic families, these are parts that are available today, from stock.

All 157* of the AHCT CMOS logic family parts are direct plug-in replacements for ALS and FAST™-parts that provide the most comprehensive selection of standard logic functions available. Which means that no matter which ALS or FAST part you're using, you can replace it with an AHCT CMOS part–and cut your power–right away.

The entire family has a successful three-year production history behind it. And the parts are competitively priced –in fact you'll pay no more than you would for ALS.

We have free samples available for you today. Or, as an additional way to learn just how good these parts are, call Samsung at (408) 434-5400 and request information on our AHCT tool box. It keeps 100 of the most popular advanced CMOS logic device types at your fingertips, whenever you need them.

**Of the 157 parts in the family, 125 are available from stock today; the remaining 32 will be available by the end of 1988.*

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64K AND 256K DRAM CROSS REFERENCE

	64K × 1 PAGE MODE NMOS	256K × 1 PAGE MODE NMOS	256K × 1 NIBBLE MODE NMOS	64K × 4 PAGE MODE NMOS
SAMSUNG	KM4164B	KM41256A	KM41257A	KM41464A
MICRON	MT4264	MT1259		MT4067
INMOS	IMS2600			
FUJITSU	MB8264A	MB81256	MB81257	
NEC	μPD4164	μPD41256	μPD41257	μPD41464
OKI	MSM3764	MSM41256	MSM41257A	MSM41464
NATIONAL	NMC4164			
TI	TMS4164	TMS4256	TMS4257	TMS4464
TOSHIBA	TMM4164A	TMM41256	TMM41257	TMM41464
PANASONIC	MN4164	MN41256		
THOMPSON	TS4164			
MOTOROLA		MCM6256B	MCM6256B	MCM41464
MITSUBISHI	M5K4164	M5M4256A	M5M4257A	M5M4464
HITACHI		HM50256	HM50257	HM50464
SIEMENS		HYB41256		

1 MEG DRAM CROSS REFERENCE

	1 MEG × 1 FAST-PAGE CMOS	1 MEG × 1 STATIC COLUMN CMOS	1 MEG × 1 NIBBLE MODE CMOS	256K × 4 FAST-PAGE CMOS	256K × 4 STATIC COLUMN CMOS
SAMSUNG	KM41C1000	KM41C1002	KM41C1001	KM44C256	KM44C258
HITACHI	HM511000	HM511002	HM511001	HM514256	HM514258
MICRON	MT4C1024	MT4C1026	MT4C1025	MT4C4256	MT4C4258
MITSUBISHI	M5M4C1000	M5M4C1002	M5M4C1001	M5M44C256	M5M44C258
MOTOROLA	MCM511000	MCM511002	MCM511001	MCM514256	MCM514258
NEC	μPD421000	μPD421002	μPD421001	μPD424256	μPD424258
OKI	MSM41000	MSM41002	MSM41001	MSM41005	
SHARP				LH64256	LH64258
TOSHIBA	TC511000	TC511002	TC511001	TC514256	TC514258
TI	TMS4C1024	TMS4C1027	TMS4C1025	TMS44C256	TMS44C257
FUJITSU	MB81C1000	MB81C1002	MB81C1001	MB81C4256	MB81C4258
SIEMENS	HYB511000	HYB511002	HYB511001		

SRAM PRODUCT DESCRIPTION

PART NUMBER	ORGANIZATION	ACCESS TIME MAX (ns)	SUPPLY VOLTAGE (V)	MAX ACTIVE/STBY CURRENT (mA)	TEMP. RANGE (°C)	PACKAGE(S)	PROCESS TECHNOLOGY
KM6264AP-12 KM6264AP-10	8,192 × 8	120 100	+5 ± 10%	40/1.0	0 to +70°C	PDIP-28 pin (600 mil)	CMOS
KM6264ALP-12 KM6264ALP-10	8,192 × 8	120 100	+5 ± 10%	40/0.1	0 to +70°C	PDIP-28 pin (600 mil)	CMOS
KM62256P-12 KM62256P-10	32,768 × 8	120 100	+5 ± 10%	45/1.0	0 to +70°C	PDIP-28 pin (600 mil)	CMOS
KM62256LP-12 KM62256LP-10	32,768 × 8	120 100	+5 ± 10%	45/0.1	0 to +70°C	PDIP-28 pin (600 mil)	CMOS

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SRAM CROSS REFERENCE

	8K × 8 CMOS	8K × 8 LOW POWER CMOS	32K × 8 CMOS	32K × 8 LOW POWER CMOS
SAMSUNG	KM6264A	KM6264AL	KM62256	KM62256L
AMD	AM99C88			
FUJITSU	MB8464A	MB8464A-L	MB84256	MB84256-L
HITACHI	HM6264	HM6264L	HM62256	HM62256L
IDT		IDT8M864L		
MITSUBISHI	M5M5165	M5M5165-L	M5M5256	M5M5256-L
MOTOROLA	MCM6064	MCM60L64	MCM60256	MCM60L256
NEC	μPD4364	μPD4364-L	μPD43256	μPD43256-L
OKI	MSM5165			
S-MOS	SRM2264C		SRM20256C	
TOSHIBA	TC5565A	TC5565AL	TC55257A	TC55257AL
VITELIC	V65C64	V65C64L		
GE/RCA	CDM6264			

FIFO* PRODUCT DESCRIPTION

PART NUMBER	ORGAN-IZATION	CYCLE TIME MAX (ns)	ACCESS TIME MAX (ns)	SUPPLY VOLTAGE (V)	MAX ACTIVE/STBY CURRENT (mA)	TEMP. RANGE (°C)	PACKAGE(S)	PROCESS TECHNOLOGY
KM75C01AP-80	512 × 9	100	80	+5 ± 10%	80/8	0 to +70°C	PDIP-28 pin	CMOS
KM75C01AP-50		65	50		80/8			
KM75C01AP-35		45	35		80/8			
KM75C01AP-25		35	25		100/15			
KM75C01AJ-80	512 × 9	100	80	+5 ± 10%	80/8	0 to +70°C	PLCC-32 pin	CMOS
KM75C01AJ-50		65	50		80/8			
KM75C01AJ-35		45	35		80/8			
KM75C01AJ-25		35	25		100/15			
KM75C02AP-80	1,024 × 9	100	80	+5 ± 10%	80/8	0 to +70°C	PDIP-28 pin	CMOS
KM75C02AP-50		65	50		80/8			
KM75C02AP-35		45	35		80/8			
KM75C02AP-25		35	25		100/15			
KM75C02AJ-80	1,024 × 9	100	80	+5 ± 10%	80/8	0 to +70°C	PLCC-32 pin	CMOS
KM75C02AJ-50		65	50		80/8			
KM75C02AJ-35		45	35		80/8			
KM75C02AJ-25		35	25		100/15			

* Production Q1, 1989

FIFO CROSS REFERENCE

	512 × 9 CMOS	1,024 × 9 CMOS
SAMSUNG	KM75C01A	KM75C02A
DALLAS SEMI	DS2009	DS2010
IDT	IDT7201A	IDT7202A
CYPRESS	CY7C412	CY7C424
THOMPSON	MK4501	

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EEPROM PRODUCT DESCRIPTION

PART NUMBER	ORGAN-IZATION	ACCESS TIME MAX (ns)	1 TO 32 BYTE PAGE-MODE WRITE?	SUPPLY VOLTAGE (V)	MAX ACTIVE/STBY CURRENT (mA)	TEMP. RANGE (°C)	PACKAGE(S)	PROCESS TECHNOLOGY
KM2816AP-35 KM2816AP-30 KM2816AP-25	2,048 × 8	350 300 250	No	+5 ± 10%	110/50	0 to +70°C	PDIP-24 pin	NMOS
KM28C16P-25* KM28C16P-20* KM28C16P-15*	2,048 × 8	250 200 150	Yes	+5 ± 10%	25/0.1	0 to +70°C	PDIP-24 pin	CMOS
KM28C16PJ-25* KM28C16PJ-20* KM28C16PJ-15*	2,048 × 8	250 200 150	Yes	+5 ± 10%	25/0.1	0 to +70°C	PLCC-32 pin	CMOS
KM2817AP-35 KM2817AP-30 KM2817AP-25	2,048 × 8 (Pin 1 = Ready/Busy)	350 300 250	No	+5 ± 10%	110/50	0 to +70°C	PDIP-28 pin	NMOS
KM28C17P-25* KM28C17P-20* KM28C17P-15*	2,048 × 8 (Pin 1 = Ready/Busy)	250 200 150	Yes	+5 ± 10%	25/0.1	0 to +70°C	PDIP-28 pin	CMOS
KM28C17PJ-25* KM28C17PJ-20* KM28C17PJ-15*	2,048 × 8 (Pin 1 = Ready/Busy)	250 200 150	Yes	+5 ± 10%	25/0.1	0 to +70°C	PLCC-32 pin	CMOS
KM28C64P-25 KM28C64P-20	8,192 × 8	250 200	Yes	+5 ± 10%	25/0.1	0 to +70°C	PDIP-28 pin	CMOS
KM28C64PJ-25* KM28C64PJ-20*	8,192 × 8	250 200	Yes	+5 ± 10%	25/0.1	0 to +70°C	PLCC-32 pin	CMOS
KM28C65P-25 KM28C65P-20	8,192 × 8 (Pin 1 = Ready/Busy)	250 200	Yes	+5 ± 10%	25/0.1	0 to +70°C	PDIP-28 pin	CMOS
KM28C65PJ-25* KM28C65PJ-20*	8,192 × 8 (Pin 1 = Ready/Busy)	250 200	Yes	+5 ± 10%	25/0.1	0 to +70°C	PLCC-32 pin	CMOS

* Engineering samples Q4'88, Production Q1'89

SERIAL I/O EEPROM PRODUCT DESCRIPTION

PART NUMBER	PROGRAMMABLE ORGANIZATION(S)	READ/WRITE CYCLE FREQUENCY	SUPPLY VOLTAGE (V)	TEMP RANGE (°C)	PACKAGE	PROCESS TECHNOLOGY
KM93C46**	256 × 4 128 × 8 64 × 16	250 KHz to 1 MHz	+5 ± 10%	0 to +70°C	PDIP-8 pin	CMOS

** Preliminary Information, Production Q1'89.

EEPROM CROSS REFERENCE

	2K × 8 NMOS	2K × 8 NMOS w/ Ready/Busy	2K × 8 CMOS	2K × 8 CMOS w/ Ready/Busy	8K × 8 CMOS	8K × 8 CMOS w/ Ready/Busy
SAMSUNG	KM2816A	KM2817A	KM28C16	KM28C17	KM28C64	KM28C65
SEEQ	2816A	2817A	28C16	28C17	28C64	
XICOR	X2816A				X2864B	
AMD		AM2817A			AM2864A	AM2864B
NATIONAL	NMC2816	NMC9817			NMC98C64	
OKI		MSM2816				
EXEL	XL2816A	XL2817A			XL2864A	XL2865A
MITSUBISHI					M5M28C64	
ATMEL			AT28C16	AT28C17	AT28C64	
HITACHI						HN58C65
NEC					μPD28C64	
FUJITSU					MBM28C64	

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REGULATOR

3 Terminal Positive Voltage Regulator

Output Current (A)	Device	Available V_{OUT} (V)	Package
3.0	KA78TXXACF	5, 12, 15	TO-3PF
3.0	KA78TXXACT	5, 12, 15	TO-220
3.0	KA78TXXCF	5, 12, 15	TO-3PF
3.0	KA78TXXCT	5, 12, 15	TO-220
1.5	LM317T	1.2 to 37 (Adjustable)	TO-220
1.0	MC78XXCT	5, 6, 8, 9, 10, 12, 15, 18, 24	TO-220
0.5	MC78MXXCT	5, 6, 8, 10, 12, 15, 18, 24	TO-220
0.15	LM723CN	2 to 37 (Adjustable)	14 DIP
0.1	MC78LXXACZ	5, 6, 8, 9, 12, 15, 18, 24	TO-92

3 Terminal Negative Voltage Regulator

Output Current (A)	Device	Available V_{OUT} (-V)	Package
1.5	KA337T	1.2 to 37 (Adjustable)	TO-220
1.0	MC79XXCT	2, 5, 6, 8, 9, 10, 12, 15, 18, 24	TO-220
0.5	MC79MXXCT	5, 6, 8, 10, 12, 15, 18, 24	TO-220
0.1	MC79LXXACZ	5	TO-92

Switching Voltage Regulator

1.5	KA78S40CN	1.3 to 40	16 DIP
0.1	KA3524N	up to 40	16 DIP

Programmable Precision Reference

	KA431CZ (TL431CLP)	2.5 to 36 (Programmable)	TO-92
	KA431CN (TL431CP)	2.5 to 36 (Programmable)	8 DIP
	KA336Z	2.5, 5 LM336Z-2.5, 5 Type	TO-92
	KA385Z-1.2	1.2, LM385Z-1.2 Type	TO-92

OP AMP, Comparator, Timer, Interface

	Single		Dual		Quad	
	Bipolar	CMOS	Bipolar	CMOS	Bipolar	CMOS
OP AMP	KA301AN KA733CN KF351N LM741CN*		KA9256 LM2904N LM358N/AN* MC1458CN* MC1458N* MC4558CN*		LM2902N LM324N/AN* LM348N* MC3303N MC3403N*	
Comparator	KA361N KA710CN LM311N*		KA319N LM2903N LM393N/AN*		LM339N/AN LM2901N LM3302N	
Timer	NE555CN*	KS555HN* KS555N*	NE556CN*	KS556N*	NE558CN*	
Interface					MC1488N* MC1489N/AN*	

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Data Converter Cross Reference Guide

Function	SAMSUNG	NATIONAL	ANALOG DEVICES	MOTOROLA
8 bit Flash A/D 10 bit D/A	KSV3110N-7 KSV3110N-8 KSV3110N-9 KSV3110N-10 KSV3100AN-7 KSV3100AN-8			
8 bit Flash A/D	KSV3208N			
8 bit Half Flash A/D	KAD0820ACN KAD0820BCN	ADC0820BCN ADC0820CCN	AD7820LN-C AD7820KN-C	
8 bit A/D	KAD0808IN KAD0809IN	ADC0808CCN ADC0809CCN		
8 bit D/A	KDA0800CN KDA0801CN KDA0802CN	DAC0800LCN DAC0801LCN DAC0802LCN	AD DAC-08E AD DAC-08C AD DAC-08H	DAC-08EP DAC-08CP DAC-08HP
8 bit D/A	KDA0806CN KDA0807CN KDA0808CN	DAC0806LCN DAC0807LCN DAC0808LCN	 AD1408-7D AD1408-8D	MC1408P6 MC1408P7 MC1408P8
3½ Digit A/D	KS7126CN			
8 bit SAR 8 bit SAR 12 bit SAR	KS25C02N KS25C03N KS25C04N	DM2502N DM2503N DM2504N		

Telecommunications ICs

Pulse Dialer	KS5805AN (MK50992) KS5805BN (MK50993)
DTMF	KS5808N (MK5089)
Tone/Pulse with Redial	KS5819 Series KS5820 Series KS5821 Series
Tone Ringer	KA2410N (ML8204) KA2411N (ML8205) KA2418
Tone Decoder	LM567CN* LM567LN (Low Power)
CODEC CODEC Filter	KT5116J KT3040J

* : Available also in surface mount package (SOIC)

Others

8CH Driver	KA2580AN (UDN2580A) KA2588AN (UDN2588A) KA2651N (UDN6118A)
Transmitter	KS5803AN
Infrared Amp	KA2181 KA2182 KA2183
LED/LAMP Driver	KA2615 KA2616 KA2617 KA2618
FM IF Amp	MC3361N
Amplifier	LM386N*

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Power MOSFET
Cross Reference/Selection Guide

CROSS REFERENCE GUIDE

The following table represents a cross reference for POWER MOSFETS. The Samsung devices are a replacement for the indicated industry part numbers.

GE	SAMSUNG Direct Replacement	GE	SAMSUNG Direct Replacement	GE	SAMSUNG Direct Replacement	GE	SAMSUNG Direct Replacement	GE	SAMSUNG Direct Replacement
D84BK1	IRF523	D84CR3	IRF823	D84EQ3	IRF740	D86DL3	IRF130	D86EQ2	IRF340
D84BK2	IRF523	D84CR4	IRF822	D84DQ4	IRF742	D86DL4	IRF130	D86EQ3	IRF340
D84BK4	IRF511	D84DK1	IRF531	D84ER1	IRF841	D86DM1	IRF230	D86EQ4	IRF340
D84BL1	IRF510	D84DK2	IRF531	D84ER2	IRF840	D86DM2	IRF230	D86ER1	IRF440
D84BL2	IRF510	D83DK3	IRF533	D84ER3	IRF840	D86DM3	IRF230	D86ER2	IRF440
D84BL3	IRF512	D84DK4	IRF533	D84ER4	IRF842	D86DM4	IRF230	D86ER3	IRF440
D84BL4	IRF512	D84DL1	IRF530	D84EU2	IRF820	D86DN1	IRF230	D86ER4	IRF440
D84BM1	IRF610	D84DL2	IRF530	D84EV1	IRF822	D86DN2	IRF230	D86ES1	IRF430
D84BM2	IRF610	D84DL3	IRF532	D84EV2	IRF822	D86DN3	IRF230	D86ES2	IRF430
D84BM3	IRF610	D84DL4	IRF532	D84EW1	IRF822	D86DN4	IRF230	D86EU2	IRF420
D84BM4	IRF610	D84DM1	IRF630	D84EW2	IRF822	D86DQ1	IRF331	D86EV1	IRF420
D84BN1	IRF610	D84DM2	IRF630	D86CK2	IRF130	D86DQ2	IRF330	D86EV2	IRF420
D84BN2	IRF610	D84DM4	IRF630	D86CK3	IRF120	D86DQ3	IRF330	D86EW1	IRF420
D84BN3	IRF612	D84DN1	IRF630	D84CK4	IRF120	D86DQ4	IRF330	D86EW2	IRF420
D84BN4	IRF612	D84DN2	IRF630	D84CL2	IRF120	D86DR1	IRF430	D86FL2	IRF150
D84BQ1	IRF711	D84DN3	IRF632	D86CL4	IRF122	D86DR2	IRF430	D86FL4	IRF150
D84BQ2	IRF710	D84DN4	IRF632	D86CM2	IRF220	D86DR3	IRF430	D86FM2	IRF251
D84BQ3	IRF710	D84DQ1	IRF731	D86CM4	IRF220	D86DR4	IRF430	D86FN2	IRF250
D84BQ4	IRF710	D84DQ2	IRF730	D86CN2	IRF220	D86DS1	IRF432	D86FN4	IRF252
D84CK3	IRF521	D84DQ3	IRF730	D86CN3	IRF220	D86DS2	IRF432	D86FQ1	IRF351
D84CK4	IRF521	D84DQ4	IRF730	D86CN4	IRF220	D86EK3	IRF432	D86FQ2	IRF350
D84CL2	IRF520	D84DR1	IRF831	D86CQ1	IRF320	D86EK4	IRF151	D86FQ3	IRF350
D84CL4	IRF522	D84DR2	IRF830	D86CQ2	IRF320	D86EL4	IRF140	D86FQ4	IRF350
D84CM2	IRF620	D84DR3	IRF830	D86CQ3	IRF323	D86EM1	IRF253	D86FR1	IRF451
D84CM4	IRF620	D84DR4	IRF832	D86CQ4	IRF320	D86EM2	IRF253	D86FR2	IRF450
D84CN1	IRF620	D84DS1	IRF832	D86CR1	IRF420	D86EM4	IRF241	D86FR3	IRF453
D84CN2	IRF620	D84DS2	IRF832	D86CR2	IRF420	D86EN2	IRF240	D86FR4	IRF452
D84CN3	IRF620	D84EL2	IRF540	D86CR3	IRF420	D86EN3	IRF242	D86FU2	IRF430
D84CN4	IRF620	D84EL4	IRF542	D86CR4	IRF420	D86EN4	IRF242		
D84CQ1	IRF720	D84EM2	IRF641	D86DK1	IRF130	D86EQ1	IRF340		
D84CQ2	IRF720	D84EM4	IRF640	D86DK2	IRF130				
D84CQ3	IRF723	D84EN2	IRF640	D86DK3	IRF133				
D84CQ4	IRF720	D84EN4	IRF642	D86DK4	IRF133				
D84CR1	IRF820	D84EQ1	IRF741	D86DL1	IRF130				
D84CR2	IRF820	D84EQ2	IRF740	D86DL2	IRF130				

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Hitachi	SAMSUNG Direct Replacement	Hitachi	SAMSUNG Direct Replacement	Hitachi	SAMSUNG Direct Replacement	Hitachi	SAMSUNG Direct Replacement	Hitachi	SAMSUNG Direct Replacement
P-CHANNEL									
2SJ47	IRF9132	2SJ112	IRF9130	2SJ119	IRFP9240				
2SJ85	IRF9512	2SJ113	IRFP9140	2SJ127	IRF9530				
2SJ86	IRF9610	2SJ114	IRF9242						
2SJ101	IRF9533	2SJ117	IRF9610						
2SJ102	IRF9521	2SJ118	IRFP9241						
N-CHANNEL MOSFETS									
2SK132	IRF122	2SK295	IRF510	2SK351		2SK440	IRF630	2SK642	IRFP450
2SK134	IRF220	2SK296	IRF610	2SK382	IRF820	2SK551	IRF522	2SK682	IRFP450
2SK135	IRF220	2SK298	IRF330	2SK383	IRF530	2SK553	IRF830	2SK683	IRFP452
2SK176	IRF220	2SK299	IRF430	2SK398	IRF120	2SK554	IRF742		
2SK220[H]	IRF220	2SK308	IRF243	2SK399	IRFP140	2SK555	IRF840		
2SK221[H]	IRF220	2SK310	IRF720	2SK400	IRFP242	2SK556	IRF450		
2SK258[H]	IRF330	2SK311	IRF820	2SK401	IRF230	2SK557	IRF450		
2SK259[H]	IRF323	2SK312	IRF340	2SK402	IRFP340	2SK559	IRF350		
2SK260[H]	IRF330	2SK313	IRF440	2SK403	IRF440	2SK560	IRF450		
2SK261	IRF512	2SK319	IRF720	2SK408	IRF612	2SK561	IRF150		
2SK262	IRF610	2SK320	IRF830	2SK409	IRF612	2SK579[L]	IRF710		
2SK263	IRF610	2SK345	IRF523	2SK412	IRFP350	2SK580[S]			
2SK289	IRF123	2SK346	IRF521	2SK413	IRFP243	2SK600	IRF541		
2SK290	IRF122	2SK349	IRFP340	2SK414	IRFP242	2SK641	IRFP440		
2SK294	IRF522	2SK350	IRFP440	2SK428	IRF543	2SK647	IRFP440		

International Rectifier	SAMSUNG Direct Replacement	International Rectifier	SAMSUNG Direct Replacement	International Rectifier	SAMSUNG Direct Replacement	International Rectifier	SAMSUNG Direct Replacement	International Rectifier	SAMSUNG Direct Replacement
IRF120	IRF120	IRF242	IRF242	IRF423	IRF420	IRF620	IRF620	IRF741	IRF741
IRF121	IRF120	IRF243	IRF243	IRF430	IRF430	IRF621	IRF620	IRF742	IRF742
IRF122	IRF122	IRF250	IRF250	IRF431	IRF430	IRF622	IRF620	IRF743	IRF740
IRF123	IRF123	IRF251	IRF251	IRF432	IRF430	IRF623	IRF620	IRF820	IRF820
IRF130	IRF130	IRF252	IRF252	IRF433	IRF430	IRF630	IRF630	IRF821	IRF820
IRF131	IRF130	IRF253	IRF253	IRF440	IRF440	IRF631	IRF630	IRF822	IRF822
IRF132	IRF130	IRF320	IRF320	IRF441	IRF440	IRF632	IRF632	IRF823	IRF823
IRF133	IRF133	IRF321	IRF320	IRF442	IRF440	IRF633	IRF630	IRF830	IRF830
IRF140	IRF140	IRF322	IRF320	IRF443	IRF440	IRF640	IRF640	IRF831	IRF831
IRF141	IRF141	IRF323	IRF323	IRF450	IRF450	IRF641	IRF641	IRF832	IRF832
IRF142	IRF140	IRF330	IRF330	IRF451	IRF451	IRF642	IRF642	IRF833	IRF830
IRF143	IRF140	IRF331	IRF330	IRF452	IRF452	IRF643	IRF640	IRF840	IRF840
IRF150	IRF150	IRF332	IRF330	IRF453	IRF453	IRF710	IRF720	IRF841	IRF841
IRF151	IRF151	IRF333	IRF330	IRF510	IRF510	IRF711	IRF711	IRF842	IRF840
IRF152	IRF150	IRF340	IRF340	IRF511	IRF511	IRF712	IRF710	IRF843	IRF840
IRF153	IRF153	IRF341	IRF340	IRF512	IRF512	IRF713	IRF710	IRF9510	IRF9510
IRF220	IRF220	IRF342	IRF340	IRF513	IRF513	IRF720	IRF720	IRF9511	IRF9511
IRF221	IRF221	IRF343	IRF340	IRF520	IRF520	IRF721	IRF720	IRF9512	IRF9512
IRF222	IRF220	IRF350	IRF350	IRF521	IRF521	IRF722	IRF720	IRF9513	IRF9513
IRF223	IRF220	IRF351	IRF351	IRF522	IRF522	IRF723	IRF723	IRF9520	IRF9520
IRF231	IRF230	IRF352	IRF350	IRF523	IRF523	IRF730	IRF730	IRF9521	IRF9521
IRF232	IRF232	IRF353	IRF350	IRF610	IRF610	IRF731	IRF731	IRF9522	IRF9520
IRF233	IRF230	IRF420	IRF420	IRF611	IRF610	IRF732	IRF730	IRF9523	IRF9523
IRF240	IRF240	IRF421	IRF420	IRF612	IRF612	IRF733	IRF730	IRF9530	IRF9530
IRF241	IRF241	IRF422	IRF420	IRF613	IRF610	IRF740	IRF740	IRF9531	IRF9531

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International Rectifier	SAMSUNG Direct Replacement	International Rectifier	SAMSUNG Direct Replacement	International Rectifier	SAMSUNG Direct Replacement	International Rectifier	SAMSUNG Direct Replacement	International Rectifier	SAMSUNG Direct Replacement
IRF9532	IRF9532	IRF9642	IRF9640	IRFP240	IRFP240	IRFP430	IRFP430	IRFP9133	IRFP9130
IRF9533	IRF9533	IRF9643	IRF9640	IRFP241	IRFP241	IRFP431	IRFP430	IRFP9140	IRFP9140
IRF9540	IRF9540			IRFP242	IRFP242	IRFP432	IRFP430	IRFP9141	IRFP9141
IRF9541	IRF9541			IRFP243	IRFP243	IRFP433	IRFP430	IRFP9142	IRFP9140
IRF9542	IRF9540			IRFP250	IRFP250	IRFP440	IRFP440	IRFP9143	IRFP9140
IRF9543	IRF9543	IRFP131	IRFP130	IRFP251		IRFP441	IRFP440	IRFP9230	IRFP9230
IRF9610	IRF9610	IRFP132	IRFP130	IRFP252		IRFP442	IRFP440	IRFP9231	IRFP9230
IRF9611	IRF9610	IRFP133	IRFP130	IRFP253		IRFP443	IRFP440	IRFP9232	IRFP9232
IRF9612	IRF9610	IRFP140	IRFP140	IRFP330		IRFP450		IRFP9233	IRFP9230
IRF9613	IRF9610	IRFP141	IRFP141	IRFP331		IRFP451		IRFP9240	IRFP9240
IRF9620	IRF9620	IRFP142	IRFP140	IRFP332	IRFP330	IRFP452	IRFP452	IRFP9241	IRFP9241
IRF9621	IRF9621	IRFP143	IRFP140	IRFP333	IRFP330	IRFP453	IRFP450	IRFP9242	IRFP9242
IRF9622	IRF9622	IRFP150	IRFP150	IRFP340	IRFP340	IRFP9130	IRFP9130	IRFP9243	IRFP9243
IRF9623	IRF9620	IRFP151	IRFP151	IRFP341	IRFP340	IRFP9131	IRFP9130		
IRF9630	IRF9630	IRFP152	IRFP150	IRFP342	IRFP340	IRFP9132	IRFP9130		
IRF9631	IRF9630	IRFP153	IRFP153	IRFP343	IRFP340				
IRF9632	IRF9630	IRFP230	IRFP230	IRFP350	IRFP350				
IRF9633	IRF9630	IRFP231	IRFP230	IRFP351	IRFP351				
IRF9640	IRF9640	IRFP232	IRFP230	IRFP352	IRFP350				
IRF9641	IRF9640	IRFP233	IRFP230	IRFP353	IRFP350				

Motorola	SAMSUNG Direct Replacement	Motorola	SAMSUNG Direct Replacement	Motorola	SAMSUNG Direct Replacement	Motorola	SAMSUNG Direct Replacement	Motorola	SAMSUNG Direct Replacement
MTH6N55	SSH6N60	MTM7N12	IRF230	MTM12N20	IRF242	MTP2N35	IRF723	MTP8N08	IRF520
MTH6N60	SSH6N60	MTM7N15	IRF230	MTM15N05	IRF140	MTP2N40	IRF720	MTP8N10	IRF520
MTH8N55	SSH8N60	MTM1N18	IRF232	MTM15N06	IRF140	MTP2N45	IRF823	MTP8N12	IRF630
MTH8N60	SSH8N60	MTM7N20	IRF232	MTM15N12	IRF243	MTP2N50	IRF822	MTP8N15	IRF630
MTH7N35	IRFP340	MTM7N45	IRF440	MTM15N15	IRF243	MTP2N55	N/A	MTP8N18	IRF632
MTH7N40	IRFP340	MTM7N50	IRF440	MTM15N18	IRF242	MTP2N60	N/A	MTP8N20	IRF632
MTH8N35	IRFP340	MTM8N08	IRF120	MTM15N20	IRF242	MTP3N12	IRF620	MTP8P08	IRF9532
MTH8N40	IRFP340	MTM8N10	IRF120	MTM15N35	IRF351	MTP3N15	IRF620	MTP8P10	IRF9532
MTH15N18	IRFP242	MTM8N12	IRF230	MTM15N40	IRF350	MTP3N18	IRF620	MTP10N05	IRF533
MTH15N20	IRFP242	MTM8N15	IRF230	MTM15N45	SSM20N50	MTP3N20	IRF620	MTP10N06	IRF533
MTH20N12	IRFP253	MTM8N18	IRF232	MTM15N50	SSM20N50	MTP3N35	IRF720	MTP10N08	IRF532
MTH20N15	IRFP253	MTM8N20	IRF232	MTM20N08	IRF140	MTP3N40	IRF720	MTP10N10	IRF532
MTH25N08	IRFP140	MTM8N35	IRF340	MTM20N10	IRF140	MTP3N55	N/A	MTP10N12	IRF640
MTH25N10	IRFP140	MTM8N40	IRF340	MTM20N12	IRF253	MTP3N60	SSP4N60	MTP10N15	IRF640
MTH35N05	IRFP151	MTM8P08	IRF9132	MTM20N15	IRF253	MTP4N08	IRF510	MTP10N25	IRF740
MTH35N06	IRFP151	MTM8P10	IRF9132	MTM25N05	IRF141	MTP4N10	IRF510	MTP12N05	IRF533
MTM2N45	IRF420	MTM10N05	IRF133	MTM25N06	IRF141	MTP4N12	IRF620	MTP12N06	IRF533
MTM2N50	IRF420	MTM10N06	IRF133	MTM25N08	IRF140	MTP4N15	IRF620	MTP12N08	IRF532
MTM3N35	IRF320	MTM10N08	IRF130	MTM25N10	IRF140	MTP4N45	IRF830	MTP12N10	IRF532
MTM3N40	IRF320	MTM10N10	IRF130	MTM35N05	IRF151	MTP4N50	IRF832	MTP12N18	IRF642
MTM3N55	N/A	MTM10N12	IRF243	MTM35N06	IRF151	MTP5N05	IRF523	MTP12N20	IRF642
MTM3N60	SSM4N60	MTM10N15	IRF243	MTM40N18	N/A	MTP5N06	IRF523	MTP15N05	IRF543
MTM4N45	IRF430	MTM10N25	IRF350	MTM40N20	N/A	MTP5N18	IRF620	MTP15N06	IRF543
MTM4N50	IRF430	MTM12N05	IRF133	MTP1N45	IRF823	MTP5N20	IRF620	MTP15N12	IRF643
MTM5N18	IRF220	MTM12N06	IRF133	MTP1N50	IRF822	MTP5N35	IRF731	MTP15N15	IRF640
MTM5N20	IRF220	MTM12N08	IRF130	MTP1N55	N/A	MTP5N40	IRF730	MTP20N08	IRF542
MTM5N35	IRF330	MTM12N10	IRF130	MTP1N60	N/A	MTP7N12	IRF630	MTP20N20	IRF542
MTM5N40	IRF330	MTM12N12	IRF243	MTP2N18	IRF612	MTP7N15	IRF630	MTP25N05	IRF541
MTM6N55	N/A	MTM12N15	IRF243	MTP2N20	IRF612	MTP7N18	IRF630	MTP25N06	IRF541
MTM6N60	SSM6N60	MTM12N18	IRF242	MTP2N25	IRF723	MTP7N20	IRF630		

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CROSS REFERENCE GUIDE (Continued)

RCA	SAMSUNG Direct Replacement	RCA	SAMSUNG Direct Replacement	RCA	SAMSUNG Direct Replacement	RCA	SAMSUNG Direct Replacement	RCA	SAMSUNG Direct Replacement
RCA9192A	IRF120	RFK35N08	IRF150	RFM12N18	IRF242	RFP3N45	IRF820	RFP8N10	IRF9532
RCA9192B	IRF243	RFK35N10	IRF150	RFM12N20	IRF242	RFP3N50	IRF820	RFP10N12	IRF640
RCA9195A	IRF140	RFM3N45	IRF421	RFM15N05	IRF140	RFP4N05	IRF513	RFP10N15	IRF640
RCA9195B	IRF253	RFM3N50	IRF420	RFM15N06	IRF140	RFP4N06	IRF513	RFP10P12	IRF9532
RCA9212A	IRF520	RFM4N35	IRF320	RFM15N12	IRF253	RFP4N35	IRF720	RFP12N08	IRF530
RCA9212B	IRF640	RFM4N40	IRF320	RFM15N15	IRF253	RFP4N40	IRF720	RFP12N10	IRF530
RCA9213A	IRF512	RFM5P12	IRF9230	RFM18N08	IRF140	RFP5P12	IRF9630	RFP12N20	IRF642
RCA9213B	IRF610	RFM5P15	IRF9230	RFM18N10	IRF140	RFP5P15	IRF9630	RFP15N05	IRF543
RCA9230A	IRF542	RFM6P08	IRF9132	RFM25N05	IRF141	RFP6P08	IRF9520	RFP15N06	IRF543
		RFM6P10	IRF9230	RFM25N06	IRF141	RFP6P10	IRF9520	RFP15N12	IRF640
RFK15N35	IRF350	RFM7N45	IRF430	RFP1N35	IRF710	RFP7N45	IRF831	RFP18N10	IRF542
RFK15N40	IRF350	RFM7N50	IRF430	RFP1N40	IRF710	RFP7N50	IRF830	RFP25N05	IRF541
RFK15N45	IRF440	RFM8N18	IRF230	RFP2N08	IRF512	RFP8N18	IRF630		
RFK15N50	IRF440	RFM8N20	IRF230	RFP2N10	IRF512	RFP8N20	IRF630		
RFK20P08	IRF9140	RFM8P08	IRF9132	RFP2N12	IRF610	RFP8N08	IRF9532		
RFK20P10	IRF9140	RFM8P10	IRF9132	RFP2N15	IRF610				
RFK25N18	IRF252	RFM10N12	IRF243	RFP2N18	IRF612				
RFK25N20	IRF252	RFM10N15	IRF243	RFP2N20	IRF612				
RFK30N12	IRF251	RFM10P12	IRF9240	RFP2P08	IRF9512				
RFK30N15	IRF251	RFM10P15	IRF9240	RFP2P10	IRF9512				

Siemens	SAMSUNG Direct Replacement	Siemens	SAMSUNG Direct Replacement	Siemens	SAMSUNG Direct Replacement	Siemens	SAMSUNG Direct Replacement	Siemens	SAMSUNG Direct Replacement
BUZ10	IRF541	BUZ25	IRF140	BUZ237	IRFP242	BUZ45A	IRF452	BUZ63B	IRF330
BUZ10A	IRF543	BUZ27	IRFP140	BUZ38	IRFP240	BUZ45B	IRF452	BUZ63C	IRF330
BUZ10B	IRF533	BUZ28	IRFP141	BUZ382	IRFP350	BUZ45C	IRF453	BUZ63D	IRF320
BUZ11A	IRF541	BUZ31	IRF640	BUZ385	IRFP440	BUZ46	IRF430	BUZ64	IRF350
BUZ14A	IRF151	BUZ32	IRF630	BUZ41	IRF840	BUZ46A	IRF433	BUZ64A	IRF350
BUZ14B	IRF153	BUZ32A	IRF630	BUZ41A	IRF830	BUZ46B	IRF420	BUZ67	IRFP340
BUZ17	IRF153	BUZ32B	IRF632	BUZ41B	IRF831	BUZ48	IRFP450	BUZ71	IRF541
BUZ18	IRF151	BUZ32C	IRF633	BUZ42	IRF832	BUZ48A	IRFP452	BUZ71A	IRF543
BUZ20	IRF530	BUZ34	IRF240	BUZ42A	IRF830	BUZ60	IRF730	BUZ72A	IRF532
BUZ20A	IRF532	BUZ35	IRF230	BUZ42B	IRF820	BUZ60A	IRF730	BUZ73A	IRF632
BUZ20B	IRF520	BUZ35A	IRF230	BUZ42C	IRF820	BUZ60B	IRF730	BUZ74	IRF820
BUZ201	IRF353	BUZ351	IRFP350	BUZ44	IRF420	BUZ60C	IRF730	BUZ74A	IRF822
BUZ21	IRF540	BUZ353	IRFP450	BUZ44A	IRF430	BUZ60D	IRF720	BUZ76	IRF720
BUZ211	IRF452	BUZ354	IRFP450	BUZ44B	IRF430	BUZ63	IRF330	BUZ76A	IRF720
BUZ23	IRF130	BUZ36	IRF252	BUZ45	IRF452	BUZ63A	IRF331		
BUZ23A	IRF130								
BUZ23B	IRF120								
BUZ24	IRF150								
BUZ24A	IRF150								
BUZ24B	IRF150								

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CROSS REFERENCE GUIDE (Continued)

Siliconix	SAMSUNG Direct Replacement	Siliconix	SAMSUNG Direct Replacement	Siliconix	SAMSUNG Direct Replacement	Siliconix	SAMSUNG Direct Replacement	Siliconix	SAMSUNG Direct Replacement
VN30AA	IRF123	VN0215N5	IRF610	VN1115N5	IRF610	VN4000D	IRF730	VP0335N1	IRF9230
VN33AJ	IRF123	VN0216N1	IRF220	VN1116N1	IRF220	VN4001A	IRF330	VP0335N5	IRF9610
VN35AA	IRF123	VN0216N5	IRF612	VN1116N5	IRF612	VN4001D	IRF730	VP0340N1	IRF9230
VN35AJ	IRF123	VN0220N1	IRF220	VN1120N1	IRF220	VN4002A	IRF320	VP0340N5	IRF9610
VN40AD	IRF513	VN0220N5	IRF612	VN1120N5	IRF612	VN4501A	IRF430	VP0345N1	IRF9230
VN46AD	IRF513	VN0300D	IRF513	VN1200A	IRF241	VN4501D	IRF831	VP0345N5	IRF9610
VN64AG	IRF123	VN0330N1	IRF323	VN1200D	IRF641	VN4502A	IRF430	VP1102N1	IRF9130
VN66AD	IRF513	VN0330N5	IRF723	VN1201A	IRF243	VN4502D	IRF830	VP1102N5	IRF9523
VN66AJ	IRF123	VN0335N1	IRF323	VN1201D	IRF640	VN5001A	IRF430	VP1103N1	IRF9130
VN67AA	IRF123	VN0335N5	IRF723	VN1202N1	IRF133	VN5001D	IRF830	VP1103N5	IRF9523
VN67AD	IRF513	VN0340N1	IRF320	VN1202N5	IRF533	VN5002A	IRF430	VP1104N1	IRF9130
VN67AJ	IRF123	VN0340N5	IRF720	VN1203N1	IRF133	VN5002D	IRF832	VP1104N5	IRF9513
VN88AD	IRF512	VN0345A1	IRF440	VN1203N5	IRF533	VNL001A	IRF331	VP1106N1	IRF9130
VN89AA	IRF122	VN0345N1	IRF420	VN1204N1	IRF123	VNM001A	IRF330	VP1106N5	IRF9513
VN89AD	IRF512	VN0345N5	IRF820	VN1204N5	IRF523	VNM002A	IRF430	VP1109N1	IRF9132
VN90AA	IRF122	VN0350A1	IRF440	VN1206D	IRF610	VNP002A	IRF430	VP1109N5	IRF9512
VN98AJ	IRF122	VN0350N1	IRF420	VN1206N1	IRF123	VNS008A	SSM6N60	VP1110N1	IRF9132
VN99AA	IRF122	VN0355N1	N/A	VN1206N5	IRF523	VNS008D	SSP6N60	VP1110N5	IRF9512
VN99AJ	IRF122	VN0360N1	SSM4N60	VN1208N1	IRF122	VNS009A	SSM5N60	VP1114N1	IRF9230
VN0102N1	IRF123	VN0400A	IRF140	VN1208N5	IRF522	VNS009D	SSP5N60	VP1114N5	IRF9610
VN0102N5	IRF513	VN0400D	IRF543	VN1209N1	IRF122	VNT008A	SSM6N70	VP1115N1	IRF9230
VN0103N1	IRF123	VN0401A	IRF140	VN1209N5	IRF522	VNT008D	SSP6N70	VP1115N5	IRF9610
VN0103N5	IRF513	VN0401D	IRF543	VN1210N1	IRF122	VNT009A	SSM6N70	VP1116N1	IRF9230
VN0104N1	IRF123	VN0430N1	IRF340	VN1210N5	IRF522	VNT009D	SSP6N70	VP1116N5	IRF9610
VN0104N5	IRF513	VN0435N1	IRF340	VN1215N1	IRF230	VP0102N5	IRF9513	VP1120N1	IRF9230
VN0106N1	IRF123	VN0440N1	IRF340	VN1215N5	IRF633	VP0103N5	IRF9513	VP1120N5	IRF9610
VN0106N5	IRF513	VN0445N1	IRF453	VN1216N1	IRF222	VP0104N5	IRF9513	VP1202N1	IRF9130
VN0108N1	IRF122	VN0450N1	IRF440	VN1216N5	IRF610	VP0106N5	IRF9513	VP1202N5	IRF9533
VN0108N5	IRF512	VN0600A	IRF140	VN1220N1	IRF222	VP0108N1	IRF9132	VP1203N1	IRF9130
VN0109N1	IRF122	VN0600D	IRF543	VN1220N5	IRF610	VP0108N5	IRF9512	VP1203N5	IRF9533
VN0109N5	IRF512	VN0601A	IRF140	VN1706D	IRF612	VP0109N1	IRF9132	VP1204N1	IRF9130
VN0110N1	IRF122	VN0601D	IRF543	VN2306N1	IRF141	VP0109N5	IRF9512	VP1204N5	IRF9523
VN0110N5	IRF512	VN0800A	IRF130	VN2306N5	IRF541	VP0110N5	IRF9512	VP1206N1	IRF9130
VN0114N1	IRF223	VN0800D	IRF530	VN2310N1	IRF140	VP0114N5	IRF9610	VP1206N5	IRF9523
VN0114N5	IRF610	VN0801A	IRF130	VN2310N5	IRF540	VP0202N1	IRF9130	VP1208N1	IRF9132
VN0116N1	IRF220	VN0801D	IRF532	VN2315N1	IRF241	VP0202N5	IRF9513	VP1208N5	IRF9520
VN0116N5	IRF612	VN1000A	IRF130	VN2315N5	IRF641	VP0203N1	IRF9130	VP1209N1	IRF9132
VN0120N1	IRF220	VN1000D	IRF530	VN2320N1	IRF242	VP0203N5	IRF9513	VP1209N5	IRF9520
VN0120N5	IRF612	VN1001A	IRF130	VN2320N5	IRF642	VP0204N1	IRF9130	VP1210N1	IRF9132
VN0202N1	IRF123	VN1001D	IRF532	VN2330N1	IRF341	VP0204N5	IRF9513	VP1210N5	IRF9520
VN0202N5	IRF513	VN1102N1	IRF123	VN2330N5	IRF741	VP0206N1	IRF9130	VP1215N1	IRF9230
VN0203N1	IRF123	VN1102N5	IRF523	VN2335N1	IRF341	VP0206N5	IRF9513	VP1215N5	IRF9621
VN0203N5	IRF513	VN1103N1	IRF123	VN2335N5	IRF741	VP0208N1	IRF9132	VP1216N1	IRF9230
VN0204N1	IRF123	VN1103N5	IRF523	VN2340N1	IRF340	VP0208N5	IRF9512	VP1216N5	IRF9610
VN0204N5	IRF513	VN1104N1	IRF123	VN2340N5	IRF740	VP0209N1	IRF9132	VP1220N1	IRF9230
VN0206N1	IRF123	VN1104N5	IRF523	VN2345N1	IRF453	VP0209N5	IRF9512	VP1220N5	IRF9610
VN0206N5	IRF513	VN1106N1	IRF123	VN2350N1	IRF440	VP0210N1	IRF9132	ZVN0102L	IRF513
VN0208N1	IRF122	VN1106N5	IRF523	VN2350N5	IRF840	VP0210N5	IRF9512	ZVN0106L	IRF513
VN0208N5	IRF512	VN1109N1	IRF122	VN2406D	IRF710	VP0214N1	IRF9230	ZVN0108L	IRF512
VN0209N1	IRF122	VN1109N5	IRF522	VN3500A	IRF331	VP0214N5	IRF9610		
VN0209N5	IRF512	VN1110N1	IRF122	VN3500D	IRF731	VP0215N5	IRF9610		
VN0210N1	IRF122	VN1110N5	IRF522	VN3501A	IRF330	VP0216N1	IRF9230		
VN0210N5	IRF512	VN1114N1	IRF220	VN3501D	IRF730	VP0216N5	IRF9610		
VN0214N1	IRF220	VN1114N5	IRF611	VN3502A	IRF320	VP0220N1	IRF9230		
VN0214N5	IRF610	VN1115N1	IRF223	VN4000A	IRF330	VP0220N5	IRF9610		

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MOSFET SELECTION GUIDE (N/P CHANNEL)

BV_{DSS} (V)	I_D (A)	$R_{DS(on)}$ (Ω)	TO-3	TO-220	TO-3P	TO-247 FULL PACK
N-CHANNEL						
50	10.00	.28	SSM10N05	—	—	—
50	12.00	.20	—	SSP12N05	SSH12N05	—
60	3.50	.80	—	IRF513	—	—
60	4.00	.60	—	IRF511	—	—
60	7.00	.40	IRF123	IRF523	IRFP123	—
60	8.00	.30	IRF121	IRF521	IRFP121	—
60	10.00	.28	SSM10N06	SSP10N06	—	—
60	12.00	.25	IRF133	IRF533	IRFP133	—
60	14.00	.18	—	IRF531	IRFP131	—
60	24.00	.11	—	IRF543	IRFP143	—
60	27.00	.085	IRF141	IRF541	IRFP141	—
60	33.00	.08	IRF153	—	IRFP153	—
60	40.00	.055	IRF151	SSP40N06	IRFP151	—
80	10.00	.33	—	SSP10N08	SSH10N08	—
80	12.00	18.00	SSM12N08	SSP12N08	—	—
100	3.50	.80	—	IRF512	—	—
100	4.00	.60	—	IRF510	—	—
100	7.00	.40	IRF122	IRF522	IRFP122	—
100	8.00	.30	IRF120	IRF520	IRFP120	—
100	10.00	.33	—	—	SSH10N10	—
100	12.00	.25	—	IRF532	IRFP132, SSH12N10	—
100	14.00	.18	IRF130	IRF530	IRFP130	IRFS130
100	24.00	.11	—	IRF542	IRFP142	—
100	27.00	.085	IRF140	IRF540	IRFP140	IRFS140
100	33.00	.08	—	—	IRFP152	—
100	40.00	.055	IRF150	—	IRFP150	IRFS150
120	7.00	.70	SSM7N12	—	—	—
120	8.00	.50	SSM8N12	—	SSH8N12	—
150	4.00	1.20	—	—	IRFP223	—
150	5.00	.80	—	—	IRFP221	—
150	7.00	.70	—	—	SSH7N15	—
150	8.00	.60	—	—	IRFP233	—
150	8.00	.50	—	—	SSH8N15	—
150	9.00	.40	SSM8N15	—	IRFP231	—
150	16.00	.22	IRF243	—	IRFP243	—
150	18.00	.18	IRF241	IRF641	IRFP241	—
150	25.00	.12	IRF253	—	IRFP253	—
150	30.00	.085	IRF251	—	IRFP251	—
180	7.00	.70	—	—	SSH7N18	—
180	8.00	.50	SSM8N18	—	—	—
200	2.00	2.40	—	IRF612	—	—
200	2.50	1.50	—	IRF610	—	—
200	4.00	1.20	SSM40N20	—	IRFP222, SSH40N20	—
200	5.00	.80	IRF220	IRF620	IRFP220	—
200	7.00	.70	SSM7N20	—	—	—
200	8.00	.60	IRF232	IRF632	IRFP232, SSH8N20	—
200	9.00	.40	IRF230	IRF630	IRFP230	IRFS230
200	16.00	.22	IRF242	IRF642	IRFP242	—
200	18.00	.18	IRF240	IRF640	IRFP240	IRFS240
200	25.00	.12	IRF252	—	IRFP252	—
200	30.00	.085	IRF250	—	IRFP250	IRFS250
200	40.00	.05	SSM40N20	—	—	SSS40N20
350	1.50	3.60	—	IRF711	—	—
350	2.50	2.50	IRF323	IRF723	IRFP323	—
350	3.00	1.80	—	—	IRFP321	—
350	5.00	1.50	—	SSP5N35	IRFP333	—
350	5.50	1.00	IRF331	IRF731	IRFP331	—
350	8.00	.80	—	—	IRFP343	—
350	10.00	.55	—	IRF741	IRFP341	—
350	13.00	.40	—	—	IRFP353	—
350	15.00	.30	IRF351	—	IRFP351	—
350	25.00	.20	SSM25N35	—	—	—
400	2.50	2.50	—	—	IRFP322	—
400	3.00	1.80	IRF320	IRF720	IRFP320	—
400	5.00	1.50	—	—	IRFP332	—

BV_{DSS} (V)	I_D (A)	$R_{DS(on)}$ (Ω)	TO-3	TO-220	TO-3P	TO-247 FULL PACK
N-CHANNEL						
400	5.00	1.00	IRF330	—	IRFP332	IRFS330
400	5.50	1.00	—	IRF730	—	—
400	8.00	.80	—	IRF742	IRFP342	—
400	10.00	.55	IRF340	IRF740	IRFP340	—
400	13.00	.40	—	—	IRFP352	—
400	15.00	.30	IRF350	—	IRFP350	IRFS350
400	25.00	.40	SSM25N40	—	SSH25N40	SSS25N40
450	2.00	4.0	—	IRF823	IRFP423	—
450	2.50	3.00	—	—	IRFP421	—
450	4.00	2.00	—	SSP4N50	IRFP433, SSH4N45	—
450	4.50	1.50	—	IRF831	IRFP431	—
450	7.00	1.10	—	—	IRFP443	—
450	8.00	0.85	—	IRF841	IRFP441	—
450	12.00	.50	IRF453	—	IRFP453	—
450	13.00	.40	IRF451	—	IRFP451	—
450	20.00	.30	—	—	—	—
500	2.00	4.00	—	IRF822	IRFP422, SSH4N50	—
500	2.50	30.00	—	IRF820	IRFP420	—
500	4.00	2.00	—	IRF831	IRFP432	—
500	4.50	1.50	—	IRF830	IRFP430	IRFS430
500	7.00	1.10	—	—	IRFP442	—
500	8.00	.85	—	IRF840	IRFP440	IRFS440
500	12.00	.50	—	IRF452	IRFP452	—
500	13.00	.40	IRF450	—	IRFP450	IRFS450
500	20.00	.30	SSM20N50	—	SSH20N50	SSS20N50
550	2.00	3.00	—	SSP2N55	—	—
550	4.00	3.00	—	—	SSH4N55	—
550	8.00	1.00	—	—	SSH8N55	SSS8N50
550	10.00	.50	SSM10N55	—	SSH15N55	—
550	15.00	.50	SSM15N55	—	SSH15N55	—
600	4.00	3.00	SSM4N60	SSP4N60	—	—
600	6.00	1.80	SSM6N60	SSP6N60	SSH6N60	SSS6N60
600	8.00	1.00	SSM8N60	—	SSH8N60	—
600	15.00	.50	SSM15N60	—	SSH15N60	—
700	3.00	6.00	—	SSP3N70	—	—
700	4.00	3.30	SSM4N70	SSP4N70	SSH4N70	SSS4N70
700	6.00	1.90	SSM6N70	SSP6N70	SSH6N70	SSS6N70
700	10.00	.80	SSM10N70	—	SSH10N70	SSS10N70
P-CHANNEL						
-60	-2.50	1.6	—	IRF9513	—	—
-60	-3.00	1.2	—	IRF9511	—	—
-60	-5.00	.80	—	IRF9523	—	—
-60	-6.00	.60	—	IRF9521	—	—
-60	-10.00	.40	—	IRF9533	—	—
-60	-12.0	.30	IRF9131	IRF9531	—	—
-60	-15.0	.30	—	IRF9543	—	—
-60	-19.00	.20	—	IRF9541	IRF9141	—
-100	-2.50	1.60	—	IRF9512	—	—
-100	-3.00	1.20	—	IRF9510	—	—
-100	-6.00	.60	IRF9120	IRF9520	IRFP9120	—
-100	-10.00	.40	—	IRF9532	—	—
-100	-12.00	.30	IRF9130	IRF9530	IRFP9130	—
-100	-19.00	.20	IRF9140	IRF9540	IRFP9140	—
-150	-4.00	.50	—	—	IRFP241	—
-150	-5.50	1.20	—	—	—	—
-150	-9.00	.70	IRF9243	—	IRFP9243	—
-200	-1.75	3.00	—	IRF9610	—	—
-200	-3.00	2.40	—	IRF9622	—	—
-200	-3.50	1.50	—	—	IRFP9220	—
-200	-4.00	.50	—	—	IRFP9240	—
-200	-5.50	1.20	—	—	IRF9232	—
-200	-6.50	.80	IRF9230	IRF9630	IRFP9230	—
-200	-9.00	.70	—	—	IRFP9242	—
-200	-11.00	.50	IRF9240	IRF9640	—	—

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Transistor
Selection Guide

TO-92 Type J-FET

DEVICE	V_{GDO} (V)	I_G (mA)	P_D (mW)	I_{DSS} (mA)			gm (mS)			$V_{GS(OFF)}$ (V)			
				MIN	MAX	V_{DS} (V)	MIN	TYP	V_{DS} (V)	V_{DS} (V)	I_D (μA)	MIN	MAX
KSK30	50	10	100	0.3	6.5	10	1.2		10	10	0.1	0.4	5
KSK117	50	10	300	0.6	14	10	4	15	10	10	0.1	0.2	1.5

Power Transistor Selection Guide

I_C Cont Amps Max	V_{CBO} Volts Min	V_{CEO} Volts Min	Polarity NPN	Polarity PNP	h_{FE} Min	h_{FE} Max	at I_C Amp	t_S μs Max	t_F μs Max	at I_C Amp	f_T MHz Min	P_D Watts at 25°C	Package
0.1	180	180	KSC2682	KSA1142	160	320	0.01				*200	8	TO-126
0.2	300	300	KSC2688		40	250	0.01				50	10	TO-126
0.5	300	300	MJE340	MJE350	30	240	0.05					20	TO-126
	375	350	2N5657		30	250	0.1				10	20	TO-126
	500	400	KSC2752		20	80	0.05	2.5	1	0.3		10	TO-126
1	40	40	TIP29	TIP30	15	75	1				3	30	TO-220
	60	60	TIP29A	TIP30A	15	75	1				3	30	TO-220
	80	80	TIP29B	TIP30B	15	75	1				3	30	TO-220
	100	100	TIP29C	TIP30C	15	75	1				3	30	TO-220
	350	250	TIP47		30	150	0.3				10	40	TO-220
	400	300	TIP48		30	150	0.3				10	40	TO-220
	450	350	TIP49		30	150	0.3				10	40	TO-220
	500	400	TIP50		30	150	0.3				10	40	TO-220
1.2	120	120	KSC2690	KSA1220	60	320	0.3				*155	20	TO-126
	160	160	KSC2690A	KSA1220A	60	320	0.3				*155	20	TO-126
2.5	1500	800	KSD5010**		8		0.5		0.4	2	*3	50	TO-3PF
	1500	800	KSD5014		8		0.5		0.4	2	*3	50	TO-3PF
3	30	30	KSC1173	KSA473	70	240	0.5				*100	10	TO-220
	40	30	KSD882	KSB772	60	400	1				*90	10	TO-126
	40	40	TIP31	TIP32	10	50	3				3	40	TO-220
	60	40	MJE180	MJE170	50	250	0.1				50	12.5	TO-126
	70	45	KSD794	KSB744	60	320	0.5				*60	10	TO-126
	60	60	TIP31A	TIP32A	10	50	3				3	40	TO-220
	60	60	KSD880	KSB834	60	320	0.5				*3	30	TO-220
	70	60	KSD794A	KSB744A	60	320	0.5				*45	10	TO-126
	80	60	KSC1983		500		0.5				*15	30	TO-220
	80	60	MJE181	MJE171	50	250	0.1				50	12.5	TO-126
	80	80	TIP31B	TIP32B	10	50	3				3	40	TO-220
	100	80	MJE182	MJE172	50	250	0.1				50	12.5	TO-126
3.5	1500	800	KSD5011**		8		0.5		0.4	3	*3	50	TO-3PF
	1500	800	KSD5015		8		0.5		0.4	3	*3	50	TO-3PF
4	200	60	KSC2233		30	150	1				*10	40	TO-220
	80	80	KSD526	KSB596	40	240	0.5				3	30	TO-220
5	40	25	MJE200	MJE210	45	180	2				60	15	TO-126
	100	60	KSD73		70	240	1				*20	30	TO-220
	150	70	KSD362		20	140	5				*10	40	TO-220
	150	100	KSC2517		40	200	2	2.5	0.5	3		30	TO-220
	1500	800	KSD5012**		8		1		0.4	4	*3	60	TO-3PF
	1500	800	KSD5016		8		1		0.4	4	*3	60	TO-3PF

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Power Transistor Selection Guide (Continued)

I_C Cont Amps Max	V_{CBO} Volts Min	V_{CEO} Volts Min	Polarity NPN	Polarity PNP	h_{FE} Min	h_{FE} Max	at I_C Amp	t_S μs Max	t_F μs Max	at I_C Amp	f_T MHz Min	P_D Watts at 25°C	Package
6	40	40	TIP41	TIP42	15	75	3				3	65	TO-220
	60	60	TIP41A	TIP42A	15	75	3				3	65	TO-220
	80	80	TIP41B	TIP42B	15	75	3				3	65	TO-220
	100	100	TIP41C	TIP42C	15	75	3				3	65	TO-220
	1500	800	KSD5013**		8		1		0.4	4	*3	60	TO-3PF
	1500	800	KSD5017		8		1		0.4	4	*3	60	TO-3PF
7	100	60	KSD568	KSB707	40	200	3					40	TO-220
	100	80	KSD569	KSB708	40	200	3					40	TO-220
	150	100	KSC2334	KSA1010	40	240	3	1.5	0.5	5		40	TO-220
	500	400	KSC2335		20	80	1	2.5	1	3		40	TO-220
10	70	60	MJE3055T	MJE2955T	20	100	4				2	75	TO-220
	500	400	KSC2749#		7		6	2.5	0.7	6		100	TO-3PF
15	500	400	KSC2751#		7		10	2.5	0.7	10		120	TO-3PF

Darlington Power Transistor Selection Guide

I_C Cont Amps Max	V_{CBO} Volts Min	V_{CEO} Volts Min	Polarity NPN	Polarity PNP	h_{FE} Min	h_{FE} Max	at I_C Amp	t_S μs Max	t_F μs Max	at I_C Amp	f_T MHz Min	P_D Watts at 25°C	Package
1.5	150	60	KSD985	KSB794	2K	30K	1	1	1	1		10	TO-126
	150	80	KSD986	KSB795	2K	30K	1	1	1	1		10	TO-126
2	60	60	TIP110	TIP115	1K		1					50	TO-220
	80	80	TIP111	TIP116	1K		1					50	TO-220
	100	100	TIP112	TIP117	1K		1					50	TO-220
4	60	60	MJE800	MJE700	750		1.5					40	TO-126
	60	60	MJE801	MJE701	750		2					40	TO-126
	80	80	MJE802	MJE702	750		1.5					40	TO-126
	80	80	MJE803	MJE703	750		2					40	TO-126
5	60	60	TIP120	TIP125	1K		3					65	TO-220
	80	80	TIP121	TIP126	1K		3					65	TO-220
	100	100	TIP122	TIP127	1K		3					65	TO-220
	150	100	KSD560	KSB601	2K	15K	3	*3.5	*1.2	3		30	TO-220
8	60	60	TIP100	TIP105	1K	20K	3					80	TO-220
	80	80	TIP101	TIP106	1K	20K	3					80	TO-220
	100	100	TIP102	TIP107	1K	20K	3					80	TO-220
	330	150	BU807		100		5	*0.55	*0.2	5		60	TO-220
	400	200	BU806		100		5	*0.55	*0.2	5		60	TO-220
10	60	60	TIP140F	TIP145F	1K		5	2.5	2.5	5		125	TO-3PF
	60	60	TIP140T	TIP145T	1K		5	2.5	2.5	5		125	TO-220
	80	80	TIP141F	TIP146F	1K		5	2.5	2.5	5		125	TO-3PF
	80	80	TIP141T	TIP146T	1K		5	2.5	2.5	5		125	TO-220
	100	100	TIP142F	TIP147F	1K		5	2.5	2.5	5		125	TO-3PF
	100	100	TIP142T	TIP147T	1K		5	2.5	2.5	5		125	TO-220

* Typ
** Damper Diode Built-in Transistor
\# Available 4Q'88

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Major Transistors List

TO-92	
2N3904	MPS5172
2N3906	MPS5179
2N4123	MPS6520
2N4124	MPS8098
2N4125	MPS8099
2N4126	MPS8598
2N4400	MPS8599
2N4401	MPSA05
2N4402	MPSA06
2N4403	MPSA14
2N5086	MPSA20
2N5087	MPSA42
2N5088	MPSA43
2N5089	MPSA55
2N5210	MPSA56
2N5400	MPSA70
2N5401	MPSA92
2N5550	MPSA93
2N5551	MPSH10
2N6427	MPSH17
2N6428	MPSH20
2N6515	MPSH24
2N6517	PN2222A
2N6520	PN2907A

SOT-23	
BCX70G	MMBTA20
BCX71G	MMBTA42
MMBR5179	MMBTA43
MMBT2222A	MMBTA55
MMBT2484	MMBTA56
MMBT2907A	MMBTA63
MMBT3904	MMBTA64
MMBT3906	MMBTA70
MMBT4123	MMBTA92
MMBT4124	MMBTA93
MMBT4125	MMBTH10
MMBT4126	MMBTH17
MMBT4401	MMBTH24
MMBT4403	
MMBT5087	
MMBT5088	
MMBT5089	
MMBT5401	
MMBT5550	
MMBT6428	
MMBTA05	
MMBTA06	
MMBTA13	
MMBTA14	

TIP Series		
TIP29	TIP47	TIP141F
TIP29A	TIP48	TIP141T
TIP29B	TIP49	TIP142F
TIP29C	TIP50	TIP142T
TIP30	TIP100	TIP145F
TIP30A	TIP101	TIP145T
TIP30B	TIP102	TIP146F
TIP30C	TIP105	TIP146T
TIP31	TIP106	TIP147F
TIP31A	TIP107	TIP147T
TIP31B	TIP110	
TIP31C	TIP111	
TIP32	TIP112	
TIP32A	TIP115	
TIP32B	TIP116	
TIP32C	TIP117	
TIP41	TIP120	
TIP41A	TIP121	
TIP41B	TIP122	
TIP41C	TIP125	
TIP42	TIP126	
TIP42A	TIP127	
TIP42B	TIP140F	
TIP42C	TIP140T	

MJE Series
MJE170
MJE171
MJE172
MJE180
MJE181
MJE182
MJE200
MJE210
MJE340
MJE350
MJE700
MJE701
MJE702
MJE703
MJE800
MJE801
MJE802
MJE803
MJE2955T
MJE3055T

Ordering Information

	TO-92/TO-92L	SOT-23
Tape & Reel		
Availability	Now	Now
Mininum Quantity	2000 per reel	3000 per reel
Suffix	2N3904-T&R	MMBT3904-T1
Increment	2000 pcs	3000 pcs
Ammo Pack		
Availability	Now	N/A
Minimum Quantity	2000 per reel	
Suffix	2N3904-AMPK	
Increment	2000 pcs	
Bulk		
Availability	Now	Samples Only
Minimum Quantity	2000 pcs	
Suffix	2N3904	MMBT3904
Increment	2000 pcs	

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Surface Mount Device
Selection Guide

SOT-23 Transistors

General Purpose, High Voltage, High Frequency and Darlington Transistor

Type	V_{CBO} Volts	V_{CEO} Volts	I_C mA	P_D mw	h_{FE} Min/Max at I_C/V_{CE}	mA/Volts	$V_{CE(Sat)}$ Max at I_C/I_B Volts	mA	f_T MHz min	Marking
BCX70G	45	45	100	350	120/220	2/5	0.35	10/0.25	125	AG
BCX71G	45	45	100	350	120/220	2/5	0.25	10/0.25		BG
MMBR5179	20	12	50	350	25/	3/1	0.4	10/1	900	7H
MMBT2222A	75	40	600	350	100/300	150/10	0.3	150/15	300	1P
MMBT2484	60	60	50	350	/800	10/5	0.35	1/0.1	15	1U
MMBT2907A	60	60	600	350	100/300	150/10	0.4	150/15	200	2F
MMBT3904	60	40	200	350	100/300	10/1	0.2	10/1	300	1A
MMBT3906	40	40	200	350	100/300	10/1	0.25	10/1	250	2A
MMBT4123	40	30	200	350	50/150	2/1	0.3	50/5	250	5B
MMBT4124	30	25	200	350	120/360	2/1	0.3	50/5	300	ZC
MMBT4125	30	30	200	350	50/150	2/1	0.4	50/5	200	ZD
MMBT4126	25	25	200	350	120/360	2/1	0.4	50/5	250	C3
MMBT4401	60	40	600	350	100/300	150/1	0.4	150/15	250	2X
MMBT4403	40	40	600	350	100/300	150/1	0.4	150/15	200	2T
MMBT5087	50	50	50	350	250/800	0.1/5	0.3	10/1	40	2Q
MMBT5088	30	35	50	350	300/900	0.1/5	0.5	10/1	50	1Q
MMBT5401	160	150	500	350	60/240	10/5	0.2	10/1	100	2L
MMBT5550	160	140	600	350	60/250	10/5	0.15	10/1	100	1F
MMBT6428	60	50	200	350	250/650	0.1/5	0.2	10/0.5	100	1K
MMBTA05	60	60	500	350	50/	100/1	0.25	100/10	100	1H
MMBTA06	80	80	500	350	50/	100/1	0.25	100/10	100	1G
MMBTA13	30	30	300	350	10K/	100/5	1.5	100/0.1	125	1M
MMBTA14	30	30	300	350	20K/	100/5	1.5	100/0.1	125	1N
MMBTA20	40	40	100	350	40/400	5/10	0.25	10/1	125	1C
MMBTA42	300	300	500	350	40/	30/10	0.5	20/2	50	1D
MMBTA43	200	200	500	350	40/	30/10	0.5	20/2	50	1E
MMBTA55	60	60	500	350	50/	100/1	0.25	100/10	50	2H
MMBTA56	80	80	500	350	50/	100/1	0.25	100/10	50	2G
MMBTA63	30	30	500	350	10K/	100/5	1.5	100/0.1	125	2V
MMBTA64	30	30	500	350	20K/	1000/5	1.5	100/0.1	125	2U
MMBTA70	40	40	100	350	40/400	5/10	0.25	10/1	125	2C
MMBTA92	300	300	500	350	25/	30/10	0.5	20/2	50	2D
MMBTA93	200	200	500	350	25/	20/10	0.5	20/2	50	2E
MMBTH10	30	25	100	350	60/	4/10	0.5	4/0.4	650	3E
MMBTH17	20	15		350	25/250	5/10	0.5	10/1	800	

Digital Transistor

Device and Polarity						Cond		h_{FE}		Cond		V(sat)(V) $V_{CE(SAT)}$		Cond		
NPN	PNP	R1 KΩ	R2 KΩ	V_{CEO} (V)	I_C (mA)	V_{CE} (V)	I_C (mA)	MIN	MAX	I_C (mA)	I_B (mA)	TYP	MAX	V_{CE} (V)	I_C (mA)	f_T(MHz) TYP
KSR1101	KSR2101	4.7	4.7	50	100	5	10	20		10	0.5	0.1	0.3	10	5	250/200
KSR1102	KSR2102	10	10	50	100	5	5	30		10	0.5	0.1	0.3	10	5	250/200
KSR1103	KSR2103	22	22	50	100	5	5	56		10	0.5	0.1	0.3	10	5	250/200
KSR1104	KSR2104	47	47	50	100	5	5	68		10	0.5	0.1	0.3	10	5	250/200

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Linear SOIC

Op Amp, Comparator, Timer

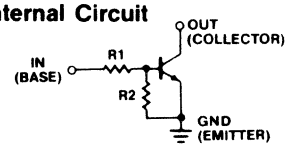
	Op Amp	Comparator	Timer	
			Bipolar	CMOS
Single	LM741CD KA301AD (LM301A)	LM311D	NE555CD	KS555D KS555HD
Dual	MC1458CD MC4558CD LM358D LM358AD	LM393D LM393AD	NE556CD	KS556D
Quad	LM324D LM324AD LM348D MC3403D	LM339D LM339AD	NE558CD	

Interface MC1488D MC1489D MC1489AD **Power Amp** LM386D **Tone Decoder** LM567CD

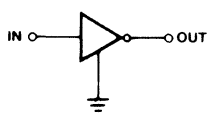
Digital Transistor

Save cost and space by 50% or more. Digital transistor is a bias resistors built-in device that helps making circuits designs simple, especially in the area where the logic circuits are being interfaced to electromechanical system.

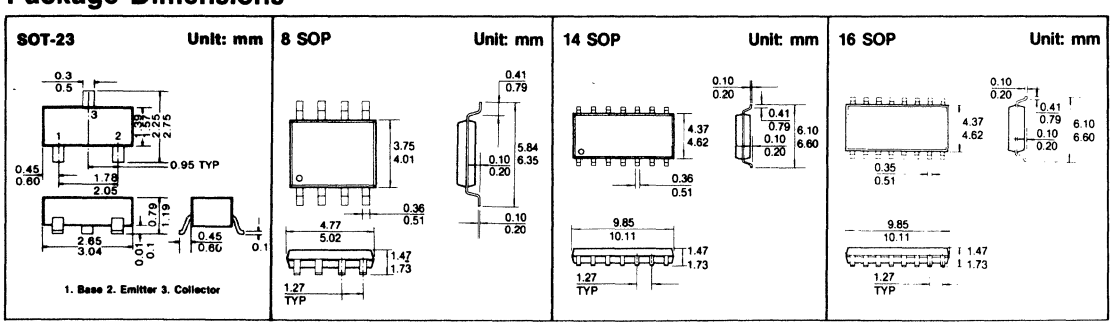
Internal Circuit



Function



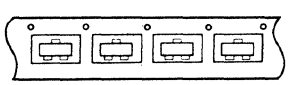
Package Dimensions



SOT-23 Ordering Information

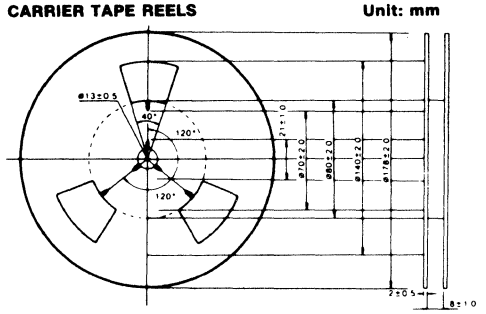
Samsung's Tape & Reel fully meets EIA Standard RS481 (8mm tape). Suffix "T1" must be indicated for Tape & Reel

Quantity Per Reel	Minimum Order
3,000	1 reel



User direction of feed

CARRIER TAPE REELS **Unit: mm**



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Samsung Semiconductor

SHARP

64K × 4 CMOS Static RAM

LH52252

Description

The LH52252 is a high speed 262,144 bit static RAM organized as 64K × 4. A fast, efficient design is obtained with a CMOS periphery and a matrix constructed with polysilicon load memory cells.

This RAM is fully static in operation. The Chip Enable ($\overline{E}$) gates power to the chip when $\overline{E}$ is high. Standby power drops to its lowest level (I_{SB1}) when $\overline{E}$ is raised to within 0.2V of Vcc.

Write cycles occur when both $\overline{E}$ and Write Enable ($\overline{W}$) are low. Data is transferred from the DQ pins to the memory location specified by the 16 address lines.

Read cycles occur when $\overline{E}$ is low and $\overline{W}$ is high. A Read Cycle will begin upon an address transition, on a falling edge of $\overline{E}$, or on a rising edge of $\overline{W}$.

High frequency design techniques should be employed to obtain the best performance from this device. Solid, low impedance power and ground planes, with high frequency decoupling capacitors, are desirable. Series termination of the inputs should be considered when transmission line effects occur.

Sharp

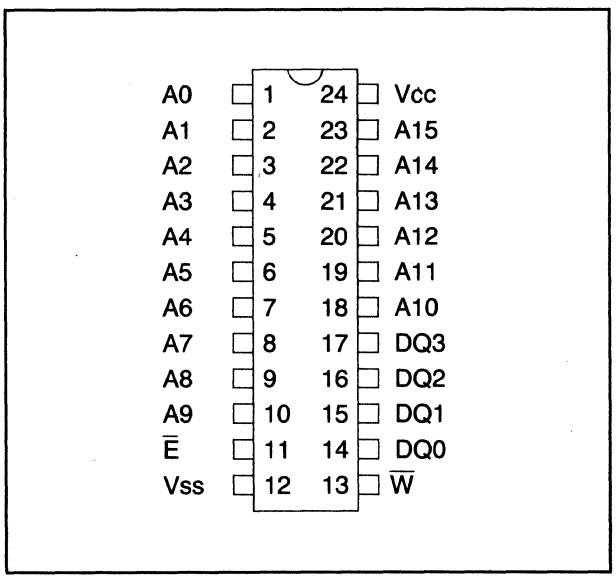
Truth Table

$\overline{E}$	$\overline{W}$	Mode	DQ	Icc
H	X	Not Selected	High Z	Standby
L	H	Read	Data Out	Active
L	L	Write	Data In	Active

Features

- Fast Access Times 25/35/45/55 ns
- Space Saving 300 Mil DIP
- JEDEC Standard Pinout
- Low Power Standby When Deselected
- TTL Compatible I/O
- 5V ± 10% Supply
- Fully Static Operation
- Common I/O for Low Pin Count

Pin Diagram



PIN Identification

A_0–A_{15}: Address Inputs
DQ_0–DQ_3: Data Inputs/Outputs
$\overline{E}$: Chip Enable
$\overline{W}$: Write Enable
Vcc: Positive Power Supply
Vss: Ground

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SHARP

CMOS 1048576-Bit Dynamic Random Access Memory

LH64258-10/-12/-15

Description

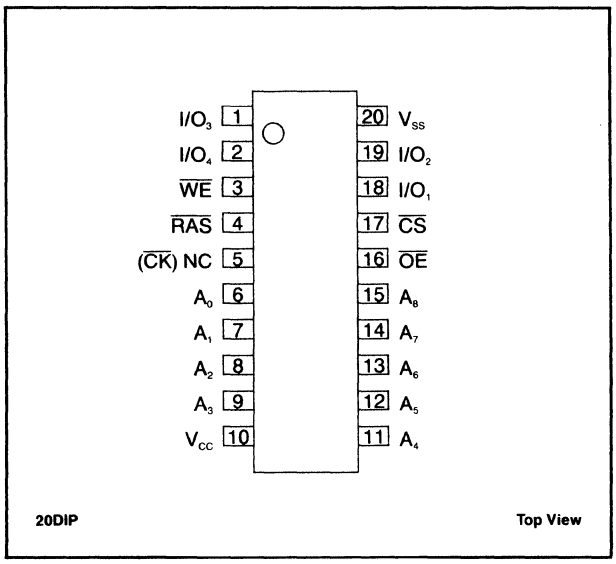
The LH64258 is 262,144 words × 4 bits Dynamic Random Access Memories fabricated on SHARP's advanced CMOS double-level polysilicon gate technology. With its address inputs multiplexed and packaged in the standard 300 mil wide 20 pin DIP, it is easy to realize memory systems with high speed, low power dissipation and large memory capacity. The LH64258 operates on single +5V power supply and the built-in biasing voltage generator circuit.

The LH64258 allows static column mode operation.

Features

- 262,144 word × 4 bits
- Standard 20 pin DIP
- Access time (MAX.)
  100ns (LH64258-10)
  120ns (LH64258-12)
  150ns (LH64258-15)
- Cycle time (MIN.)
  160ns (LH64258-10)
  190ns (LH64258-12)
  240ns (LH64258-15)
- Static column mode operation
- Power supply +5V ± 10%
- Power consumption (MAX.)
  330mW (LH64258-10 operating t_{RC} = 190ns)
  275mW (LH64258-12 operating t_{RC} = 220ns)
  220mW (LH64258-15 operating t_{RC} = 260ns)
  11mW (stand-by)
- All inputs and outputs are TTL compatible
- $\overline{OE}$ = Don't care in early write operation
- Effective $\overline{RAS}$ time-out function (is is easy to set up the rising time of $\overline{RAS}$ at minimum cycle using $\overline{RAS}$ time-out function)
- $\overline{RAS}$ only refresh, Hidden refresh and $\overline{CS}$ before $\overline{RAS}$ refresh capability
- On-chip refresh counter
- 512 refresh cycle (refresh period (MAX.) = 8ns)

Pin Connections



PIN Description

Signal	Pin name
$A_0 \sim A_8$	Address input
$\overline{RAS}$	Row address strobe
$\overline{CS}$	Chip select enable
$\overline{WE}$	Write enable
$\overline{OE}$	Output enable
$I/O_1 \sim I/O_4$	Data input/output
V_{CC}	Power supply (+5V)
V_{SS}	Power supply (0V)

Sharp

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SHARP

Preliminary Data Sheet

LH52259

32K x 9 CMOS Static RAM

Functional Description

The LH52259 is a high speed 294,912 bit static RAM organized as 32K x 9. A fast, efficient design is obtained with a CMOS periphery and a matrix constructed with polysilicon load memory cells.

This RAM is fully static in operation. The Chip Enable ($\overline{E}$) gates power to the chip when $\overline{E}$ is high. Standby power drops to its lowest level (I_{SB1}) if $\overline{E}$ is raised to within 0.2V of V_{CC}.

Write cycles occur when both $\overline{E}$ and Write Enable ($\overline{W}$) are low. Data is transferred from the DQ pins to the memory location specified by the 15 address lines. Bus contention during Write Cycles can be avoided by using the Output Enable ($\overline{G}$) input to disable the outputs.

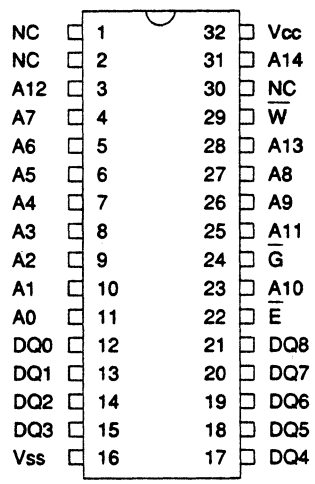
When $\overline{E}$ is low and $\overline{W}$ is high, a static read of the memory location specified by the address lines will occur. $\overline{G}$ independently is used to enable the outputs. Since the device is fully static in operation, new read cycles can be performed by simply changing the address.

High frequency design techniques should be employed to obtain the best performance from this device. Solid, low impedance power and ground planes, with high frequency decoupling capacitors, are desireable. Series termination of the inputs should be considered when transmission line effects occur.

Features

- Fast Access Times 35/45/55 ns
- Low Power Standby When Deselected
- 9 Bit Wide Data I/O
- TTL Compatible I/O
- 5V ±10% Supply
- Fully Static Operation
- Data Retention Mode
- JEDEC Standard Pinout

Pin Diagram



Truth Table

$\overline{E}$	$\overline{G}$	$\overline{W}$	Mode	DQ	Icc
H	X	X	Not Selected	Hi-Z	Standby
L	H	H	Selected	Hi-Z	Active
L	L	H	Read	D_{OUT}	Active
L	X	L	Write	D_{IN}	Active

Pin Identification

A_0-A_{14} . . . . . Address Inputs
DQ_0-DQ_8 . . . . . Data Inputs/Outputs
$\overline{E}$ . . . . . Chip Enable
$\overline{G}$ . . . . . Output Enable
$\overline{W}$ . . . . . Write Enable
V_{CC} . . . . . Positive Power Supply
V_{SS} . . . . . Ground

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SHARP

Preliminary

LH5496/97/98

512/1K/2K x 9 CMOS FIFO

Functional Description

The LH5496/97/98 are dual port memories with internal addressing to implement a First-In-First-Out algorithm. Through an advanced dual port architecture, they provide fully asynchronous read/write operation. Empty, Full, and Half-Full status flags are provided to prevent data overflow and underflow. In addition, internal logic is provided for unlimited expansion in both word size and depth.

Read and Write operations automatically access sequential locations in memory in such a way that data is read out in the same order that it was written, that is on a First-In-First-Out basis. Since the address sequence is internally predefined, no external address information is required for the operation of this device. A ninth data bit is provided for parity or control information often needed in communication applications.

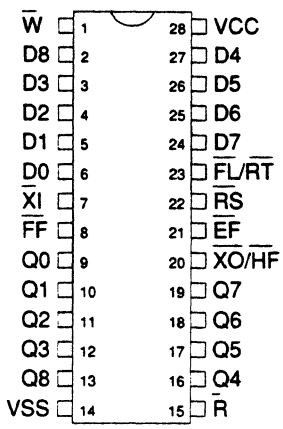
Empty, Full, and Half-Full status flags monitor the extent to which data has been written into the FIFO, and prevent improper operations (i.e. Read if the FIFO is empty, or Write if the FIFO is full). A retransmit feature resets the Read address pointer to its initial position, thereby allowing repetitive readout of the same data. Expansion-in and Expansion-out pins implement an expansion scheme that allows individual FIFOs to be cascaded to greater depth without incurring additional latency (bubblethrough) delays.

Features

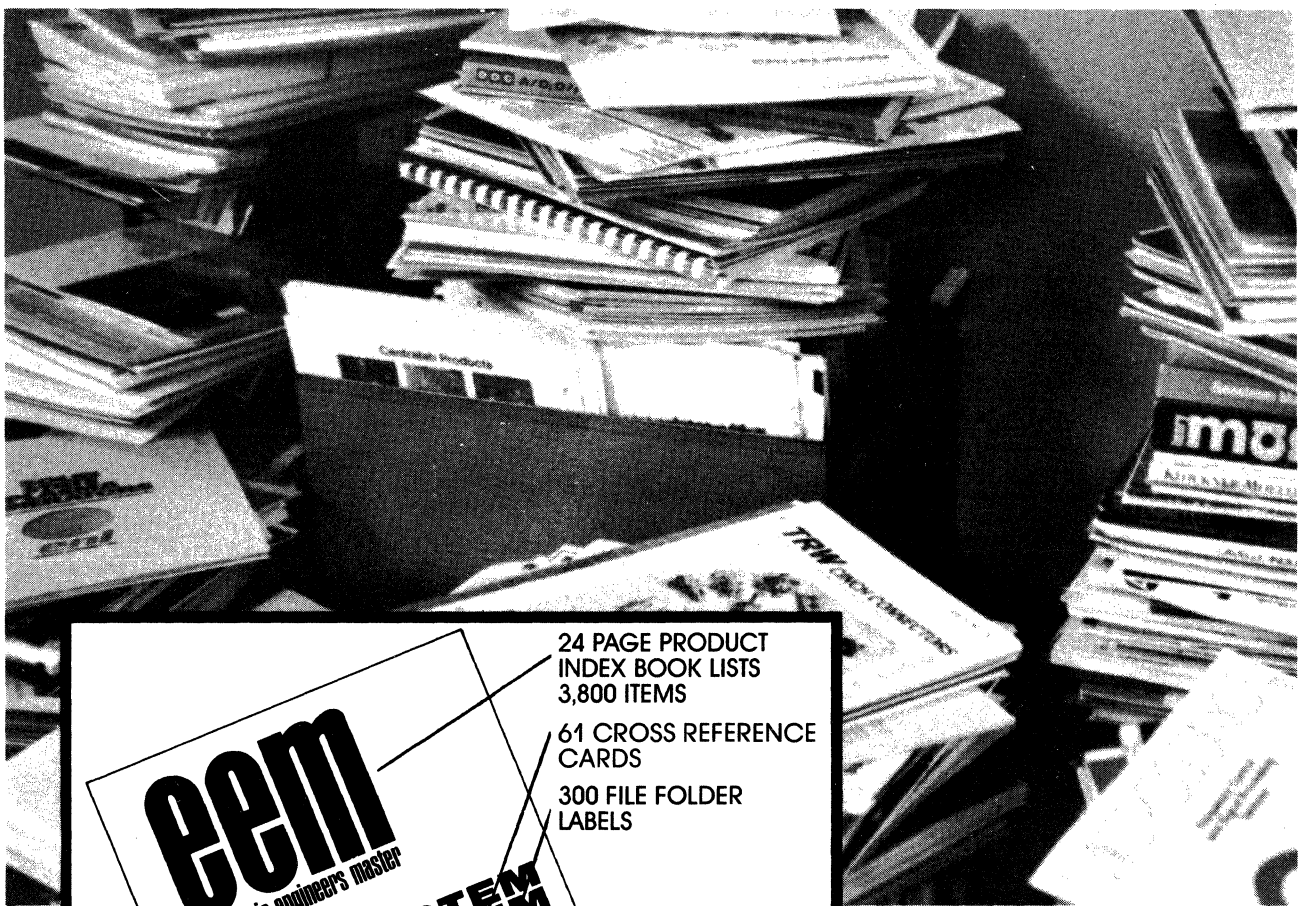
- Fast Access Times - 20/35/50/65/80/120 ns
- Full CMOS Dual Port Memory Array
- Fully Asynchronous Read and Write
- LH5496 - 512 x 9
  LH5497 - 1024 x 9
  LH5498 - 2048 x 9
- Expandable in Width and Depth
- Empty, Half-Full, and Full Status Flags
- Read Retransmit Capability
- TTL compatible I/O
- 28 Pin 300 mil PDIP, 28 Pin 600 mil PDIP or 32 Pin PLCC
- Pin and functionally compatible with IDT7201/2/3

Sharp

Pinout Diagrams



28 Pin DIP - Top View



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The EEM File System was invented over twenty-five years ago to help people who specify, buy, or work with electronic products and equipment. It is upgraded on a constant basis to reflect the current state of the art. It's easy to use and easy to customize to your particular needs.

You say you want to file catalogs by type of product? That's easy to do with The System. But, what are you going to do when there are multiple products in one catalog? Take Mallory for example. There are all kinds of products in the Mallory Short Form Catalog. With the EEM File System all you do is file the catalog under "M" for Mallory and refer to it on all of the cross reference cards that apply.

There are thousands of EEM File Systems in everyday use in engineering and procurement offices all over the world. Shouldn't you be using this proven system?

The EEM File System is shipped in one neat package. The package contains everything you need to set up your very own filing system. Best of all, it's easy to get and very affordable. Send a check or money order for $25.00 and EEM will pay the postage and sales tax. If you must use a purchase order, please add $2.00 for postage and handling. An invoice will be mailed to you under separate cover.

Don't waste any more time. Get organized now!

EEM FILE SYSTEM,
645 stewart ave., garden city, ny 11530

Technology Selection Guide

DEVICE NUMBER	DESCRIPTION	STD	S	LS	FAST	HC	HCT
00	Quad 2-Input NAND Gate	A	A	A	A	A	A
01	Quad 2-Input NAND Gate, OC			A			
02	Quad 2-Input NOR Gate	A	A	A	A	A	A
03	Quad 2-Input NAND Gate	A	A			A	A
04	Hex Inverter	A	A	A	A	A	A
05	Hex Inverter, OC	A	A	A			
06	Hex Inverter Buffer/Driver, OC	A					
07	Hex Buffer/Driver, OC	A					
08	Quad 2-Input AND Gate	A	A	A	A	A	A
09	Quad 2-Input AND Gate, OC			A			
10	Triple 3-Input NAND Gate	A	A	A	A	A	A
11	Triple 3-Input AND Gate	A	A	A	A	A	A
13	Dual 4-Input NAND Schmitt Trigger	A		A	A		
14	Hex Inverter Schmitt Trigger	A		A	A	A	A
16	Hex Inverter Buffer/Driver, OC	A					
17	Hex Buffer/Driver, OC	A					
20	Dual 4-Input NAND Gate	A	A	A	A	A	A
21	Dual 4-Input AND Gate	A		A		Q1 '87	Q1 '87
25	Dual 4-Input NOR with Strobe	A					
26	Quad 2-Input NAND Gate, OC	A		A			
27	Triple 3-Input NOR Gate	A		A	A	A	A
28	Quad 2-Input NOR Buffer	A					
30	8-Input NAND Gate	A		A	A	Q1 '87	A
32	Quad 2-Input OR Gate	A	A	A	A	A	A
33	Quad 2-Input NOR Buffer, OC	A		A			
37	Quad 2-Input NAND Buffer	A	A	A	A		
38	Quad 2-Input NAND Buffer, OC	A	A	A	A		
39	Quad 2-Input NAND Buffer, OC	A					
40	Dual 4-Input NAND Buffer	A	A	A	A		
42	BCD-to-Decimal Decoder	A		A		A	A
45	BCD-to-Decimal Decoder/Driver, OC	A					
50	Expandable Dual 2-Wide 2-Input AOI Gate	A					
51	Dual 2-Wide 2-Input AOI Gate	A	A	A	A		
54	4-Wide 2-Input AOI Gate			A			
58	Dual 4-Input AND/OR Gate					A	A
64	4-2-3-2 Input AOI Gate		A		A		
73	Dual J-K Master-Slave Flip-Flop	A		A		A	A
74	Dual D-Type Positive Edge-Triggered Flip-Flop	A	A	A*	A	A	A
75	Quad Bistable Latch	A		A		A	A
76	Dual J-K Master-Slave Flip-Flop	A		A			
83	4-Bit Binary Full Adder, Ripple Carry	A		A*			
85	4-Bit Magnitude Comparator	A	A	A	A	A	A
86	Quad 2-Input EXCLUSIVE-OR Gate	A	A	A	A	A	A
90	Decade Ripple Counter	A		A			
91	8-Bit Shift Register	A					
92	Divide-by-12 Counter	A		A			
93	4-Bit Binary Ripple Counter	A		A		A	A
94	4-Bit PISO Shift Register	A					
95	4-Bit Shift Register	A		A**			
96	5-Bit Shift Register	A		A			
107	Dual J-K Master-Slave Flip-Flop	A		A		A	A
109	Dual J-K Positive Edge-Triggered Flip-Flop	A		A*	A	A	A
112	Dual J-K Negative Edge-Triggered Flip-Flop		A	A	A	A	A
113	Dual J-K Negative Edge-Triggered Flip-Flop		A	A	A		
114	Dual J-K Negative Edge-Triggered Flip-Flop				A		
116	Dual 4-Bit Latch with Clear	A					

*A Version; **B Version; A = Available; 1H '87 = 1st Half of 1987; Q1 '87 = 1st Quarter of 1987; Q2 '87 = 2nd Quarter of 1987

Technology Selection Guide

DEVICE NUMBER	DESCRIPTION	STD	S	LS	FAST	HC	HCT
121	Monostable Multivibrator	A					
123	Quad 3-State Buffer	A				A	A
125	Quad Retriggerable Monostable Multivibrator	A		A*	A	A	A
126	Quad 3-State Buffer	A		A*	A	A	A
128	Quad 2-Input NOR Buffer	A					
132	Quad 2-Input NAND Schmitt Trigger	A		A	A	A	A
133	13-Input NAND Gate		A				
134	12-Input NAND Gate, 3-State		A				
135	Quad EXCLUSIVE-OR/NOR Gate		A				
136	Quad EXCLUSIVE-OR, OC			A			
137	3-to-8 Decoder/Demultiplexer, Inverting					Q1 '87	Q1 '87
138	3-to-8 Decoder/Demultiplexer				A	A	A
139	Dual 2-to-4 Decoder/Demultiplexer		A	A	A	A	A
140	Dual 4-Input NAND Line Driver		A				
145	BCD-to-Decimal Decoder/Driver, OC	A					
147	10-to-4 Priority Encoder	A				A	A
148	8-to-3 Priority Encoder	A			A		
150	16-to-6 Multiplexer	A					
151	8-to-1 Multiplexer	A	A	A	A	A	A
153	Dual 4-to-1 Multiplexer	A	A	A	A	A	A
154	4-to-16 Decoder/Demultiplexer	A		A		A	A
155	Dual 2-to-4 Decoder/Demultiplexer	A		A			
156	Dual 2-to-4 Decoder/Demultiplexer, OC	A		A			
157	Quad 2-to-1 Multiplexer	A	A	A	A	A	A
158	Quad 2-to-1 Multiplexer	A	A	A	A	A	A
160	Synchronous 4-Bit Decade Counter	A		A*	A*	A	A
161	Synchronous 4-Bit Binary Counter	A		A*	A*	A	A
162	Synchronous 4-Bit Decade Counter			A*	A*	A	A
163	Synchronous 4-Bit Binary Counter	A		A*	A*	A	A
164	8-Bit PISO Shift Register	A		A		A	A
165	8-Bit PISO Shift Register	A				A	A
166	8-Bit PISO Shift Register	A			A	A	A
168	Decade Up/Down Counter		A*	A*	A		
169	Binary Up/Down Counter		A*	A*	A		
170	4 x 4 Register File, OC	A		A			
172	16-Bit Multiple Port Register File		A				
173	Quad D-Type Flip-Flop, 3-State	A		A		A	A
174	Hex D-Type Flip-Flop with Clear	A	A	A	A		
175	Quad D-Type Flip-Flop	A			A	A	A
180	8-Bit Odd/Even Parity Checker	A					
181	4-Bit Arithmetic Logic Unit	A	A	A	A	Q1 '87	Q1 '87
182	Look-Ahead Carry Generator		A		1H '87	A	A
189	64-Bit Random Access Memory						
190	Decade Up/Down Counter	A			A	A	A
191	Binary Up/Down Counter	A		A	A	A	A
192	Decade Up/Down Counter	A		A	A	Q1 '87	Q1 '87
193	4-Bit Binary Up/Down Counter	A		A	A	A	A
194	4-Bit Bidirectional Shift Register	A	A	A*	A	A	A
195	4-Bit Parallel-Access Shift Register	A	A	A*	A	A	A
197	Presettable Binary Counter			A			
198	8-Bit Bidirectional Universal Shift Register				A	A	A
199	8-Bit Universal Shift Register	A			A		
221	Dual Monostable Multivibrator	A					
225	FIFO Register, 3-State		A				
227	1-to-8 Line Decoder					A	A
238	1-of-8 Decoder/Demultiplexer, True/Inverting					A	A
240	Octal Buffer, 3-State		A	A	A	A	A
241	Octal Buffer, 3-State		A	A	A	A	A

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Technology Selection Guide

DEVICE NUMBER	DESCRIPTION	STD	S	LS	FAST	HC	HCT
242	Quad Inverting Bus Transceiver, 3-State		A	A	A	A	A
243	Quad Bus Transceiver, 3-State		A	A	A	A	A
244	Octal Buffer, 3-State		A	A	A	A	A
245	Octal Bus Transceiver, 3-State			A	A	A	A
251	8-to-1 Multiplexer, 3-State		A	A	A	A	A
253	Dual 4-to-1 Multiplexer, 3-State		A	A	A	A	A
256	Dual 4-Bit Addressable Latch			A	A		
257	Quad 2-to-1 Multiplexer, 3-State		A	A*	A	A	A
258	Quad 2-to-1 Multiplexer, 3-State		A	A*	A	A	A
259	8-Bit Addressable Latch			A	A	A	A
260	Dual 5-Input NOR Gate		A	A	A		
266	Quad EXCLUSIVE-OR, OC			A		A	
269	8-Bit Up/Down Counter				A		
273	Octal D Flip-Flop		A	A	A	A	A
279	Quad S-R Latch	A					
280	9-Bit Odd/Even Parity Generator/Checker		A		A*	A	A
283	4-Bit Adder			A	A	A	A
290	Decade Counter			A			
293	4-Bit Binary Counter			A			
295	4-Bit Shift Register, 3-State			A**			
297	Digital Phase-Locked Loop Filter					A	A
298	Quad 2-Port Register	A		A	A		
299	Octal Shift/Storage Register, 3-State				A	A	A
322	Octal Shift/Storage Register				A		
323	Octal Shift/Storage Register				A		
350	4-Bit Four-Way Shifter		A		A		
352	Dual 4-to-1 Multiplexer, Inverting			A	A		
353	Dual 4-to-1 Multiplexer, Inverting, 3-State			A	A		
354	8-Input Multiplexer/Register, 3-State					Q1 '87	Q1 '87
356	8-Input Multiplexer/Register, 3-State					A	A
363	Octal Latch, 3-State, MOS Compatible Outputs			A			
364	Octal D Flip-Flop, 3-State, MOS Compatible Outputs			A			
365	Hex Buffer with Common Enable, 3-State	A		A*	A	A	A
366	Hex Inverter Buffer/Driver with Common Enable, 3-State	A		A*	A	A	A
367	Hex Buffer, 4-Bit and 2-Bit, 3-State	A		A*	A	A	A
368	Hex Inverter, 4-Bit and 2-Bit, 3-State	A		A*	A	A	A
373	Octal Latch, 3-State		A	A	A	A	A
374	Octal D Flip-Flop, 3-State		A	A	A	A	A
375	Quad Latch			A			
377	Octal D-Type Flip-Flop with Enable			A	A	A	A
378	Hex D Flip-Flop with Enable			A	A		
379	Quad D Flip-Flop with Enable				A		
381	4-Bit Arithmetic Logic Unit				A		
382	4-Bit Arithmetic Logic Unit				A		
384	8-Bit Serial/Parallel Two's Complement Multiplier				Q1 '87		
385	Quad Serial Adder/Subtractor				1H '87		
390	Dual Decade Ripple Counter			A		A	A
393	Dual Binary Ripple Counter			A		A	A
395	4-Bit Cascadable Shift Register, 3-State			A*	A		
398	Quad 2-Port Register with True and Complement Outputs				A		
399	Quad 2-Port Register				A		
412	Octal Multi-Mode Buffered Latch				1H '87		
423	Dual Retriggerable Monostable Multivibrator					A	A
432	Octal Multi-Mode Buffered Latch				1H '87		
445	BCD-to-Decimal Decoder with 7V Output			A			

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Technology Selection Guide

DEVICE NUMBER	DESCRIPTION	STD	S	LS	FAST	HC	HCT
490	Dual Decade Ripple Counter			A			
521	8-Bit Comparator				A		
524	8-Bit Register Comparator				A		
533	Inverting Octal D Latch, 3-State				A	A	A
534	Octal D Flip-Flop, 3-State				A	A	A
537	1-of-10 Decoder, 3-State				A		
538	1-of-8 Decoder, 3-State				A		
539	Dual 1-of-4 Decoder, 3-State				A		
540	Octal Driver, 3-State			A	A	A	A
541	Octal Driver, 3-State			A	A	A	A
543	Octal Transparent Bidirectional Latch				A		
544	Octal Transparent Bidirectional Latch				A		
545	Octal Bus Transceiver				A		
547	Octal Decoder/Mux w/Addr. Latches and Acknowledge				1H '87		
548	Octal Decoder/Multiplexer with Acknowledge				1H '87		
550	Octal Registered Transceiver with Status Flags				1H '87		
551	Octal Registered Transceiver with Status Flags				1H '87		
557	8 x 8 Multiplier with Latch, 3-State				1H '87		
558	8 x 8 Multiplier, 3-State				1H '87		
563	Octal Transparent Inverting Latch, 3-State				1H '87	A	A
564	Octal D-Type Inverting Flip-Flop, 3-State				1H '87	A	A
568	BCD Decade Up/Down Synchronous Counter			A*	A		
569	4-Bit Binary Up/Down Synchronous Counter			A*	A		
573	Octal Transparent Latch, 3-State				1H '87	A	A
574	Octal D-Type Flip-Flop. Positive Edge-Triggered, 3-State					A	A
579	8-Bit Up/Down Counter, Common I/O				A		
583	BCD Adder					Q1 '87	Q1 '87
588	GPIB Compatible Octal Transceiver				A		
595	8-Bit Shift Register with Output Latch				1H '87		
596	8-Bit Shift Register with Output Latch						
597	8-Bit Shift Register with Input Latch				1H '87	A	A
598	8-Bit Shift Register with Input Latch				1H '87		
604	Dual 8-Bit Latch, 3-State				A		
605	Dual 8-Bit Latch, OC				A		
620	Octal Transceiver, 3-State			A	A		
621	Octal Transceiver, OC			A	A		
622	Octal Transceiver, OC			A	A		
623	Octal Transceiver, 3-State			A	A		
630	Memory Error Detector/Corrector, 3-State				1H '87		
631	Memory Error Detector/Corrector				1H '87		
640	Octal Bus Transceiver, 3-State			A	A	A	A
640-1	Octal Bus Transceiver, 3-State 48 mA Sink Capability			A			
641	Octal Bus Transceiver, OC			A	A		
641-1	Octal Bus Transceiver, OC				A		
642	Octal Bus Transceiver, OC			A	A		
643	Octal True/Inverting Transceiver, 3-State					A	A
645	Octal Bus Transceiver, 3-State			A			
645-1	Octal Bus Transceiver, 3 State			A	A		
646	Octal Bus Transceiver with Registers, 3-State				A	A	A
647	Octal Bus Transceiver with Registers, OC					A	A
648	Octal Bus Transceiver with Registers, 3-State				A	A	A
649	Octal Bus Transceiver with Registers, OC				A		
655	Octal Buffer with Parity Generator-Checker, 3-State				A*		
656	Octal Buffer with Parity Generator-Checker, 3-State				A*		
657	Octal Bus Transceiver with Parity Generator-Checker, 3-State				A		
670	4 × 4 Register File, 3-State					A	A
673	16-Bit SIPO Shift Register				A		
674	16-Bit PISO Shift Register				A		
675	16-Bit PISO Shift Register with Serial Output Capability				A		
676	16-Bit PISO Shift Register with Parallel Output Capability				A		

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DEVICE NUMBER	DESCRIPTION	STD	S	LS	FAST	HC	HCT
688	8-Bit Magnitude Comparator					A	A
764	Dual Port RAM Controller with DRAM Refresh, with Latch			A	1H '87		
765	8-Bit Counter				A		
779	8-Bit Counter				A		
784	8-Bit Serial Multiplier and Adder/Subtractor				A		
786	4-Bit Asynchronous Arbiter						
821	10-Bit Register, Noninverting, 3-State				1H '87		
822	10-Bit Register, Inverting, 3-State				1H '87		
823	9-Bit Register, Noninverting, 3-State				1H '87		
824	9-Bit Register, Inverting, 3-State				1H '87		
825	8-Bit Register, Noninverting, 3-State				1H '87		
826	8-Bit Register, Inverting, 3-State				1H '87		
827	10-Bit Buffer, Noninverting, 3-State				1H '87		
828	10-Bit Buffer, Inverting, 3-State				1H '87		
841	10-Bit Latch, Noninverting, 3-State				1H '87		
842	10-Bit Latch, Inverting, 3-State				1H '87		
843	9-Bit Latch, Noninverting, 3-State				1H '87		
844	9-Bit Latch, Inverting, 3-State				1H '87		
845	8-Bit Latch, Noninverting, 3-State				1H '87		
846	8-Bit Latch, Inverting, 3-State				1H '87		
861	10-Bit Transceiver, Noninverting, 3-State				1H '87		
862	10-Bit Transceiver, Inverting, 3-State				1H '87		
863	9-Bit Transceiver, Noninverting, 3-State						
864	9-Bit Transceiver, Inverting, 3-State						
881	ALU/Function Generator				1H '87		
882	32-Bit Carry-Look-Ahead Generator				1H '87		
1240	Octal Buffer, 3-State				A		
1241	Octal Buffer, 3-State				A		
1242	Quad Transceiver, Inverting, 3-State				A		
1243	Quad Bus Transceiver, 3-State				A		
1244	Octal Bus/Line Driver, 3-State				A		
1245	Octal Bus Transceiver, 3-State				A		
3037	30 Ohm Transmission Line Driver Quad 2-Input NAND, OC				A		
3038	30 Ohm Transmission Line Driver Quad 2-Input NAND, OC				A		
3040	30 Ohm Transmission Line Driver Dual 4-Input NAND, OC				A		
30240	Octal Inverting 30 Ohm Transmission Line Driver, OC				1H '87		
30241	Octal 30 Ohm Transmission Line Driver				1H '87		
30244	Octal 30 Ohm Transmission Line Driver				1H '87		
30245	Octal Transceiver, 30 Ohm Transmission Line Driver				1H '87		
30640	Octal Transceiver, 30 Ohm Transmission Line Driver, Inverting				1H '87		
4002	Dual 4-Input NOR Gate					A	A
4015	Dual 4-Bit SIPO Shift Register					A	A
4016	Quad Bilateral Switch					A	A
4017	Johnson Decade Counter with 10 Decoded Outputs					A	A
4020	14-Stage Binary Counter					A	A
4024	7-Stage Binary Counter					A	A
4040	12-Stage Binary Counter					A	A
4046A	Phase Locked Loop with V_{CO}					A	A
4049	Hex Inverting HIGH-to-LOW Level Shifter					A	
4050	Hex HIGH-to-LOW Level Shifter					A	
4051	8-Channel Analog MUX/DMUX					A	A
4052	Dual 4-Channel Analog MUX/DMUX					A	A
4053	Triple 2-Channel Analog MUX/DMUX					A	A
4059	Programmable Divide By n Counter					Q1 '87	Q1 '87
4060	14-Stage Ripple-Carry Binary Counter					A	A
4066	Quad Bilateral Switch					A	A
4067	16-Channel Analog MUX/DMUX					A	A

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DEVICE NUMBER	DESCRIPTION	STD	S	LS	FAST	HC	HCT
4075	Tripple 3-Input OR Gate					A	A
4094	8-Stage Shift-And-Store Bus Register					A	A
4316	Quad Bilateral Switch					A	A
4351	8-Channel Analog MUX/DMUX with Latch					A	A
4352	Dual 4-Channel Analog MUX/DMUX with Latch					Q1'87	Q1'87
4353	Triple 2-Channel Analog MUX/DMUX with Latch					A	A
4510	BCD Up/Down Counter					Q1'87	Q1'87
4511	BCD to 7-Segment Latch/Decoder/Driver					A	A
4514	1-of-16 Decoder/DMUX with Input Latches					A	A
4515	1-of-16 Decoder/DMUX with Input Latches					A	A
4516	Binary Up/Down Counter					Q1'87	Q1'87
4518	Dual BCD Counter					A	A
4520	Dual 4-Bit Binary Counter					A	A
4538	Dual Retriggerable Precision Monostable Multivibrator					A	A
4543	BCD to 7-Segment Latch/Decoder/Driver for LCDs					A	A
7030	9-Bit x 16 Word Expandable FIFO Register					Q1'87	Q1'87
7046	Phase-Locked Loop with Lock Detector					A	A
7597	8-Bit Shift Register with Latches					A	A
40102	Presettable 2-Decade BCD Down Counter					Q1'87	Q1'87
40103	8-Bit Binary Down Counter					A	A
40104	4-Bit Bidirectional Universal Shift Register					A	A
40105	4-Bit x 16-Word FIFO Register					A	A

*A Version; **B Version; A = Available; 1H '87 = 1st Half of 1987; Q1 '87 = 1st Quarter of 1987; Q2 '87 = 2nd Quarter of 1987

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Function Cross Reference Guide

The Function Cross Reference Guide is provided for customer reference only. It does not represent all the devices available from Signetics' Logic Division.
The device number given is a base number. Check the Number Cross Reference Guide for the complete part number and availability.

GATES

FUNCTION	DEVICE NO.
Inverters	
Hex Inverter	04
Hex Inverter, OC	05
Hex Inverter buffer/Driver, OC (30V)	06
Hex Inverter Schmitt Trigger	14
Hex Inverter Buffer/Driver, OC (15V)	16
Octal Inverting Transmission Line Driver	30240
Hex Inverter (15V to TTL Levels)	4049
Hex Inverter Unbuffered Outputs	4069UB
Hex Inverter Schmitt Trigger	40106
Dual Complementary Pair and Inverter, Unbuffered	4007UB
NAND	
Quad 2-Input	00
Quad 2-Input, OC	01
Quad 2-Input, OC	03
Quad 2-Input, OC	26
Quad 2-Input NAND Buffer	37
Quad 2-Input NAND Buffer, OC	38
Quad 2-Input NAND Transmission Line Driver, OC	3037
Quad 2-Input NAND Transmission Line Driver, OC	3038
Triple 3-Input	10
Dual 4-Input, Schmitt Trigger	13
Dual 4-Input	20
8-Input	30
Dual 4-Input NAND Buffer	40
Dual 4-Input NAND Line Driver	140
Dual 4-Input NAND Line Driver	3040
Quad 2-Input, Schmitt Trigger	132
Quad 2-Input	4011
Quad 2-Input, Unbuffered Outputs	4011UB
Dual 4-Input	4012
Triple 3-Input	4013
8-Input	4068
12-Input	134
13-Input	133
AND	
Quad 2-Input	08
Quad 2-Input	4081
Quad 2-Input, OC	09
Triple 3-Input	11
Dual 4-Input	21
Dual 4-Input	4082
NOR	
Quad 2-Input	02
Quad 2-Input	28

FUNCTION	DEVICE NO.
NOR (Continued)	
Quad 2-Input	128
Quad 2-Input	4001
Quad 2-Input, Unbuffered Output	4001UB
Quad 2-Input, OC	33
Triple 3-Input	27
Triple 3-Input	4025
Dual 3-Input, with Inverter	4000
Dual 4-Input	4002
Dual 4-Input, with Strobe	25
Dual 5-Input	260
8-Input	4078
OR	
Quad 2-Input	32
Quad 2-Input	4071
Triple 3-Input	4075
Dual 4-Input	4072
Exclusive-OR	
Quad	86
Quad	4030
Quad, OC	136
Quad	4070
Quad Exclusive OR-NOR	135
Exclusive-NOR	
Quad	4077
Quad, OC	266
Quad Exclusive OR-NOR	135
Combination Gates	
Expandable Dual 2-Wide 2-Input AND-OR-Invert	50
Dual 2-Wide 2-Input AND-OR-Invert	51
4-Wide 2-Input AND-OR-Invert	54
Dual 4-Input AND/OR Gate	58
4-2-3-2 Input AND-OR-Invert	64
Dual 3-Input NOR Gate with Inverter	4000
Dual Complementary Pair and Inverter, Unbuffered	4007UB
Dual 2-Wide 2-Input AND-OR-Invert	4085
4-Wide 2-Input AND-OR-Invert	4086

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Function Cross Reference Guide

DUAL FLIP-FLOPS

FUNCTION	DEVICE NUMBER	CLOCK EDGE	SET	CLEAR
D	74	↑	LOW	LOW
D	4013	↑	HIGH	HIGH
JK	73	↓		LOW
JK	76	↓	LOW	LOW
JK	107	↓		LOW
JK	109	↑	LOW	LOW
JK	112	↓	LOW	LOW
JK	113	↓	LOW	
JK	114	↓	LOW	LOW
JK	4027	↑	HIGH	HIGH

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MULTIPLE FLIP-FLOPS

FUNCTION	DEVICE NUMBER	RESET (LEVEL)	CLOCK EDGE	OUTPUT
Quad	173	HIGH	↑	True
Quad D	175	LOW	↑	True, Comp
Quad D	40175	LOW	↑	True
Quad D with Enable	379		↑	True, Comp
Quad D, 3-State	4079	HIGH	↑	True
Quad D, 3-State	8T10	HIGH	↑	True
Hex D	174	LOW	↑	True
Hex D with Enable	378		↑	True
Octal D	273	LOW	↑	True
Octal D, 3-State	374		↑	True
Octal D with Enable	377		↑	True
Octal D, 3-State	534		↑	Comp
Octal D, 3-State	564		↑	Comp
Octal D, 3-State	574		↑	True
Octal D, 3-State	40374		↑	True
Octal D, 3-State	8TS806		↑	True
Octal D, 3-State	8TS808		↑	Comp
Octal D, 3-State, MOS Compatible Outputs	364		↑	True

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OTHER REGISTERS, REGISTER FILES

FUNCTION	DEVICE NUMBER	BITS	SERIAL ENTRY	PARALLEL ENTRY*	CLOCK
Quad 2 Port	298	4 x 2		2D (mux)	⌜
Quad 2 Port	398	4 x 2		2D (mux)	⌟
Quad 2 Port	399	4 x 2		2D (mux)	⌟
Register File, OC	170	4 x 4		4A	⌜
Multiple Port Register File, 3-State	172	16		3D (mux)	⌜
4 x 4 Register File, 3-State	670	4 x 4		4A	⌜
16 x 5 FIFO, 3-State	225	5		5S	⌟
4 x 16 FIFO	40105	4	D	4S	
10-Bit Register, Noninverting, 3-State	821	10		2D	⌟
10-Bit Register, Inverting, 3-State	822	10		2D	⌟
9-Bit Register, Noninverting, 3-State	823	9		2D	⌟
9-Bit Register, Inverting, 3-State	824	9		2D	⌟
8-Bit Register, Noninverting, 3-State	825	8		2D	⌟
8-Bit Register, Inverting, 3-State	826	8		2D	⌟

*D = D type input, A = Asynchronous data input, S = Synchronous data input

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Function Cross Reference Guide

SHIFT REGISTERS

S = Synchronous, A = Asynchronous

FUNCTION	DEVICE NUMBER	BITS	SERIAL ENTRY	PARALLEL ENTRY	CLOCK
Serial In/Serial Out Shift Register	91	8	D_A and D_B		⎍
Serial In/Serial Out Shift Right	4006	(2 x 4) (2 x 5)	D		⎏
Serial In/Serial Out Shift Right	4031	64	D_A + D_B		⎍
Dual Serial In/Serial Out Shift Right, 3-State	4517	(4 x 16)	D		⎍
Quad Serial In/Serial Out Shift Right	4731	64	D		⎏
Serial In/Serial Out Variable Length Shift Right	4557	1 to 64	D_A + D_B		⎍ and ⎏
Serial In/Serial Out Shift Right, 3-State	4094	8	D		⎍
Parallel In/Serial Out	674	16	D	16S	⎏
Serial In/Serial/Parallel Out	675	16	D		⎏
Serial/Parallel In/Serial Out	676	16	D	16S	⎏
Parallel/Serial In/Serial Out Shift Right	94	4	D	2 x 4A (mux)	⎍
Parallel/Serial In/Serial Out Shift Right	165	8	D	8A	⎍
Parallel/Serial In/Serial Out Shift Right	166	8	D	8S	⎍
Parallel/Serial In/Serial Out Shift Right	195	4	J, $\overline{K}$	4S	⎍
Parallel/Serial In/Serial Out Shift Right	199	8	J, K	8S	⎍
Parallel/Serial In/Serial Out Shift Right	597	8	D	8S	⎍
Parallel/Serial In/Serial Out Shift Right	4014	8	D	8S	⎍
Parallel/Serial In/Serial Out Shift Right	4021	8	D	8A	⎍
Parallel/Serial In/Serial Out Shift Right	8274	10	D	10S	⎏
Parallel/Serial In/Serial Out Shift Right, 3-State	598	8	S0, S1	8S	⎍
Serial In/Parallel Out Shift Right	164	8	D_0 and D_1		⎍
Serial In/Parallel Out Shift Right, with Reset	8273	10	D		⎏ or ⎍
Dual Serial In/Parallel Out Shift Right	4015	4	D		⎍
Serial In/Parallel Out, 3-State	595	8	D		⎍
Serial In/Parallel Out, OC	596	8	D		⎍
Serial In/Parallel Out	673	16	D		⎏
Parallel In/Serial In/Parallel Out Shift Right	95	4	D	5A	⎏
Parallel In/Serial In/Parallel Out Shift Right	96	5	D	5A	⎍
Parallel In/Serial In/Parallel Out Shift Right	40195	4	J, $\overline{K}$	4S	⎍
Parallel In/Serial In/Parallel Out Shift Right	8271	4	D	4S	⎏
Parallel In/Serial In/Parallel Out Shift Right	82S71	4	D	4S	⎏
Parallel In/Serial In/Parallel Out Shift Right	4035	4	J, $\overline{K}$	4S	⎍
Parallel In/Serial In/Parallel Out Shift Right, 3-State	295	4	D	4S	⎏
Parallel In/Serial In/Parallel Out Shift Right, 3-State	395	4	D	4S	⎏
Parallel In/Serial In/Parallel Out Shift Right, 3-State	322	8	D_0 + D_1	8S (I/O)	⎍
Parallel In/Serial In/Parallel Out Bidirectional	194	4	Dr, D_L	4S	⎍
Parallel In/Serial In/Parallel Out Bidirectional	198	8	Dr, D_L	8S	⎍
Parallel In/Serial In/Parallel Out Bidirectional	40194	4	Dr, D_L	4S	⎍
Parallel In/Serial In/Parallel Out Bidirectional, 3-State	299	8	Dr, D_L	8S	⎍
Parallel In/Serial In/Parallel Out Bidirectional, 3-State	323	8	Dr, D_L	8S (I/O)	⎍
Parallel In/Serial In/Parallel Out Bidirectional, 3-State	40194	4	Dr, D_L	4S	⎍
4-Bit Shifter, 3-State	350	4		4A	

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LATCHES

FUNCTION	DEVICE NUMBER	COMMON CLEAR (LEVEL)	ENABLE INPUT (LEVEL)	OUTPUT
Quad D	75		2 (H)	True, Comp
Quad D	375		2 (H)	True, Comp
Quad D	4042		2 (H)	True
Quad SR	279			True
Quad SR, 3-State	4043			True
Quad SR, 3-State	4044			True
Dual 4-Bit Transparent	116	LOW	2 (L)	True
Dual 4-Bit Addressable	256	LOW	1 (L)	True
Dual 4-Bit, Strobed	4508	HIGH	1 (L)	True
Dual 8-Bit, 3-State	604			True
Dual 8-Bit, OC	605			True
6-Bit (2-Bit and 4-Bit)	8T3404		1 (L)	Comp
8-Bit Addressable	259	LOW	1 (H)	True
8-Bit Addressable	4724	HIGH	1 (L)	True
8-Bit Addressable	9334	LOW	1 (L)	True
8-Bit, Noninverting, 3-State	845	LOW	1 (H)	True
8-Bit, Inverting, 3-State	846	LOW	1 (H)	Comp
9-Bit, Noninverting, 3-State	843	LOW	1 (H)	True
9-Bit, Inverting, 3-State	844	LOW	1 (H)	Comp
10-Bit, Noninverting, 3-State	841		1 (H)	True
10-Bit, Inverting, 3-State	842		1 (H)	Comp
Octal, 3-State	373		1 (H)	True
Octal, Multimode, Buffered	412	LOW		True
Octal, Multimode, Buffered	432	LOW		Comp
Octal Inverting, 3-State	533		1 (H)	Comp
Octal, Transparent, Bidirectional	543		4 (L)	True
Octal, Transparent, Bidirectional	544		4 (L)	Comp
Octal, Transparent, Inverting, 3-State	563		1 (H)	Comp
Octal, Transparent, 3-State	573		1 (H)	True
Octal Inverting, 3-State	533		1 (H)	Comp
Octal Transparent, 3-State	40373		1 (H)	True
Octal Transparent, 3-State	8TS805		1 (H)	True
Octal Inverting, 3-State	8TS807		1 (H)	Comp
Octal, 3-State with MOS Compatible Outputs	363		1 (H)	True

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Function Cross Reference Guide

MULTIPLEXERS

FUNCTION	DEVICE NUMBER	ENABLE INPUT (LEVEL)	SELECT INPUTS	OUTPUT
Quad 2-Input	157	1 (L)	1	True
Quad 2-Input	158	1 (L)	1	True
Quad 2-Input	298	Clocked ⌐	1	True, Latched
Quad 2-Input	398	1 (H)	1	True, Comp Registered
Quad 2-Input	399	1 (H)	1	True, Registered
Quad 2-Input	4019		2	True
Quad 2-Input	4519		2	True
Quad 2-Input	8266		2	True
Quad 2-Input	9322	1 (L)	1	True
Quad 2-Input, 3-State	257		1	True
Quad 2-Input, 3-State	258		1	Comp
Quad 2-Input, OC	8234		2	Comp
Dual 4-Input	153	2 (L)	2	True, Comp
Dual 4-Input	352	2	2	Comp
Dual 4-Input	9309		2	True, Comp
Dual 4-Input	4539	2 (L)	2	True
Dual 4-Input, 3-State	253		2	True
Dual 4-Input, 3-State	353	2	2	Comp
8-Input	9312	1 (L)	3	True, Comp
8-Input	151	1 (L)	3	True, Comp
8-Input, 3-State	251		1	True, Comp
8-Input, 3-State	356	1 (L)	3	True, Latched
8-Input, 3-State	354	2 (L)	3	True, Latched
8-Input, 3-State	4512	1 (L)	3	True
16-Input	150	1 (L)	4	Comp

ANALOG MULTIPLEXERS/DEMULTIPLEXERS AND SWITCHES

FUNCTION	DEVICE NUMBER
Triple 2-Channel Mux/Demux	4053
Dual 4-Channel Mux/Demux	4052
8-Channel Mux/Demux	4051

FUNCTION	DEVICE NUMBER
16-Channel Mux/Demux	4066
Quad Bilateral Switches	4016
Quad Bilateral Switches	4067
Quad Bilateral Switch	4316
8-Channel Analog MUX/DeMUX with Latch	4351
Dual 4-Channel Analog MUX/DeMUX with Latch	4352
Triple 2-Channel Analog MUX/DeMUX with Latch	4353

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COUNTERS

FUNCTION	DEVICE NUMBER	MODULUS	PARALLEL ENTRY	PRESETTABLE	CLOCK EDGE
Asynchronous	90	2 × 5			↓
Asynchronous	290	2 × 5			↓
Asynchronous	92	2 × 6			↓
Asynchronous	93	2 × 8			↓
Asynchronous	293	2 × 8			↓
Asynchronous	176	2 × 5	A	X	↓
Asynchronous	177	2 × 8	A	X	↓
Asynchronous	197	2 × 8	A	X	↓
Asynchronous	290	2 × 5			↓
Asynchronous	293	2 × 8			↓
Asynchronous	390	2 × 5			↓
Asynchronous	393	2 × 8			↓
Asynchronous	490	2 × 5			↓
Asynchronous	4020	12			↓
Asynchronous	4024	7			↓
Asynchronous	4040	14			↓
Asynchronous with Oscillator	4060	14			
Synchronous	160	10	S	X	↑
Synchronous	161	16	S	X	↑
Synchronous	162	10	S	X	↑
Synchronous	163	16	S	X	↑
Synchronous, 3-State	751	256	S	X	↑
Synchronous, 3-State	752	100	S	X	↑
Synchronous	4256	16	A		↑ or ↓
Synchronous	40161	16	S	X	↑
Synchronous	40163	16	S	X	↑
Synchronous (Dual)	4518	10			↑ or ↓
Synchronous (Dual)	4520	16			↑ or ↓
Up/Down	168	10	S	X	↑
Up/Down	169	16	S	X	↑
Up/Down	190	10	A	X	↑
Up/Down	191	16	A	X	↑
Up/Down	192	10	A	X	↑
Up/Down	193	16	A	X	↑
Up/Down	269	8	S	X	↑
Up/Down	4029	10, 16	A	X	↑
Up/Down	4510	10	A	X	↑
Up/Down	4516	16	A	X	↑
Up/Down	40193	16	A	X	↑
Up/Down, 3-State	568	10	S	X	↑
Up/Down, 3-State	569	16	S	X	↑
Up/Down, 3-State	579	8	S (I/O)	X	↑
Up/Down, 3-State	779	8	S (I/O)	X	↑
Frequency Divider	4059	Programmable 3 to 15,999			↑
Johnson	4017	10			↑ or ↓
Johnson	4018	5	A		↑ or ↓
Johnson	4022	8			↑ or ↓

S = Synchronous A = Asynchronous

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Function Cross Reference Guide

TRI-STATE BUFFERS, DRIVERS AND TRANSCEIVERS

FUNCTION	DEVICE NUMBER	OUTPUT
Quad Buffer	125	True
Quad Buffer	126	True
Quad Bus Driver	8T09	
Quad Bus Transceiver	242	Comp
Quad Bus Transceiver	243	True
Quad Bus Transceiver	1242	Comp
Quad Bus Transceiver	1243	True
Quad Bus Transceiver	8T34	Comp
Quad Bus Transceiver	8T126	Comp
Quad Bus Transceiver	8T127	Comp
Quad Bus Transceiver	8T128	True
Quad Bus Transceiver	8T129	True
Hex Buffer	365	True
Hex Inverter	366	Comp
Hex Buffer, 4-Bit and 2-Bit	367	True
Hex Inverter, 4-Bit and 2-Bit	368	Comp
Hex Buffer	8T95	True
Hex Inverter	8T96	Comp
Hex Buffer	8T97	True
Hex Inverter	8T98	Comp
Hex Buffer	40097	True
Hex Buffer	40098	Comp
Octal Buffer	240	Comp
Octal Buffer	241	True
Octal Buffer	244	True
Octal Buffer	40240	Comp
Octal Buffer	40244	True
Octal Buffer	540	Comp
Octal Buffer	541	True
Octal Buffer with Parity Generator/Checker	455	Comp
Octal Buffer with Parity Generator/Checker	456	True
Octal Buffer	1240	Comp
Octal Buffer	1241	True
Octal Buffer	1244	True
Octal Buffer with Parity Generator-Checker	655	Comp
Octal Buffer with Parity Generator-Checker	656	True
10-Bit Buffer	827	True
10-Bit Buffer	828	Comp
Octal Transceiver	245	True
Octal Transceiver	545	True
Octal Transceiver with IEEE-488 Termination Resistors	588	True
Octal Transceiver	620	Comp
Octal Transceiver	623	True
Octal Transceiver	640, 640-1	Comp
Octal Transceiver	643	True, Comp
Octal Transceiver	645, 645-1	True
Octal Bus Transceiver with Parity Generator-Checker	657	True
Octal Bus Transceiver	1245	True
Octal Transceiver	40245	True
Octal Transceiver	8T125	Comp
Octal Transceiver/Register	646	True
Octal Transceiver/Register	648	Comp
10-Bit Transceiver	861	True
10-Bit Transceiver	862	Comp
9-Bit Transceiver	863	True
9-Bit Transceiver	864	Comp

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LEVEL TRANSLATORS

FUNCTION	DEVICE NUMBER
Hex Inverting Buffer, Up to 15V Input, TTL Level Output	4049
Hex Non-Inverting Buffer, Up to 15V Input, TTL Level Output	4050
Quad Voltage Translator, 3-State, TTL Input, 15V Output	4104
Quad Transceiver, MOS/CMOS to TTL	8T26
Quad Transceiver, MOS/CMOS to TTL	8T28

PRIORITY ENCODERS

FUNCTION	DEVICE NUMBER	INPUT ENABLE (LEVEL)	INPUT/OUTPUT (LEVEL)
8-to-3	148	LOW	Active-LOW
8-to-3	4532	HIGH	Active-HIGH
10-to-4 (BCD)	147		Active-LOW

DECODERS/DEMULTIPLEXERS

FUNCTION	DEVICE NUMBER	ADDRESS INPUTS	ENABLE (LEVEL)	OUTPUT (LEVEL)
Dual 1 of 4	139	2 + 2	1 (L) + 1 (L)	4 (L) + 4 (L)
Dual 1 of 4	155	2	2 (L) + 1 (L), 1 (H)	4 (L) + 4 (L)
Dual 1 of 4	156	2	2 (L) + 1 (L), 1 (H)	4 (L) + 4 (L)
Dual 1 of 4	539	2 + 2	1 (L) + 1 (L)	4 (H) + 4 (H)
Dual 1 of 4	4555	2 + 2	1 (L) + 1 (L)	4 (H)
Dual 1 of 4	4556	2 + 2	1 (L) + 1 (L)	4 (L)
1 of 8	138	3	2 (L) 1 (H)	8 (L)
1 of 8	237	3	1 (L), 1 (H)	8 (H)
1 of 8	238	3	2 (L), 1 (H)	8 (H)
1 of 8	538	3	2 (L), 2 (H)	8 (H)
1 of 8	82S50	4 (BCD)		8 (L)
1 of 10	42	4 (BCD)		10 (L)
1 of 10, OC	45	4 (BCD)		10 (L)
1 of 10, OC	145	4 (BCD)		10 (L)
1 of 10, OC	445	4 (BCD)		10 (L)
1 of 10	537	4	1 (L), 1 (H)	10 (H)
1 of 10	4028	4 (BCD)		10 (H)
1 of 10	9301	4 (BCD)		10 (L)
1 of 10	82S52	4 (BCD)		10 (L)
1 of 16	154	4	2 (L)	16 (L)
1 of 16	4514	4 (Latched)	1 (L)	16 (H)
1 of 16	4515	4 (Latched)	1 (L)	16 (L)
Octal, with Address Latches and Acknowledge	547	3	1 (L), 2 (H)	8 (L)
Octal, with Acknowledge	548	3	2 (L), 2 (H)	8 (L)
BCD to 7 Segment Decoder/Driver	4511	4 (Latched)	1 (L)	7 (H)
BCD to 7 Segment Decoder/Driver	4543	4 (Latched)		7 (H)

BUFFERS, DRIVERS AND RECEIVERS

FUNCTION	DEVICE NUMBER	OUTPUT
Quad 2-Input NOR Buffer	128	
Quad Buffer	4041	True, Comp
Hex Buffer	4049	Comp
Hex Buffer	4050	True
Strobed Hex Inverter/Buffer	4502	Comp
Dual 4-Input NAND Line Driver	140	
Dual Line Driver (AND/OR)	8T13	
Dual EIA-232B/MIL Line Driver	8T15	Comp
Dual EIA-232B/MIL Receiver	8T16	
Dual Line Driver for IBM 360/370 Interface	8T23	
Dual Line Receiver for IBM 360/370 Interface	8T24	
Hex Bus Receiver (DM8837)	8T37	

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Function Cross Reference Guide

OPEN COLLECTOR, BUFFERS, DRIVERS, AND TRANSCEIVERS

FUNCTION	DEVICE NUMBER	OUTPUT
Quad Bus Transceiver	8T38	
Quad Bus Transceiver	8T26	Comp
Quad Bus Transceiver	8T28	True
Hex Inverter	05	Comp
Hex Inverter/Driver	06	Comp
Hex Buffer/Driver	07	True
Hex Buffer/Driver	16	Comp
Hex buffer/Driver	17	True
Octal Transceiver	621	True
Octal Transceiver	622	Comp
Octal Transceiver	641, 641-1	True
Octal Transceiver	642, 642-2	Comp
Octal Transceiver and Registers	647	True
Octal Transceiver and Registers	649	Comp
BCD to Decimal Decoder/Driver	45	Active-LOW
BCD to Decimal Decoder/Driver	145	Active-LOW

MULTIVIBRATORS AND PHASE LOCKED LOOPS

FUNCTION	DEVICE NUMBER
Monostable Multivibrator	121
Dual Retriggerable Monostable Multivibrator	123
Dual Monostable Multivibrator	221
Dual Retriggerable Monostable Multivibrator	423
Dual Monostable Multivibrator	4528
Dual Retriggerable Monostable Multivibrator	4538
Monostable/Astable Multivibrator	4047
Digital Phase Locked Loop Filter	297
Phase Locked Loop	4046

COMPARATORS

FUNCTION	DEVICE NUMBER
4-Bit Comparator	85
4-Bit Comparator	4585
5-Bit Comparator	9324
8-Bit Comparator	521
8-Bit Comparator	688

PARITY

FUNCTION	DEVICE NUMBER
8-Bit Odd/Even Parity Checker	180
8-Bit Parity Generator/Checker	8262
8-Bit Parity Generator/Checker	82S62
9-Bit Odd/Even Parity Generator/Checker	280
13-Bit Parity Generator/Checker	4531

ARITHMETIC FUNCTIONS

FUNCTION	DEVICE NUMBER
4-Bit Binary Full Adder, Ripple Carry	83
4-Bit Binary Full Adder, Fast Carry	283
4-Bit Binary Full Adder	4008
4-Bit BCD Full Adder	82S83
4-Bit ALU	181
4-Bit ALU	381
4-Bit ALU	382
4-Bit ALU	82S83
Look Ahead Carry Generator	182
8-Bit Serial/Parallel Two's Complement Multiplier	384
8 x 8 Multiplier w/Latch	557
8 x 8 Multiplier	558
BCD Adder	583
8-Bit Serial Multiplier Adder, Subtractor	784
ALU Function Generator	881
32-Bit Look-Ahead-Carry Generator	882

SPECIAL FUNCTIONS

FUNCTION	DEVICE NUMBER
64-Bit FAST Random Access Memory	189
Memory Error Detector/Corrector, 3-State	630
Memory Error Detector/Corrector, OC	631
Dual-Port RAM Controller with Dynamic Memory Refresh	764
Dual Port RAM Controller without Latch	765
IEC/IEEE Bus Interface	4738
Frequency Synthesizer	4750
A.C. Motor Control Circuit	4752
18-Element Bar Graph LCD Driver	4754

☐ Function not continued in this manual. Please check Technology Selection Guide for appropriate technology—FAST or CMOS.

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Family Characteristic Specifications

INTERFACING COMMON LOGIC FAMILIES

From	To	ECL		TTL				CMOS			
										4000B	
		10K	100K	STD	S	FAST	LS	HC	HCT	$V_{DD} = 5V$	$V_{DD} > 5V$
ECL	10K	D	D	T	T	T	T	T	T	T	T
	100K	D	D	T	T	T	T	T	T	T	T
TTL	STD	T	T	D	D	D	D	P	D	P	T
	S	T	T	D	D	D	D	P	D	P	T
	FAST	T	T	D	D	D	D	P	D	P	T
	LS	T	T	D	D	D	D	P	D	P	T
CMOS	HC	T	T	D	D	D	D	D	D	D	T
	HCT	T	T	D	D	D	D	D	D	D	T
	4000B at 5V	T	T	D	D	D	D	D	D	D	T
	4000B $V_{DD} > 5V$	T	T	T	T	T	T	T	T	T	D

D — Direct interface
P — Pullup resistor required
T — Level translator required

10K & 100K ECL Product List

10K ECL

DEVICE TYPE	DESCRIPTION
10100	Quad 2-Input NOR Gate
10101	Quad OR/NOR Gate
10102	Quad 2-Input NOR Gate
10103	Quad 2-Input OR Gate
10104	Quad 2-Input AND Gate
10105	Triple 2-3-2-Input OR/NOR Gate
10106	Triple 4-3-3-Input NOR Gate
10107	Triple 2-Input Exclusive-OR/Exclusive-NOR Gate
10108	Dual 3-Input AND/NAND Gate
10109	Dual 4-5-Input OR/NOR Gate
10110	Dual 3-Input/3-Output OR Gate (Line Driver)
10111	Dual 3-Input/3-Output NOR Gate (Line Driver)
10113	Quad Exclusive-OR Gate with Enable
10114	Triple Line Receiver
10115	Quad Line Receiver
10116	Triple Line Receiver
10117	Dual 2-Wide 2-3-Input OR-AND/OR-AND-INVERT Gate
10118	Dual 2-Wide 3-Input OR-AND Gate
10119	4-Wide 4-3-3-3-Input OR-AND Gate
10121	4-Wide OR-AND/OR-AND-INVERT Gate
10123	Triple 4-3-3-Input Bus Driver
10124	Quad TTL to ECL Translator
10125	Quad ECL to TTL Translator
10130	Dual D-Type Latch
10131	Dual D-Type Master-Slave Flip-Flop
10132	Dual 2-Input Multiplexer with Clocked D-Type Latches and Common Reset
10133	Quad Latch with D-Type Inputs and Enable Outputs
10134	Dual 2-Input Multiplexer with Clocked D-Type Latches

DEVICE TYPE	DESCRIPTION
10135	Dual J-K Master-Slave Flip-Flop
10136	Universal Hexadecimal Counter
10137	Universal Decade Counter
10141	4-Bit Universal Shift Register
10149	1024-Bit, 4 Bits per Word PROM
10149A	1024-Bit, 4 Bits per Word PROM
10158	Quad 2-to-1 Multiplexer (Non-Inverting)
10159	Quad 2-to-1 Multiplexer (Inverting)
10160	12-Bit Parity Generator/Checker
10161	3-Bit Decoder with 2 Enable Inputs (1-of-8 LOW)
10162	3-Bit Decoder with 2 Enable Inputs (1-of-8 HIGH)
10164	8-Input Multiplexer with Enable Input
10165	8-Input Priority Encoder
10171	Dual 2-Bit Decoder (1-of-4 Lines LOW)
10172	Dual 2-Bit Decoder (1-of-4 Lines HIGH)
10173	Quad 2-Input Multiplexer with Latched Outputs
10174	Dual 4-to-1 Multiplexer with Enable
10175	Quint D-Latch w/Common Reset & 2 Wire-OR Common Clock Inputs
10176	Hex D-Type Master-Slave Flip-Flop
10179	Look-Ahead Carry Block-Arithmetic Functions
10180	Dual High-Speed Adder/Subtractor
10181	4-Bit Logic Unit/Function Generator
10188	Hex Buffer (Non-Inverting)
10189	Hex Inverter
10192	Quad Differential Line Driver
10210	Dual 3-Input/3-Output (High-Speed) OR Gate
10211	Dual 3-Input/3-Output (High-Speed) NOR Gate
10216	Triple Differential OR/NOR Line Receiver (High-Speed)
10231	Dual D-Type Master-Slave Flip-Flop (High-Speed)

100K ECL

DEVICE TYPE	DESCRIPTION
100101	Triple 5-Input Gate
100102	Quint 2-Input Gate
100107	Quint Exclusive-OR/NOR
100112	Quad Driver
100113	Line Driver
100114	Line Receiver
100117	Triple AOI
100118	5-Wide AOI
100122	9-Bit Buffer Gate
100123	Hex Bus Driver
100124	TTL-to-ECL Translator
100125	ECL-to-TTL Translator
100126	Back Plane Driver
100131	Triple D Flip-Flop (2ns)
100136	Multipurpose Counting Register
100141	8-Bit Universal Shift Register
100145	16 x 4 Register File
100149	1024-Bit, 4 Bits per Word PROM
100149A	1024-Bit, 4 Bits per Word PROM
100150	Hex D-Latch
100151	Hex D Flip-Flop

DEVICE TYPE	DESCRIPTION
100155	Quad Multiplexer/Latch
100158	Shift Matrix
100160	Dual 9-Bit Parity
100163	Dual 8-Input Multiplexer
100164	16-Input Multiplexer
100165	Universal Priority Encoder
100166	9-Bit Comparator
100170	Universal Decoder
100171	Triple 4-Input Multiplexer
100175	100K-10K Translator
100179	Carry Look-Ahead Generator
100180	Fast 6-Bit Adder
100181	4-Bit ALU Binary/Decimal
100231	Triple D Flip-Flop (1.8ns)
100255	TTL-100K Translator/Bidirectional
100310	28-Bit ALU (144-Pin)
100330	4 Byte MUX (64-Pin)
100331	16-to-8 Connection Matrix (64-Pin)
100340	4 Byte Comparator w/MUX (64-Pin)
100380	FIFO RAM Controller (144-Pin)

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10K & 100K ECL Selection Guide

DEVICE TYPE	DESCRIPTION
OR/NOR Gates	
10100	Quad 2-Input NOR Gate
10101	Quad OR/NOR Gate
10102	Quad 2-Input NOR Gate
10103	Quad 2-Input OR Gate
10105	Triple 2-3-2-Input OR/NOR Gate
10106	Triple 4-3-3-Input NOR Gate
10109	Dual 4-5-Input OR/NOR Gate
10110	Dual 3-Input/3-Output OR Gate (Line Driver)
10111	Dual 3-Input/3-Output NOR Gate (Line Driver)
10210	Dual 3-Input/3-Output (High-Speed) OR Gate
10211	Dual 3-Input/3-Output (High-Speed) NOR Gate
100101	Triple 5-Input Gate
100102	Quint 2-Input Gate
Exclusive OR/NOR Gates	
10107	Triple 2-Input Exclusive-OR/Exclusive-NOR Gate
10113	Quad Exclusive-OR Gate with Enable
100107	Quint Exclusive-OR/NOR
AND, AND/NAND Gates	
10104	Quad 2-Input AND Gate
10108	Dual 3-Input AND/NAND Gate
AND-OR-Invert Combination Gates	
10117	Dual 2-Wide 2-3-Input OR-AND/OR-AND-INVERT Gate
10118	Dual 2-Wide 3-Input OR-AND Gate
10119	4-Wide 4-3-3-3-Input OR-AND Gate
10121	4-Wide OR-AND/OR-AND-INVERT Gate
100117	Triple AOI
100118	5-Wide AOI
Buffer Gates	
10188	Hex Buffer (Non-Inverting)
10189	Hex Inverter
100122	9-Bit Buffer Gate
Flip-Flops	
10131	Dual D-Type Master-Slave Flip-Flop
10135	Dual J-K Master-Slave Flip-Flop
10176	Hex D-Type Master-Slave Flip-Flop
10231	Dual D-Type Master-Slave Flip-Flop (High-Speed)
100131	Triple D Flip-Flop (2ns)
100151	Hex D Flip-Flop
100231	Triple D Flip-Flop (1.8ns)
Latch	
10130	Dual D-Type Latch
10133	Quad Latch with D-Type Inputs and Enable Outputs
10175	Quint D-Latch w/Common Reset & 2 Wire-OR Common Clock Inputs
100150	Hex D-Latch
Registers/Shift Registers	
10141	4-Bit Universal Shift Register
10175	Quint D-Latch w/Common Reset & 2 Wire-OR Common Clock Inputs
100136	Multipurpose Counting Register
100141	8-Bit Universal Shift Register
100145	16 x 4 Register File
100158	Shift Matrix
100150	Hex D-Latch
100331	16-to-8 Connection Matrix (64-Pin)
Counters	
10136	Universal Hexadecimal Counter
10137	Universal Decade Counter
100136	Multipurpose Counting Register

DEVICE TYPE	DESCRIPTION
Multiplexers/Encoders	
10132	Dual 2-Input Multiplexer with Clocked D-Type Latches and Common Reset
10134	Dual 2-Input Multiplexer with Clocked D-Type Latches
10158	Quad 2-to-1 Multiplexer (Non-Inverting)
10159	Quad 2-to-1 Multiplexer (Inverting)
10164	8-Input Multiplexer with Enable Input
10165	8-Input Priority Encoder
10173	Quad 2-Input Multiplexer with Latched Outputs
10174	Dual 4-to-1 Multiplexer with Enable
100155	Quad Multiplexer/Latch
100163	Dual 8-Input Multiplexer
100164	16-Input Multiplexer
100165	Universal Priority Encoder
100171	Triple 4-Input Multiplexer
100330	4 Byte MUX (64-Pin)
100340	4 Byte Comparator w/MUX (64-Pin)
Decoders/Demuliplexer	
10161	3-Bit Decoder with 2 Enable Inputs (1-of-8 LOW)
10162	3-Bit Decoder with 2 Enable Inputs (1-of-8 HIGH)
10171	Dual 2-Bit Decoder (1-of-4 Lines LOW)
10172	Dual 2-Bit Decoder (1-of-4 Lines HIGH)
100170	Universal Decoder
Arithmetic Operators	
10160	12-Bit Parity Generator/Checker
10179	Look-Ahead Carry Block-Arithmetic Functions
10180	Dual High-Speed Adder/Subtractor
10181	4-Bit Logic Unit/Function Generator
100160	Dual 9-Bit Parity
100166	9-Bit Comparator
100179	Carry Look-Ahead Generator
100180	Fast 6-Bit Adder
100181	4-Bit ALU Binary/Decimal
100310	28-Bit ALU (144-Pin)
Bus and Line Drivers	
10110	Dual 3-Input/3-Output OR Gate (Line Driver)
10111	Dual 3-Input/3-Output NOR Gate (Line Driver)
10123	Triple 4-3-3-Input Bus Driver
10192	Quad Differential Line Driver
100112	Quad Driver
100113	Line Driver
100123	Hex Bus Driver
100126	Back Plane Driver
Receivers	
10114	Triple Line Receiver
10115	Quad Line Receiver
10116	Triple Line Receiver
10216	Triple Differential OR/NOR Line Receiver (High-Speed)
100114	Line Receiver
Translators	
10124	Quad TTL to ECL Translator
10125	Quad ECL to TTL Translator
100124	TTL-to-ECL Translator
100125	ECL-to-TTL Translator
100175	100K-10K Translator
100255	TTL-100K Translator/Bidirectional
Memories	
10149	1024-Bit, 4 Bits per Word PROM
10149A	1024-Bit, 4 Bits per Word PROM
100380	FIFO RAM Controller (144-Pin)

8T/8200/82S00/9300/9600 Availability Guide

DEVICE	DESCRIPTION	AVAIL-ABILITY
8234	2-Input, 4-Bit Digital Multiplexer	A
82S41	Quad Exclusive-OR Gate	A
8242	Quad Exclusive-NOR Gate	A
82S50	Binary-to-Octal Decoder	A
82S52	BCD-to-Decimal Decoder	A
8262	8-Bit Parity Generator/Checker	A
82S62	8-Bit Parity Generator/Checker	A
8266	2-Input, 4-Bit Digital Multiplexer	A
8271	4-Bit Shift Register	A
8273	10-Bit SIPO Shift Register	A
8274	10-Bit PISO Shift Register	A
82S82	4-Bit Arithmetic Unit	A
82S83	4-Bit BCD Adder	A
8881	Quad 2-Input NAND (O/C)	A
8890	Hex Inverter	A
8891	Hex Inverter	A
9309	Dual 4-Input Multiplexer	A
9310	4-Bit Decade Counter	A
9316	4-Bit Binary Counter	A
9322	Data Selector/Multiplexer	A
9324	5-Bit Comparator	A
9334	8-Bit Addressable Latch	A
9386	Quad Exclusive-NOR	A
9602	Dual Monostable Multivibrator	A
8T09	Quad Bus Driver (3-State)	A
8T10	Quad D-Type Bus Latch	A
8T13	Dual Line Driver	A
8T15	Dual EIA/MIL Line Receiver	A
8T16	Dual Communications EIA/MIL Line Receiver	A
8T20	Bidirectional Monostable Multivibrator	A

DEVICE	DESCRIPTION	AVAIL-ABILITY
8T23	Dual Line Driver for IBM 360/370 Interface (75123)	A
8T24	Triple Line Receiver for IBM 360/370 Interface (75124)	A
8T26A	Quad Bus Driver/Receiver	A
8T28	Quad Bus Driver/Receiver (Non-Inverting)	A
8T34	Quad Bus Transceiver (DM8834)	A
8T37	Hex Bus Receiver (DM8837)	A
8T38	Quad Bus Transceiver (DM8838)	A
8T95	Hex Buffer	A
8T96	Hex Inverter	A
8T97	Hex Buffer	A
8T98	Hex Inverter	A
8T125	Octal Transceiver (Inverting)	A
8T126	Quad Bus Driver/Receiver (Inverting)	A
8T127	Quad Bus Driver/Receiver (Inverting)	A
8T129	Quad Bus Driver/Receiver (Non-Inverting)	A
8T245	Octal Transceiver	A
8T380	Quad Bus Receiver	A
8T3404	6-Bit Latch	A
8TS805	Octal Transparent Latch	A
8TS806	Octal Clocked D-Latch	A
8TS807	Octal Transparent Latch, Inverting Outputs	A
8TS808	Octal Clocked D-Latch, Inverting Outputs	A

A = Available

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FAST™ Product Availability Guide

DEVICE	PIN	DESCRIPTION	AVAIL-ABILITY
74F00	14	Quad 2-Input NAND Gate	A
74F02	14	Quad 2-Input NOR Gate	A
74F04	14	Hex Inverter	A
74F08	14	Quad 2-Input NAND Gate	A
74F10	14	Triple 3-Input NAND Gate	A
74F11	14	Triple 3-Input AND Gate	A
74F13	14	Dual 4-Input Schmitt Trigger	A
74F14	14	Hex Schmitt Trigger	A
74F20	14	Dual 4-Input NAND Gate	A
74F27	14	Triple 3-Input NOR Gate	A
74F30	14	8-Input NAND Gate	A
74F32	14	Quad 2-Input OR Gate	A
74F37	14	Quad 2-Input NAND Buffer	A
74F38	14	Quad 2-Input NAND Buffer (O/C)	A
74F40	14	Dual 4-Input NAND Buffer	A
74F51	14	Dual 3-Wide 2-Input AND-NOR	A
74F64	14	AND/OR Invert Gate	A
74F74	14	Dual D-Type Flip-Flop	A
74F83	16	4-Bit Full Adder	P
74F85	16	4-Bit Magnitude Comparator	A
74F86	14	Quad 2-Input Exclusive-OR Gate	A
74F109	16	Dual J-K Flip-Flop	A
74F112	16	Dual J-K Flip-Flop	A
74F113	16	Dual J-K Flip-Flop	A
74F114	16	Dual J-K Flip-Flop	A
74F125	14	Quad Buffer (3-State)	A
74F126	14	Quad Buffer (3-State)	A
74F132	14	Quad 2-Input Schmitt Trigger	A
74F138	16	1-of-8 Decoder/Demultiplexer	A
74F139	16	Dual 1-of-4 Decoder/Demultiplexer	A
74F148	16	8-Bit Priority Encoder	A
74F151	16	8-Input Multiplexer	A
74F153	16	Dual 4-Input Multiplexer	A
74F154	24	1-of-16 Decoder/Demultiplexer	Q1 '87
74F157/A	16	Quad 2-Input Multiplexer NINV	A
74F158/A	16	Quad 2-Input Multiplexer INV	A
74F160A	16	BCD Decade Counter, Asynchronous Reset	A
74F161A	16	4-Bit Binary Counter, Asychronous Reset	A
74F162A	16	BCD Decade Counter, Synchronous Reset	A
74F163A	16	4-Bit Binary Counter, Synchronous Reset	A
74F164	14	8-Bit PISO Shift Register	A
74F166	16	8-Bit Serial/Parallel-In Serial Out	A
74F168	16	4-Bit BCD Decade Up/Down Counter	A
74F169	16	4-Bit Binary Up/Down Counter	A
74F174	16	Hex D Flip-Flop w/Common Master Reset	A

DEVICE	PIN	DESCRIPTION	AVAIL-ABILITY
74F175	16	Quad D Flip-Flop w/Common Master Reset	A
74F181	24	Arithmetic Logic Unit	A
74F182	16	Carry Look-Ahead Generator	A
74F189	16	64-Bit RAM	Q1 '87
74F190	16	Up/Down Decade Counter	Q4 '86
74F191	16	Up/Down Binary Counter	Q4 '86
74F192	16	Up/Down Decade Counter	Q4 '86
74F193	16	Up/Down Binary Counter	Q4 '86
74F194	16	4-Bit Bidirectional Universal Shift Register	A
74F195	16	4-Bit Parallel Access Shift Register	A
74F198	24	8-Bit Bidirectional Universal Shift Register	Q4 '86
74F199	24	8-Bit Parallel-Access Shift Register	Q4 '86
74F240	20	Octal Inverting Bus/Line Driver	A
74F241	20	Octal Bus/Line Driver	A
74F242	14	Quad Bus Transceiver	A
74F243	14	Quad Bus Transceiver	A
74F244	20	Octal Bus/Line Driver	A
74F245	20	Octal Bus Transceiver	A
74F251	16	8-Input Multiplexer (3-State)	A
74F253	16	Dual 4-Input Multiplexer (3-State)	A
74F256	16	Dual 4-Bit Addressable Latch	A
74F257/A	16	Quad 2-Input Multiplexer NINV (3-State)	A
74F258/A	16	Quad 2-Input Multiplexer INV (3-State)	A
74F259	16	8-Bit Addressable Latch	A
74F260	14	Dual 5-Input NOR	A
74F269	24	8-Bit Up/Down Counter	A
74F273	20	Octal D Flip-Flop	A
74F280A/B	14	9-Bit Parity Generator/Checker	A
74F283	16	4-Bit Adder	A
74F298	16	Quad 2-Input Multiplexer w/Storage	A
74F299	20	Octal Shift/Storage Register (3-State)	A
74F322	20	Octal Shift/Storage Register (3-State)	Q4 '86
74F323	20	Octal Shift/Storage Register (3-State)	Q4 '86
74F350	16	4-Bit Shifter (3-State)	A
74F352	16	Dual 4-Input Multiplexer (Inverted '153)	A
74F353	16	Dual 4-Input Multiplexer (Inverted '253)	A
74F365	16	Hex Buffer with Common Enable (3-State)	A
74F366	16	Hex Inverter with Common Enable (3-State)	A
74F367	16	Hex Buffer, 4-Bit and 2-Bit (3-State)	A
74F368	16	Hex Inverter, 4-Bit and 2-Bit (3-State)	A
74F373	20	Octal D-Latch (3-State)	A
74F374	20	Octal D Flip-Flop (3-State)	A
74F377	20	Octal D-Type Flip-Flop with Enable	A
74F378	16	Hex D Flip-Flop with Enable	A
74F379	16	Quad D Flip-Flop with Enable	A

A = Available *no SMD yet.
Q1' 86 = 1st Quarter of 1986 Q2 '86 = 2nd Quarter of 1986 Q3 '86 = 3rd Quarter of 1986

FAST™ Product Availability Guide

DEVICE	PIN	DESCRIPTION	AVAIL-ABILITY
74F381	20	4-Bit Arithmetic Logic Unit	A
74F382	20	4-Bit Arithmetic Logic Unit	A
74F384	16	8-Bit Serial/Parallel Two's Complement Multiplier	Q1 '87
74F385	20	Quad Serial Adder/Subtractor	Q4 '86
74F393	14	Dual Binary Ripple Counter	Q4 '86
74F395	16	4-Bit Cascadable S/R (3-State)	A
74F398	20	4-Bit Flip-Flop, Complementary Outputs	A
74F399	16	4-Bit Flip-Flop, True Outputs	A
74F412	24	Multi-Mode Buffered Latch	Q4 '86
74F432	24	Multi-Mode Buffered Latch	Q4 '86
74F455	24	Octal Buffer w/Parity Generator/Checker	A
74F456	24	Octal Buffer w/Parity Generator/Checker	A
74F521	20	Octal Comparator	A
74F524	20	8-Bit Register Comparator	Q4 '86
74F533	20	Inverting Octal D-Latch (3-State)	A
74F534	20	Inverting Octal D Flip-Flop (3-State)	A
74F537	20	1-of-10 Decoder (3-State)	A
74F538	20	1-of-8 Decoder (3-State)	Q4 '86
74F539	20	Dual 1-of-4 Decoder (3-State)	Q4 '86
74F540	20	Octal Buffer/Line Driver (3-State)	A
74F541	20	Octal Buffer/Line Driver (3-State)	A
74F543	24	Octal Registered Transceiver	Q4 '86
74F544	24	Octal Registered Transceiver	A
74F545	20	Octal Bus Transceiver	A
74F547	20	Octal Decoder/MUX w/Addressable Latches	Q4 '86
74F548	20	Octal Decoder/Multiplier w/Acknowledge	Q4 '86
74F550	28	Octal Registered XCVR w/Flags NINV (3-State)	Q4 '86
74F551	28	Octal Registered XCVR w/Flags INV (3-State)	Q4 '86
74F552	28	Octal Registered XCVR w/Flags INV (3-State)	Q4 '86
74F563	20	Octal D-Latch, Broadside Pinout 'F533	Q4 '86
74F564	20	Octal D Flip-Flop, Broadside Pinout 'F534	Q4 '86
74F568	20	4-Bit BCD Decade Up/Down Counter (3-State)	Q4 '86
74F569	20	4-Bit Binary Up/Down Counter (3-State)	Q4 '86
74F573	20	Octal D-Latch, Broadside Pinout 'F373	Q4 '86
74F574	20	Octal D Flip-Flop, Broadside Pinout 'F374	Q4 '86
74F579	20	8-Bit Up/Down Counter, Common I/O	A
74F582	24	4-Bit BCD ALU	Q4 '86
74F583	16	4-Bit BCD Adder	Q4 '86
74F588	20	GPIB Compatible Octal Transceiver	A
74F595	16	8-Bit Shift Register w/Output Latch	Q4 '86
74F597	16	8-Bit Shift Register w/Input Latch	Q4 '86
74F598	16	8-Bit Shift Register w/Input Latch	Q4 '86
74F604	28	Dual 8-Bit Latch (3-State)	A
74F605	28	Dual 8-Bit Latch (O/C)	A
74F620	20	Octal Bus Transceiver (3-State)	A
74F621	20	Octal Bus Transceiver (O/C)	A
74F622	20	Octal Bus Transceiver (O/C)	A
74F623	20	Octal Bus Transceiver (3-State)	A
74F640	20	Octal Bus Transceiver, Inverting (3-State)	A
74F641	20	Octal Bus Transceiver (O/C)	A
74F642	20	Octal Bus Transceiver, Inverting (O/C)	A
74F646	24	Octal Bus XCVR/Register INV (3-State)	A
74F647	24	Octal Bus XCVR/Register NINV (O/C)	A
74F648	24	Octal Bus XCVR/Register INV (3-State)	A
74F649	24	Octal Bus XCVR/Register NINV (O/C)	A
74F651	24	Octal XCVR/Register INV (3-State)	A
74F652	24	Octal XCVR/Register NINV (3-State)	A
74F653	24	Octal XCVR/Register INV (O/C)	A
74F654	24	Octal XCVR/Register NINV (O/C)	A
74F655A	24	Octal Inverting Buffer w/Parity Generator/Checker	A
74F656A	24	Octal Buffer w/Parity Generator/Checker	A
74F657	24	Octal Bus Transceiver w/Parity Generator/Checker	A
74F670	16	4 × 4 Register File	Q4 '86
74F673A	24	16-Bit Serial-In/Parallel-Out Shift Register	Q4 '86
74F674	24	16-Bit Parallel-In/Serial-Out Shift Register	Q4 '86
74F675	24	16-Bit SIPO Shift Register w/SO Capability	Q4 '86
74F676	24	16-Bit SIPO Shift Register w/SO Capability	Q4 '86
74F711	20	Quint 2-Input Multiplexer	Q1 '87
74F712	24	Quint 3-Input Multiplexer	Q1 '87
74F723	24	Quad 3-Input Multiplexer	Q1 '87
74F725	24	Quad 3-Input Multiplexer	Q1 '87
74F732	20	Quad Data Multiplexer	Q1 '87
74F733	20	Quad Data Multiplexer	Q1 '87
74F764	40	Dual Port RAM Controller with Latch	A
74F765	40	Dual Port RAM Controller without Latch	A
74F779	16	8-Bit Counter w/Common I/O (3-State)	A
74F784	20	8-Bit Serial Multiplier and Adder/Subtractor	Q4 '86
74F804	20	Hex 2-Input NAND Driver	Q4 '86
74F805	20	Hex 2-Input NOR Driver	Q4 '86
74F808	20	Hex 2-Input AND Driver	Q4 '86

A = Available *no SMD yet.
Q1 '86 = 1st Quarter of 1986 Q2 '86 = 2nd Quarter of 1986 Q3 '86 = 3rd Quarter of 1986

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FAST™ Product Availability Guide

DEVICE	PIN	DESCRIPTION	AVAIL-ABILITY
74F821	24	10-Bit Register, Non-Inverting (3-State)	Q1 '87
74F822	24	10-Bit Register, Inverting (3-State)	Q1 '87
74F823	24	9-Bit Register, Non-Inverting (3-State)	Q1 '87
74F824	24	9-Bit Register, Inverting (3-State)	Q1 '87
74F825	24	8-Bit Register, Non-Inverting (3-State)	Q1 '87
74F826	24	8-Bit Register, Inverting (3-State)	Q1 '87
74F827	24	10-Bit Buffer, Non-Inverting (3-State)	A
74F828	24	10-Bit Buffer, Inverting (3-State)	A
74F832	20	Hex 2-Input OR Driver	Q1 '87
74F841	24	10-Bit Latch, Non-Inverting (3-State)	Q4 '86
74F842	24	10-Bit Latch, Inverting (3-State)	Q4 '86
74F843	24	9-Bit Latch, Non-Inverting (3-State)	Q4 '86
74F844	24	9-Bit Latch, Inverting (3-State)	Q4 '86
74F845	24	8-Bit Latch, Non-Inverting (3-State)	Q4 '86
74F846	24	8-Bit Latch, Inverting (3-State)	Q4 '86
74F861	24	10-Bit Transceiver, Non-Inverting (3-State)	Q4 '86
74F862	24	10-Bit Transceiver, Inverting (3-State)	Q4 '86
74F863	24	9-Bit Transceiver, Non-Inverting (3-State)	Q4 '86
74F864	24	9-Bit Transceiver, Inverting (3-State)	Q4 '86
74F881	24	ALU/Function Generator	A
74F882	24	32-Bit Look-Ahead Carry Generator	A
74F1240	20	Octal Buffer, Light Load 'F240	A
74F1241	20	Octal Buffer, Light Load 'F241	A
74F1242	14	Quad Transceiver, Light Load 'F242	A
74F1243	14	Quad Transceiver, Light Load 'F243	A

DEVICE	PIN	DESCRIPTION	AVAIL-ABILITY
74F1244	20	Octal Driver, Light Load 'F244	A
74F1245	20	Octal Bus Transceiver, Light Load 'F245	A
74F1764	48	1MBit DRAM Dual Ported Controller w/Latch	P
74F1765	48	1MBit DRAM Dual Ported Controller w/o Latch	P
74F2952	24	Octal Transceiver, Non-Inverting (3-State)	P
74F2953	24	Octal Transceiver, Inverting (3-State)	P
74F3037	16	30Ω Transmission Line Driver (Quad 2-Input NAND)	A
74F3038	16	30Ω Transmission Line Driver (Quad 2-Input NAND, O/C)	A
74F3040	16	30Ω Transmission Line Driver (Dual 4-Input NAND)	A
74F30240	24	Octal Inverting 30Ω Transmission Line Driver (O/C)	A
74F30244	24	Octal 30Ω Transmission Line/Backplane Driver	Q4 '86
74F30245	24	Octal Transceiver 30Ω Transmission Line Driver (O/C)	A
74F30640	24	Octal Transceiver 30Ω Transmission Line Driver Inverting (O/C)	A

A = Available *no SMD yet.
Q1' 86 = 1st Quarter of 1986 Q2 '86 = 2nd Quarter of 1986 Q3 '86 = 3rd Quarter of 1986

FAST ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGES $V_{CC} = 5V \pm 10\%$; $T_A = 0°C$ to $+70°C$
Plastic DIP	N74F--N
Plastic SO[1]	N74F--D

NOTE:
1. SO package is surface-mounted micro-miniature DIP.

FAST™ Family Characteristics

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		74F	UNIT
V_{CC}	Supply voltage		−0.5 to +7.0	V
V_{IN}	Input voltage		−0.5 to +7.0	V
I_{IN}	Input current		−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state		−0.5 to V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	Standard outputs	40	mA
		3-State outputs	48	mA
		Buffer outputs	128	mA
T_A	Operating free-air temperature range		0 to 70	°C

NOTE:
1. For 3-State outputs, $V_{OUT} = -0.5\,V$ to $5.5\,V$ with $V_{CC} = 0\,V$.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		74F			UNIT
			Min	Typ	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage				0.8	V
I_{IK}	Input clamp current				−18	mA
V_{OH}	HIGH-level output voltage	Open collector			4.5	V
I_{OH}	HIGH-level output current	Standard outputs			−1	mA
		3-State outputs			−3	mA
		Buffer outputs			−15	mA
I_{OL}	LOW-level output current	Standard outputs			20	mA
		3-State outputs			24	mA
		Buffer outputs			64	mA
T_A	Operating free-air temperature range		0		70	°C

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FAST™ Family Characteristics

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER			LIMITS[2] Min	LIMITS[2] Typ[3]	LIMITS[2] Max	UNITS	V_{CC}[4]	CONDITIONS[2]
V_{IH}	Input HIGH Voltage			2.0			V		Recognized as a HIGH Signal over Recommended V_{CC} and T_A Range
V_{IL}	Input LOW Voltage					0.8	V		Recognized as a LOW Signal over Recommended V_{CC} and T_A Range
V_{IK} (V_{DC})	Input Clamp Diode Voltage					−1.2	V	Min	$I_{IN} = -18mA$
V_{OH}	Output HIGH Voltage	Std[5]	±10%	2.5	3.4		V	Min	$I_{OH} = -1mA$
			±5%	2.7	3.4		V	Min	$I_{OH} = -1mA$
		3-State	±10%	2.4	3.3		V	Min	$I_{OH} = -3mA$
			±5%	2.7	3.3		V	Min	$I_{OH} = -3mA$
		Buffers	±10%	2.0	3.1		V	Min	$I_{OH} = -15mA$
			±5%	2.0	3.1		V	Min	$I_{OH} = -15mA$
V_{OL}	Output LOW Voltage	Std[5]	±10%		0.35	0.5	V	Min	$I_{OL} = 20mA$
			±5%		0.35	0.5	V	Min	$I_{OL} = 20mA$
		3-State	±10%		0.35	0.5	V	Min	$I_{OL} = 24mA$
			±5%		0.35	0.5	V	Min	$I_{OL} = 24mA$
		Buffers	±10%		0.35	0.5	V	Min	$I_{OL} = 48mA$
			±5%		0.40	0.55	V	Min	$I_{OL} = 84mA$
I_I	Input HIGH Current Breakdown Test	Diode inputs[6]				100	μA	Max	$V_{IN} = 7.0V$
		NPN inputs				100	μA	0.0V	$V_{IN} = 7.0V$
		Transceiver I/O pins				1.0	mA	5.5V	$V_{IN} = 5.5V$
I_{IH}	Input HIGH Current					n(28)	μA	Max	$V_{IH} = 2.7V$ (20μA × n HIGH U.L.)
I_{IL}	Input LOW Current	Diode inputs[6]				n(−600)	μA	Max	$V_{IL} = 0.5V$ (−600μA × n LOW U.L.)
		NPN inputs				n(−20)	μA	Max	$V_{IL} = 0.5V$ (−20μA × n LOW U.L.)
I_{IH} + I_{OZH}	Input HIGH Current (I/O pins)					n(20) +50	μA	Max	$V_{IH} = 2.7V$ (20μA × n HIGH U.L.)
I_{IL} + I_{OZL}	Input LOW Current (I/O pins)	Diode inputs[6]				n(−0.6)	μA	Max	$V_{IL} = 0.5V$ (−0.5μA × n LOW U.L.)
		NPN inputs				n(−20) +50	μA	Max	$V_{IL} = 0.5V$ (−20μA × n LOW U.L.)
I_{OZH}	3-State OFF Current HIGH					50	μA	Max	$V_{OUT} = 2.7V$
I_{OZL}	3-State OFF Current LOW					−50	μA	Max	$V_{OUT} = 0.5V$
I_{OH}	Open-Collector Output Leakage					250	μA	Min	$V_{OH} = 4.5V$
I_{OS}[7]	Output Short-Circuit Current	Std.[5] 3-State		−80		−158	μA	Max	$V_{OUT} = 0V$
		Buffer Driver		−100		−225	μA	Max	$V_{OUT} = 0V$

NOTE:

1. Unless otherwise noted, conditions and limits apply throughout the temperature range for which the particular device type is rated. The ground pin is the reference level for all applied and resultant voltages.
2. Unless otherwise stated on individual data sheets.
3. Typical characteristics refer to $T_A = +25°C$ and $V_{CC} = +5.0V$.
4. Min and Max refer to the values listed in the data sheet table of recommended operating conditions.
5. Standard refers to the totem-pole pull-up circuitry commonly used for the particular family, as distinguished from buffers, line drivers or 3-state outputs.
6. On certain part types, Signetics uses a high impedance NPN base input structure to enhance device performance. Parts which have this structure are indicated in the FAST Data Manual. NPN inputs are tested with $V_{CC} = 0V$ and 7.0V at the input. It is necessary to turn V_{CC} off for the NPN input test to measure leakage. Otherwise, the current source is on and the leakage is undetectable.
7. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operation values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} test should be performed last.

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Signetics

FAST 74F455, 74F456
Buffers/Drivers

'F455 Octal Buffer/Line Driver with Parity, Inverting (3-State)
'F456 Octal Buffer/Line Driver with Parity, Inverting (3-State)
Product Specification

Logic Products

FEATURES

- **High impedance NPN base inputs for reduced loading (20μA in HIGH and LOW states)**
- **'F455 combines 'F240 and 'F280A functions in one package**
- **'F456 combines 'F241 and 'F280A functions in one package**
- **'F455A and 'F456A are center pin versions of the 'F655A and 'F656A respectively**
- **'F455 Inverting**
  'F456 Non-inverting
- **3-State outputs sink 64mA and source 15mA**
- **24-pin plastic slim DIP (300 mil) package**
- **Inputs on one side and outputs on the other side simply PC board layout**

DESCRIPTION

The 'F455 and 'F456 are octal buffers and line drivers with parity generation/checking designed to be employed as memory address drivers, clock drivers and bus-oriented transmitters/receivers. These parts include parity generator/checker to improve PC board density.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F455	3.5ns	70mA
74F456	4.5ns	70mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±10%; T_A = 0°C to +70°C
Plastic DIP	N74F455N, N74F456N
Plastic SOL-24	N74F455D, N74F456D

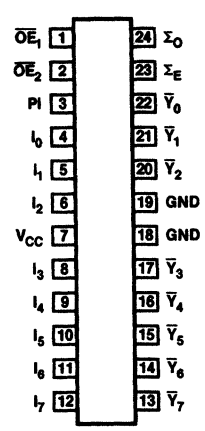
NOTES:
1. SO package is surface-mounted micro-miniature DIP.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I_n	Data inputs	1.0/0.033	20μA/20μA
PI	Parity input	1.0/0.033	20μA/20μA
$\overline{OE}_1$, $\overline{OE}_2$	3-State output enable inputs (active LOW)	1.0/0.033	20μA/20μA
$\overline{Y}_n$	Data outputs ('F455)	750/106.7	15mA/64mA
Y_n	Data outputs ('F456)	750/106.7	15mA/64mA
Σ_E, Σ_O	Parity outputs	750/106.7	15mA/64mA

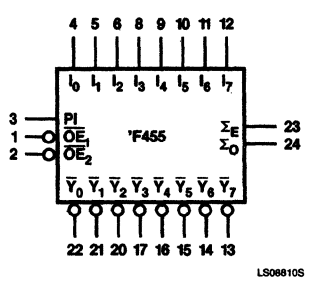
PIN CONFIGURATION

'F455



LOGIC SYMBOL

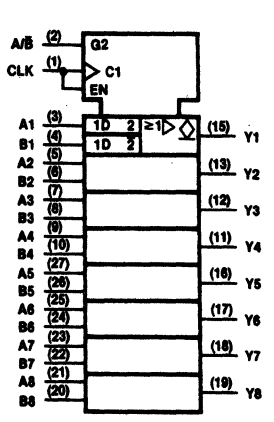
'F455



V_{CC} = Pin 16
GND = Pin 18 and 19

LOGIC SYMBOL (IEEE/IEC)

'F455



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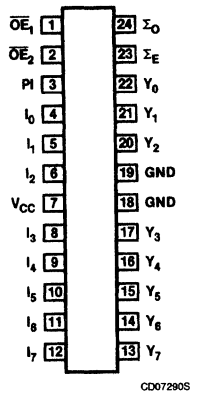
Buffers/Drivers

FAST 74F455, 74F456

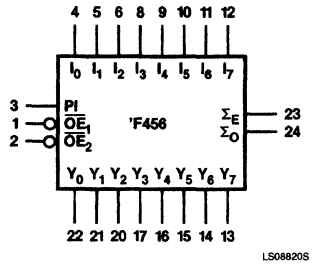
PIN CONFIGURATION

'F456



LOGIC SYMBOL

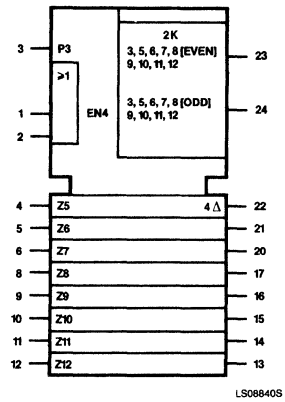
'F456



V_{CC} = Pin 16
GND = Pin 18 and 19

LOGIC SYMBOL (IEEE/IEC)

'F456



FUNCTION TABLES

INPUTS			DATA OUTPUTS	
$\overline{OE}_1$	$\overline{OE}_2$	I_n	'F455	'F456
L	L	L	H	L
L	L	H	L	H
H	X	X	(Z)	(Z)
X	H	X	(Z)	(Z)

H = HIGH voltage level
L = LOW voltage level
X = Don't care
(Z) = HIGH impedance level

INPUTS	PARITY OUTPUTS	
Number of inputs HIGH (PI, $I_0 - I_7$)	Σ_E	Σ_O
Even – 0, 2, 4, 6, 8	H	L
Odd – 1, 3, 5, 7, 9	L	H
Any $\overline{OE}$ = HIGH	(Z)	(Z)

Signetics

Signetics

FAST 74F646, 74F648
Transceivers/Registers

'F646 — Octal Transceiver/Register, Non-Inverting (3-State)
'F648 — Octal Transceiver/Register, Inverting (3-State)
Preliminary Specification

Logic Products

FEATURES

- **High impedance NPN base inputs for reduced loading (20μA in HIGH and LOW states)**
- **Independent registers for A and B buses**
- **Multiplexed real-time and stored data**
- **Choice of non-inverting and inverting data paths**
- **3-State outputs**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F646	7.5ns	115mA
74F648	7.5ns	115mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±10%; T_A = 0°C to +70°C
Plastic DIP	N74F646N, N74F648N
Plastic SOL-24	N74F646D, N74F648D

NOTES:
1. SO package is surface-mounted micro-miniature DIP.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

DESCRIPTION

These devices consist of bus transceiver circuits with 3-State outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes to a HIGH logic level. Enable $\overline{G}$ and DIR pins are provided to control the transceiver function. In the transceiver mode, data present at the high impedance port may be stored in either the A or B register or both.

The Select (S) controls can multiplex stored and real-time (transparent mode) data. The DIR determines which bus will receive data when the Enable $\overline{G}$ is active (LOW). In the isolation mode (Enable G, HIGH), A data may be stored in the B register and/or B data may be stored in the A register.

When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B, may be driven at a time. Figure 1 demonstrates the four fundamental bus-management functions that can be performed with the 'F646 and 'F648.

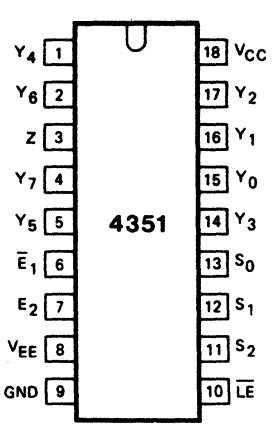
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$A_1 - A_8$, $B_1 - B_8$	A and B inputs	1/0.033	20μA/20μA
CPAB, CPBA	Clock pulse input	1/0.033	20μA/20μA
SAB, SBA	Transmit/receive input	1/0.033	20μA/20μA
DIR, $\overline{G}$	Output enable inputs	1/0.033	20μA/20μA
$A_1 - A_8$, $B_1 - B_8$	A and B outputs	150/33.3	3mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

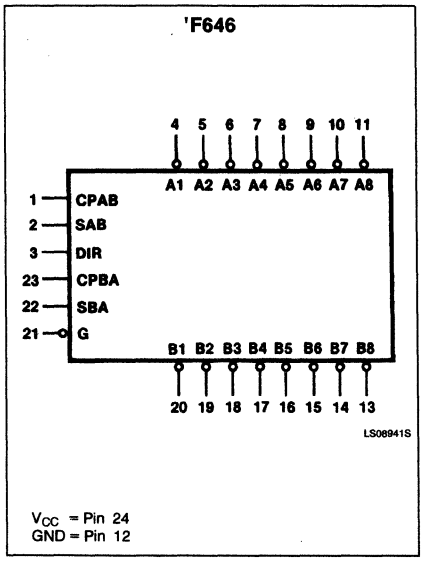
PIN CONFIGURATION

'F646



LOGIC SYMBOL

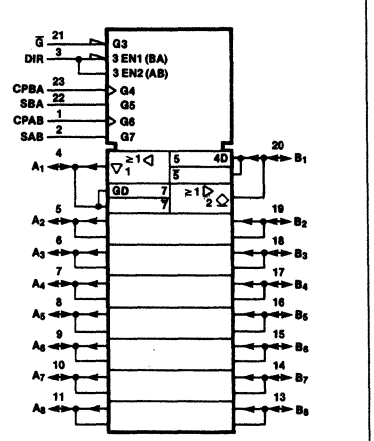
'F646



V_{CC} = Pin 24
GND = Pin 12

LOGIC SYMBOL (IEEE/IEC)

'F646



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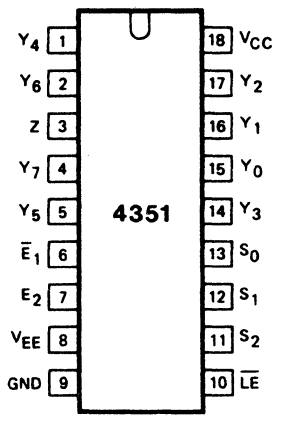
Transceivers/Registers

FAST 74F646, 74F648

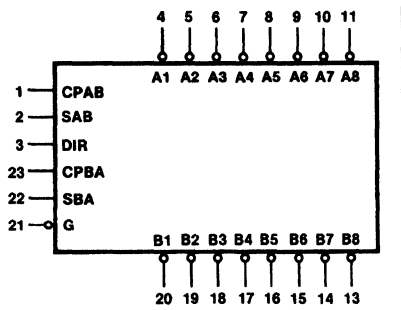
PIN CONFIGURATION

'F648



LOGIC SYMBOL

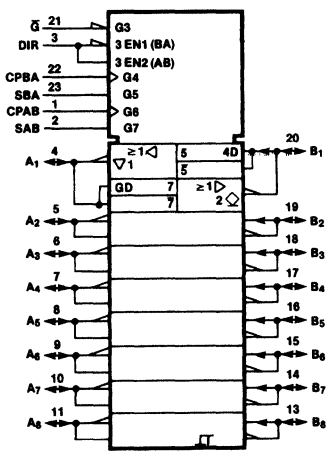
'F648



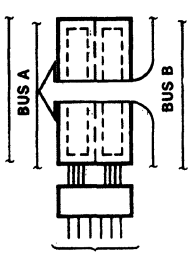
V_{CC} = Pin 24
GND = Pin 12

LOGIC SYMBOL (IEEE/IEC)

'F648

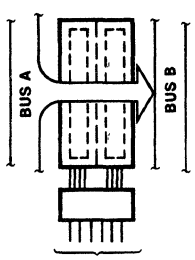


REAL-TIME TRANSFER BUS B TO BUS A



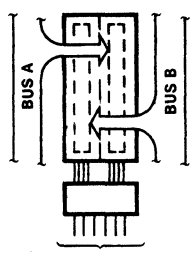
(3) DIR	(21) $\overline{G}$	(1) CPAB	(23) CPBA	(2) SAS	(22) SBA
H	L	X	X	X	L

REAL-TIME TRANSFER BUS A TO BUS B



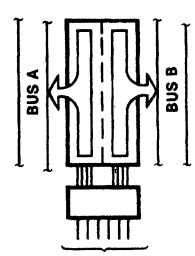
(3) DIR	(21) $\overline{G}$	(1) CPAB	(23) CPBA	(2) SAS	(22) SBA
H	L	X	X	L	X

STORAGE



(3) DIR	(21) $\overline{G}$	(1) CPAB	(23) CPBA	(2) SAS	(22) SBA
X	H	↑	↑	X	X

TRANSFER STORAGE DATA TO A OR B



(3) DIR	(21) $\overline{G}$	(1) CPAB	(23) CPBA	(2) SAS	(22) SBA
L	L	H or L	H or L	X	X
H				H	X

Figure 1

FUNCTION TABLE

INPUTS						DATA I/O*		OPERATION OR FUNCTION	
$\overline{G}$	DIR	CPAB	CPBA	SAB	SBA	$A_1 - A_8$	$B_1 - B_8$	'F646, 'F647	'F648, 'F649
H	X	H or L	H or L	X	X	Input	Input	Isolation	Isolation
H	X	↑	↑	X	X			Store A and B data	Store A and B data
L	L	X	X	X	L	Output	Input	Real time B data to A bus	Real time $\overline{B}$ data to A bus
L	L	X	X	X	H			Stored B data to A bus	Stored $\overline{B}$ data to A bus
L	H	X	X	L	X	Input	Output	Real time A data to B bus	Real time $\overline{A}$ data to B bus
L	H	H or L	X	H	X			Stored A data to B bus	Stored $\overline{A}$ data to B bus

*The data output functions may be enabled or disabled by various signals at the $\overline{G}$ and DIR inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

H = high level X = irrelevant
L = low level ↑ = low-to-high level transition

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FAST 74F655A, 74F656A
Buffers/Drivers

Octal Buffer/Line Driver with Parity
('F655A — Inverting 3-State)
('F656A — Non-Inverting 3-State)
Product Specification

Logic Products

FEATURES

- **Significantly improved AC performance over 'F655 and 'F656**
- **High impedance NPN base input for reduced loading (20μA in HIGH and LOW states)**
- **Ideal in applications where high output drive and light bus loading are required (I_{IL} is 20μA vs FAST std of 600μA)**
- **'F655A combines 'F240 and 'F280 functions in one package**
- **'F656A combines 'F244 and 'F280A functions in one package**
- **'F655A Inverting 'F656A Non-inverting**
- **3-State outputs sink 64mA**
- **Inputs source 15mA**
- **24-pin plastic Slim DIP (300mil) package**
- **Inputs on one side and outputs on the other side simplify PC board layout**
- **Combined functions reduce part count and enhance system performance**

DESCRIPTION

The 'F655A and 'F656A are octal buffers and line drivers with parity generation/checking designed to be employed as memory address drivers, clock drivers and bus-oriented transmitters/receivers. These parts include parity generator/checker to improve PC board density.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F655A	6.5ns	64mA
74F656A	6.5ns	64mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±10%; T_A = 0°C to +70°C
Plastic DIP	N74F655AN, N74F656AN
Plastic SOL-24	N74F655AD, N74F656AD

NOTES:
1. SO package is surface-mounted micro-miniature DIP.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I_n	Data inputs	1.0/0.033	20μA/20μA
PI	Parity input	1.0/0.033	20μA/20μA
$\overline{OE}_1$, $\overline{OE}_2$ $\overline{OE}_3$	3-State output enable inputs (active LOW)	1.0/0.033	20μA/20μA
$\overline{Y}_n$	Data outputs ('F655A)	750/106.7	15mA/64mA
Y_n	Data outputs ('F656A)	750/106.7	15mA/64mA
Σ_E, Σ_O	Parity outputs	750/106.7	15mA/64mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

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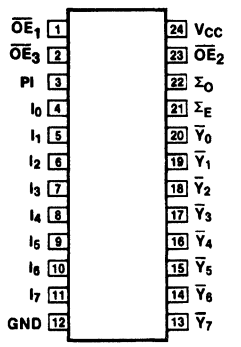
Buffers/Drivers

FAST 74F655A, 74F656A

PIN CONFIGURATION

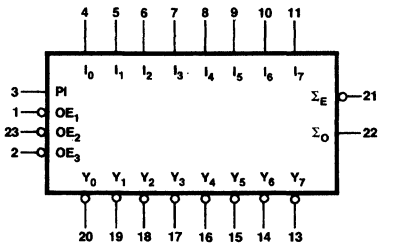
'F655A



CD08061S

LOGIC SYMBOL

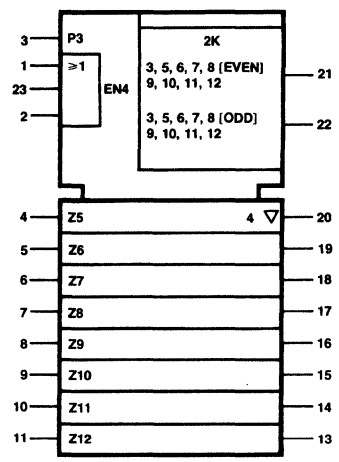
'F655A



LS10340S

LOGIC SYMBOL (IEEE/IEC)

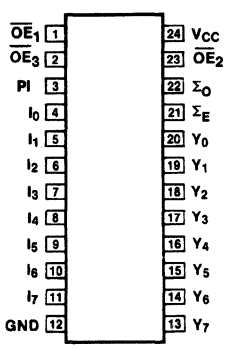
'F655A



LS10310S

PIN CONFIGURATION

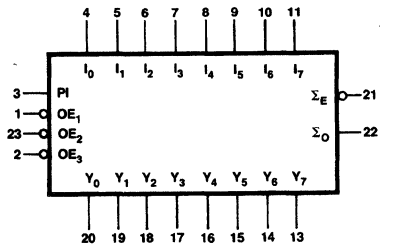
'F656A



CD08071S

LOGIC SYMBOL

'F656A



LS10330S

LOGIC SYMBOL (IEEE/IEC)

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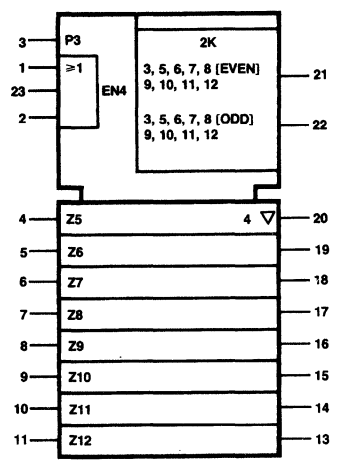


LS10320S

Signetics

FAST 74F657
Transceiver

Octal Bidirectional Transceiver With 8-Bit Parity Generator/Checker (3-State Outputs)
Product Specification

Logic Products

FEATURES

- **High-impedance NPN base input for reduced loading (20μA in HIGH and LOW states)**
- **Ideal in applications where high output drive and light bus loading are required (I_{IL} is 20μA Vs FAST std of 600μA)**
- **24-pin plastic slim dip (300-mil) package**
- **Combines 'F245 and 'F280A functions in one package**
- **3-State outputs**
- **Outputs sink 64mA**
- **15mA source current**
- **Input diodes for termination effects**

DESCRIPTION

The 'F657 contains eight non-inverting buffers with 3-State outputs and an 8-bit parity generator/checker, and is intended for bus-oriented applications. The buffers have a guaranteed current sinking capability of 20mA at the A ports and 64mA at the B ports. The Transmit/Receive (T/$\overline{R}$) input determines the direction of the data flow through the bidirectional transceivers. Transmit (active HIGH) enables data from A ports to B ports; Receive (active LOW) enables data from B ports to A ports.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F657	5ns	120mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±10%; T_A = 0°C to +70°C
Plastic DIP	N74F657N
Plastic SOL-24	N74F657D

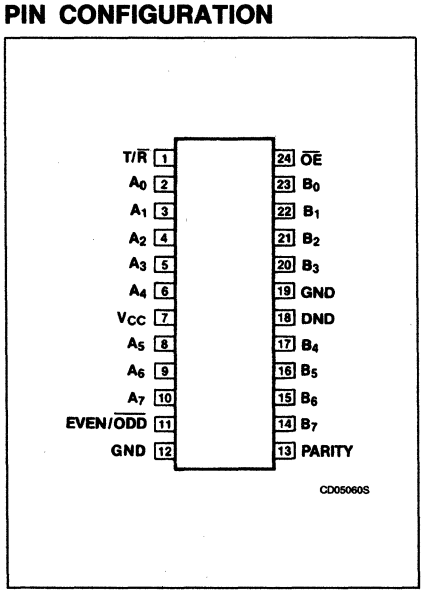
NOTES:
1. SO package is surface-mounted micro-miniature DIP.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

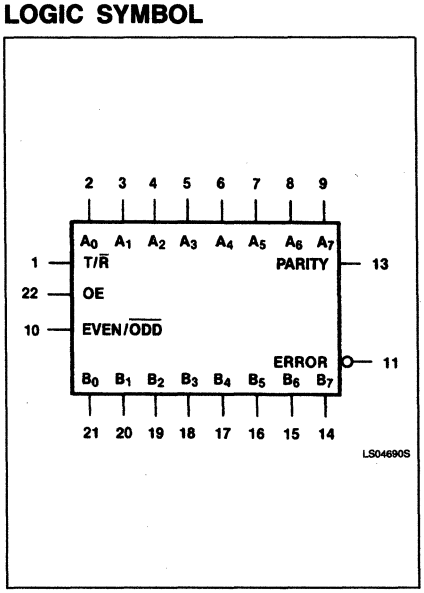
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$A_0 - A_7$	A ports 3-State inputs	5.0/0.167	100μA/100μA
$B_0 - B_7$	B ports 3-State inputs	3.5/0.117	70μA/70μA
PARITY	Parity input	3.5/0.117	70μA/70μA
T/$\overline{R}$	Transmit/receive input	2.0/0.066	40μA/40μA
EVEN/$\overline{ODD}$	EVEN/ODD input	1.0/0.033	20μA/20μA
$\overline{OE}$	Output enable input (active LOW)	2.0/0.066	40μA/40μA
$A_0 - A_7$	A ports 3-State outputs	150/40	3mA/24mA
$B_0 - B_7$	B ports 3-State outputs	750/106.7	15mA/64mA
PARITY	Parity output	150/40	3mA/24mA
$\overline{ERROR}$	Error output	150/40	3mA/24mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

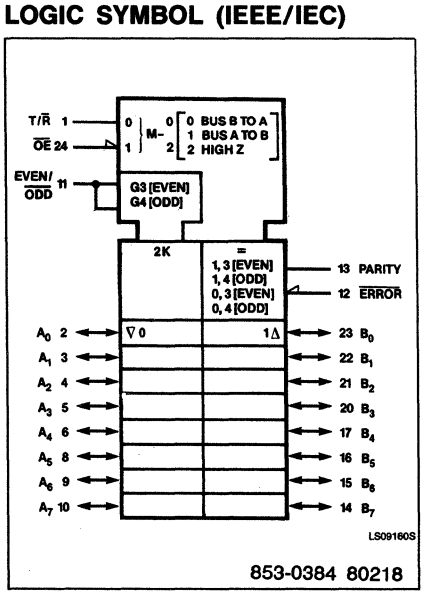
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



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Signetics

FAST 74F1240, F1241 Buffers

'F1240 Octal Inverter Buffer (3-State)
'F1241 Octal Buffer (3-State)
Product Specification

Logic Products

FEATURES

- **High impedance NPN base inputs for reduced loading (20μA in HIGH and LOW states)**
- **Low power, light bus loading**
- **Functional pin for pin equivalent of 'F240 and 'F241**
- **1/30th the bus loading of 'F240 or 'F241**
- **Provides ideal interface and increases fan-out of MOS Microprocessors**
- **Octal bus interface**
- **3-State buffer outputs sink 64mA**
- **15mA source current**

DESCRIPTION

The 'F1240 and 'F1241 are octal buffers that are ideal for driving bus lines or buffer memory address registers. The outputs are capable of sinking 64mA and sourcing up to 15mA, producing very good capacitive drive characteristics. The device features two Output Enables, $\overline{OE}_n$, each controlling four of the 3-State outputs.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F1240	3.5ns	40mA
74F1241	4.5ns	46mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±10%; T_A = 0°C to +70°C
Plastic DIP	N74F1240N, N74F1241N
Plastic SOL-20	N74F1240D, N74F1241D

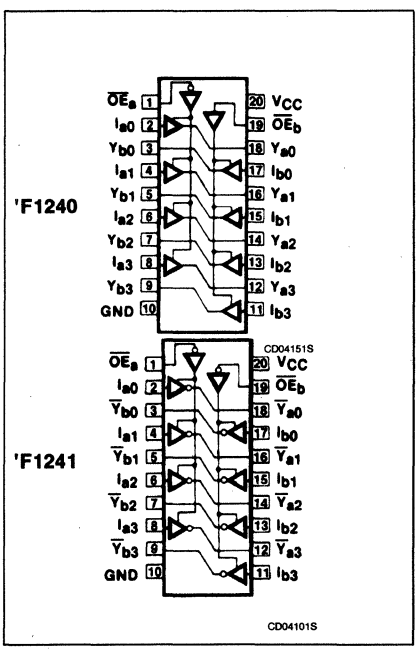
NOTES:
1. SO package is surface-mounted micro-miniature DIP.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

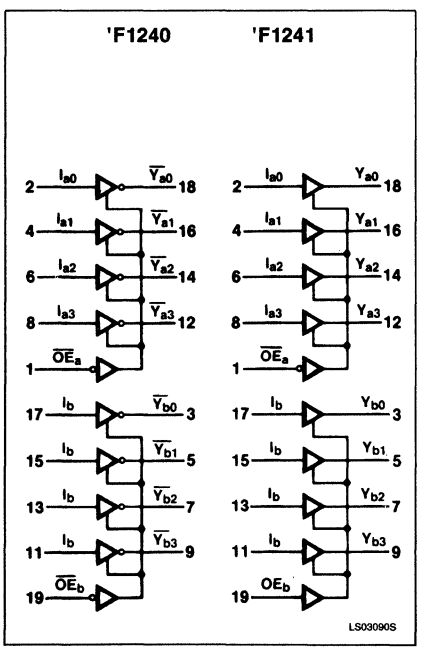
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$\overline{OE}_a$, $\overline{OE}_b$	3-State output enable input (active LOW)	1.0/0.033	20μA/20μA
OE_b	3-State output enable input (active HIGH)	1.0/0.033	20μA/20μA
$I_{a0} - I_{a3}$, $I_{b0} - I_{b3}$	Data inputs	1.0/0.033	20μA/20μA
$\overline{Y}_{a0} - \overline{Y}_{a3}$, $\overline{Y}_{b0} - \overline{Y}_{b3}$ 'F1240	Data outputs	750/106.7	15mA/64mA
$Y_{a0} - Y_{a3}$, $Y_{b0} - Y_{b3}$ 'F1241	Data outputs	750/106.7	15mA/64mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

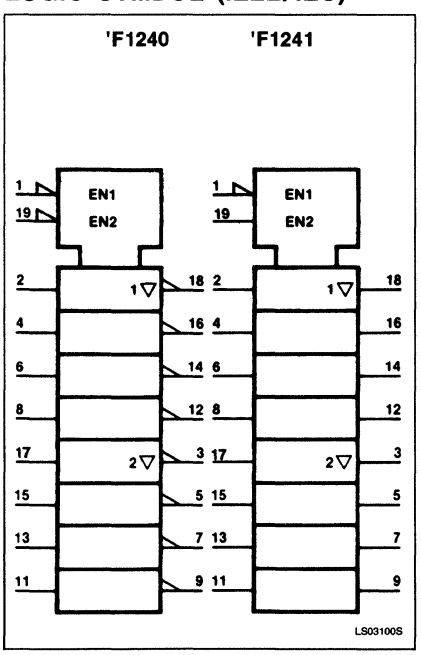
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



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Buffers

FAST 74F1240, F1241

FUNCTION TABLE for 'F1240

INPUTS				OUTPUTS	
$\overline{OE}_a$	I_a	$\overline{OE}_b$	I_b	$\overline{Y}_{an}$	$\overline{Y}_{bn}$
L	L	L	L	H	H
L	H	L	H	L	L
H	X	H	X	(Z)	(Z)

FUNCTION TABLE for 'F1241

INPUTS				OUTPUTS	
$\overline{OE}_a$	I_a	OE_b	I_b	Y_{an}	Y_{bn}
L	L	H	L	L	L
L	H	H	H	H	H
H	X	L	X	(Z)	(Z)

H = HIGH voltage level
L = LOW voltage level
X = Don't care
(Z) = High impedance (off) state

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

	PARAMETER	74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	128	mA
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

	PARAMETER	74F			UNIT
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	HIGH-level output current			−15	mA
I_{OL}	LOW-level output current			64	mA
T_A	Operating free-air temperature	0		70	°C

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FAST 74F166
Shift Register

8-Bit Serial/Parallel-In, Serial Out Shift Register
Product Specification

Logic Products

FEATURES

- **High impedance NPN base inputs for reduced loading (20μA in HIGH and LOW states)**
- **Synchronous parallel to serial applications**
- **Synchronous serial data input for easy expansion**
- **Clock enable for "do nothing" mode**
- **Asynchronous Master Reset**
- **Exandable to 16-bits in 8-bit increments**

DESCRIPTION

The 166 is a high speed 8-bit shift register that has fully synchronous serial parallel data entry selected by an active LOW Parallel Enable ($\overline{PE}$) input. When the $\overline{PE}$ is LOW one set-up time before the LOW-to-HIGH clock transistion, parallel data is entered into the register. When $\overline{PE}$ is HIGH, data is entered into internal bit position Q_0 from Serial Data Input (D_S), and the remaining bits are shifted one place to the right ($Q_0 - Q_1 - Q_2$, etc.), with each positive-going clock transition.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F166	175MHz	41mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±10%; T_A = 0°C to +70°C
Plastic DIP	N74F166N
Plastic SO-16	N74F166D

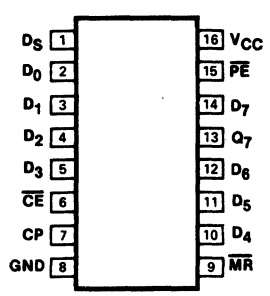
NOTES:
1. SO package is surface-mounted micro-miniature DIP.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

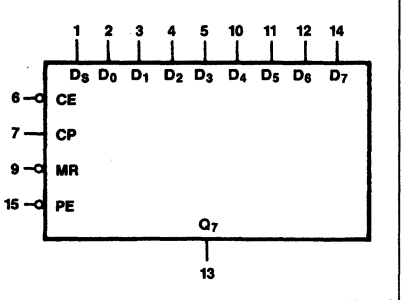
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$\overline{PE}$	Parallel enable input	1/0.033	20μA/20μA
$\overline{CE}$	Clock enable input	1/0.033	20μA/20μA
CP	Clock input (active rising edge)	1/0.033	20μA/20μA
D_s	Serial data input	2/0.066	40μA/40μA
$D_0 - D_7$	Parallel data input	1/0.033	20μA/20μA
$\overline{MR}$	Master Reset input (active LOW)	2/0.066	40μA/40μA
Q_7	Output	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

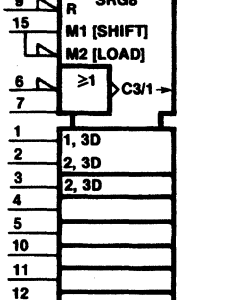
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



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FAST 74F269
8-Bit Counter

8-Bit Bidirectional Binary Counter
Product Specification

Logic Products

FEATURES
- **Synchronous counting and loading**
- **Built-in lookahead carry capability**
- **Count frequency 115MHz typ**
- **Supply current 95mA typ**

DESCRIPTION
The 'F269 is a fully synchronous 8-stage up/down counter featuring a preset capability for programmable operation, carry lookahead for easy cascading and a U/$\overline{D}$ input to control the direction of counting. All state changes, whether in counting or parallel loading, are initiated by the rising edge of the clock.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F269	115MHz	95mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±10%; T_A = 0°C to +70°C
Plastic DIP	N74F269N
Plastic SOL-24	N74F269D

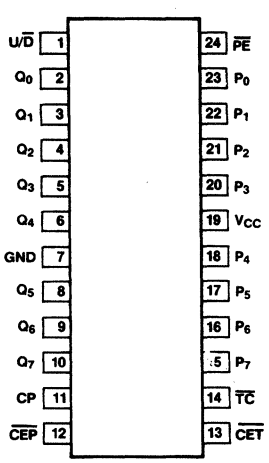
NOTES:
1. SO package is surface-mounted micro-miniature DIP.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

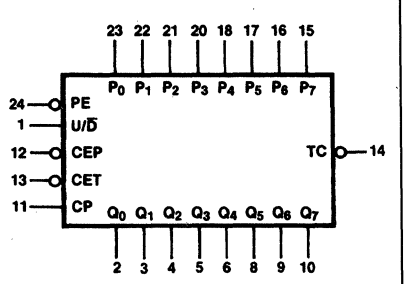
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$P_0 - P_7$	Parallel data inputs	1.0/1.0	20μA/0.6mA
$\overline{PE}$	Parallel enable input (active LOW)	1.0/1.0	20μA/0.6mA
U/$\overline{D}$	Up-Down count control input	1.0/1.0	20μA/0.6mA
$\overline{CEP}$	Count enable parallel input (active LOW)	1.0/1.0	20μA/0.6mA
$\overline{CET}$	Count enable trickle input (active LOW)	1.0/1.0	20μA/0.6mA
CP	Clock input	1.0/1.0	20μA/0.6mA
$\overline{TC}$	Terminal count output (active LOW)	1.0/1.0	20μA/0.6mA
$Q_0 - Q_7$	Flip-flop outputs	50/33	1mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

PIN CONFIGURATION

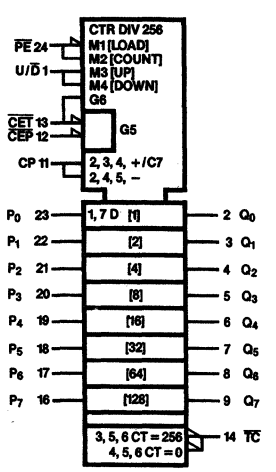


LOGIC SYMBOL



V_{CC} = Pin 19
GND = Pin 7

LOGIC SYMBOL (IEEE/IEC)



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FAST 74F579
Counter

8-Bit Bidirectional Binary Counter (3-State)
Product Specification

Logic Products

FEATURES

- **Multiplexed 3-State I/O ports for bus-oriented applications**
- **Built-in cascading carry capability**
- **Count frequency 115MHz typ**
- **Supply current 100mA typ**
- **Fully synchronous operation**
- **U/$\overline{D}$ pin to control direction of counting**
- **Separate pins for Master Reset and Synchronous Reset**
- **Center power pins to reduce effects of package inductance**
- **See 'F269 for 24-pin separate I/O port version**
- **See 'F779 for 16-pin version**

DESCRIPTION

The 'F579 is a fully synchronous 8-stage up/down counter with multiplexed 3-State I/O ports for bus-oriented applications. It features a preset capability for programmable operation, carry look-ahead for easy cascading and a U/$\overline{D}$ input to control the direction of counting. All state changes, except for the case of asynchronous reset, are initiated by the rising edge of the clock.

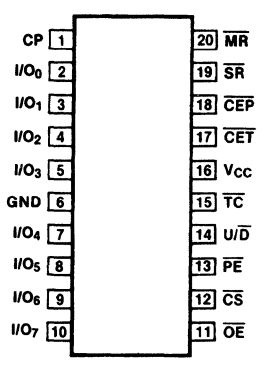
TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F579	115MHz	100mA

ORDERING CODE

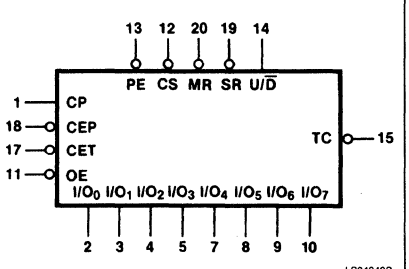
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±10%; T_A = 0°C to +70°C
Plastic DIP	N74F579N
Plastic SOL-20	N74F579D

NOTES:
1. SO package is surface-mounted micro-miniature DIP.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

PIN CONFIGURATION

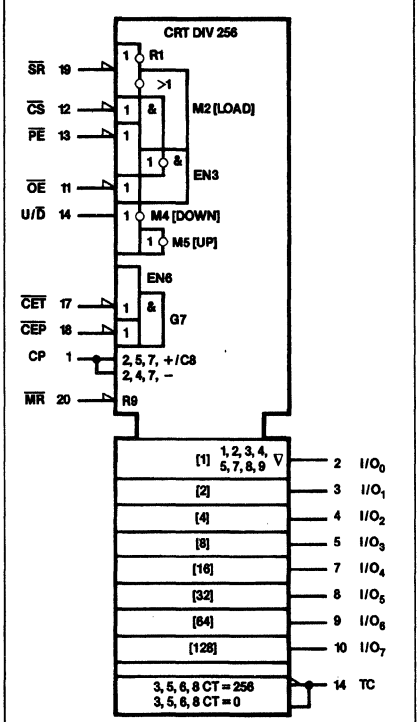


LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 18 and 19

LOGIC SYMBOL (IEEE/IEC)



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Counter

FAST 74F579

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$I/O_0 - I/O_7$	Data inputs	1.0/1.0	20μA/0.6mA
	Data outputs	150/40	3mA/24mA
$\overline{PE}$	Parallel enable input (active LOW)	1.0/1.0	20μA/0.6mA
$U/\overline{D}$	Up-down count control input	1.0/1.0	20μA/0.6mA
$\overline{MR}$	Master reset input (active LOW)	1.0/1.0	20μA/0.6mA
$\overline{SR}$	Synchronous reset input (active LOW)	1.0/1.0	20μA/0.6mA
$\overline{CEP}$	Count enable parallel input (active LOW)	1.0/1.0	20μA/0.6mA
$\overline{CET}$	Count enable trickle input (active LOW)	1.0/1.0	20μA/0.6mA
$\overline{CS}$	Chip select input (active LOW)	1.0/1.0	20μA/0.6mA
$\overline{OE}$	Output enable input (active LOW)	1.0/1.0	20μA/0.6mA
CP	Clock pulse input (active rising edge)	1.0/1.0	20μA/0.6mA
$\overline{TC}$	Terminal count output (active LOW)	150/33	3mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

FUNCTION TABLE

$\overline{MR}$	$\overline{SR}$	$\overline{CS}$	$\overline{PE}$	$\overline{CEP}$	$\overline{CET}$	$U/\overline{D}$	$\overline{OE}$	CP	FUNCTION
X	X	H	X	X	X	X	X	X	I/Oa to I/Oh in High-Z ($\overline{PE}$ disabled)
X	X	L	H	X	X	X	H	X	I/Oa to I/Oh in High-Z
X	X	L	H	X	X	X	L	X	Flip-flop outputs appear on I/O lines
L	X	X	X	X	X	X	X	X	Asynchronous reset for all flip-flops
H	L	X	X	X	X	X	X	↑	Synchronous reset for all flip-flops
H	H	L	L	X	X	X	X	↑	Parallel load all flip-flops
H	H	(not LL)		H	X	X	X	↑	Hold
H	H	(not LL)		X	H	X	X	↑	Hold ($\overline{TC}$ held high)
H	H	(not LL)		L	L	H	X	↑	Count up
H	H	(not LL)		L	L	L	X	↑	Count down

H = HIGH voltage level
L = LOW voltage level
X = Don't Care
↑ = LOW-to-HIGH clock transition not LL means $\overline{CS}$ and $\overline{PE}$ should never both be LOW voltage level at the same time.

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Signetics

FAST 74F779
8-Bit Counter

8-Bit Bidirectional Binary Counter (3-State)
Product Specification

Logic Products

FEATURES

- **Multiplexed 3-State I/O ports**
- **Built-in lookahead carry capability**
- **Count frequency 145MHz typical**
- **Supply current 90mA typical**
- **See 'F269 for 24-pin separate I/O port version**
- **See 'F579 for 20-pin version**

DESCRIPTION

The 'F779 is a fully synchronous 8-stage up/down counter with multiplexed 3-State I/O ports for bus-oriented applications. All control functions (hold, count up, count down, synchronous load) are controlled by two mode pins (S_0, S_1). The device also features carry lookahead for easy cascading. All state changes are initiated by the rising edge of the clock.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F779	145MHz	90mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±10%; T_A = 0°C to +70°C
Plastic DIP	N74F779N
Plastic SOL-16	N74F779D

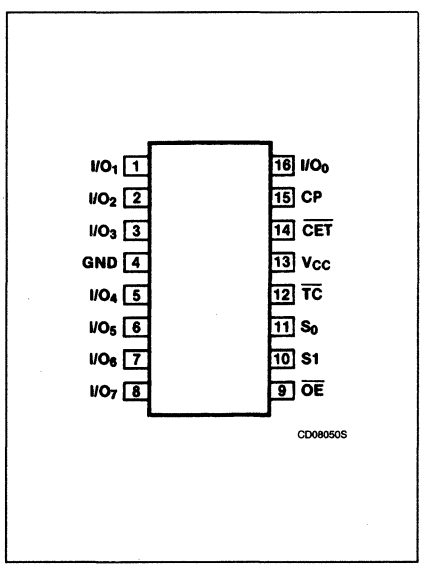
NOTES:
1. SO package is surface-mounted micro-miniature DIP.
2. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

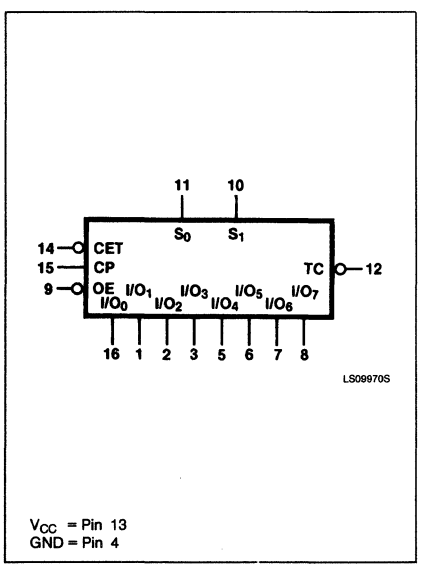
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$I/O_0 - I/O_7$	Data inputs	3.5/1.0	70μA/0.6mA
	Data outputs	150/40	3mA/24mA
S_0, S_1	Select inputs	1.0/1.0	20μA/0.6mA
$\overline{OE}$	Output enable input (active LOW)	1.0/1.0	20μA/0.6mA
$\overline{CET}$	Count enable trickle input (active LOW)	1.0/1.0	20μA/0.6mA
CP	Clock input pulse (active rising edge)	1.0/1.0	20μA/0.6mA
$\overline{TC}$	Terminal count output (active LOW)	50/33	1mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

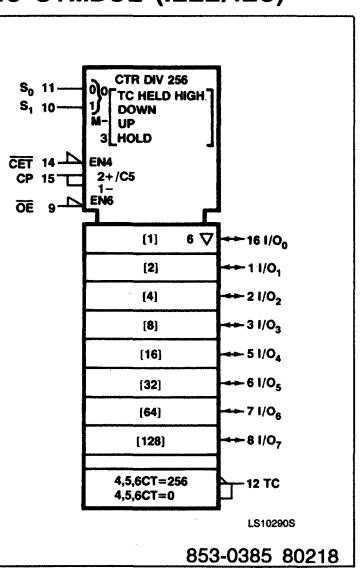
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



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8-Bit Counter

FAST 74F779

FUNCTION TABLE

INPUTS					OPERATING MODE
S1	S0	$\overline{CET}$	$\overline{OE}$	CP	
X	X	X	H	X	I/Oa to I/Oh in HIGH Z
X	X	X	L	X	Flip-flop outputs appear on I/O lines
L	L	X	X	↑	Parallel load all flip-flops
(not LL)		H	X	↑	Hold ($\overline{TC}$ held HIGH)
H	L	L	X	↑	Count up
L	H	L	X	↑	Count down

H = HIGH voltage level
L = LOW voltage level
X = don't care
not LL means S0 and S1 should never both be LOW level at the same time.
↑ = LOW-to-HIGH clock transition

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Signetics

FAST 74F3037
30Ω Line Driver

Quad 2-Input NAND 30Ω Line Driver
Product Specification

Logic Products

FEATURES
- **30Ω line driver**
- **160mA output drive capability in the LOW state**
- **67mA output drive capability in the HIGH state**
- **High speed**
- **Facilitates incident wave switching**
- **3nh lead inductance each on V_{CC} and GND when both side pins are used**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F3037	3.8ns	15mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±10%; T_A = 0°C to +70°C
Plastic DIP	N74F3037N

NOTE:
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A, B	Data inputs	1.0/1.0	20μA/0.6mA
$\overline{Y}$	Data outputs	3350/266	67mA/160mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

DESCRIPTION

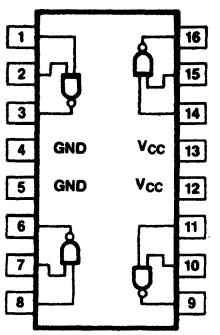
The F3037 is a high current Line driver composed of four 2-input NAND gates. It has been designed to deal with the transmission line effects of PC boards which appear when fast edge rates are used.

The drive capability of the F3037 is 67mA source and 160mA sink with a V_{CC} as low as 4.5 volts. This guarantees incident wave switching with V_{OH} not less than 2.0V and V_{OL} not more than 0.8V while driving impedances as low as 30Ω. This is applicable with any combination of outputs using continuous duty.

The propagation delay of the part is minimally affected by reflections when terminated only by the TTL inputs of other devices. Performance may be improved by full or partial line termination.

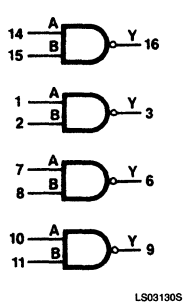
Signetics

PIN CONFIGURATION



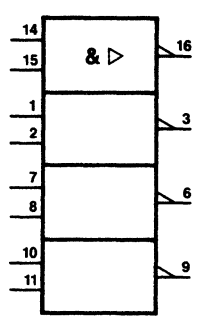
CD04120S

LOGIC SYMBOL



LS03130S

LOGIC SYMBOL (IEEE/IEC)



LS03140S

853-0021 76480

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30Ω Line Driver

FAST 74F3037

FUNCTION TABLE

INPUTS		OUTPUT
A	B	$\overline{Y}$
L	L	H
L	H	H
H	L	H
H	H	L

H = HIGH voltage level
L = LOW voltage level

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

	PARAMETER	74F	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	320	mA
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

	PARAMETER	74F			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	HIGH level input voltage	2.0			V
V_{IL}	LOW level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	HIGH level output current			−67	mA
I_{OL}	LOW level output current			160	mA
T_A	Operating free-air temperature	0		70	°C

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Signetics

SCN2674
Advanced Video Display Controller (AVDC)

Product Specification

Microprocessor Products

DESCRIPTION

The Signetics SCN2674 Advanced Video Display Controller (AVDC) is a programmable device designed for use in CRT terminals and display systems that employ raster scan techniques. The AVDC generates the vertical and horizontal timing signals necessary for the display of interlaced or non-interlaced data on a CRT monitor. It provides consecutive addressing to a user-specified display buffer memory domain and controls the CPU display buffer interface for various buffer configuration modes. A variety of operating modes, display formats and timing profiles can be implemented by programming the control registers in the AVDC.

A minimum CRT terminal system configuration consists of an AVDC, an SCN2671 Keyboard and Communication Controller (PKCC), an SCN2670 Display Character and Graphics Generator (DCGG), an SCB2675 Color/Monochrome Attributes Controller (CMAC), a single-chip microcomputer such as the 8048, a display buffer RAM, and a small amount of TTL for miscellaneous address decoding, interface, and control. Typically, the package count for a minimum system is between 15 and 20 devices; system complexity can be enhanced by upgrading the microprocessor and expanding via the system address and data buses.

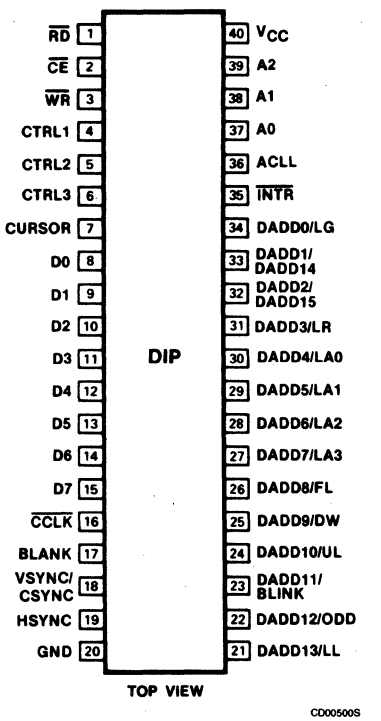
FEATURES

- **2.7MHz and 4MHz character rates**
- **1 to 256 characters per row**
- **1 to 16 raster lines per character row**
- **1 to 128 character rows per frame**
- **Bit-mapped graphics mode**
- **Programmable horizontal and vertical sync generators**
  - **RS-170 compatible sync**
- **Interlaced or non-interlaced operation**
- **Up to 64k RAM addressing for multiple page operation**
- **Readable, writable and incrementable cursor**
  - **Programmable cursor size and blink**
- **AC line lock**
- **Automatic wraparound of RAM**
- **Automatic split screen**
- **Automatic bidirectional soft scrolling**
  - **Programmable scan line increment**
- **Row table addressing mode**
- **Double height tops and bottoms**
- **Double width control output**
- **Selectable buffer interface modes**
- **Dynamic RAM refresh**
- **Completely TTL compatible**
- **Single +5V power supply**
- **Power-on reset circuit**

APPLICATIONS

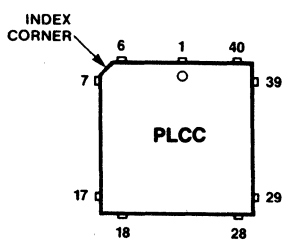
- **CRT terminals**
- **Word processing systems**
- **Small business computers**
- **Home computers**

PIN CONFIGURATIONS



TOP VIEW

CD00500S



TOP VIEW

CD0044PS

Pin	Function	Pin	Function	Pin	Function
1	NC	17	D7	31	DADD6/LA2
2	$\overline{RD}$	18	$\overline{CCLK}$	32	DADD5/LA1
3	$\overline{CE}$	19	BLANK	33	DADD4/LA0
4	$\overline{WR}$	20	VSYNC	34	NC
5	CTRL1		CSYNC/	35	DADD3/LR
6	CTRL2	21	HSYNC	36	DADD2/
7	CTRL3	22	GND		DADD15
8	CURSOR	23	NC	37	DADD1/
9	D0	24	DADD13/LL		DADD14
10	D1	25	DADD12/	38	DADD0/LG
11	D2		ODD	39	$\overline{INTR}$
12	NC	26	DADD11/	40	ACLL
13	D3		BLINK	41	A0
14	D4	27	DADD10/UL	42	A1
15	D5	28	DADD9/DW	43	A2
16	D6	29	DADD8/FL	44	V_{CC}
		30	DADD7/LA3		

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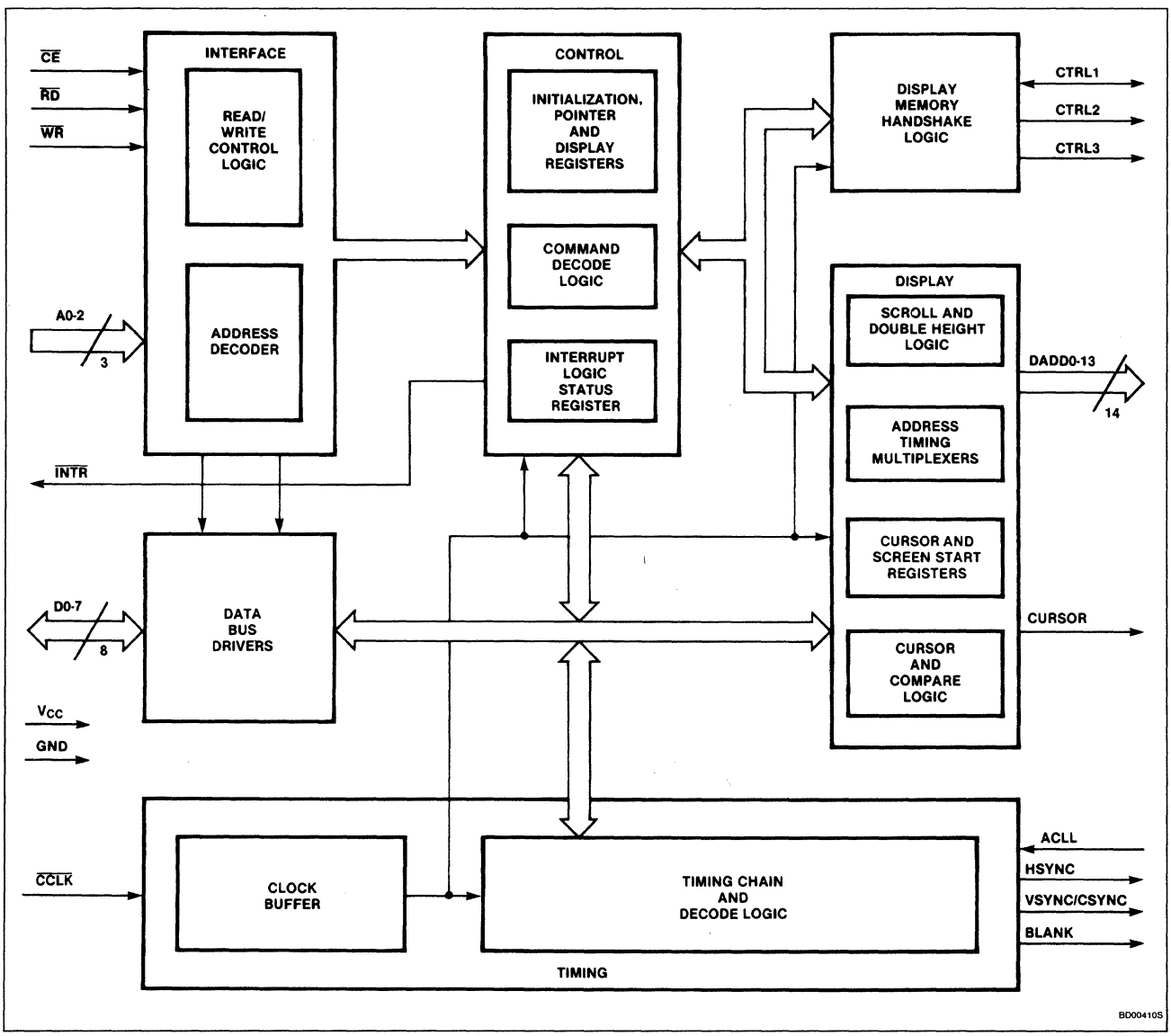
Advanced Video Display Controller (AVDC) SCN2674

ORDERING CODE

PACKAGES	V_{CC} = +5V ±5%, T_A = 0°C to +70°C	
	4MHz	2.7MHz
Ceramic DIP	SCN2674BC4I40	SCN2674BC3I40
Plastic DIP	SCN2674BC4N40	SCN2674BC3N40
Plastic LCC	SCN2674BC4A44	SCN2674BC3A44

BLOCK DIAGRAM



Signetics

Signetics

SCB2675T
Turbo Color/Monochrome Attributes Controller (Turbo-CMAC)

Microprocessor Products

Preliminary Specification

DESCRIPTION

HThe Signetics SCB2675T Turbo Color/Monochrome Attributes Controller (Turbo-CMAC) is a bipolar LSI device designed for CRT terminals and display systems that employ raster scan techniques. It contains a programmable dot clock divider to generate a character clock, a high speed shift register to serialize input dot data into a video stream, latches and logic to apply visual attributes to the resulting display, and logic to display a cursor on the display.

The Turbo-CMAC provides control of visual attributes on a character by character basis for two operating modes: monochrome and color. The monochrome mode provides reverse video, blank, highlight and two general purpose user definable attributes. In this mode, the display characters can be specified to appear on either a light or dark screen background. Retrace video suppression can be automatically or externally controlled. The color mode provides eight colors for foreground (character) video and eight colors for background video together with a luminance output for external color set selection or to simultaneously drive a monochrome monitor. Additionally, both modes provide double width, underline, blink, dot stretching and dot width attributes. In monochrome mode, the SCB2675T emulates the attribute characteristics of Digital Equipment Corporation's VT100 terminal.

The horizontal dot frequency is the basic timing input to the Turbo-CMAC. This clock is divided internally to provide a character clock output for system synchronization. Up to nine bits of dot data are parallel loaded into the video shift register on each character boundary. The two TTL video data outputs in monochrome mode are encoded to provide four video intensities (black, gray, white and highlight). The video data in color mode is encoded to provide eight foreground colors and shifted out on three TTL outputs, together with the luminance output.

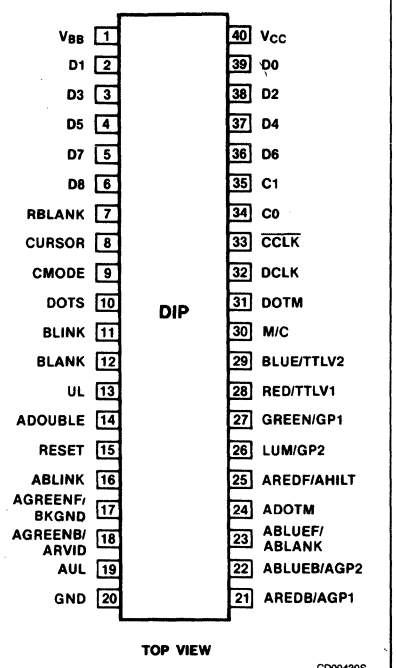
FEATURES

- **40MHz video dot rate version**
- **Four video intensities encoded on two TTL outputs (monochrome mode)**
- **Eight foreground and background colors encoded on three TTL outputs (color mode)**
- **Internally latched character attributes:**
  - **Reverse video**
  - **Blank**
  - **Blink**
  - **Underline**
  - **Highlight**
  - **Two general purpose**
  - **Eight foreground colors**
  - **Eight background colors**
  - **Dot width control**
  - **Double width characters**
- **VT100 compatible attributes**
- **Reverse video cursor with optional white cursor in color mode**
- **Up to 10 dots per character**
- **Light or dark background in monochrome mode**
  - **Automatic retrace blanking**
- **Programmable dot stretching**
- **Compatible with SCN2674 AVDC and SCN2670 DCGG**
- **TTL compatible**
- **40-pin dual in-line package**

APPLICATIONS

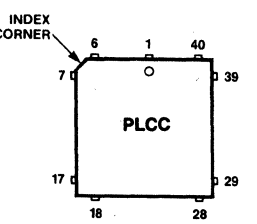
- **CRT terminals**
- **Word processing systems**
- **Small business computers**

PIN CONFIGURATION



TOP VIEW

CD00430S



TOP VIEW

CD0044PS

Pin	Function	Pin	Function
2	V_{BB}	24	AREDB/AGP1
3	D1	25	ABLUEB/AGP2
4	D3	26	ABLUEF/ABLANK
5	D5	27	ADOTM
6	D7	28	AREDF/AHILT
7	D8	29	LUM/GP2
8	RBLANK	30	GREEN/GP1
9	CURSOR	31	RED/TTLV1
10	CMODE	32	BLUE/TTLV2
11	DOTS	33	M/C
13	BLINK	35	DOTM
14	BLANK	36	DCLK
15	UL	37	$\overline{CCLK}$
16	ADOUBLE	38	C0
17	RESET	39	C1
18	ABLINK	40	D6
19	AGREENF/BKGND	41	D4
20	AGREENB/ARVID	42	D2
21	AUL	43	D0
22	GND	44	V_{CC}

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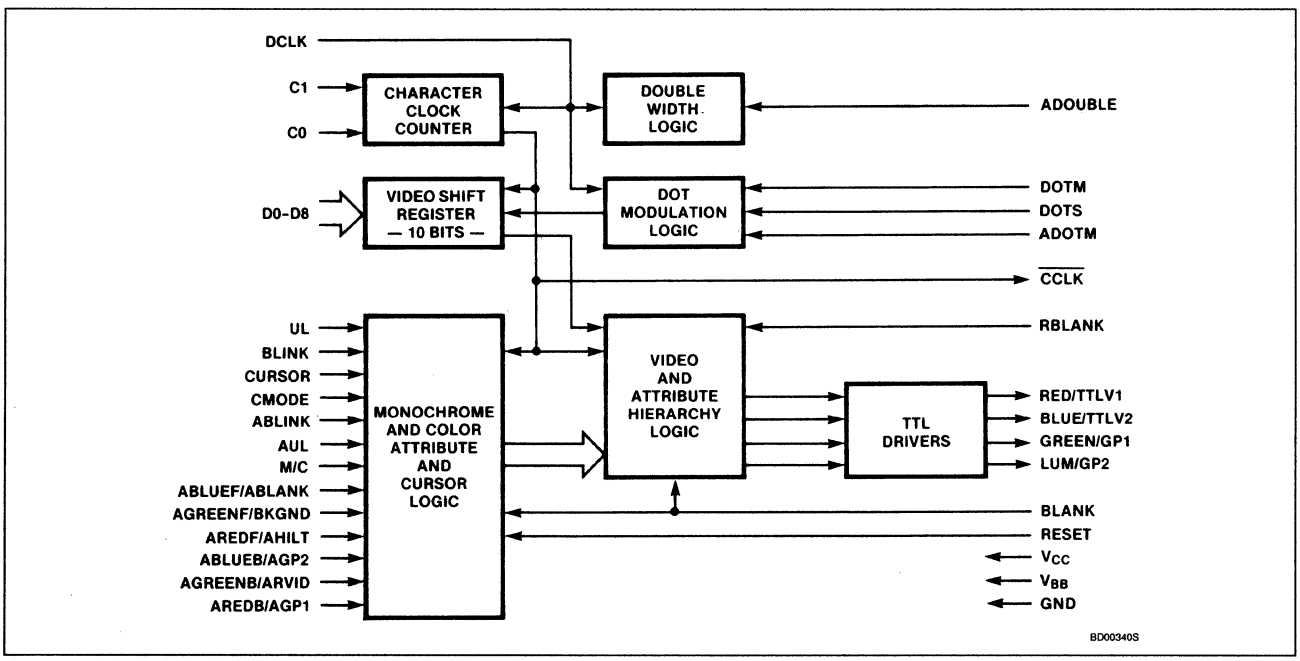
Turbo Color/Monochrome Attributes Controller (Turbo-CMAC) SCB2675T

ORDERING CODE

PACKAGES	DOTS PER CHARACTER	V_{CC} = 5V ± 5%, 0°C to +70°C
		40MHz
Plastic DIP Plastic LCC	7, 8, 9, 10	SCB2675TC4N40 SCB2675TC4A44

BLOCK DIAGRAM



Signetics

Signetics

SCC63484
Advanced CRT Controller (ACRTC)

Objective Specification

Microprocessor Products

DESCRIPTION

The Signetics SCC63484 Advanced CRT Controller (ACRTC) is a CMOS VLSI microcomputer peripheral device capable of controlling raster scan type CRTs to display both graphics and characters. The ACRTC is a new generation CRT controller that is based on a bit-mapped technology and has more display control functions than those of an SCN2674 Advanced Video Display Controller (AVDC).

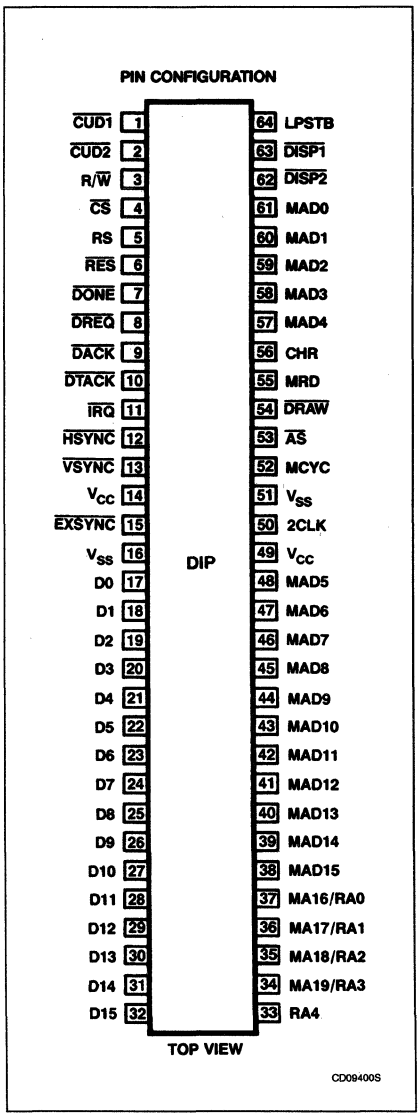
The ACRTC prepares the mechanisms to use in one of three modes; character only, graphic only and multiplexed character/graphic modes. Therefore, the ACRTC can be applied to many applications, from character-only display devices to large full-graphic systems.

The ACRTC can reduce CPU software overhead and enhance system throughput.

FEATURES

- **High-speed graphic drawings**
  - **Drawing rate: maximum 500ns/pixel (color drawing)**
  - **Drawn graphics: Dot, line, rectangle, polyline, polygon, circle, ellipse, paint, copy, etc.**
  - **Drawn colors: 16 bits/word, 1, 2, 4, 8, 16 bits/pixel (5 types) monochrome to max 64k colors**
- **Large frame memory space**
  - **Maximum 2Mbytes graphic memory**
  - **Maximum 128-byte character memory separated from the MPU memory**
  - **Available to maximum 4096 × 4096 high-resolution CRT (1 bit/pixel mode)**
- **Various CRT display controls**
  - **Split screens (3 displays and 1 window)**
  - **Zooming up (1 to 16 times)**
  - **Scroll (vertical and horizontal)**
- **External synchronization**
  - **Synchronization between ACRTCs or between the ACRTC and external device, e.g. TV system or other controller**
- **DMA interface**
- **Two programmable cursors**
- **Three scan modes**
  - **Non-interlace, interlace sync., and interlace sync. and video modes**
- **Interrupt request to MPU**
- **256 characters/line, 32 rasters/line, 4096 rasters/screen**
- **Maximum clock frequency 8MHz**
- **CMOS, +5V single power supply**

PIN CONFIGURATION



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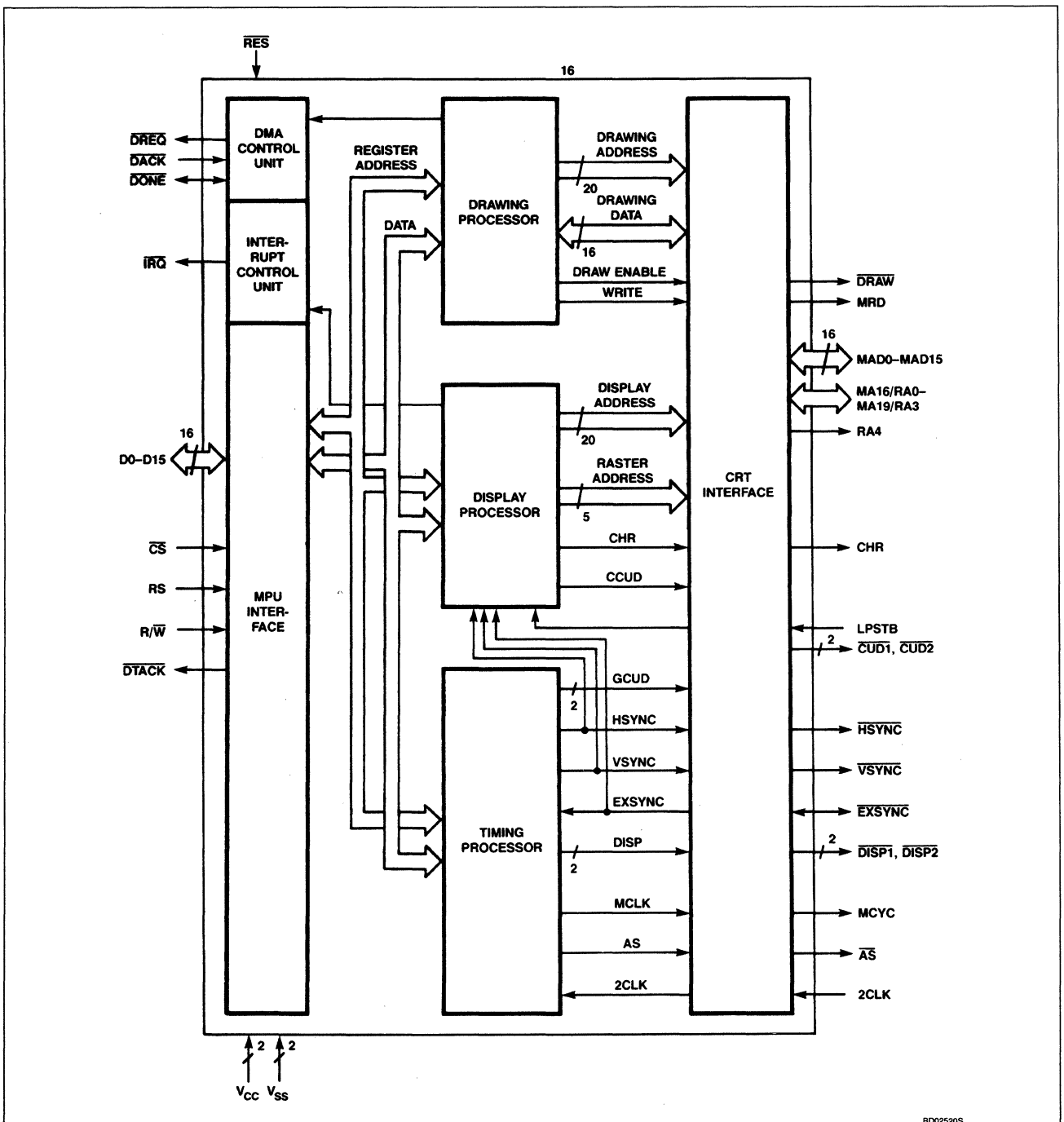
Advanced CRT Controller (ACRTC) SCC63484

ORDERING CODE

PACKAGE	V_{CC} = 5V ± 5%, T_A = 0°C to +70°C		
			8MHz
Plastic DIP			SCC63484C8A64
Ceramic DIP			SCC63484C8I64

BLOCK DIAGRAM



Signetics

SCN2681
Dual Asynchronous Receiver/ Transmitter (DUART)

Product Specification

Microprocessor Products

DESCRIPTION

The Signetics SCN2681 Dual Universal Asynchronous Receiver/Transmitter (DUART) is a single-chip MOS-LSI communications device that provides two independent full-duplex asynchronous receiver/transmitter channels in a single package. It interfaces directly with microprocessors and may be used in a polled or interrupt driven system.

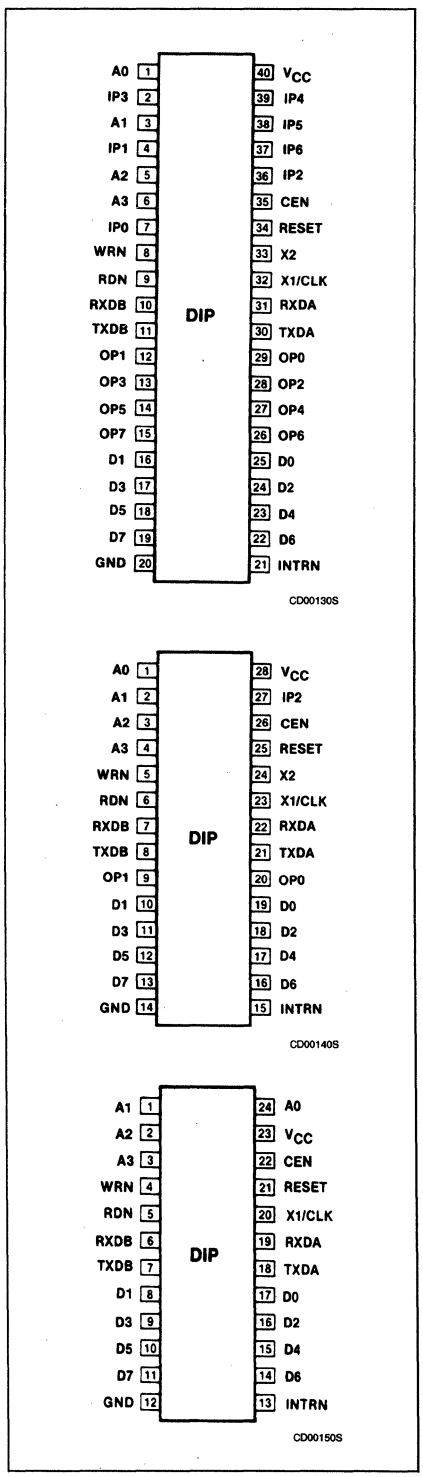
The operating mode and data format of each channel can be programmed independently. Additionally, each receiver and transmitter can select its operating speed as one of eighteen fixed baud rates, a 16× clock derived from a programmable counter/timer, or an external 1× or 16× clock. The baud rate generator and counter/timer can operate directly from a crystal or from external clock inputs. The ability to independently program the operating speed of the receiver and transmitter make the DUART particularly attractive for dual-speed channel applications such as clustered terminal systems.

Each receiver is quadruply buffered to minimize the potential of receiver overrun or to reduce interrupt overhead in interrupt driven systems. In addition, a flow control capability is provided to disable a remote DUART transmitter when the buffer of the receiving device is full.

FEATURES

- **Dual full-duplex asynchronous receiver/transmitter**
- **Quadruple buffered receiver data registers**
- **Programmable data format**
  - **5 to 8 data bits plus parity**
  - **Odd, even, no parity or force parity**
  - **1, 1.5 or 2 stop bits programmable in 1/16-bit increments**
- **Programmable baud rate for each receiver and transmitter selectable from:**
  - **18 fixed rates: 50 to 38.4k baud**
  - **One user-defined rate derived from programmable timer/counter**
  - **External 1× or 16× clock**
- **Parity, framing, and overrun error detection**
- **False start bit detection**
- **Line break detection and generation**
- **Programmable channel mode**
  - **Normal (full-duplex)**
  - **Automatic echo**
  - **Local loopback**
  - **Remote loopback**
- **Multi-function programmable 16-bit counter/timer**
- **Multi-function 7-bit input port**
  - **Can serve as clock or control inputs**
  - **Change of state detection on four inputs**
- **Multi-function 8-bit output port**
  - **Individual bit set/reset capability**
  - **Outputs can be programmed to be status/interrupt signals**
- **Versatile interrupt system**
  - **Single interrupt output with eight maskable interrupting conditions**
  - **Output port can be configured to provide a total of up to six separate wire-ORable interrupt outputs**
- **Maximum data transfer: 1× – 1MB/s, 16× – 125kB/s**
- **Automatic wake-up mode for multidrop applications**
- **Start-end break interrupt/status**
- **Detects break which originates in the middle of a character**
- **On-chip crystal oscillator**
- **TTL compatible**
- **Single +5V power supply**

PIN CONFIGURATIONS



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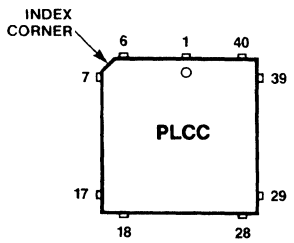
Dual Asynchronous Receiver/Transmitter (DUART) SCN2681

PIN CONFIGURATIONS (Continued)



CD0044PS

Pin	Function	Pin	Function
1	NC	23	NC
2	A0	24	INTRN
3	IP3	25	D6
4	A1	26	D4
5	IP1	27	D2
6	A2	28	D0
7	A3	29	OP6
8	IP0	30	OP4
9	WRN	31	OP2
10	RDN	32	OP0
11	RXDB	33	TXDA
12	NC	34	NC
13	TXDB	35	RXDA
14	OP1	36	X1/CLK
15	OP3	37	X2
16	OP5	38	RESET
17	OP7	39	CEN
18	D1	40	IP2
19	D3	41	IP6
20	D5	42	IP5
21	D7	43	IP4
22	GND	44	V_{CC}

ORDERING CODE

PACKAGES	V_{CC} = +5V ±5%, T_A = 0°C to +70°C			
	24-Pin[1]	28-Pin[2]	40-Pin[2]	44-Pin
Ceramic DIP	Not available	SCN2681AC1I28	SCN2681AC1I40	Not available
Plastic DIP	SCN2681AC1N24	SCN2681AC1N28	SCN2681AC1N40	Not available
Plastic LCC	Not available	Not available	Not available	SCN2681AC1A44

NOTES:
1. [1]400 mil wide DIP
2. [2]600 mil wide DIP

Also provided on the SCN2681 are a multipurpose 7-bit input port and a multipurpose 8-bit output port. These can be used as general purpose I/O ports or can be assigned specific functions (such as clock inputs or status/interrupt outputs) under program control.

The SCN2681 is available in four package versions: 40-pin and 28-pin, both 0.6″ wide DIPs; a compact 24-pin 0.4″ wide DIP; and a 44-pin PLCC.

Signetics

SCN68681
Dual Asynchronous Receiver/ Transmitter (DUART)

Product Specification

Microprocessor Products

DESCRIPTION

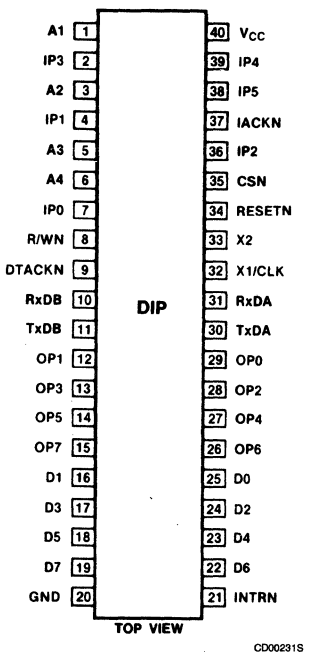
The Signetics SCN68681 Dual Universal Asynchronous Receiver/Transmitter (DUART) is a single-chip MOS-LSI communications device that provides two independent full-duplex asynchronous receiver/transmitter channels in a single package. It is compatible with other S68000 family devices, and can also interface easily with other microprocessors. The DUART can be used in polled or interrupt driven systems.

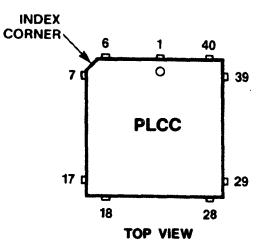
The operating mode and data format of each channel can be programmed independently. Additionally, each receiver and transmitter can select its operating speed as one of eighteen fixed baud rates, a 16× clock derived from a programmable counter/timer, or an external 1× or 16× clock. The baud rate generator and counter/timer can operate directly from a crystal or from external clock inputs. The ability to independently program the operating speed of the receiver and transmitter make the DUART particularly attractive for dual-speed channel applications such as clustered terminal systems.

FEATURES

- **S68000 bus compatible**
- **Dual full-duplex asynchronous receiver/transmitter**
- **Quadruple buffered receiver data registers**
- **Programmable data format**
  - **5 to 8 data bits plus parity**
  - **Odd, even, no parity or force parity**
  - **1, 1.5 or 2 stop bits programmable in 1/16-bit increments**
- **Programmable baud rate for each receiver and transmitter selectable from:**
  - **18 fixed rates: 50 to 38.4K baud**
  - **One user-defined rate derived from programmable timer/ counter**
  - **External 1× or 16× clock**
- **Parity, framing, and overrun error detection**
- **False start bit detection**
- **Line break detection and generation**
- **Programmable channel mode**
  - **Normal (full-duplex)**
  - **Automatic echo**
  - **Local loopback**
  - **Remote loopback**
- **Multi-function programmable 16-bit counter/timer**
- **Multi-function 6-bit input port**
  - **Can serve as clock or control inputs**
  - **Change-of-state detection on four inputs**
- **Multi-function 8-bit output port**
  - **Individual bit set/reset capability**
  - **Outputs can be programmed to be status/interrupt signals**
- **Versatile interrupt system**
  - **Single interrupt output with eight maskable interrupting conditions**
  - **Interrupt vector output on interrupt acknowledge**
  - **Output port can be configured to provide a total of up to six separate wire-ORable interrupt outputs**
- **Maximum data transfer: 1× - 1MB/sec, 16× - 125kB/sec**
- **Automatic wake-up mode for multidrop applications**
- **Start-end break interrupt/status**
- **Detects break which originates in the middle of a character**
- **On-chip crystal oscillator**
- **TTL compatible**
- **Single +5V power supply**

PIN CONFIGURATIONS





Pin	Function	Pin	Function
1	NC	23	NC
2	A1	24	INTRN
3	IP3	25	D6
4	A2	26	D4
5	IP1	27	D2
6	A3	28	D0
7	A4	29	OP6
8	IP0	30	OP4
9	R/WN	31	OP2
10	DTACKN	32	OP0
11	RxDB	33	TxDA
12	NC	34	NC
13	TxDB	35	RxDA
14	OP1	36	X1/CLK
15	OP3	37	X2
16	OP5	38	RESET
17	OP7	39	CSN
18	D1	40	IP2
19	D3	41	IACKN
20	D5	42	IP5
21	D7	43	IP4
22	GND	44	VCC

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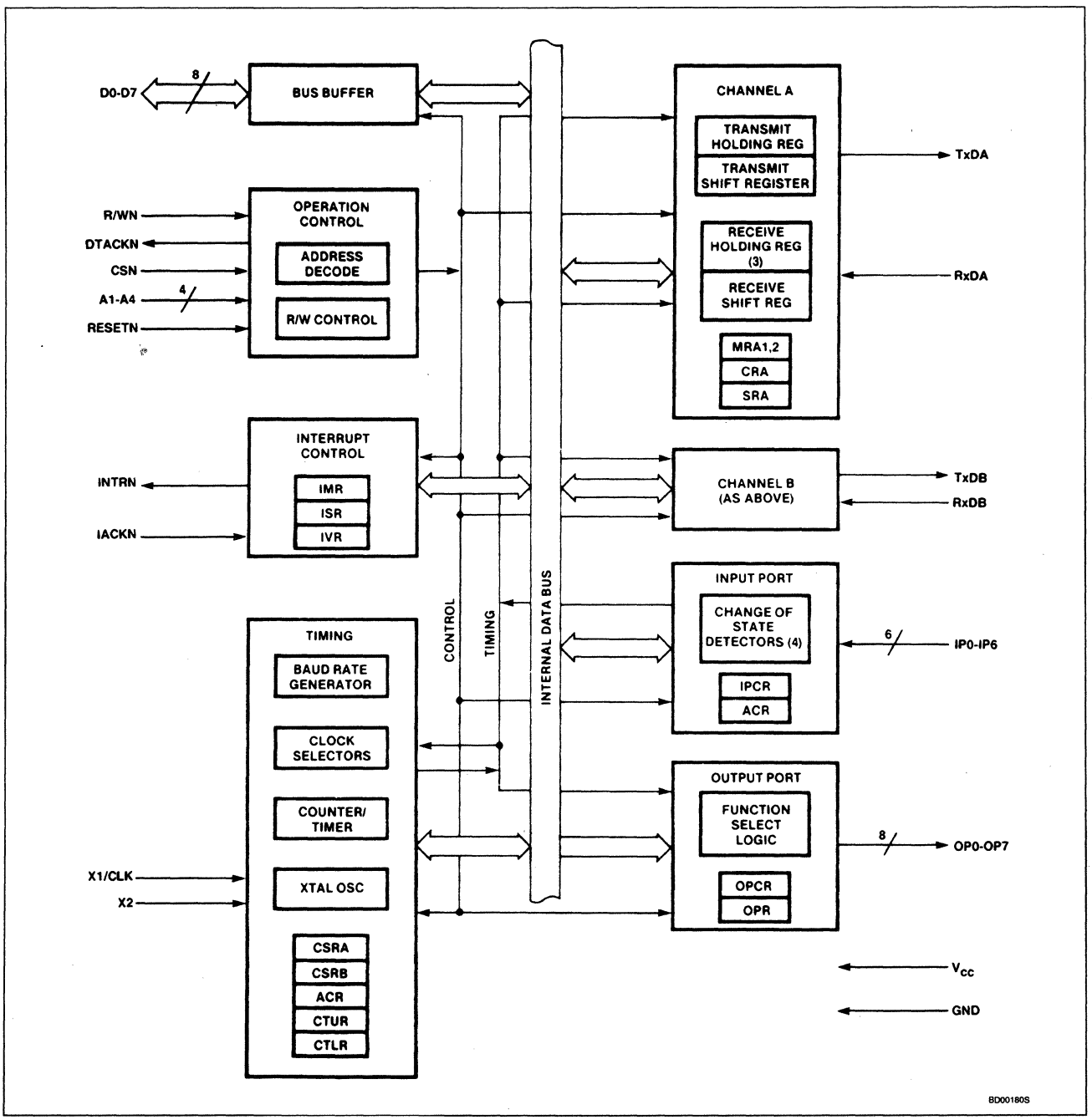
Dual Asynchronous Receiver/Transmitter (DUART) SCN68681

ORDERING CODE

PACKAGES	V_{CC} = +5V ±5%, T_A = 0°C to +70°C
Ceramic DIP	SCN68681C1I40
Plastic DIP	SCN68681C1N40
Plastic LCC	SCN68681CIA44

BLOCK DIAGRAM



Signetics

Signetics

SCC2691
Universal Asynchronous Receiver/Transmitter (UART)

Objective Specification

Microprocessor Products

DESCRIPTION

The Signetics SCC2691 Universal Asynchronous Receiver/Transmitter (UART) is a single-chip CMOS-LSI communications device that provides a full-duplex asynchronous receiver/transmitter in a single 24-pin DIP. It is fabricated with Signetics CMOS technology which combines the benefits of high density and low power consumption.

The operating speed of the receiver and transmitter can be selected independently as one of eighteen fixed baud rates, a 16× clock derived from a programmable counter/timer, or an external 1× or 16× clock. The baud rate generator and counter/timer can operate directly from a crystal or from external clock inputs. The ability to independently program the operating speed of the receiver and transmitter make the UART particularly attractive for dual-speed channel applications such as clustered terminal systems.

The receiver is quadruple buffered to minimize the potential of receiver overrun or to reduce interrupt overhead in interrupt driven systems. In addition, a handshaking capability is provided to disable a remote UART transmitter when the receiver buffer is full.

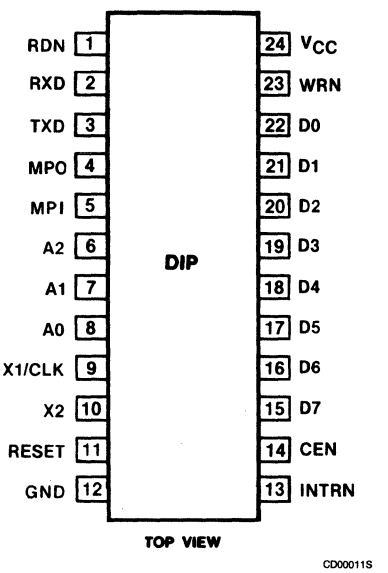
The UART provides a power-down mode in which the oscillator is frozen but the register contents are stored. This results in reduced power consumption on the order of several magnitudes.

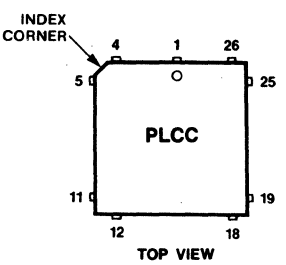
The UART is fully TTL compatible and operates from a single +5V power supply.

FEATURES

- **Full-duplex asynchronous receiver/transmitter**
- **Quadruple buffered receiver data register**
- **Programmable data format:**
  - **5 to 8 data bits plus parity**
  - **Odd, even, no parity or force parity**
  - **1, 1.5 or 2 stop bits programmable in $^1/_{16}$-bit increments**
- **Baud rate for the receiver and transmitter selectable from:**
  - **18 fixed rates: 50 to 38.4k baud**
  - **One user-defined rate derived from programmable timer/counter**
  - **External 1× or 16× clock**
- **Parity, framing, and overrun error detection**
- **False start bit detection**
- **Line break detection and generation**
- **Programmable channel mode**
  - **Normal (full-duplex)**
  - **Automatic echo**
  - **Local loopback**
  - **Remote loopback**
- **Multi-function programmable 16-bit counter/timer**
- **Single interrupt output with seven maskable interrupting conditions**
- **On-chip crystal oscillator**
- **Low power mode**
- **TTL compatible**
- **Single +5V power supply**

PIN CONFIGURATIONS





Pin	Function	Pin	Function
1	NC	15	NC
2	RDN	16	INTRN
3	RXD	17	CEN
4	TXD	18	D7
5	MPO	19	D6
6	MPI	20	D5
7	NC	21	D4
8	A2	22	D3
9	A1	23	NC
10	A0	24	D2
11	X1/CLK	25	D1
12	X2	26	D0
13	RESET	27	WRN
14	GND	28	V_{CC}

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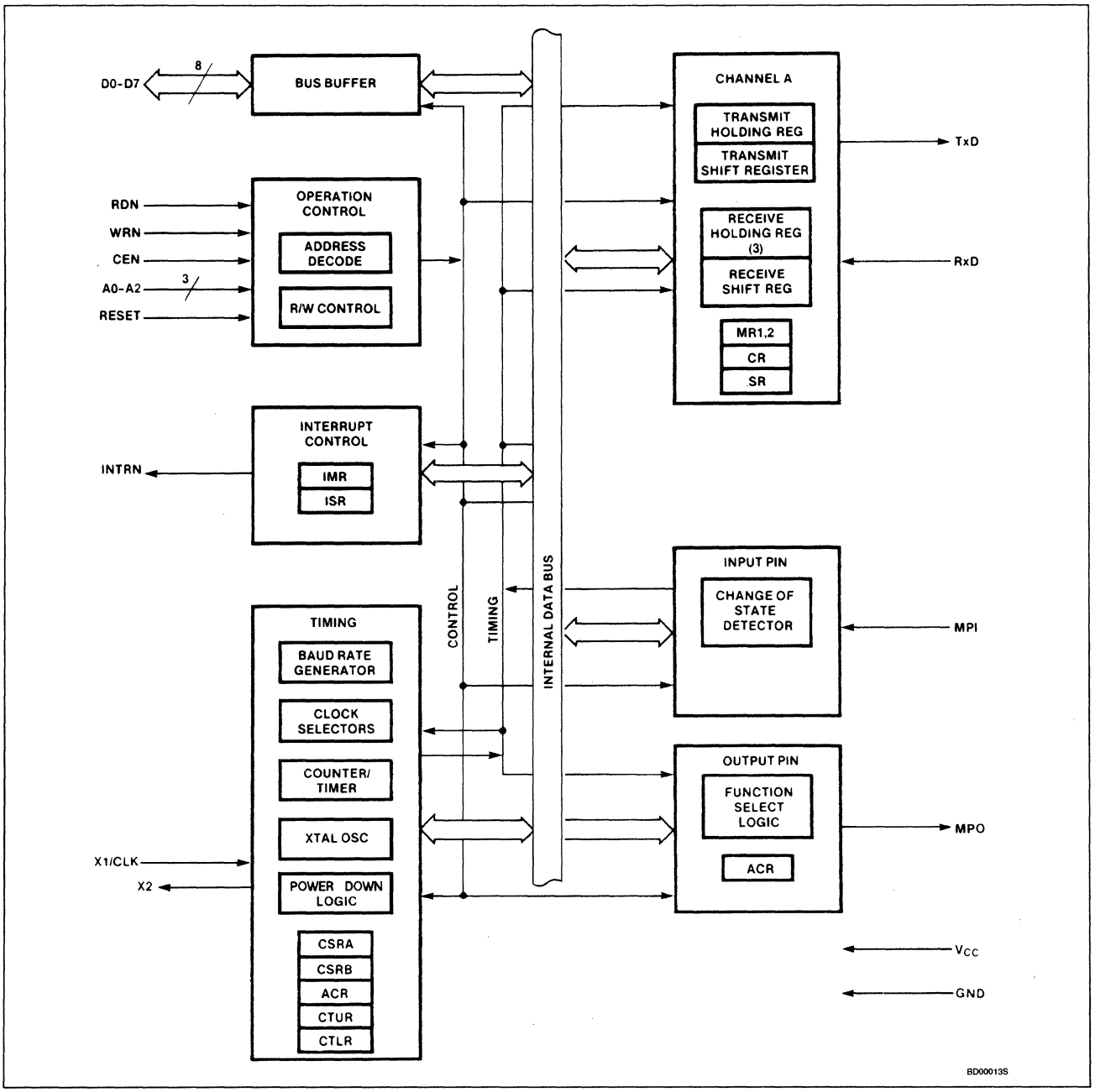
Universal Asynchronous Receiver/Transmitter (UART) SCC2691

ORDERING CODE

PACKAGES	V_{CC} = +5V ± 10%, T_A = 0°C to +70°C
Plastic DIP	SCC2691AC1N24
Plastic LCC	SCC2691AC1A28

BLOCK DIAGRAM



Signetics

Signetics

SCC2698
Octal Universal Asynchronous Receiver/Transmitter (Octal-UART)

Microprocessor Products

Preliminary Specification

DESCRIPTION

The Signetics SCC2698 Octal Universal Asynchronous Receiver/Transmitter (Octal-UART) is a single-chip MOS-LSI communications device that provides an eight-channel full-duplex asynchronous receiver/transmitter in a single package. It is fabricated with Signetics' CMOS technology, which combines the benefits of high density and low power consumption.

The operating speed of each receiver and transmitter can be selected independently as one of eighteen fixed baud rates, a 16× clock derived from a programmable counter/timer, or an external 1× or 16× clock. The baud rate generator and counter/timer can operate directly from a crystal or from external clock inputs. The ability to independently program the operating speed of the receiver and transmitter make the Octal-UART particularly functional for dual-speed channel applications such as clustered terminal systems.

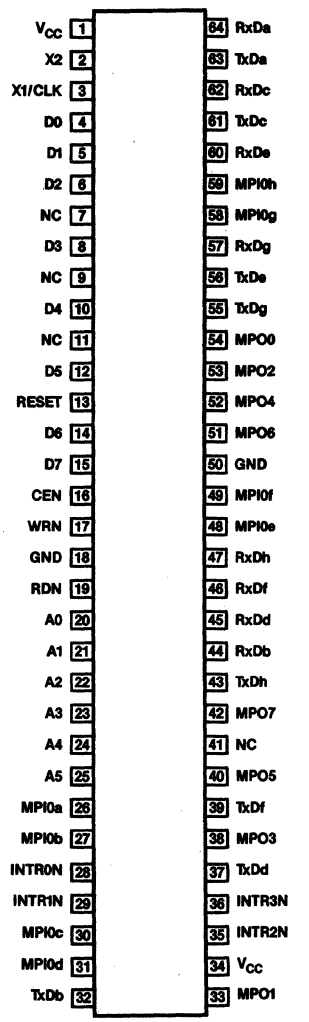
The receiver is quadruply buffered to minimize the potential of receiver overrun, or to reduce interrupt overhead in interrupt driven systems. In addition, a handshaking capability is provided to disable a remote UART transmitter when the receiver buffer is full.

The Octal-UART provides a power-down mode in which the oscillator is frozen but the register contents are stored. This results in reduced power consumption on the order of several magnitudes. The Octal-UART is fully TTL compatible and operates from a single +5V power supply.

FEATURES

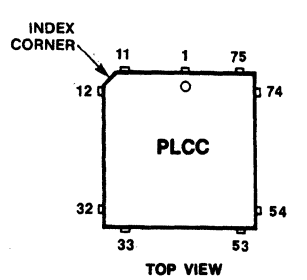
- **Eight full-duplex asynchronous receiver/transmitters**
- **Quadruple buffered receiver data register**
- **Programmable data format:**
  - **5 to 8 data bits plus parity**
  - **Odd, even, no parity or force parity**
  - **1, 1.5 or 2 stop bits programmable in 1/16-bit increments**
- **Baud rate for the receiver and transmitter selectable from:**
  - **18 fixed rates: 50 to 38.4k baud**
  - **One user-defined rate derived from programmable counter/timer**
  - **External 1× or 16× clock**
- **Parity, framing, and overrun error detection**
- **False start bit detection**
- **Line break detection and generation**
- **Programmable channel mode**
  - **Normal (full-duplex), automatic echo, local loopback, remote loopback**
- **Four multi-function programmable 16-bit counter/timers**
- **Single interrupt output with eight maskable interrupting conditions**
- **On-chip crystal oscillator**
- **TTL compatible**
- **Single +5V power supply with low power mode**

PIN CONFIGURATIONS



TOP VIEW

CD09380S



TOP VIEW

CD0045PS

PLCC Pin Functions (Next Page)

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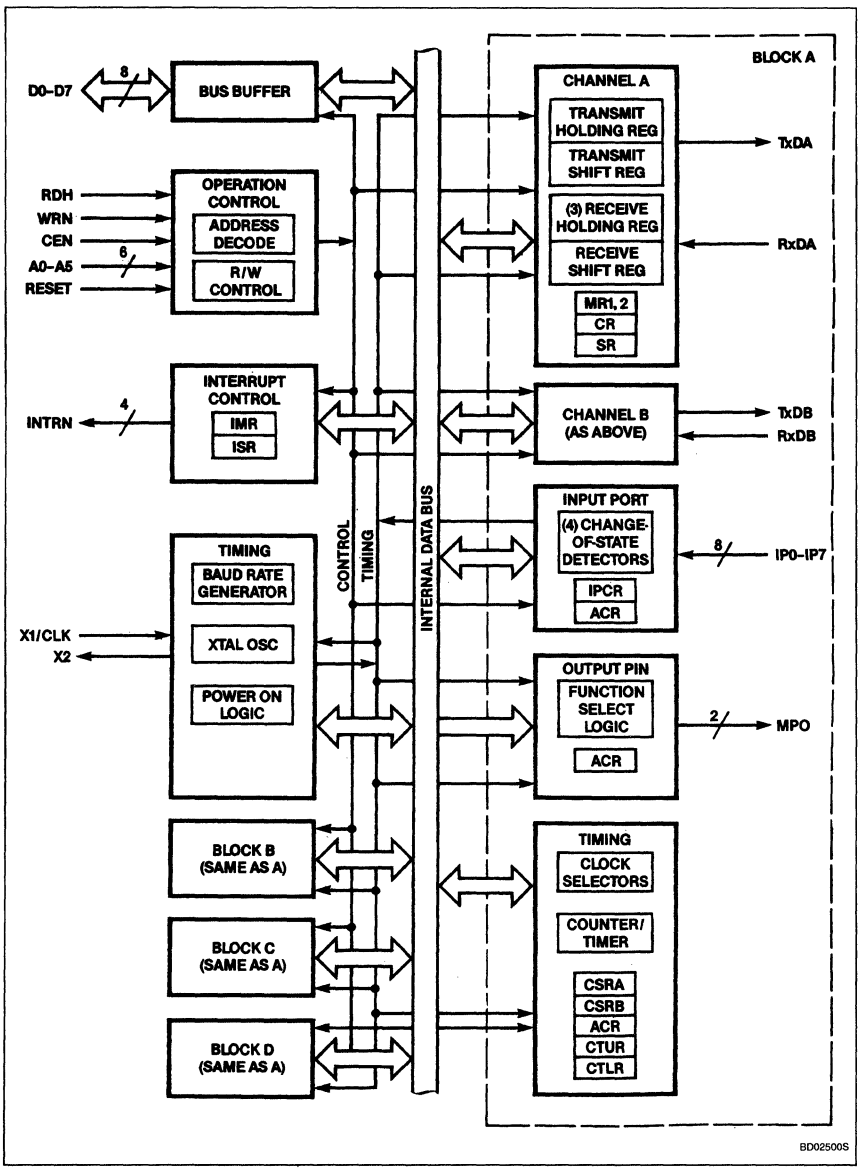
Octal Universal Asynchronous Receiver/Transmitter (Octal-UART)

SCC2698

ORDERING CODE

PACKAGES	$V_{CC} = +5V \pm 5\%$, $T_A = 0$ to $+70°C$
Plastic DIP	SCC2698AC1N64
Plastic LCC	SCC2698AC1A84

BLOCK DIAGRAM



PIN CONFIGURATION (Continued)

PLCC Pin	Function	PLCC Pin	Function
1	TxDa	43	MPO1
2	MPI13g	44	MPI2d
3	RxDa	45	V_{CC}
4	MPI13h	46	INTR2N
5	V_{CC}	47	INTR3N
6	X2	48	MPI3c
7	X1/CLK	49	TxDd
8	D0	50	MPI3d
9	D1	51	MPO3
10	D2	52	TxDf
11	D3	53	MPO5
12	D4	54	MPO7
13	D5	55	TxDh
14	MPI1a	56	RxDb
15	RESET	57	RxDd
16	D6	58	RxDf
17	D7	59	RxDh
18	CEN	60	MPI1e
19	WRN	61	MPI0e
20	GND	62	MPI1f
21	MPI1b	63	MPI0f
22	RDN	64	MPI2e
23	A0	65	GND
24	MPI2a	66	MPI2f
25	A1	67	MPO6
26	MPI2b	68	MPI3e
27	A2	69	MPO4
28	MPI3a	70	MPI3f
29	A3	71	MPO2
30	MPI3b	72	MPO0
31	A4	73	TxDg
32	A5	74	TxDe
33	MPI0a	75	RxDg
34	MPI0b	76	MPI0g
35	INTR0N	77	MPI0h
36	INTR1N	78	MPI1g
37	MPI0c	79	RxDe
38	MPI1c	80	MPI1h
39	MPI0d	81	TxDc
40	MPI1d	82	MPI2g
41	TxDb	83	RxDc
42	MPI2c	84	MPI2h

SCN68562
Dual Universal Serial Communications Controller (DUSCC)

Products

Preliminary Specification

DESCRIPTION

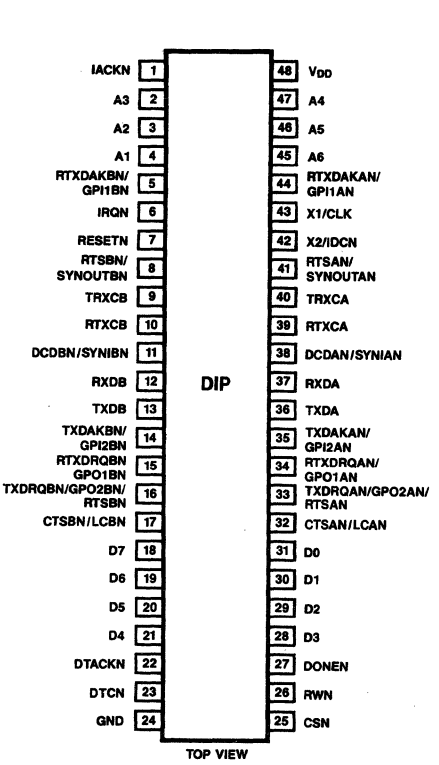
The Signetics SCN68562 Dual Universal Serial Communications Controller (DUSCC) is a single-chip MOS-LSI communications device that provides two independent, multi-protocol, full-duplex receiver/transmitter channels in a single package. It supports bit-oriented and character-oriented (byte count and byte control) synchronous data link controls as well as asynchronous protocols. The SCN68562 interfaces to the 68000 MPU via asynchronous bus control signals and is capable of program-polled, interrupt-driven, block-move or DMA data transfers.

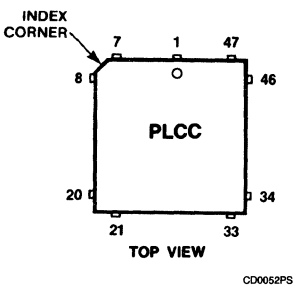
The operating mode and data format of each channel can be programmed independently. Each channel consists of a receiver, a transmitter, a 16-bit multifunction counter/timer, a digital phase-locked loop (DPLL), a parity/CRC generator and checker, and associated control circuits. The two channels share a common bit rate generator (BRG), operating directly from a crystal or an external clock, which provides sixteen common bit rates simultaneously. The operating rate for the receiver and transmitter of each channel can be independently selected from the BRG, the DPLL, the counter/timer, or from an external 1× or 16× clock, making the DUSCC well suited for dual-speed channel applications. Data rates up to 4Mbits are supported.

The transmitter and receiver each contain a four-deep FIFO with appended transmitter command and receiver status bits and a shift register. This permits reading and writing of up to four characters at a time, minimizing the potential of receiver overrun or transmitter underrun, and reducing interrupt or DMA overhead. In addition, a flow control capability is provided to disable a remote transmitter when the FIFO of the local receiving device is full.

Two modem control inputs (DCD and CTS) and three modem control outputs (RTS and two general purpose) are provided. Because the modem control inputs and outputs are general purpose in nature, they can be optionally programmed for other functions.

PIN CONFIGURATIONS





Pin	Function	Pin	Function
1	IACKN	27	CSN
2	A3	28	R/WN
3	A2	29	DONEN
4	A1	30	D3
5	RTxDAKBN/ GPI1BN	31	D2
		32	D1
6	IRQN	33	D0
7	NC	34	NC
8	RESETN	35	CTSAN/LCAN
9	RTSBN/ SYNOUTBN	36	TxDRQAN/ GPO2AN/RTSAN
10	TRxCB	37	RTxDRQAN/ GPO1AN
11	RTxCB		
12	DCDBN/SYNIBN	38	TxDAKAN/GPI2AN
13	NC	39	TxDA
14	RxDB	40	RxDA
15	TxDB	41	NC
16	TxDAKBN/ GPI2BN	42	DCDAN/SYNIAN
		43	RTxCA
17	RTxDRQBN/ GPO1BN	44	TRxCA
		45	RTSAN/ SYNOUTAN
18	TxDRQBN/ GPO2BN/RTSBN	46	X2/IDCN
		47	X1/CLK
19	CTSBN/LCBN	48	RTxDAKAN/ GPI1AN
20	D7	49	A6
21	D6	50	A5
22	D5	51	A4
23	D4	52	V_{DD}
24	DTACKN		
25	DTCN		
26	GND		

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Dual Universal Serial Communications Controller (DUSCC) SCN68562

FEATURES

General Features

- Dual full-duplex synchronous/ asynchronous receiver and transmitter
- Multi-protocol operation
  - BOP: HDLC/ADCCP, SDLC, SDLC loop, X.25 or X.75 link level, e tc.
  - COP: BISYNC, DDCMP, X.21
  - ASYNC: 5 – 8 bits plus optional parity
- Four character receiver and transmitter FIFOs
- 0 to 4MHz data rate
- Programmable bit rate for each receiver and transmitter selectable from:
  - 16 fixed rates: 50 to 38.4K baud
  - One user-defined rate derived from programmable counter/timer
  - External 1× or 16× clock
  - Digital phase-locked loop
- Parity and FCS (frame check sequence LRC or CRC) generation and checking
- Programmable data encoding/ decoding: NRZ, NRZI, FM0, FM1, Manchester
- Programmable channel mode: full-half-duplex, auto-echo, or local loopback
- Programmable data transfer mode: polled, interrupt, DMA, wait
- DMA interface
  - Compatible with Signetics' SCB68430 Direct Memory Access Interface (DMAI) and other DMA controllers
  - Half- or full-duplex operation
  - Single or dual address data transfers
  - Automatic frame termination on counter/timer terminal count or DMA DONE
- Interrupt capabilities
  - Daisy chain option
  - Vector output (fixed or modified by status)
  - Programmable internal priorities
  - Maskable interrupt conditions
  - 68000 compatible
- Multi-function programmable 16-bit counter/timer
  - Bit rate generator
  - Event counter
  - Count received or transmitted characters
  - Delay generator
  - Automatic bit length measurement
- Modem controls
  - RTS, CTS, DCD, and up to four general purpose I/O pins per channel
  - CTS and DCD programmable auto-enables for Tx and Rx
  - Programmable interrupt on change of CTS or DCD
- On-chip oscillator for crystal
- TTL compatible
- Single +5V power supply

Asynchronous Mode Features

- Character length: 5 to 8 bits
- Odd or even parity, no parity, or force parity
- Up to two stop bits programmable in 1/16- bit increments
- 1× or 16× Rx and Tx clock factors
- Parity, overrun, and framing error detection
- False start bit detection
- Start bit search 1/2 bit time after framing error detection
- Break generation with handshake for counting break characters
- Detection of start and end of received break
- Character compare with optional interrupt on match

Character-Oriented Protocol Features

- Character length: 5 to 8 bits
- Odd or even parity, no parity, or force parity
- LRC or CRC generation and checking
- Optional opening PAD transmission
- One or two SYN characters
- External sync capability
- SYN detection and optional stripping
- SYN or MARK linefill on underrun
- Idle in MARK or SYNs
- Parity, FCS, overrun, and underrun error detection
- BISYNC Features
  - EBCDIC or ASCII header, text and control messages
  - SYN, DLE stripping
  - EOM (end of message) detection and transmission
  - Auto transparency mode switching
  - Auto hunt after receipt of EOM sequence (with closing PAD check after EOT or NAK)
  - Control character sequence detection for both transparent and normal text

Bit-Oriented Protocol Features

- Character length: 5 to 8 bits
- Detection and transmission of residual character: 0 – 7 bits
- Automatic switch to programmed character length for I field
- Zero insertion and deletion
- Optional opening PAD transmission
- Detection and generation of FLAG, ABORT, and IDLE bit patterns
- Detection and generation of shared (single) FLAG between frames
- Detection of overlapping (shared zero) FLAGs
- ABORT, ABORT-FLAGs, or FCS-FLAGs line fill on underrun
- Idle in MARK or FLAGs
- Secondary address recognition including group and global address
- Single- or dual-octet secondary address
- Extended address and control fields
- Short frame rejection for receiver
- Detection and notification of received end of message
- CRC generation and checking
- SDLC loop mode capability

ORDERING CODE

PACKAGES	V_{CC} = +5V± 10%, T_A = 0 to +70°C
Ceramic DIP	SCN68562C4I48
Plastic DIP	SCN68562C4N48
Plastic LCC	SCN68562C4A52

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Signetics

SCN68454
Intelligent Multiple Disk Controller (IMDC)

Preliminary Specification

Products

DESCRIPTION

The SCN68454 Intelligent Multiple Disk Controller (IMDC) provides the traditional and advanced features required to control Winchester type rigid disks and floppy disks. It can control up to four rigid or floppy disk drives, in any combination. It can be used to control, with a minimum of external hardware, any drive that has an SA1000 interface standard or an ST506 Seagate interface standard.

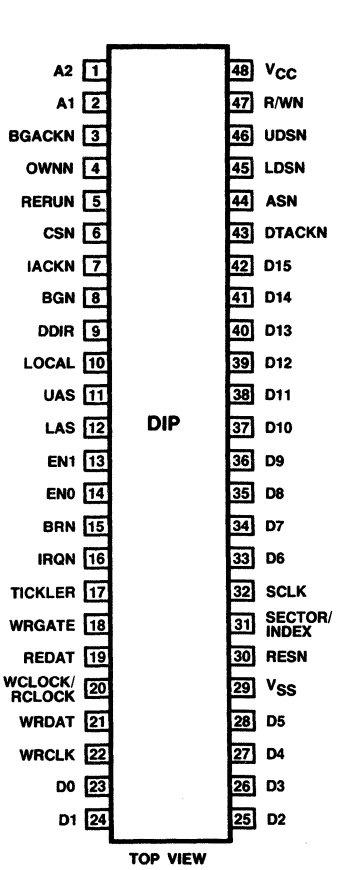
The IMDC supports soft or hard sectored disk track format and standard IBM track formats for floppy disks (both single and double density).

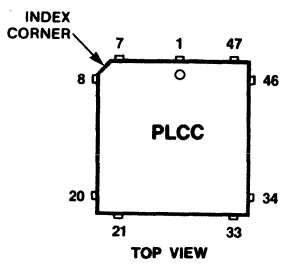
The controller is programmable via an external host processor by the use of high level commands. Data transfer on the host data bus can be 8 or 16-bit in parallel. The IMDC is capable of handling a serial data rate of up to 10Mbits per second. The SCN68454 is constructed using Signetics MOS-VLSI technology.

FEATURES

- **Bus compatible with SCN68000 microprocessor**
- **Automatic rerun on bus error**
- **Supports SCN68000 vectored interrupts**
- **31-bit address counter**
- **16/8-bit data transfers**
- **Supports up to 4 rigid disks and floppy disks in any combination**
- **Supports SA1000 and ST506 Winchester interfaces**
- **Data rates up to 10Mbits per second for MFM**

PIN CONFIGURATION





Pin	Function	Pin	Function
1	NC	27	NC
2	A2	28	D2
3	A1	29	D3
4	BGACKN	30	D4
5	OWNN	31	D5
6	RERUNN	32	V_{SS}
7	CSN	33	RESN
8	IACKN	34	SECTOR/INDEX
9	BGN	35	SCLK
10	DDIR	36	D6
11	LOCAL	37	D7
12	UAS	38	D8
13	LAS	39	D9
14	NC	40	NC
15	EN1	41	D10
16	EN0	42	D11
17	BRN	43	D12
18	IRQN	44	D13
19	TICKLER	45	D14
20	WRGATE	46	D15
21	REDAT	47	DTACKN
22	WCLOCK/RCLOCK	48	ASN
23	WRDAT	49	LDSN
24	WRCLK	50	UDSN
25	D0	51	R/WN
26	D1	52	V_{CC}

- **Data rates up to 2Mbits per second for FM**
- **Handles FM and MFM data encoding/decoding**
- **On chip DMA controller and FIFO buffer (128 bytes)**
- **Multiple sector read/write with implied seek**
- **Automatic bad sector handling**
- **32 and 40-bit ECC programmable polynomials**
- **Supports computer generated ECC polynomials**

Signetics

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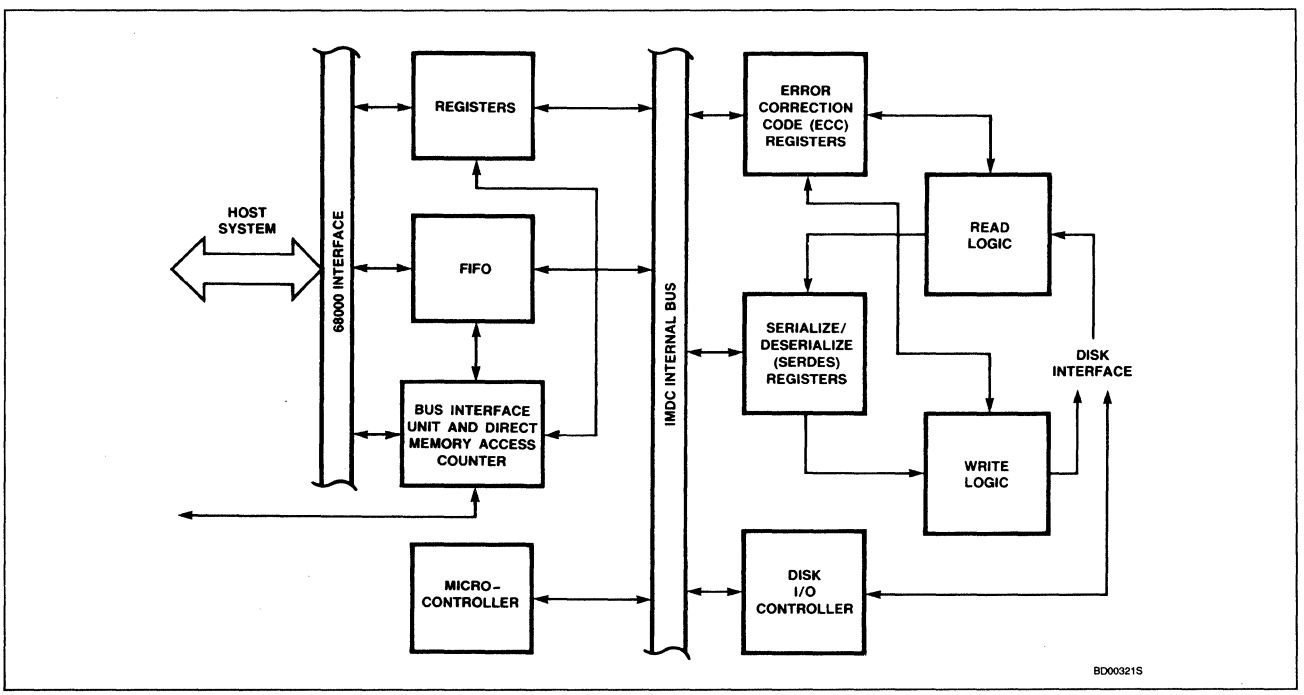
Intelligent Multiple Disk Controller (IMDC) SCN68454

ORDERING CODE

PACKAGES	V_{CC} = 5V ± 5%, T_A = 0 to 70°C
Ceramic DIP	SCN68454C6I48
Plastic DIP	SCN68454C6N48
Plastic LCC	SCN68454C6A52

BLOCK DIAGRAM



SCB68459
Disk Phase-Locked Loop (DPLL)

Product Specification

Microprocessor Products

DESCRIPTION

The SCB68459 Disk Phase-Locked Loop (DPLL) is a bipolar device that complements the SCN68454 Intelligent Multiple Disk Controller (IMDC). Together, with an external voltage controlled oscillator (VCO), the DPLL and IMDC provide all the functions required to control up to four disks with SA800, ST500, or SA1000 type interfaces.

The DPLL uses an external VCO for the variable clock rate which tracks the read data from the disk unit. This VCO can be any device that can interface to the DPLL. The IMDC can control up to four disks; if these are all the same, only one DPLL is needed. If different disk types are driven by the same IMDC, then a DPLL is required for each disk drive type.

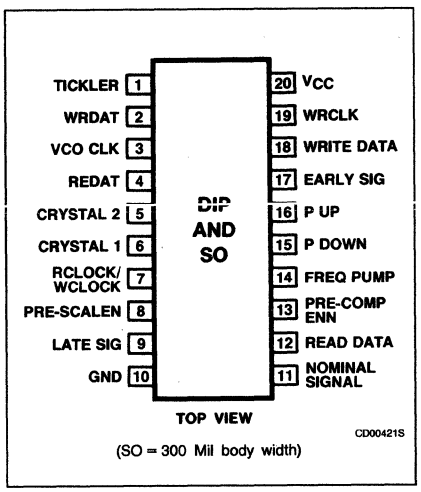
The SCB68459 DPLL operates by producing an oscillator frequency to match the frequency of an input signal. In this locked condition, any slight change in the input frequency (called jitter) will appear as a change in phase between the input frequency and the VCO frequency. This phase shift then acts as an error signal to change the frequency of the local DPLL VCO to match the input frequency.

The SCB68459 is constructed using Signetics extended performance logic (EPL) bipolar technology.

FEATURES

- **Supports composite data rate of 100kHz to 10MHz**
- **On-chip multiplexer for read and write clock**
- **Supports MFM and FM data formats**
- **Generates synchronous clock for read data**
- **Built-in pre-compensation circuit**
- **Phase detector and frequency detection for improved operation**
- **External loop gain control**
- **Minimal amount of external components required for operation**
- **Single +5V power supply**
- **Crystal-controlled write clock**

PIN CONFIGURATION



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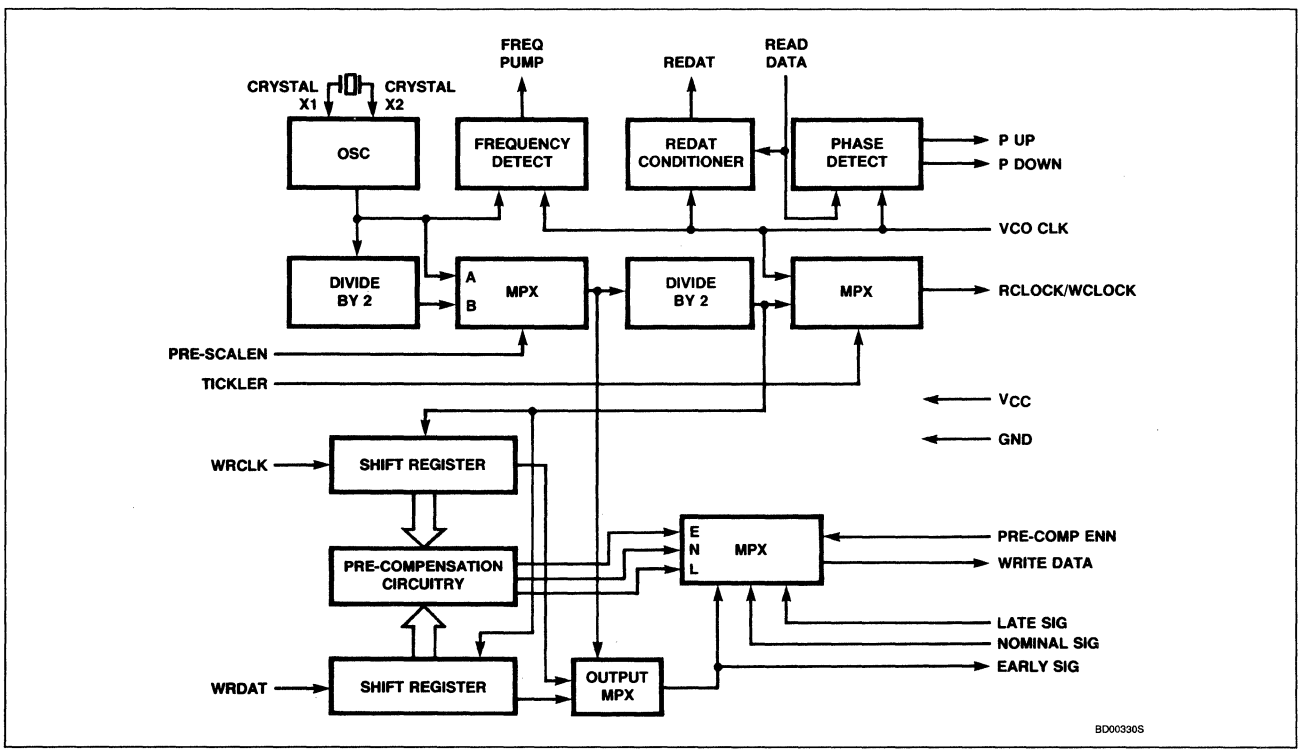
Disk Phase-Locked Loop (DPLL) SCB68459

ORDERING CODE

PACKAGES	V_{CC} = +5V ± 5%, T_A = 0 to +70°C
Ceramic DIP	SCB68459CAI20
Plastic DIP	SCB68459CAN20
Small Outline	SCB68459CAD20

BLOCK DIAGRAM



Signetics

SCB68172
VMEbus Controller (BUSCON)

Objective Specification

Microprocessor Products

DESCRIPTION

The Signetics SCB68172 VMEbus Controller (BUSCON) is an interface device for the VMEbus. It can be used in three different configurations: master-only, slave-only, and master/slave. The SCB68172 can be used with a processor-type interface or with a DMA controller-type interface. In all configurations, it handles the VMEbus signaling protocol in compliance with revisions B and C of the VMEbus Specification.

CONFIGURATION/VERSION

Applications of the BUSCON are identified as follows (see Figures 1 through 4):

VERSION	APPLICATION
PMS	Processor-type master/slave
DMAC	DMA controller-type master/slave
MS	Either PMS or (DMAC)
M	Master-only
S	Slave-only

All of these applications are handled by the SCB68172, with unused pins tied to stated logic levels in some of the applications.

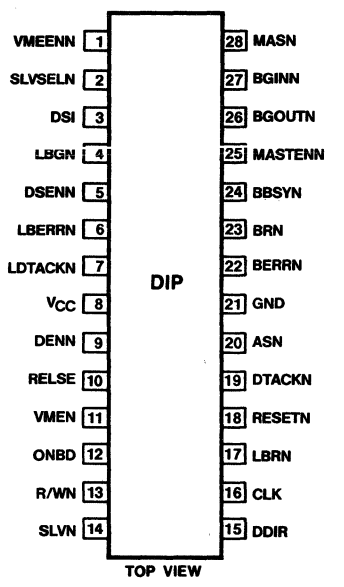
Figure 5 shows a functional model of the SCB68172 logic. The ASN, MASN, LBRN, BGINN, and RELSE inputs are internally synchronized to CLK before being presented to the state machine which determines the major functions of the device. The SLVN, ONBD, and VMEN signals are used directly in the state machine, although they are highly qualified to prevent metastable conditions on the state machine outputs. The BRN, BBSYN and LBGN signals are direct state machine outputs, while ASN, MASTENN, VMEENN, SLVSELN, and BGOUTN are derived from the state machine outputs plus some combinatorial qualification.

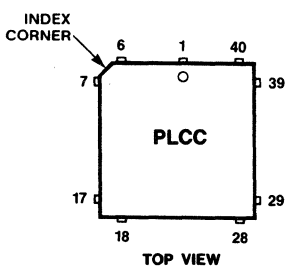
The DSI, R/WN, DTACKN, BERRN, LDTACKN, and LBERRN inputs function largely as direct combinatorial inputs. The DDIR, DTACKN, BERRN, LDTACKN, LBERRN, and (when applicable) MASN outputs are largely derived directly from these direct inputs, with some qualification from the state machine outputs. The DENN and DSENN outputs have complex multi-case logic which uses both the direct inputs and the state machine outputs.

FEATURES

- **Master, slave, or master/slave (dual ported) applications**
- **Helps assure VMEbus compatibility**
- **Allows for address decoding time**
- **Processor or DMA controller interface for master/requester**
- **Master/requester logic allows release on request (ROR) or release when done (RWD) operation, early or intercycle release**
- **Supports and exploits address lookahead**

PIN CONFIGURATIONS





Pin	Function	Pin	Function
1	NC	23	NC
2	VMEENN	24	DDIR
3	SLVSELN	25	CLK
4	DSI	26	LBRN
5	LBGN	27	RESETN
6	NC	28	NC
7	NC	29	NC
8	DSENN	30	DTACKN
9	LBERRN	31	ASN
10	NC	32	NC
11	LDTACKN	33	GND
12	NC	34	NC
13	V_{CC}	35	BERRN
14	NC	36	NC
15	DENN	37	BRN
16	RELSE	38	BBSYN
17	NC	39	NC
18	NC	40	NC
19	VMEN	41	MASTENN
20	ONBD	42	BGOUTN
21	R/WN	43	BGINN
22	SLVN	44	MASN

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VMEbus Controller (BUSCON)

SCB68172

ORDERING CODE

PACKAGES	V_{CC} = 5V± 5%, T_A = 0°C to 70°C
CERDIP	SCB68172C2F28
Plastic DIP	SCB68172C2N28
Plastic LCC	SCB68172C2A44

PIN DESCRIPTION

MNEMONIC	PIN NO.		TYPE	CONFIG	NAME AND FUNCTION
	DIP	PLCC			
CLK	16	25	I	All	**Clock:** User-supplied clock signal.
SLVN	14	22	I	S,MS	**Slave:** Active-low decode of the VMEbus address and address modifier lines indicating that the current cycle is for this board. SLVN should not be qualified with ASN nor VMEENN. It is first sampled on the rising clock edge after the rising edge on which ASN is first detected. It must remain valid until after the next low-going edge on DTACKN or BERRN. In a master-only application, SLVN should be pulled up to V_{CC}.
ASN	20	31	I/O I	M,MS S	**Address Strobe:** Direct connect to VMEbus ASN.
VMEN	11	19	I	M,MS	**VME Decode:** Active-low decode of the master's address lines, indicating that the master's current cycle is for a slave on the VMEbus. VMEN should not be qualified with MASN nor MASTENN. It is first sampled on the rising clock edge after the one on which MASN is first detected. Thereafter, it must remain valid until MASN goes false (high). In a slave-only configuration, VMEN should be pulled up to V_{CC}.
LBRN	17	26	I	M,MS	**Local Bus Request:** Connected to the low-active bus request output of a DMA controller. Typically tied to a high logic level in processor-type interfaces.
ONBD	12	20	I	MS	**Onboard:** Active-high decode of the master's address lines, indicating that the master's current cycle is for an onboard slave that is dual-ported with the VMEbus. ONBD should not be qualified with MASN or MASTENN. It is first sampled on the rising clock edge after the one on which MASN is first detected. Thereafter, it must remain valid until after MASN goes false (high). In a master-only or slave-only application, ONBD should be grounded. If a master/slave configuration does not contain "local slaves" as shown in figure 3, VMEN and ONBD should both be connected to an active-low "VME decode". A cycle between the onboard master and a local slave (VMEN high, ONBD low) is ignored by BUSCON, and can proceed concurrently with a cycle between another VMEbus master and an onboard dual-ported slave.
MASN	28	44	I I/O	M,PMS DMAC	**Master's Address Strobe:** RMW and Sequential VMEbus master cycles are accomplished by holding MASN low across several data strobes. If LBGN is high at the end of the RESETN low time, the state of ASN is driven onto MASN whenever BUSCON does not have control of the VMEbus. In a slave-only application, MASN should be pulled up to V_{CC}.
MASTENN	25	41	O	MS	**Master Enable:** In a master/slave application, the low state of this signal enables the master onto the shared bus and enables shared-bus responses back to the master. MASTENN also provides the direction control for the VMEbus address transceivers.
VMEENN	1	2	O	M,MS	**VME Enable:** Active-low enable for the VMEbus address drivers (master-only) or transceivers (master/slave).
SLVSELN	2	3	O	S,MS	**Slave Select:** Active-low select for the onboard slave resources (the shared/dual ported slaves in a master/slave application). Derived from MASN and ONBD, or from ASN and SLVN. If necessary, MASTENN and VMEENN are cycled to provide address setup time before SLVSELN is asserted.
BRN	23	37	O	M,MS	**Bus Request:** Active-low, open collector VMEbus request. Direct connect to the selected level among VMEbus BR0* – BR3*.
BGINN	27	43	I	M,MS	**Bus Grant In:** Direct connect to the selected level among VMEbus BG0IN* – BG3IN*.

SCC80C451/SCC83C451 I/O Expanded CMOS Microcontroller

Preliminary Specification

Products

DESCRIPTION

The Signetics SCC80C451/SCC83C451 is an I/O expanded, single-chip microcontroller fabricated with Signetics' high-density epitaxial CMOS technology. It is offered in a 68-pin PLCC and a 64-pin DIP. The Signetics CMOS technology combines the high-speed and high-density characteristics of HMOS with the low power of CMOS. Signetics' epitaxial substrate minimizes latch-up sensitivity.

The SCC80C451/SCC83C451 is a functional extension of the SCC80C31/SCC80C51 microcontroller with three additional I/O ports and four I/O control lines. The PLCC version has a total of 68 pins. The DIP version has a total of 64 pins. The four added control lines associated with port 6 facilitate high-speed asynchronous I/O functions.

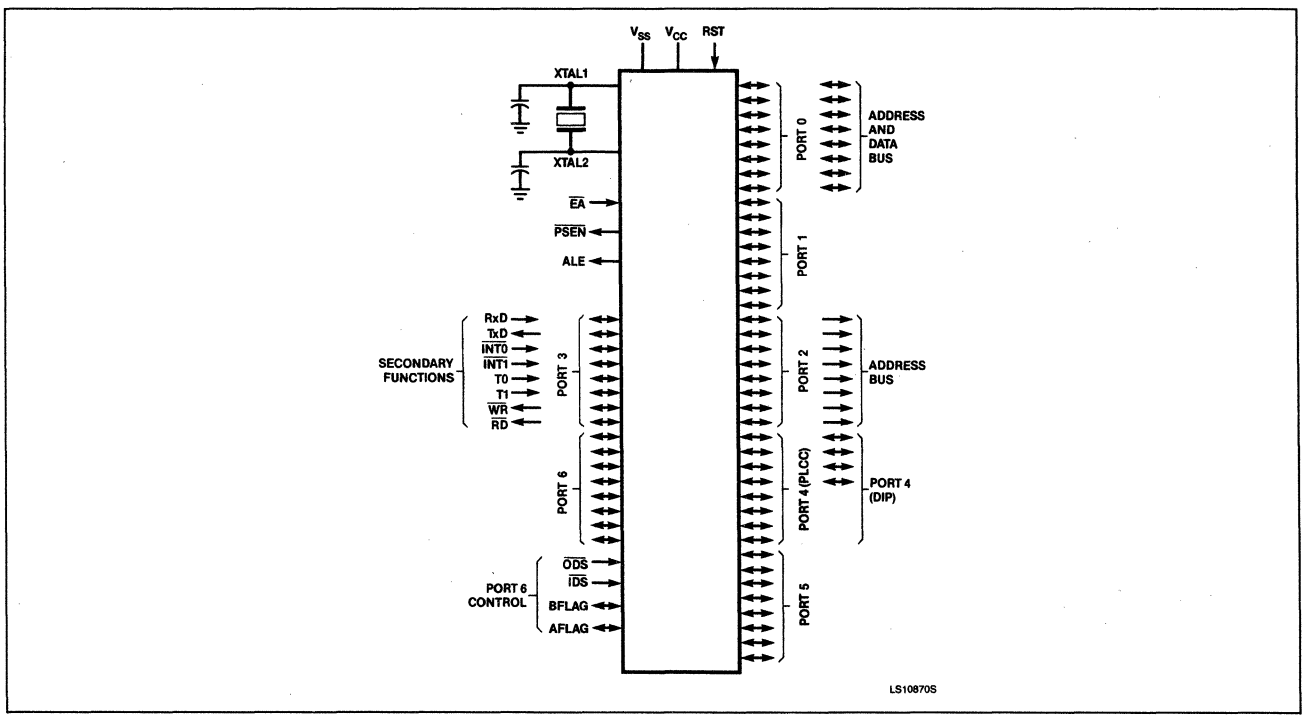
The SCC80C451/SCC83C451 includes a 4k × 8 ROM; a 128 × 8 RAM; 56 (PLCC) or 52 (DIP) I/O lines; two 16-bit timer/counters; a five source, two priority level, nested interrupt structure; a serial I/O port for either a full-duplex UART, I/O expansion, or multiprocessor communications; and on-chip oscillator and clock circuits.

The SCC80C451/SCC83C451 has two software selectable modes of reduced activity for further power reduction; idle mode and power-down mode. Idle mode freezes the CPU while allowing the RAM, timers, serial port, and interrupt system to continue functioning. Power-down mode freezes the oscillator, causing all other chip functions to be inoperative while maintaining the RAM contents.

FEATURES

- **SCC80C451 — CPU with RAM and I/O**
- **SCC83C451 — 80C451 with mask-programmable ROM**
- **68-pin PLCC and 64-pin DIP packages**
  - **Seven 8-bit I/O ports (PLCC version)**
  - **Six 8-bit ports and one 4-bit port (DIP version)**
- **Port 6 features:**
  - **8 data pins**
  - **4 control pins**
  - **Direct MPU bus interface**
  - **Parallel printer interface**
- **Pin compatible with 87C451 microcontroller**
- **On the microcontroller:**
  - **SCC80C51 CPU**
  - **4k × 8 ROM (SCC83C451 only)**
  - **128 × 8 RAM**
  - **Two 16-bit timer/counters**
  - **Full-duplex serial I/O**
  - **Two external interrupts**
- **External memory addressing capability:**
  - **64k ROM and 64k RAM**
- **Low power consumption:**
  - **Normal operation: 24mA typical @ 5V, 12MHz**
  - **Idle mode: 3mA typical @ 5V, 12MHz**
  - **Power-down mode: 50μA typical @ 2V**

LOGIC SYMBOL



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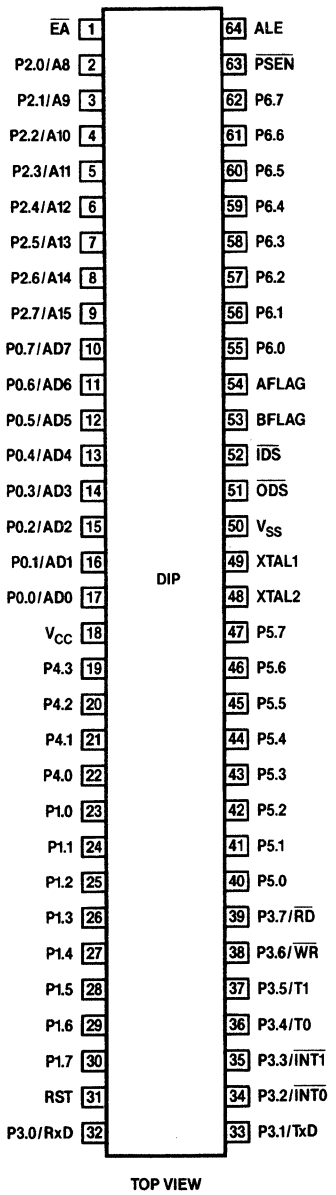
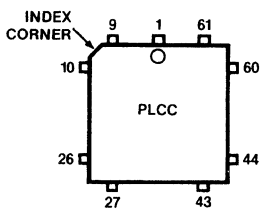
I/O Expanded CMOS Microcontroller — SCC80C451/SCC83C451

PIN CONFIGURATION



TOP VIEW

CD09510S



TOP VIEW

CD09520S

Pin	Function	Pin	Function
1	$\overline{EA}$	35	RST
2	P2.0/A8	36	P3.0/R × D
3	P2.1/A9	37	P3.1/T × D
4	P2.2/A10	38	P3.2/$\overline{INT0}$
5	P2.3/A11	39	P3.3/$\overline{INT1}$
6	P2.4/A12	40	P3.4/T0
7	P2.5/A13	41	P3.5/T1
8	P2.6/A14	42	P3.6/$\overline{WR}$
9	P2.7/A15	43	P3.7/$\overline{RD}$
10	P0.7/AD7	44	P5.0
11	P0.6/AD6	45	P5.1
12	P0.5/AD5	46	P5.2
13	P0.4/AD4	47	P5.3
14	P0.3/AD3	48	P5.4
15	P0.2/AD2	49	P5.5
16	P0.1/AD1	50	P5.6
17	P0.0/AD0	51	P5.7
18	V_{CC}	52	XTAL2
19	P4.7	53	XTAL1
20	P4.6	54	V_{SS}
21	P4.5	55	$\overline{ODS}$
22	P4.4	56	$\overline{IDS}$
23	P4.3	57	BFLAG
24	P4.2	58	AFLAG
25	P4.1	59	P6.0
26	P4.0	60	P6.1
27	P1.0	61	P6.2
28	P1.1	62	P6.3
29	P1.2	63	P6.4
30	P1.3	64	P6.5
31	P1.4	65	P6.6
32	P1.5	66	P6.7
33	P1.6	67	$\overline{PSEN}$
34	P1.7		
68	ALE		

Signetics

Signetics

SC84C00/20/40
CMOS Single-Chip 8-Bit Microcontroller

Objective Specification

Microprocessor Products

DESCRIPTION

The SC 84CXX family are a low cost, reduced pin count, CMOS derivative of the 8048 family. The family consists of three devices of different memory configurations, including the SC 84C00 piggyback EPROM version for prototyping and small runs.

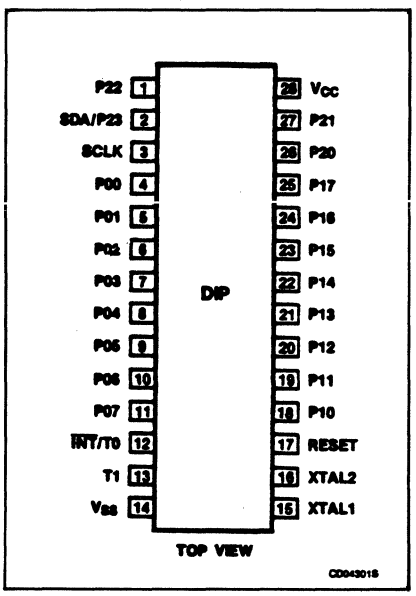
The Inter-Integrated Circuit serial bus interface (I^2C bus) facilitates I/O and Ram expansion; access to EEPROM memory and other dedicated I^2C peripherals, as well as processor to processor communication.

Members of the SC 84CXX family have the following 20 I/O lines: an Inter-Integrated Circuit serial bus interface, (I^2C bus); an 8-bit timer/counter; a three source, single level, fixed priority interrupt structure; and an on chip oscillator.

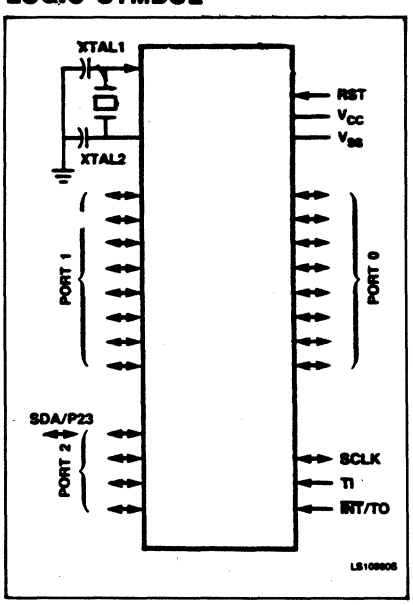
FEATURES

- Inter-Integrated Circuit (I^2C) serial bus interface
- Broad power supply voltage range: 2.5 to 5.5 volts
- Broad oscillator frequency range: .1 to 10MHz
- Low power consumption:
  - Idle mode, Stop mode
- 2K or 4K bytes of ROM plus piggyback EPROM version for prototypes
- 64 or 128 bytes of RAM
- 8-bit counter/timer
- CMOS and TTL compatible
- 20 quasi-bidirectional I/O lines
- Three vectored interrupts
  - external, I^2C counter/timer
- 40 to 85°C temperature range
- Internal power on reset and low voltage detection circuits
- Choice of DIP or SOL packages

PIN CONFIGURATION



LOGIC SYMBOL



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CMOS Single-Chip 8-Bit Microcontroller — SC84C00/20/40

ORDERING

SC 84C□□ □ □ □ 28 (CPxxxx)

ROM/RAM (bytes)
20 = 2K/64
40 = 4K/128
00 = Ext/256

*Blank = POR 1.9VMax
A = 3.5V± .5V

OPERATING TEMPERATURE RANGE
C = 0°C to +70°C

SPEED
A = 10MHz clock
6 = 16MHz

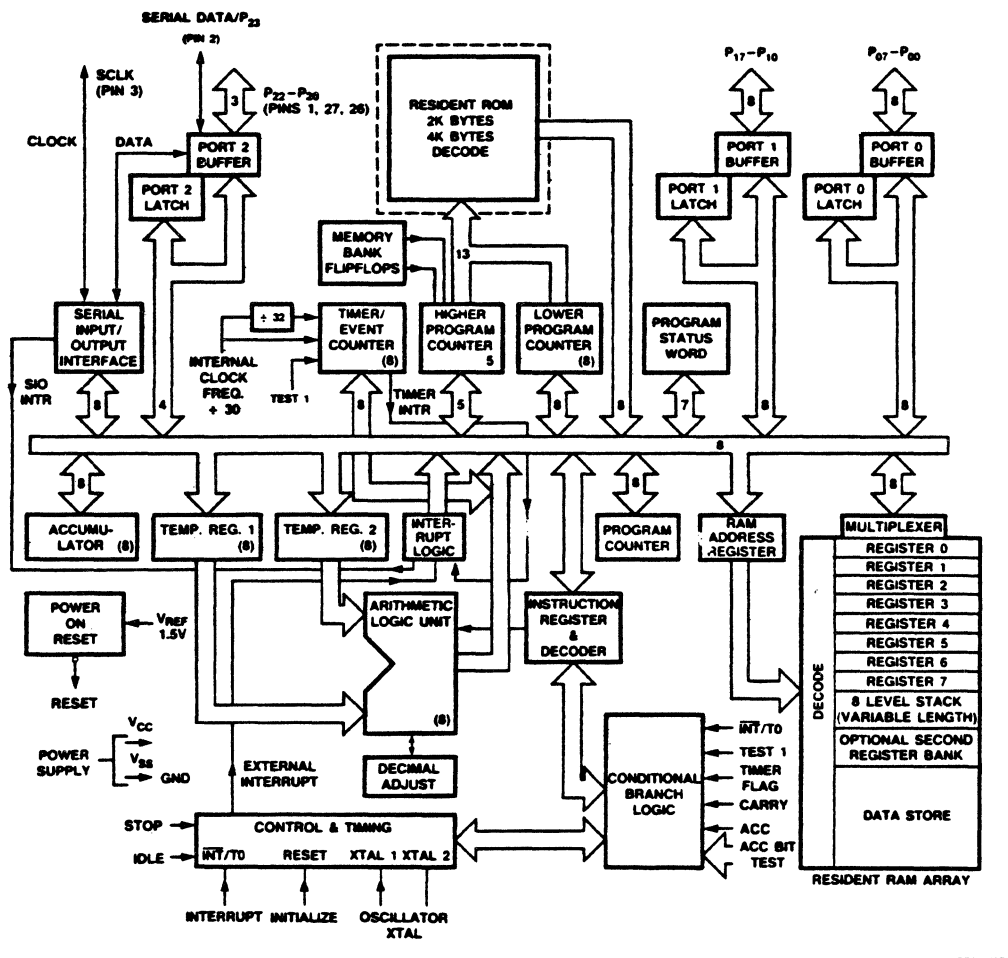
28-Pin

PACKAGE
N = Plastic DIP
I = Ceramic DIP
D = Plastic SOL

CUSTOM ROM PATTERN NUMBER
Applies to masked ROM versions only. Number will be assigned by Signetics. Contact Signetics sales office for ROM pattern submission requirements.

NOTE:
*See DC Electrical Characteristics "RESET"

BLOCK DIAGRAM



Signetics

Signetics

SC80C31B/SC80C51B
CMOS Single-Chip 8-Bit Microcontroller

Preliminary Specification

Microprocessor Products

DESCRIPTION

The Signetics SC80C31B/SC80C51B is a high-performance microcontroller fabricated with Signetics' high-density CMOS technology. The CMOS 80C31/80C51 is functionally compatible with the NMOS 8031/8051 microcontroller. The Signetics CMOS technology combines the high speed and density characteristics of HMOS with the low power attributes of CMOS. Signetics' epitaxial substrate minimizes latch-up sensitivity.

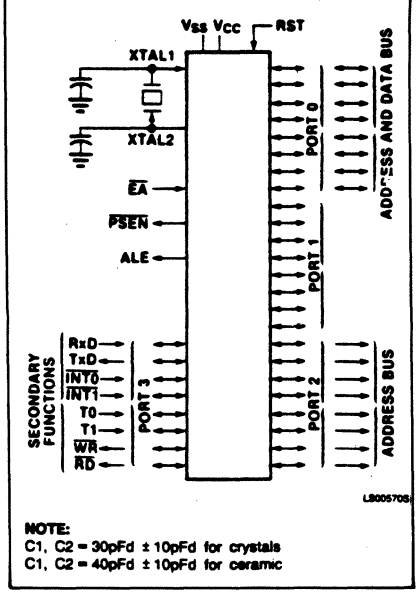
The SC80C31B/SC80C51B contains a 4K × 8 ROM; a 128 × 8 RAM; 32 I/O lines; two 16-bit timer/counters; a five-source, two-priority level, nested interrupt structure; a serial I/O port for either multiprocessor communications, I/O expansion or full duplex UART; and on-chip oscillator and clock circuits. In addition, the SC80C31B/80C51B has two software selectable modes of reduced activity for further power reduction – idle mode and power-down mode.

Idle mode freezes the CPU while allowing the RAM, timers, serial port, and interrupt system to continue functioning. Power-down mode saves the RAM contents but freezes the oscillator, causing all other chip functions to be inoperative.

FEATURES

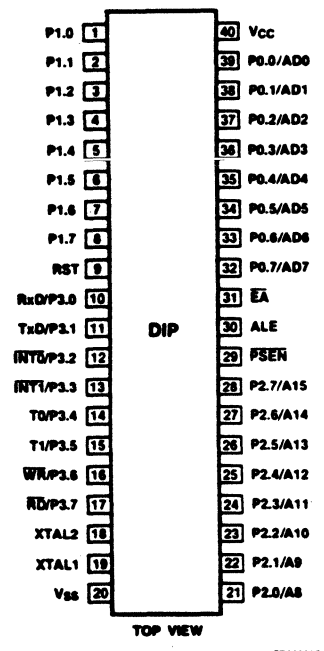
- **SC80C31 microcontroller without ROM**
- **SC80C51 control-oriented microcontroller**
- **SC8031/8051 compatible**
  - **4K × 8 ROM**
  - **128 × 8 RAM**
  - **Two 16-bit timer/counters**
  - **Full duplex serial channel**
  - **Boolean processor**
- **Memory addressing capability**
  - **64K ROM and 64K RAM**
- **Power control modes:**
  - **Idle mode**
  - **Power-down mode**
- **CMOS and TTL compatible**
- **Three speed ranges at V_{CC} = 5V ±20%**
  - **3.5 to 12 MHz**
  - **3.5 to 16 MHz**
  - **.5 to 12 MHz**

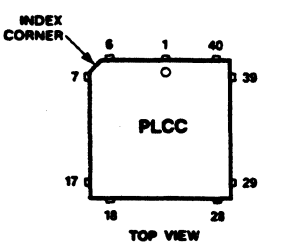
LOGIC SYMBOL



NOTE:
C1, C2 = 30pFd ± 10pFd for crystals
C1, C2 = 40pFd ± 10pFd for ceramic

PIN CONFIGURATIONS





Pin	Function	Pin	Function
1	NC	23	NC
2	P1.0	24	A8/P2.0
3	P1.1	25	A9/P2.1
4	P1.2	26	A10/P2.2
5	P1.3	27	A11/P2.3
6	P1.4	28	A12/P2.4
7	P1.5	29	A13/P2.5
8	P1.6	30	A14/P2.6
9	P1.7	31	A15/P2.7
10	RST	32	PSEN
11	RxD/P3.0	33	ALE
12	NC	34	NC
13	TxD/P3.1	35	EA
14	INT0/P3.2	36	P0.7/AD7
15	INT1/P3.3	37	P0.6/AD6
16	T0/P3.4	38	P0.5/AD5
17	T1/P3.5	39	P0.4/AD4
18	WR/P3.6	40	P0.3/AD3
19	RD/P3.7	41	P0.2/AD2
20	XTAL2	42	P0.1/AD1
21	XTAL1	43	P0.0/AD0
22	Vss	44	Vcc

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CMOS Single-Chip 8-Bit Microcontroller — SC80C31B/SC80C51B

ORDERING

SC80C□□ B □ □ □ □□ (CPxxxx)

ROM/RAM (bytes)
31 = EXT/128
51 = 4K/128

OPERATING TEMPERATURE RANGE
A = 40°C to +85°C
C = 0°C to +70°C

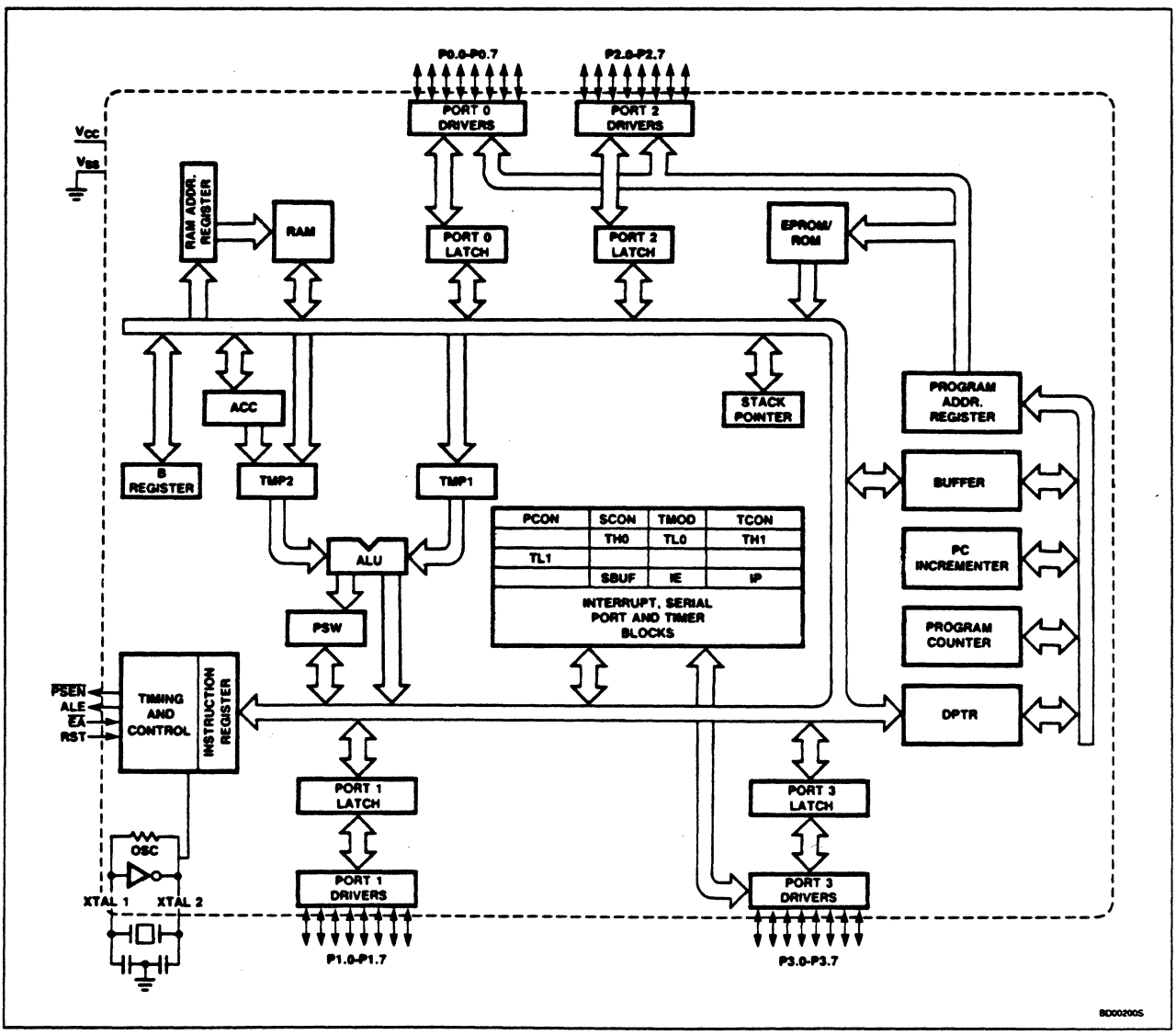
SPEED
0 = 3.5 to 12MHz
1 = 3.5 to 16MHz
2 = 0.5 to 12MHz

CUSTOM ROM PATTERN NUMBER
Applies to masked ROM versions only. Number will be assigned by Signetics. Contact Signetics sales office for ROM pattern submission requirements.

40=Pin DIP
44=Pin LCC

PACKAGE
N = Plastic DIP
I = Ceramic DIP
A = Plastic LCC

BLOCK DIAGRAM



Signetics

Signetics

SCN8032AH, SCN8052AH
Single-chip 8-Bit Microcontroller

Preliminary Specification

Microprocessor Products

DESCRIPTION

The Signetics SCN8032AH/SCN8052AH 8-bit Microcontroller is a high-performance single-chip computer, fabricated with Signetics' highly-reliable +5 volt, depletion-load, N-Channel, silicon-gate MOS technology. It provides the hardware features, architectural enhancements and new instructions that are necessary to make it a powerful and cost effective controller for applications.

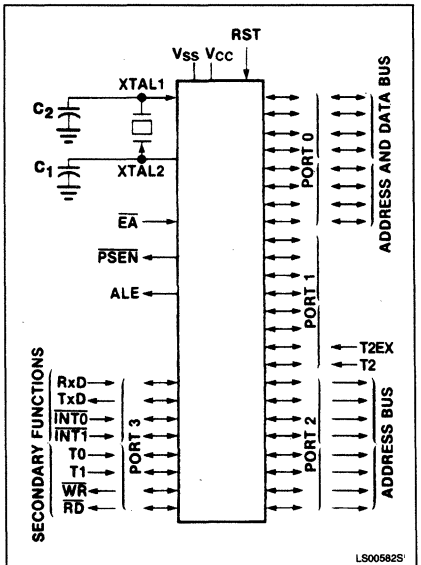
The SCN8032AH contains 256 bytes of read/write data memory; 32 I/O lines configured as four 8-bit ports; three 16-bit timer/counters; a six-source, two-priority level nested interrupt structure; a programmable serial I/O port; and an on-chip oscillator with clock circuitry. The SCN8052AH has all of these features plus 8K bytes of nonvolatile read-only program memory. Both microcontrollers have memory expansion capabilities of up to 64K bytes of data storage and 64K bytes of program memory that may be realized with standard TTL compatible memories.

Because of its' extensive BCD/binary arithmetic and bit-handling facilities, the SCN8032AH/SCN8052AH microcontroller is efficient at both computational and control-oriented tasks. Efficient use of program memory is also achieved by using the familiar compact instruction set of the 8031/8051. Forty-four percent of the instructions are one-byte, 41% two-byte and 15% three-byte. The majority of the instructions execute in just 1.0μs at 12MHz operation. The longest instructions, multiply and divide, require only 4μs at 12MHz.

FEATURES

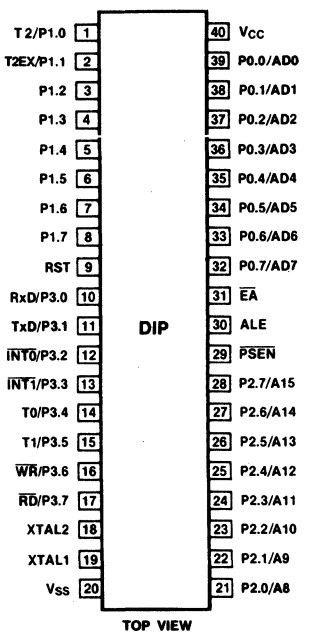
- **SCN8032AH – control-oriented CPU with RAM and I/O**
- **SCN8052AH – an SCN8032AH with factory mask-programmable ROM**
- **8K × 8 ROM (SCN8052AH only)**
- **256 × 8 RAM**
- **32 I/O lines (four 8-bit ports)**
- **Three 16-bit timer/counters**
- **Programmable full-duplex serial channel**
- **Variable transmit/receive baud rate capability**
- **Timer 2 capture capability**
- **128K accessible external memory**
- **Boolean processor**
- **128 user bit-addressable locations**
- **Upward compatible with SCN8031AH/SCN8051AH**

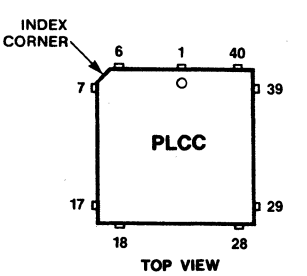
LOGIC SYMBOL



NOTES:
C1, C2 = 30 pfd. ±10pfd for crystals
= 40 pfd ±10pfd for ceramic resonators

PIN CONFIGURATIONS





Pin	Function	Pin	Function
1	NC	23	NC
2	T2/P1.0	24	A8/P2.0
3	T2EX/P1.1	25	A9/P2.1
4	P1.2	26	A10/P2.2
5	P1.3	27	A11/P2.3
6	P1.4	28	A12/P2.4
7	P1.5	29	A13/P2.5
8	P1.6	30	A14/P2.6
9	P1.7	31	A15/P2.7
10	RST	32	PSEN
11	RXD/P3.0	33	ALE
12	NC	34	NC
13	TXD/P3.1	35	EA
14	INT0/P3.2	36	AD7/P0.7
15	INT1/P3.3	37	AD6/P0.6
16	T0/P3.4	38	AD5/P0.5
17	T1/P3.5	39	AD4/P0.4
18	WR/P3.6	40	AD3/P0.3
19	RD/P3.7	41	AD2/P0.2
20	XTAL2	42	AD1/P0.1
21	XTAL1	43	AD0/P0.0
22	Vss	44	Vcc

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Single-chip 8-Bit Microcontroller SCN8032AH, SCN8052AH

ORDERING CODE

SCN80□□ H □ □ □ □□ (CPxxxx)

ROM/RAM (bytes)
32 = EXT/256
52 = 8K/256

POWER CONSUMPTION
H = Reduced Power AH

OPERATING TEMPERATURE RANGE
A = −40°C to +85°C
C = 0°C to +70°C

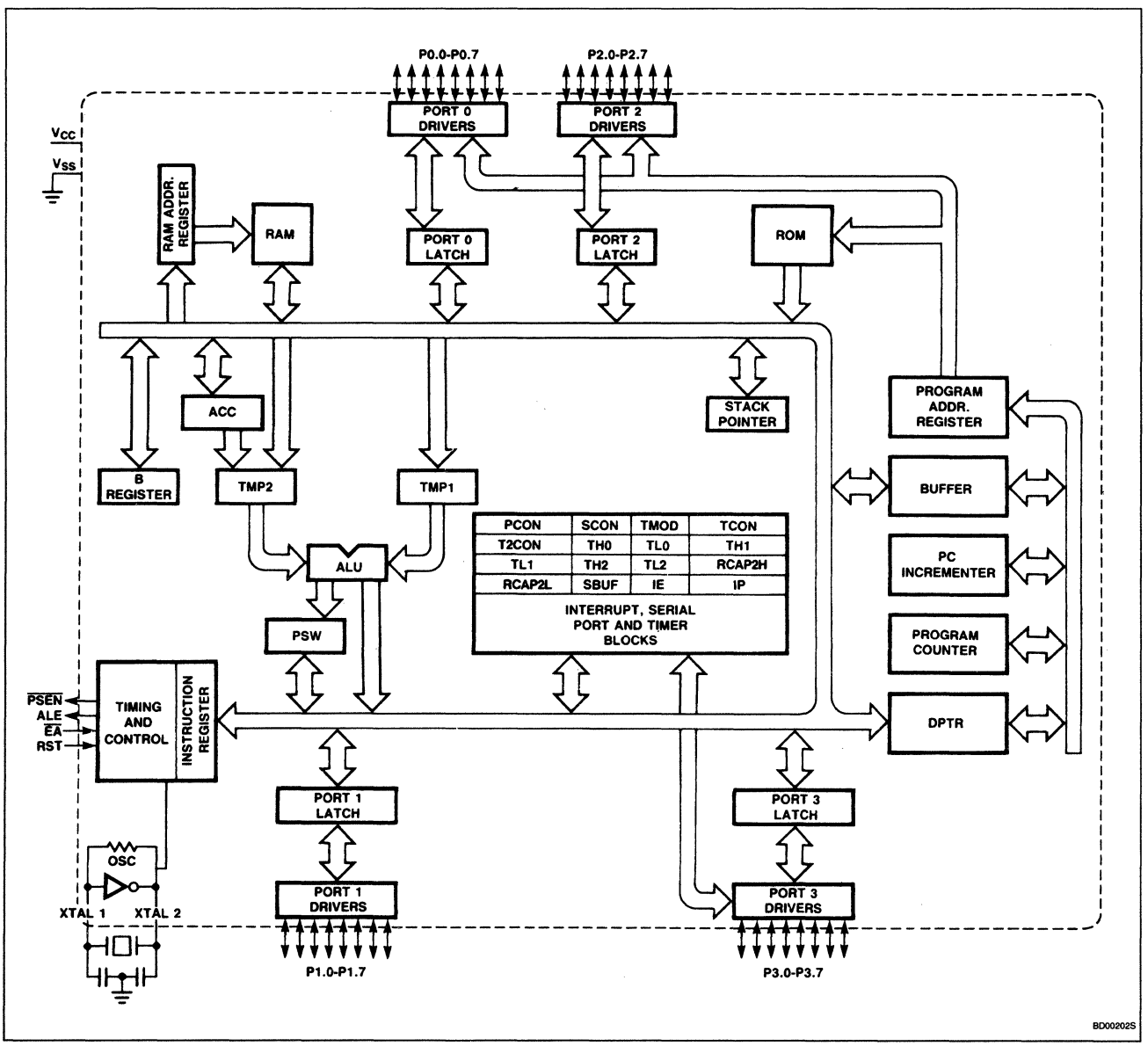
SPEED
C = 12MHz clock

PACKAGE
N = Plastic DIP
I = Ceramic DIP
A = Plastic LCC

40 = PIN DIP
44 = PIN PLCC

CUSTOM ROM PATTERN NUMBER
Applies to masked ROM versions only. Number will be assigned by Signetics. Contact Signetics sales office for ROM pattern submission requirements.

BLOCK DIAGRAM



Signetics

SCN8049
Single-Chip 8-Bit Microcontroller

Product Specification

Microprocessor Products

DESCRIPTION

The Signetics SCN80 Series microcontrollers are self-contained, 8-bit processors which contain the system timing, control logic, RAM data memory, ROM program memory (8048/49/50 only), and I/O lines necessary to implement dedicated control functions. All SCN80 Series devices are pin and program compatible, differing only in the size of the on-board program ROM and data RAM, as follows:

TYPE	RAM SIZE	ROM SIZE
SCN8049	128 × 8	2K × 8
SCN8050	256 × 8	4K × 8
SCN8039	128 × 8	—
SCN8040	256 × 8	—

Program memory can be expanded externally up to a maximum total of 4K bytes without paging. Data memory can also be expanded externally. I/O capabilities can be expanded using standard devices or the 8243 I/O expander.

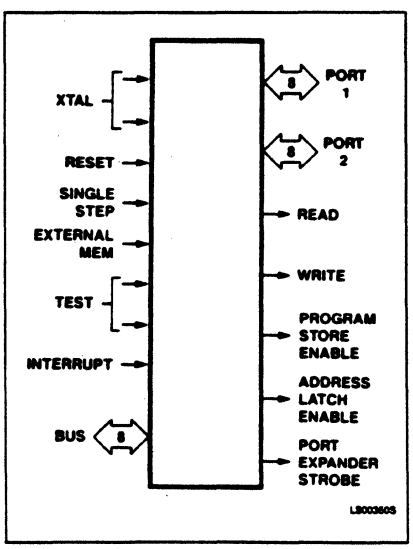
The SCN80 Series processors are designed to be efficient control processors as well as arithmetic processors. They provide an instruction set which allows the user to directly set and reset individual lines within its I/O ports as well as test individual bits within the accumulator. A large variety of branch and table look-up instructions make these processors very efficient in implementing standard logic functions. Also, special attention has been given to code efficiency. Over 70% of the instructions are a single byte long and all others are only 2 bytes long.

An on-chip 8-bit counter is provided which can count, under program control, either internal clock pulses (with a divide by 32 prescaler) or external events. The counter can be programmed to cause an interrupt on terminal count.

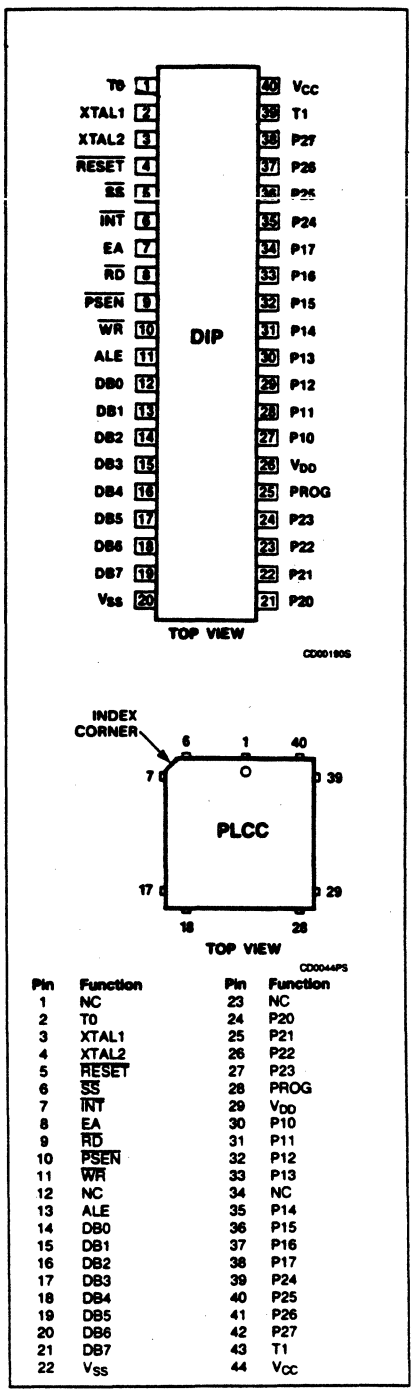
FEATURES

- **8-bit CPU, ROM, RAM, I/O in a 40-pin package**
- **24 quasi bidirectional I/O lines**
- **Two test inputs**
- **Internal counter/timer**
- **Single-level vectored interrupts: external, counter/timer**
- **Over 90 instructions, 70% single byte**
- **1.36μs or 2.5μs instruction cycle, all instructions one or two cycles**
- **Expandable memory and I/O**
- **Low voltage standby**
- **TTL compatible inputs and outputs**
- **Single +5V power supply**

LOGIC SYMBOL



PIN CONFIGURATIONS



Pin	Function	Pin	Function
1	NC	23	NC
2	T0	24	P20
3	XTAL1	25	P21
4	XTAL2	26	P22
5	$\overline{\text{RESET}}$	27	P23
6	$\overline{\text{SS}}$	28	PROG
7	$\overline{\text{INT}}$	29	V_{DD}
8	EA	30	P10
9	$\overline{\text{RD}}$	31	P11
10	$\overline{\text{PSEN}}$	32	P12
11	$\overline{\text{WR}}$	33	P13
12	NC	34	NC
13	ALE	35	P14
14	DB0	36	P15
15	DB1	37	P16
16	DB2	38	P17
17	DB3	39	P24
18	DB4	40	P25
19	DB5	41	P26
20	DB6	42	P27
21	DB7	43	T1
22	V_{SS}	44	V_{CC}

Signetics

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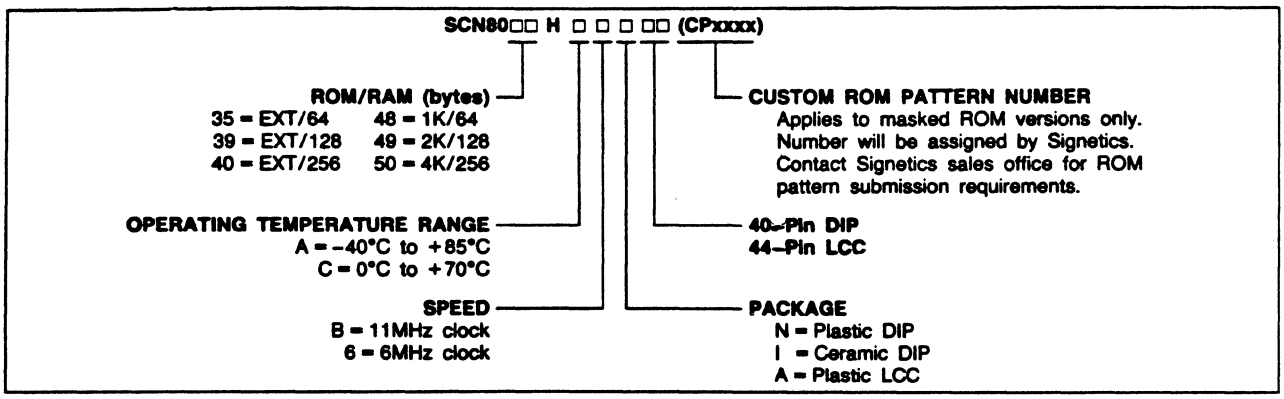
Single-Chip 8-Bit Microcontroller | SCN8049

ORDERING



PIN DESCRIPTION

MNEMONIC	PIN NO. DIP	PIN NO. PLCC	TYPE	NAME AND FUNCTION
V_{SS}	20	22		Circuit ground potential.
V_{DD}	26	29		Low power standby.
V_{CC}	40	44		**Main Power Supply:** +5V during operation.
PROG	25	28	O	Output strobe for 8243 I/O expander.
P10 - P17	27 - 34	30 - 33, 35 - 38	I/O	**Port 1:** 8-bit quasi-bidirectional port.
P20 - P27	21 - 24, 35 - 38	24 - 27, 39 - 42	I/O	**Port 2:** 8-bit quasi-bidirectional port. P20-23 contain the four high-order program counter bits during an external program memory fetch and serve as a 4-bit I/O expander bus for 8243.
DB0 - DB7	12 - 19	14 - 21	I/O	**Data Bus:** True bidirectional port which can be written or read synchronously using the $\overline{RD}$, $\overline{WR}$ strobes. The port can also be statically latched. Contains the eight low-order program counter bits during an external program memory fetch and receives the addressed instruction under the control of $\overline{PSEN}$. Also contains the address and data during an external RAM data store instruction, under control of ALE, $\overline{RD}$ and $\overline{WR}$.
T0	1	2	I	Input pin testable using the conditional transfer instructions JT0 and JNT0. T0 and be designated as a clock output using the ENT0 CLK instruction.
T1	39	43	I	Input pin testable using the JT1 and JNT1 instructions. Can be designated the timer/counter input using the STRT CNT instruction.
XTAL1	2	3	I	**Crystal 1:** One side of the crystal input for internal oscillator. Also input for external source (non-TTL V_{IH}).
XTAL2	3	4	I	**Crystal 2:** Other side of crystal input.
$\overline{INT}$	6	7	I	**Interrupt:** Initiates an interrupt if interrupt is enabled. Interrupt is disabled after a reset. Also testable with conditional jump instruction. Interrupt must remain low for at least three machine cycles for proper operation.
$\overline{RESET}$	4	5	I	**Reset:** Used to initialize the microcomputer. Active low. Internal pullup ~75KΩ. During program verification the address is latched by a "0" to "1" transition on $\overline{RESET}$ and the data at the addressed location is output on BUS.
$\overline{RD}$	8	9	O	**Read:** Output strobe activated during a bus read. Can be used to enable data onto the bus from an external device. Used as a read strobe to external data memory.
$\overline{WR}$	10	11	O	**Write:** Output strobe during a bus write. Used as write strobe to external data memory.
ALE	11	13	O	**Address Latch Enable:** Occurs once during each cycle and is useful as a clock output. The negative edge of ALE strobes address into external data and program memory.
$\overline{PSEN}$	9	10	O	**Program Store Enable:** Output occurs only during a fetch to external program memory.
$\overline{SS}$	5	6	I	**Single Step:** Can be used in conjunction with ALE to "single step" the processor through each instruction.
EA	7	8	I	**External Access:** Forces all program memory fetches to reference external memory. Useful for emulation and debug, and essential for testing and program verification.

NOTE:
Each pin on these ports can be assigned, under program control, to be an input or an output. A pin is designated as an input by writing a logic "1" to the pin. $\overline{RESET}$ sets all pins to the input mode. Each pin has an internal pullup of approximately 50kΩ.

Signetics

Signetics

8X401
Microcontroller

Product Specification

Microprocessor Products

DESCRIPTION

The Signetics 8X401 Microcontroller is a very high-speed bipolar microprocessor implemented with internal ECL technology. The 8X401 Microcontroller combines speed, flexibility, and a bit-oriented instruction set to accommodate many sophisticated applications. It excels in systems that require high-speed bit or byte manipulations, such as high-speed controllers and data communications.

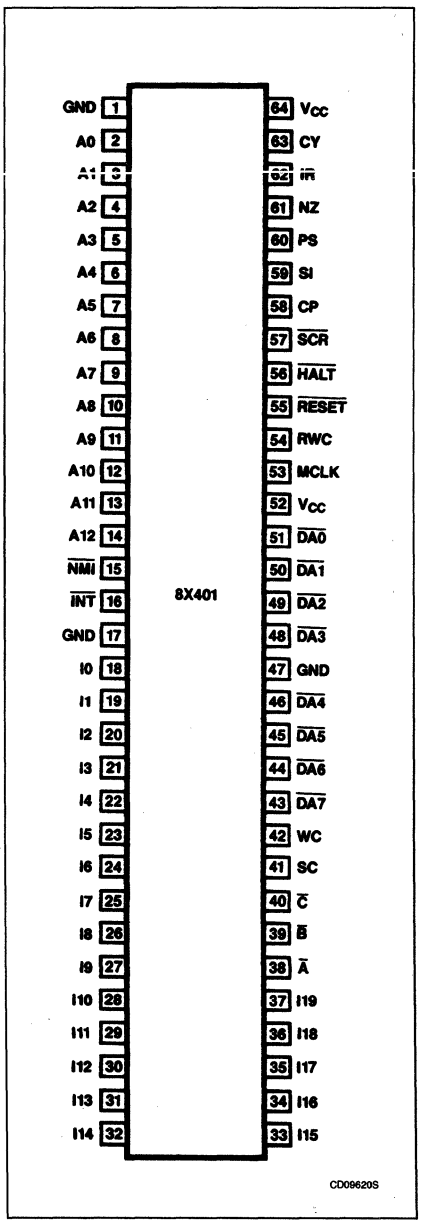
The 8X401 can fetch, execute, and generate the next instruction address for a 20-bit instruction in a minimum of 150ns. Within one instruction cycle, the 8X401 can be programmed to input, right-rotate and mask single or multiple bit subfields, perform an ALU operation, left-rotate, merge the subfield into the destination, and output.

To interface with program memory, the 8X401 uses a 13-bit address bus and a 20-bit instruction bus. An 8-bit bidirectional data/address bus, and an I/O control and timing bus is used to access external peripheral devices.

FEATURES

- **Fetches and executes all instructions in a minimum of 150ns**
- **Bit manipulation-oriented instruction set**
- **Separate buses for instruction, instruction address and I/O**
- **Sixteen 8-bit registers**
- **On-chip interrupt control**
- **TTL compatible I/O**
- **Single +5V supply**
- **0.9-inch 64-pin DIP, 68-pin plastic leaded chip carrier**
- **Two user-definable status flags**
- **Single TTL clock input**
- **Three independent I/O banks**
- **On-board control sequencer**
- **On-chip subroutine capabilities**
- **Fixed instruction set — 32 instructions**
- **Complete development support**

PIN CONFIGURATION



ORDERING CODE

DESCRIPTION	ORDER CODE
64-pin CERAMIC DIP 900 Mil Wide	N8X401I

Signetics

853-0843 83744

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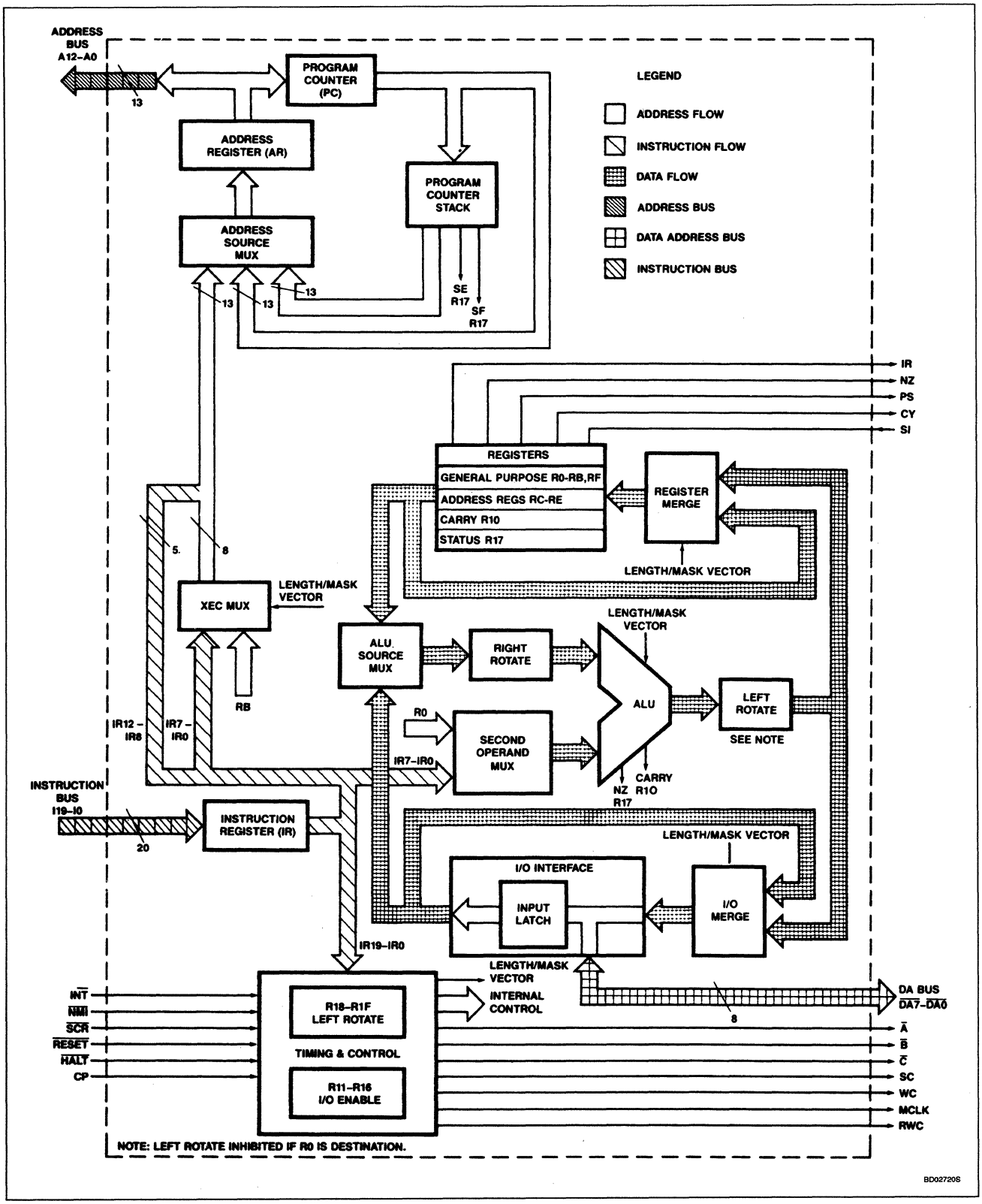
BLOCK DIAGRAM OF THE 8X401



Signetics

Signetics

8X450
RAM

Product Specification

Microprocessor Products

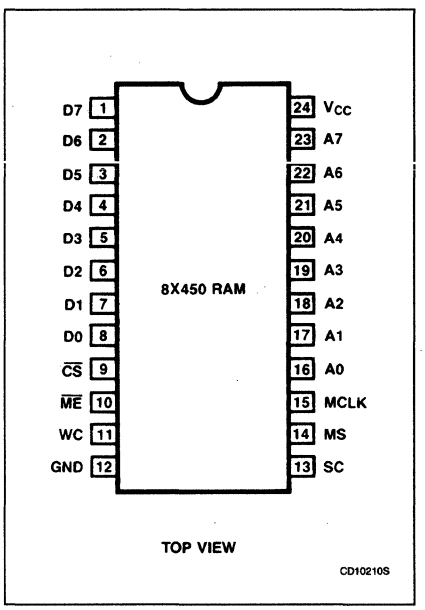
DESCRIPTION

The 8X450 is a 256-byte RAM designed primarily as a working storage element for 8X305 based systems. The 8X450 can be used as a dedicated RAM or in groups of RAMs to form a customized memory stack.

FEATURES

- **256-byte RAM**
- **Two modes of operation**
- **Paged RAM capability**
- **On-chip address latches**
- **Directly bus compatible with the 8X305 microcontroller**
- **24-pin slim line package**
- **Single + 5-volt supply**

PIN CONFIGURATION



ORDERING CODE

DESCRIPTION	ORDER CODE
24-Pin Ceramic DIP 400 Mil Wide	N8X450I

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FUNCTIONAL OPERATION

The 8X450 can be used in either of two operating modes — conventional DA select or fast select. Each mode supports either single or multiple RAM applications. The mode of operation is selected by the MS pin.

Conventional $\overline{DA}$ Select (MS = 1)

When MS is tied high, the conventional $\overline{DA}$ addressing mode is selected; in this mode, the 8X450 data and address lines are tied together. For applications that use a single RAM, the chip select ($\overline{CS}$) input is grounded. To prevent bus contention in applications that use multiple RAMs, the $\overline{CS}$ input is driven by an external source. Examples of both configurations (single and multiple RAMs) are shown in the Application Diagrams at the rear of this data sheet. Control signals and operating conditions for conventional $\overline{DA}$ addressing are summarized in Table 1.

Fast Select Operations (MS = 0)

When MS is tied low, the fast select addressing mode is invoked; in this mode, the 8X450 address lines are driven by an external source and the 8X450 data lines are tied to the 8X305 $\overline{IV}$ bus. The $\overline{CS}$ input is treated exactly the same as in conventional $\overline{DA}$ addressing; examples of single and multiple RAM configurations are shown at the rear of this data sheet. Control signals and operating conditions for fast select addressing are summarized in Table 2.

PIN CONFIGURATION AND DECRIPTIONS

PIN NO.	IDENTIFIER	FUNCTION
1 – 8	D7 – D0	Bidirectional data bus, D0 is LSB
9	$\overline{CS}$	Chip Select, active low
10	$\overline{ME}$	Master Enable, active low
11	WC	Write Control, active high
12	GND	Ground
13	SC	Select Control, active high
14	MS	Mode Select
15	MCLK	Master Clock, active high
16 – 23	A0 – A7	Address lines, A0 is LSB
24	V_{CC}	Power supply

Table 1. Conventional $\overline{DA}$ Select (MS = 1)

SC	WC	$\overline{ME}$	MCLK	FUNCTION
0	0	0	0	Read from RAM
0	0	1	X	None
0	1	0	1	Write data to RAM
0	1	1	1	None
1	0	0	1	Conventional $\overline{DA}$ select (write address to RAM)
1	0	1	1	None

NOTES:
1. Other states are not generated by the 8X305 and are not defined for operation in this mode.
2. Table 1 is valid only if the chip select ($\overline{CS}$) is low; if $\overline{CS}$ is high, the 8X450 is disabled.

Table 2. Fast Select (MS = 0)

SC	WC	$\overline{ME}$	MCLK	FUNCTION
0	0	0	0	Read from RAM
0	0	1	0	None
X	X	1	1	Write address to RAM
0	1	0	1	Write data to RAM

NOTES:
1. Other states are not generated by the 8X305 and are not defined for operation in this mode.
2. Table 2 is valid only if the chip select ($\overline{CS}$) is low. If $\overline{CS}$ is high, the 8X450 is disabled.

Signetics

8X470
I/O Port

Product Specification

Microprocessor Products

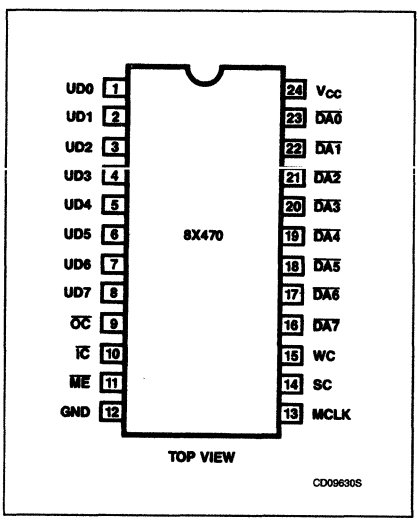
DESCRIPTION

The 8X470 I/O Port (Figure 1) is a fuse-programmable device designed to interface a user system with a Signetics 8X401 Microcontroller. The 8X470 has three internal registers — a data register and two status registers. The data register is shared between the two systems, while each system has its own dedicated status register. The 8X470 can be programmed to provide a bidirectional or unidirectional user interface with the user data entry being either synchronous or asynchronous with the 8X401.

FEATURES

- **Two independent 8-bit busses**
- **Fast polling**
- **Directly bus-compatible with the 8X401, 8X305 Microcontrollers**
- **256 Data Addresses**
- **Separate Controller and User status registers**
- **16 Status Addresses**
- **Positionable Controller Status Register output**
- **Bidirectional or unidirectional I/O capability**
- **Synchronous or asynchronous user data entry**
- **Conventional $\overline{DA}$ or Fast select addressing techniques**
- **24-pin slimline package**
- **Single +5V supply**

PIN CONFIGURATION



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I/O Port

8X470

PIN DESCRIPTION

PIN	IDENTIFIER	FUNCTION
1 – 8	UD0 – UD7	User port data lines. Active high.
9	$\overline{OC}$	**Output Control:** An active low signal which controls reading into the I/O port from the UD bus.
10	$\overline{IC}$	**Input Control:** An active low signal which controls writing into the I/O port from the UD bus.
11	$\overline{ME}$	**Master Enable:** The $\overline{ME}$ pin depends upon the addressing mode for its function. Conventional $\overline{DA}$ select: $\overline{ME}$ is an active low signal which allows read or write or address operations from the $\overline{DA}$ bus. Fast select: $\overline{ME}$ is an active high signal which allows the controller status register to be read on the $\overline{DA}$ bus.
12	GND	**Ground.**
13	MCLK	**Master Clock:** Input from the 8X401.
14	SC	**Select Command:** The SC pin depends upon the addressing mode for its function. Conventional $\overline{DA}$ select: An active high signal which compares the 8X401 $\overline{DA}$ bus and the address. An address match selects the 8X470. Fast select: SC is an active high signal which outputs the contents of the data register on the $\overline{DA}$ bus while clearing the control status register.
15	WC	**Write Command:** An active high signal which controls the writing of data into the I/O port from the 8X401 $\overline{DA}$ bus.
16 – 23	$\overline{DA7}$ – $\overline{DA0}$	Controller Data/Address ($\overline{DA}$) lines. Active low.
24	V_{CC}	+5V power supply.

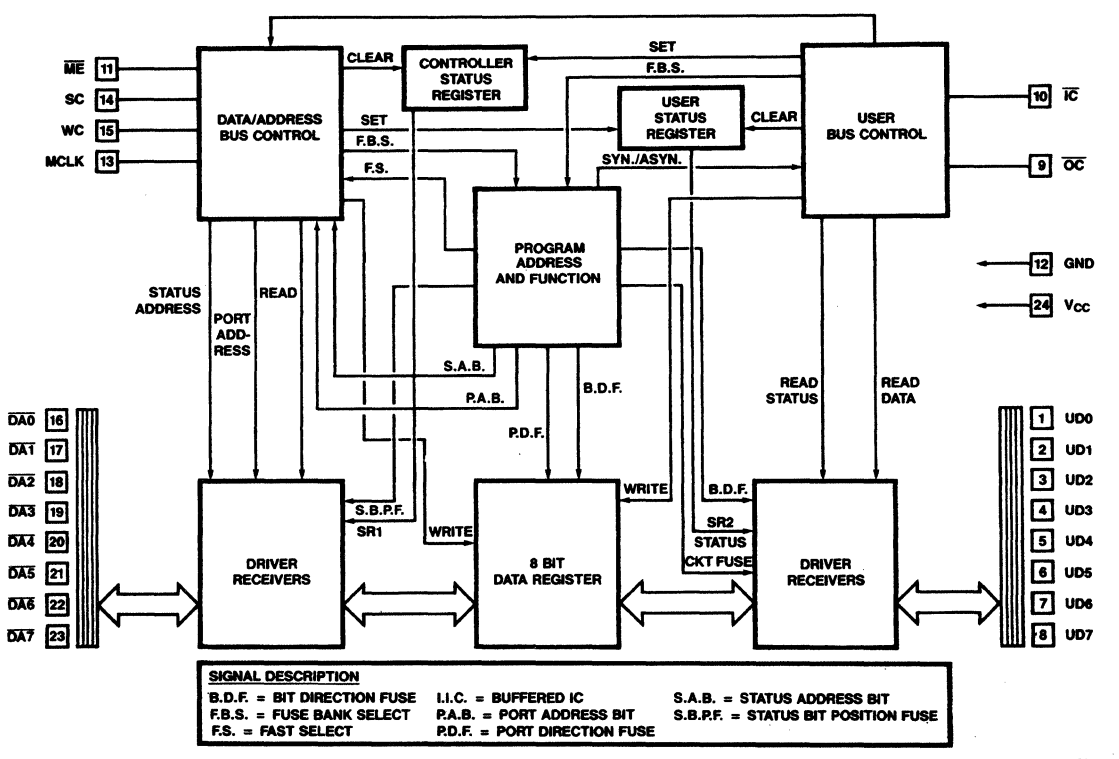

Figure 1 8x470 Block Diagram

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Signetics

2960
Error Detection and Correction (EDC) Unit

Product Specification

Products

FEATURES

- **Boosts Memory Reliability — Corrects all single-bit errors. Detects all double and some triple-bit errors. Reliability of dynamic RAM systems is increased more than 60-fold.**
- **Very High Speed — Perfect for MOS microprocessor, minicomputer and mainframe systems.**
  - **Data In to error detect: 32ns worst case.**
  - **Data In to corrected data out: 65ns worst case.**
- **High-performance systems can use the Signetics EDC in the check-only mode to avoid memory system slowdown.**
- **Replaces 25 to 50 MSI chips — All necessary features are built-in to the Signetics 2960, including diagnostics, data in, data out and check bit latches.**
- **Handles Data Words From 8 to 64 Bits — The Signetics 2960 is cascadable: 1 EDC for 8 or 16 bits, 2 for 32 bits, 4 for 64 bits.**
- **Easy Byte Operations — Separate byte enables on the data out latch simplify the steps and cuts the time required by byte writes.**
- **Built-In Diagnostics — The processor may completely exercise the EDC under software control to check for proper operation.**

DESCRIPTION

The Signetics 2960 Error Detection and Correction Unit (EDC) (Figure 1) contains the logic necessary to generate check bits on a 16-bit data field according to a modified Hamming Code, and to correct the data word when check bits are supplied. Operating on data read from memory, the EDC will correct any single-bit error and will detect all double- and some triple-bit errors. For 16-bit words, 6 check bits are used. The 2960 can be expanded to operate on 32-bit words (7 check bits) and 64-bit words (8 check bits). In all configurations, the device makes the error syndrome available on separate outputs for data logging.

The Signetics 2960 also features two diagnostic modes, in which diagnostic data can be forced into portions of the chip to simplify device testing and to execute system diagnostic functions.

The product is supplied in a 48-lead hermetic DIP package and a 48-pin plastic package.

Signetics

BLOCK DIAGRAM

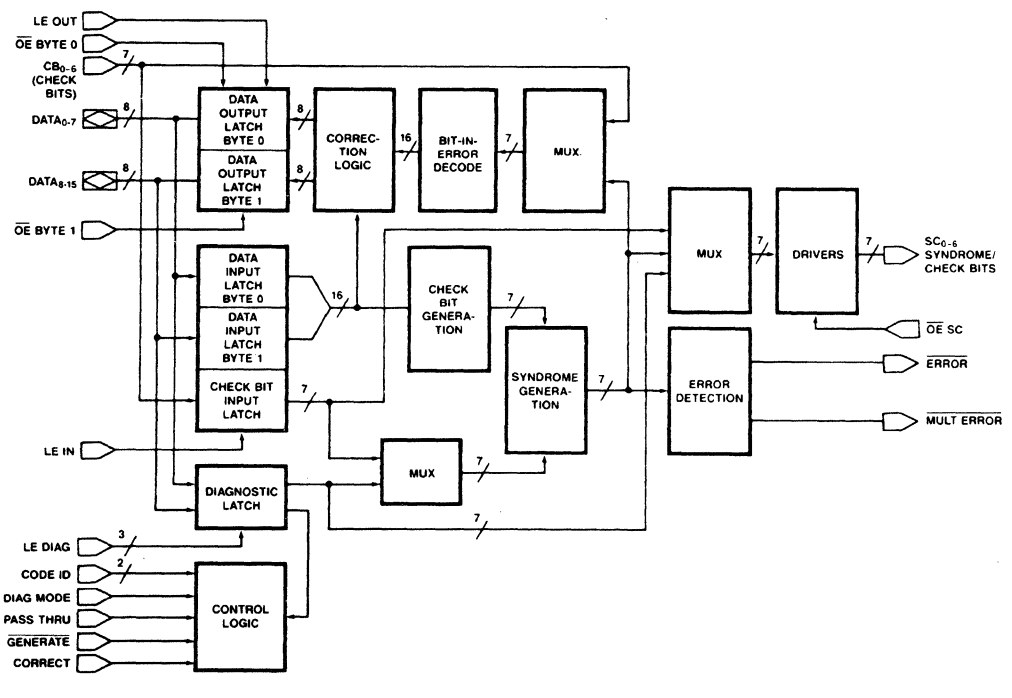


Figure 1

853-0065 82174

Signetics

NE5205
Wideband High Frequency Amplifier

Product Specification

Linear Products

DESCRIPTION

The NE5205 is a High Frequency Amplifier with a fixed insertion gain of 20dB. The gain is flat to ±0.5dB from DC to 450MHz, and the −3dB bandwidth is greater than 600MHz. This performance makes the amplifier ideal for cable TV applications. The NE5205 operates with a single supply of 6V, and only draws 25mA of supply current, which is much less than comparable hybrid parts. The noise figure is 4.8dB in a 75Ω system and 6dB in a 50Ω system.

Until now, most RF or high frequency designers had to settle for discrete or hybrid solutions to their amplification problems. Most of these solutions required trade-offs that the designer had to accept in order to use high frequency gain stages. These include high power consumption, large component count, transformers, large packages with heat sinks, and high part cost. The NE5205 solves these problems by incorporating a wideband amplifier on a single monolithic chip.

The part is well matched to 50 or 75Ω input and output impedances. The Standing Wave Ratios in 50 and 75Ω systems do not exceed 1.5 on either the input or output over the entire DC to 600MHz operating range.

Since the part is a small monolithic IC die, problems such as stray capacitance are minimized. The die size is small enough to fit into a very cost-effective 8-pin small-outline (SO) package to further reduce parasitic effects. A TO-46 metal can is also available that has a case connection for RF grounding which increases the −3dB frequency to 650MHz. The metal can is hermetically sealed, and can operate over the full −55°C to +125°C range.

No external components are needed other than AC coupling capacitors because the NE5205 is internally compensated and matched to 50 and 75Ω. The amplifier has very good distortion specifications, with second and third-order intermodulation intercepts of +24dBm and +17dBm respectively at 100MHz.

The device is ideally suited for 75Ω cable television applications such as decoder boxes, satellite receiver/decoders, and front-end amplifiers for TV receivers. It is also useful for amplified splitters and antenna amplifiers.

The part is matched well for 50Ω test equipment such as signal generators, oscilloscopes, frequency counters and all kinds of signal analyzers. Other applications at 50Ω include mobile radio, CB radio and data/video transmission in fiber optics, as well as broad-band LANs and telecom systems. A gain greater than 20dB can be achieved by cascading additional NE5205s in series as required, without any degradation in amplifier stability.

FEATURES

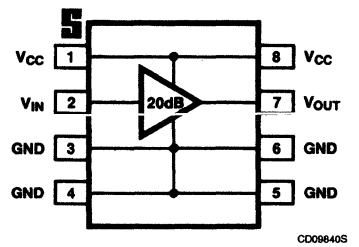
- **650MHz bandwidth**
- **20dB insertion gain**
- **4.8dB (6dB) noise figure $Z_O = 75\Omega$ ($Z_O = 50\Omega$)**
- **No external components required**
- **Input and output impedances matched to 50/75Ω systems**
- **Surface Mount package available**
- **Excellent performance in cable TV 75Ω systems**

APPLICATIONS

- **75Ω cable TV decoder boxes**
- **Antenna amplifiers**
- **Amplified splitters**
- **Signal generators**
- **Frequency counters**
- **Oscilloscopes**
- **Signal analyzers**
- **Broad-band LANs**
- **Fiber-optics**
- **Modems**
- **Mobile radio**
- **CB radio**
- **Telecommunications**

PIN CONFIGURATIONS

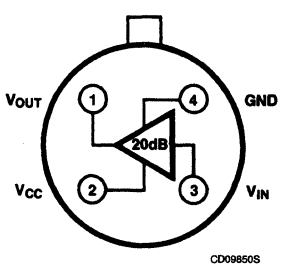
N, FE, D Packages



TOP VIEW

NOTE:
Signetics designates Pin 1.

EC Package



NOTE:
Tab denotes Pin 1.

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Signetics

SE/NE5539
Ultra-High Frequency Operational Amplifier

Linear Products

DESCRIPTION

The Signetics SE/NE5539 is a very wide bandwidth, high slew rate, monolithic operational amplifier for use in video amplifiers, RF amplifiers, and extremely high slew rate amplifiers.

Emitter-follower inputs provide a true differential high input impedance device. Proper external compensation will allow design operation over a wide range of closed-loop gains, both inverting and non-inverting, to meet specific design requirements.

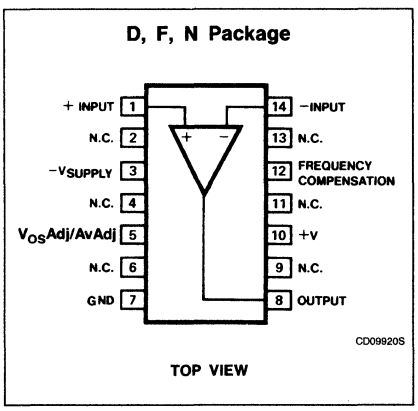
FEATURES

- **Gain bandwidth product: 1.2GHz at 17dB**
- **Slew rate: 600/Vμs**
- **Full power response: 48MHz**
- **A_{VOL}: 52dB typical**
- **350MHz unity gain**

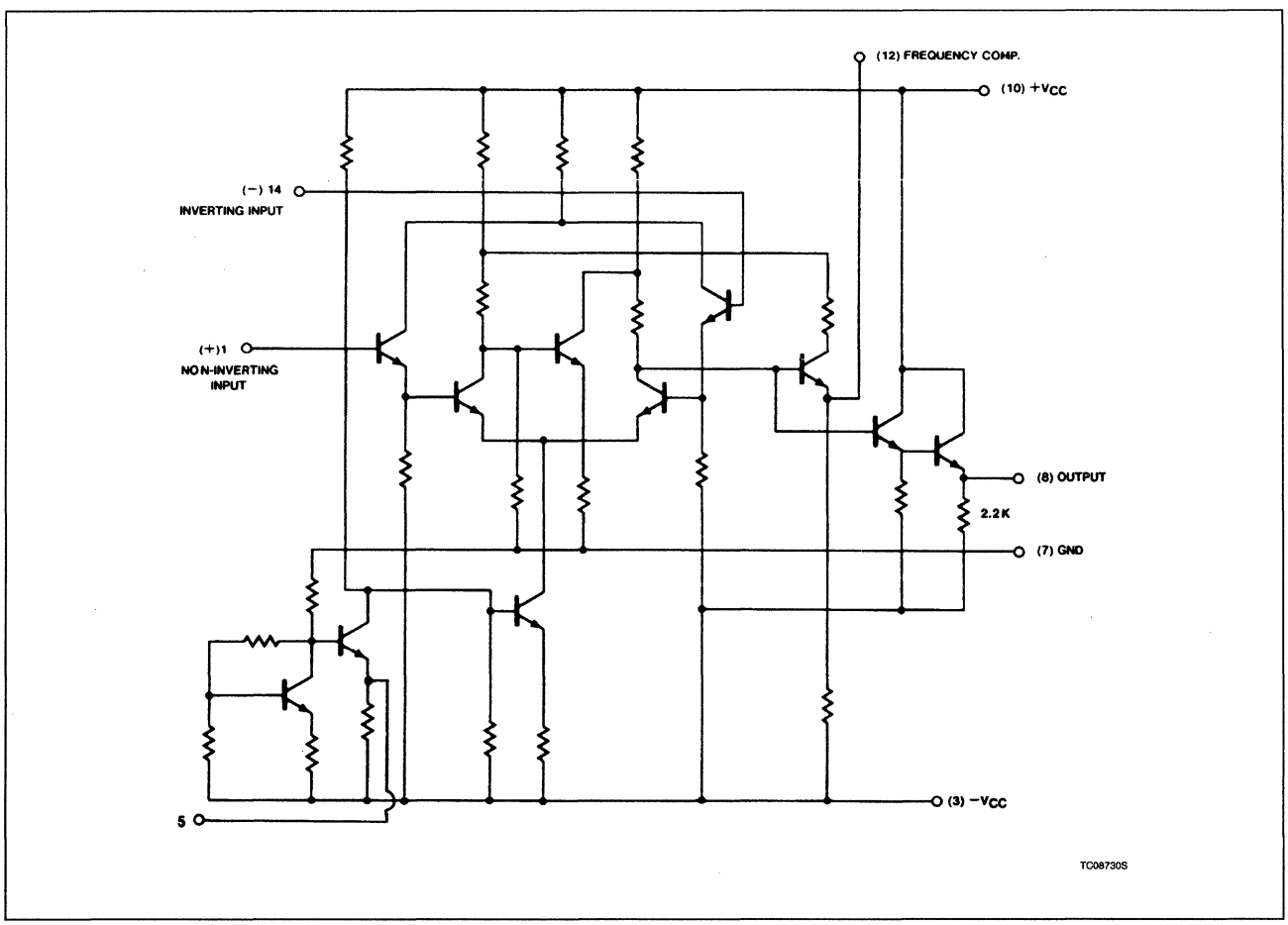
APPLICATIONS

- **Switch mode power supplies**
- **Fast pulse amplifiers**
- **RF oscillators**
- **Fast sample and hold**
- **High gain video amplifiers (BW > 20MHz)**

PIN CONFIGURATION



EQUIVALENT CIRCUIT



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NE5592
Video Amplifier

Linear Products

DESCRIPTION

The NE5592 is a dual monolithic, two-stage, differential output, wideband video amplifier. It offers fixed gains of 400 without external components and adjustable gains from 400 to 0 with one external resistor. The input stage has been designed so that with the addition of a few external reactive elements between the gain select terminals, the circuit can function as a high-pass, low-pass, or band-pass filter. This feature makes the circuit ideal for use as a video or pulse amplifier in communications, magnetic memories, display, video recorder systems, and floppy disk head amplifiers.

FEATURES

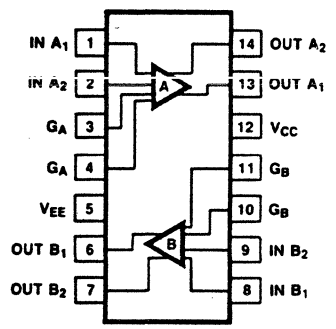
- **120MHz bandwidth**
- **Adjustable gains from 0 to 400**
- **Adjustable pass band**
- **No frequency compensation required**
- **Wave shaping with minimal external components**

APPLICATIONS

- **Floppy disk head amplifier**
- **Video amplifier**
- **Pulse amplifier in communications**
- **Magnetic memory**
- **Video recorder systems**

PIN CONFIGURATION

D, N Package

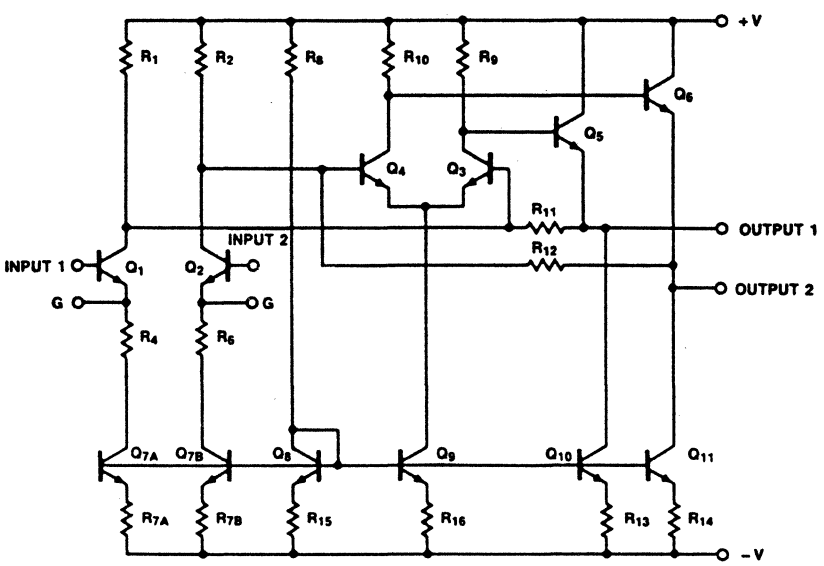


TOP VIEW

ORDERING CODE

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
14-pin plastic DIP		NE5592N
14-pin SO DIP		NE5592D

EQUIVALENT CIRCUIT



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SA/SE/NE5230
Low Voltage Operational Amplifier

Product Specification

Linear Products

DESCRIPTION

The NE5230 is a very low voltage operational amplifier that can perform with a voltage supply as low as 1.8V or as high as 15V. In addition, split or single supplies can be used, and the output will swing to ground when applying the latter. There is a bias adjusting pin which controls the supply current required by the device and thereby controls its power consumption. If the part is operated at ±0.9V supply voltages, the current required is only 110μA when the current control pin is left open. Even with this low power consumption, the device obtains a typical unity gain bandwidth of 180kHz. When the bias adjusting pin is connected to the negative supply, the unity gain bandwidth is typically 600kHz while the supply current is increased to 600μA. In this mode, the part will supply full power output beyond the audio range.

The NE5230 also has a unique input stage that allows the common-mode input range to go above the positive and below the negative supply voltages by 250mV. This provides for the largest possible input voltages for low voltage applications. The part is also internally-compensated to reduce external component count.

The NE5230 has a low input bias current of typically ±40nA, and a large open-loop gain of 115dB. These two specifications are beneficial when using the device in transducer applications. The large open-loop gain gives very accurate signal processing because of the large "excess" loop gain in a closed-loop system.

The output stage is a class AB type that can swing to within 100mV of the supply voltages for the largest dynamic range that is needed in many applications. The NE5230 is ideal for portable audio equipment and remote transducers because of its low power consumption, unity gain bandwidth, and 23nV/$\sqrt{Hz}$ noise specification.

FEATURES

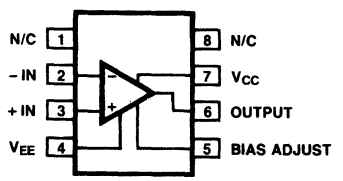
- **Works down to 1.8V supply voltages**
- **Adjustable supply current**
- **Low noise**
- **Common-mode includes both rails**
- **V_{OUT} within 100mV of both rails**

APPLICATIONS

- **Portable precision instruments**
- **Remote transducer amplifier**
- **Portable audio equipment**
- **Rail-to-Rail comparators**
- **Half-wave rectification without diodes**
- **Remote temperature transducer with 4 to 20mA output transmission**

PIN CONFIGURATION

N, FE & D Packages



TOP VIEW

CD11070S

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-pin Plastic DIP	0 to +70°C	NE5230D
8-pin Ceramic DIP	0 to +70°C	NE5230FE
8-pin Plastic DIP	0 to +70°C	NE5230N
8-pin Plastic DIP	−40 to +85°C	SA5230D
8-pin Plastic DIP	−40 to +85°C	SA5230N
8-pin Ceramic DIP	−55 to +125°C	SE5230FE
8-pin Plastic DIP	−55 to +125°C	SE5230N

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SE/NE5532/5532A
Internally Compensated Dual Low Noise OP Amp

Product Specification

Linear Products

DESCRIPTION

The 5532 is a dual high-performance low noise operational amplifier. Compared to most of the standard operational amplifiers, such as the 1458, it shows better noise performance, improved output drive capability and considerably higher small-signal and power bandwidths.

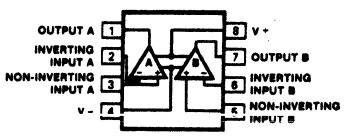
This makes the device especially suitable for application in high-quality and professional audio equipment, instrumentation and control circuits, and telephone channel amplifiers. The op amp is internally compensated for gains equal to one. If very low noise is of prime importance, it is recommended that the 5532A version be used which has guaranteed noise voltage specifications.

FEATURES

- **Small-signal bandwidth: 10MHz**
- **Output drive capability: 600Ω, 10V (rms)**
- **Input noise voltage: 5nV/√Hz (typical)**
- **DC voltage gain: 50000**
- **AC voltage gain: 2200 at 10kHz**
- **Power bandwidth: 140kHz**
- **Slew-rate: 9V/μs**
- **Large supply voltage range: ±3 to ±20V**
- **Compensated for unity gain**

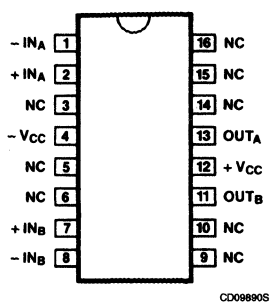
PIN CONFIGURATIONS

FE, N Packages



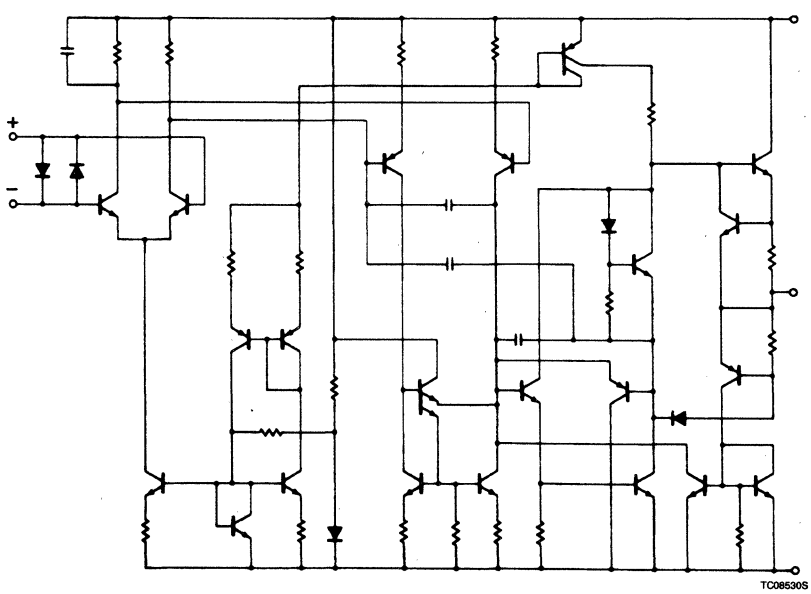
TOP VIEW

D Package[2]



TOP VIEW

EQUIVALENT SCHEMATIC (EACH AMPLIFIER)



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NE/SA/SE5534
Single and Dual Low Noise Op Amp

Linear Products

Preliminary Specification

DESCRIPTION

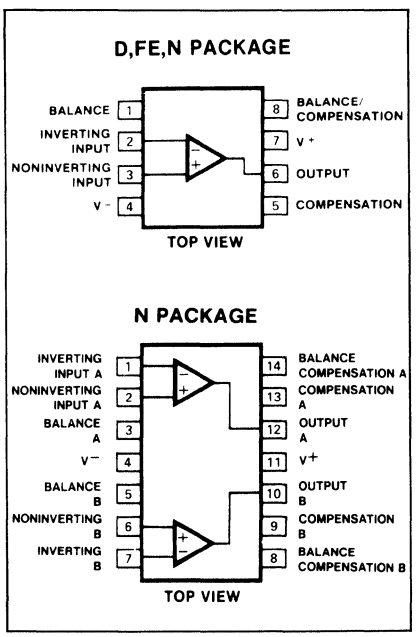
The 5534 is a dual and single high-performance low noise operational amplifier. compared to other operational amplifiers, such as TL083, they show better noise performance, improved output drive capability and considerably higher small-signal and power bandwidths.

This makes the devices especially suitable for application in high quality and professional audio equipment, in instrumentation and control circuits and telephone channel amplifiers. The op amps are internally compensated for gain equal to, or higher than, three. The frequency response can be optimized with an external compensation capacitor for various applications (unity gain amplifier, capacitive load, slew-rate, low overshoot, etc.) If very low noise is of prime importance, it is recommended that the 5534A version be used which has guaranteed noise specifications.

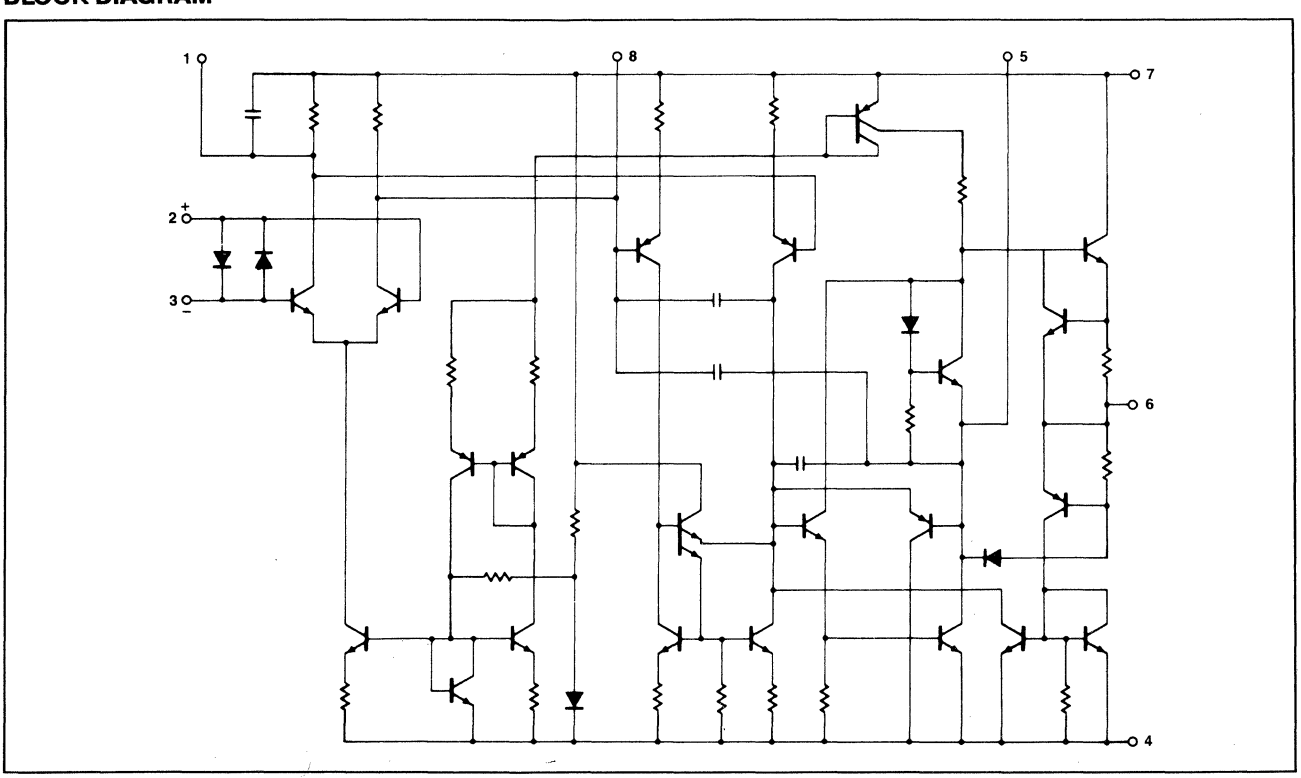
FEATURES

- **Small-signal bandwidth: 10 MHz**
- **Output drive capability: 600Ω, 10 V (rms) at $V_S = \pm 18$ V**
- **Input noise voltage: 4nV/$\sqrt{\text{Hz}}$**
- **DC voltage gain: 100000**
- **AC voltage gain: 6000 at 10 kHz**
- **Power bandwidth: 200 kHz**
- **Slew rate: 13 V/μs**
- **Large supply voltage range: ±3 to ±20 V**

PIN CONFIGURATIONS



BLOCK DIAGRAM



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SE/NE5212
Transimpedance Amplifier

Preliminary Specification

Linear Products

DESCRIPTION

The NE/SE5212 is a low noise differential amplifier, particularly suitable for signal recovery in fiber-optic receivers and in any other applications where very low signal levels obtained from high impedance sources need to be amplified.

FEATURES

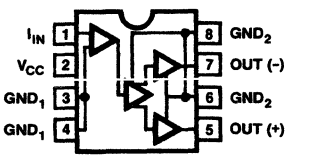
- **Extremely low noise 2.5pA/$\sqrt{Hz}$**
- **Single 5V supply**
- **Large bandwidth: 150MHz**
- **Differential outputs**
- **Low input/output impedances**
- **High power supply rejection ratio**
- **14kΩ differential transresistance**

APPLICATIONS

- **Fiber-optic receivers**
- **Wideband gain block**
- **General purpose instrumentation**
- **Sensor preamplifiers**
- **Single-ended to differential conversion**
- **Low noise RF amplifiers**

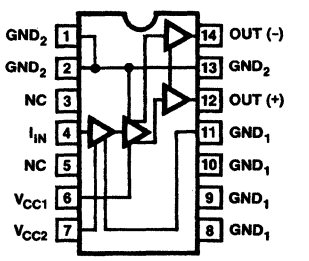
PIN CONFIGURATIONS

N, FE, D-8 Packages



CD10450S

D-14 Package



CD10440S

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-pin Plastic DIP	0°C to +70°C	NE5212N
8-pin Plastic SO	0°C to +70°C	NE5212D8
8-pin Ceramic DIP	0°C to +70°C	NE5212FE
14-pin Plastic SO	0°C to +70°C	NE5212D14
8-pin Plastic SO	−40°C to +85°C	SA5212D8
14-pin Plastic SO	−40°C to +85°C	SA5212D14
8-pin Plastic DIP	−40°C to +85°C	SA5212N
8-pin Ceramic DIP	−40°C to +85°C	SA5212FE
8-pin Plastic DIP	−55°C to +125°C	SE5212N
8-pin Ceramic DIP	−55°C to +125°C	SE5212FE

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING			
		NE5212	SA5212	SE5212	UNIT
	Temperature Range				
T_A	Operating ambient	0 to 70	−40 to 85	−55 to 125	°C
T_J	Operating junction	−55 to 150	−55 to 150	−55 to 150	°C
T_{STG}	Storage	−65 to 150	−65 to 150	−65 to 150	°C
V_{CC}	Power Supply	6	6	6	V

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TDA7050
Low Voltage Mono/Stereo Power Amplifier

Product Specification

Linear Products

DESCRIPTION
The TDA7050T is a low voltage audio amplifier for small radios with headphones (such as watch, pen and pocket radios) in mono (bridge-tied load) or stereo applications.

APPLICATIONS
- **Portable Radio**
- **Personal Computer**
- **Speech Synthesis**
- **Telephone Modem**

FEATURES
- **Limited to battery supply application only (Typ. 3 and 4V)**
- **Operates with supply voltage down to 1.6V**
- **No external components required**
- **Very low quiescent current**
- **Fixed integrated gain of 26dB, floating differential input**
- **Flexibility in use — mono BTL as well as stereo**
- **Small dimension of encapsulation (see package design example)**

ORDERING CODE

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-pin Plastic SO DIP	0°C to +70°C	TDA7050D
8-pin Plastic DIP	0°C to +70°C	TDA7050N

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_P	Supply voltage	6	V
I_{OM}	Peak output current	150	mA
P_{TOT}	Total power dissipation	see derating curve, Figure 1	
T_{stg}	Storage temperature range	−55 to +150	°C
T_C	Crystal temperature	100	°C
t_{sc}	AC and DC short-circuit duration at V_P = 3.0 V (during mishandling)	5	s

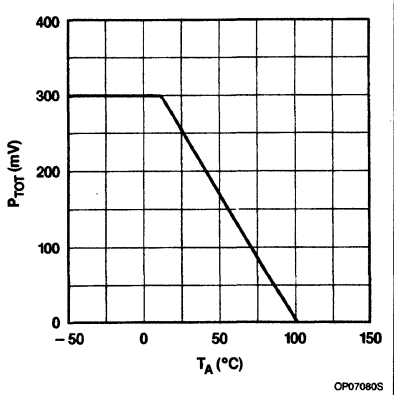

Figure 1. Power Derating Curve

SO PACKAGE DESIGN EXAMPLE
To achieve the small dimension of the encapsulation the SO package is preferred with only 8 pins. Because a heatsink is not applicable, the dissipation is limited by the thermal resistance of the 8-pin SO encapsulation until:

$$\frac{T_{J\ MAX} - T_A}{R_{TH\ J\text{-}A}} = \frac{100 - 60}{300} = 0.1\ W$$

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TDA1510
2 × 12W Audio Amplifier

Product Specification

Linear Products

DESCRIPTION

The TDA1510 is a monolithic integrated class B output amplifier in a 13-pin single in-line (SIP) plastic power package. The device is primarily developed for car radio applications, and also to drive low-impedance loads (down to 1.6Ω). At a supply voltage $V_P = 14.4V$. an output power of 24W can be delivered into a 4Ω BTL (Bridge-Tied Load), or, when used as stereo amplifier, it delivers 2 × 12W into 2Ω or 2 × 7W into 4Ω.

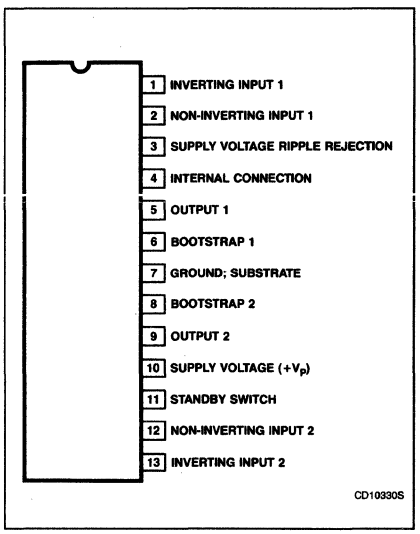
FEATURES

- **Flexibility in use — stereo as well as mono BTL**
- **High output power**
- **Low offset voltage at the output (important for BTL)**
- **Large useable gain variation**
- **Very good ripple rejection**
- **Load dump protection**
- **AC short-circuit safe to ground**
- **Thermal protection**
- **Internal limited bandwidth for high frequencies**
- **Low standby current possibility, to simplify required switches**
- **Low number and small sized external components**
- **High reliability**

APPLICATIONS

- **Car radios**
- **Low-impedance loads**
- **Stereo amplifiers**

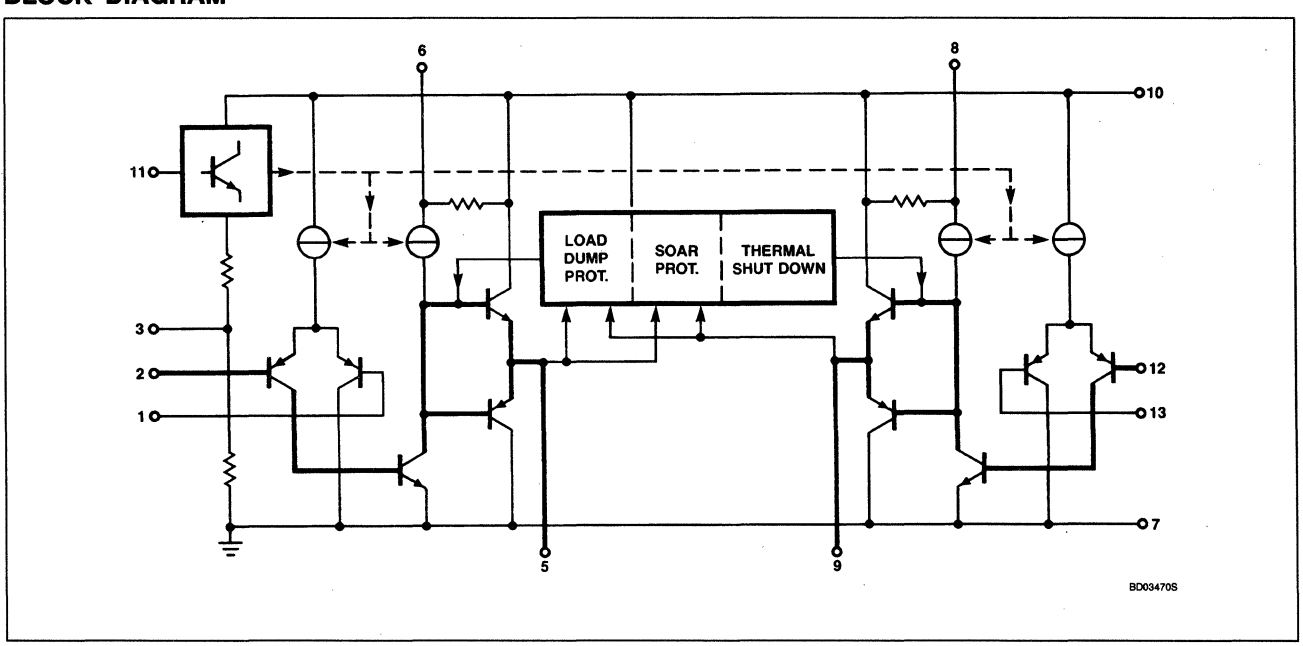
PIN CONFIGURATION



ORDERING CODE

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
13-Pin Plastic Power SIP	0 to +70°C	TDA1510U

BLOCK DIAGRAM



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TDA1515A
24W BTL Audio Amplifier

Product Specification

Linear Products

DESCRIPTION

The TDA1515 is a monolithic integrated class-B output amplifier in a 13 pin single in-line (SIP) plastic power package. The device is primarily developed for car radio applications, and also to drive low-impedance loads (down to 1.6Ω). At a supply voltage V_{CC} = 14.4V, an output power of 21W can be delivered into a 4Ω BTL (Bridge-Tied Load), or, when used as stereo amplifier, it delivers 2 × 11W into 2Ω or 2 × 6.5W into 4Ω.

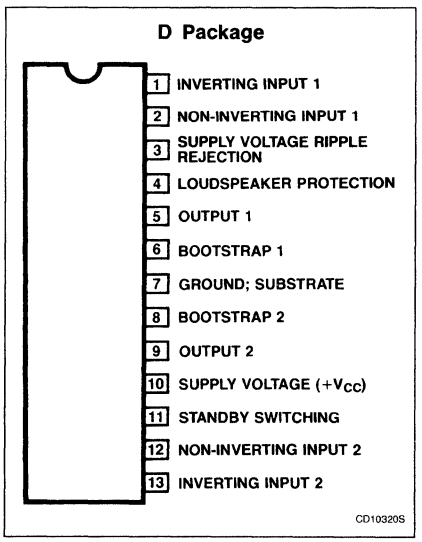
FEATURES

- **Flexibility in use — mono BTL as well as stereo**
- **High output power**
- **Low offset voltage at the output (important for BTL)**
- **Large usable gain variation**
- **Very good ripple rejection**
- **Internal limited bandwidth for high frequencies**
- **Low standby current possibility (typ. 1μA), to simplify required switches; TTL drive possible**
- **Low number and small-sized external components**
- **High reliability**
- **Load dump protection**
- **AC and DC short-circuit safe to ground up to V_{CC} = 18V**
- **Thermal protection**
- **Speaker protection in bridge configuration**
- **SOAR protection**
- **Outputs short-circuit safe to ground in BTL**
- **Reverse-polarity safe**

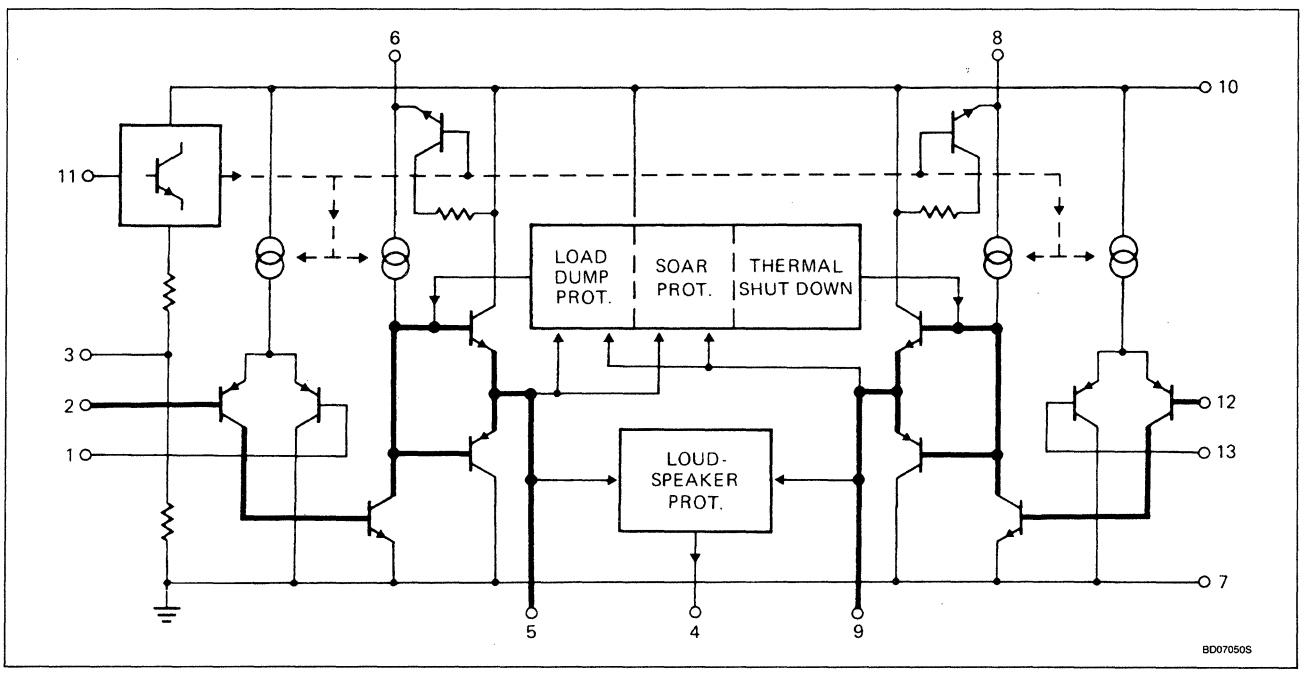
APPLICATIONS

- **Car radio applications**
- **Drive low impedance loads**
- **Stereo amplifier**

PIN CONFIGURATION



BLOCK DIAGRAM



Signetics

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TDA1512
12 to 20W Audio Amplifier

Product Specification

Linear Products

DESCRIPTION

The TDA1512 is a monolithic integrated hi-fi audio power amplifier designed for asymmetrical power supplies.

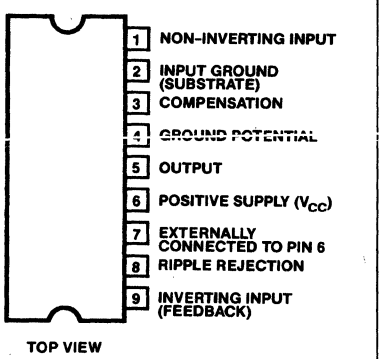
FEATURES

- **Thermal protection**
- **Low intermodulation distortion**
- **Low transient intermodulation distortion**
- **Built-in output current limiter**
- **Low input offset voltage**
- **Output stage with low cross-over distortion**
- **Single in-line (SIP) power package**

APPLICATIONS

- **Television**
- **Radio receivers**
- **Hi-Fi power amp**

PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
9-Pin Plastic SIP (SOT-131B)	−25°C to +150°C	TDA1512U
9-Pin Plastic SIP-bent-to DIP plastic power (SOT-157B)	−25°C to +150°C	TDA1512QU

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	35	V
I_{ORM}	Repetitive peak output current	3.2	A
I_{OSM}	Non-repetitive peak output current	5	A
P_{TOT}	Total power dissipation	see derating curve Figure 1	
T_{STG}	Storage temperature	−55 to +150	°C
T_A	Operating ambient temperature	−25 to +150	°C
t_{SC}	AC short-circuit duration of load during full-load sine-wave drive $R_L = 0$; $V_{CC} = 30V$ with $R_I = 4\Omega$	100	hours
θ_{JMB}	Thermal resitance From junction to mounting base	typ. 3 ⩽4	°C/W °C/W

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NE5050
Power Line Modem

Linear Products

DESCRIPTION

The NE5050 a is a modem for power line and twisted-pair communications. The modem incorporates features to overcome power line impulse noise and line impedance modulation. The modem transmitter section has a Colpitts oscillator, positive logic carrier on/off switch, and driver. The receiver has an amplifier, limiter, amplitude detector, amplitude modulation cancelling stage, impulse filter, and SR flip-flop. One NE5050 can be used to transmit Amplitude Shift Key (ASK carrier on/off) modulation. With two NE5050s, Frequency Shift Key Modulation (FSK) can be implemented. The modem accepts and sends out TTL or CMOS compatible serial data information.

FEATURES

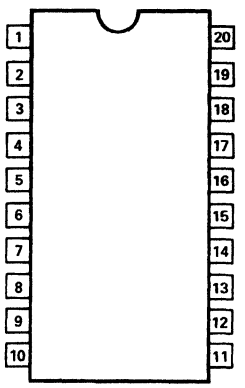
- **High receiver sensitivity — 1mV**
- **Limiter protects overload for signals up to $70V_{P-P}$**
- **High data rates — 300k bit/s over twisted-pair**
- **Has CSMA/CD carrier-sense, multiple access/collision detection capability**
- **Useful balanced interstage ports are available for bandpass filter**
- **Colpitts oscillator tank can be made with crystal or LC network**
- **Receiver signals are processed in real-time making this device suitable for repeater applications**

APPLICATIONS

- **Power line data communications**
- **Twisted-pair data communications**

PIN CONFIGURATION

D[1] and N Packages



CD05031S

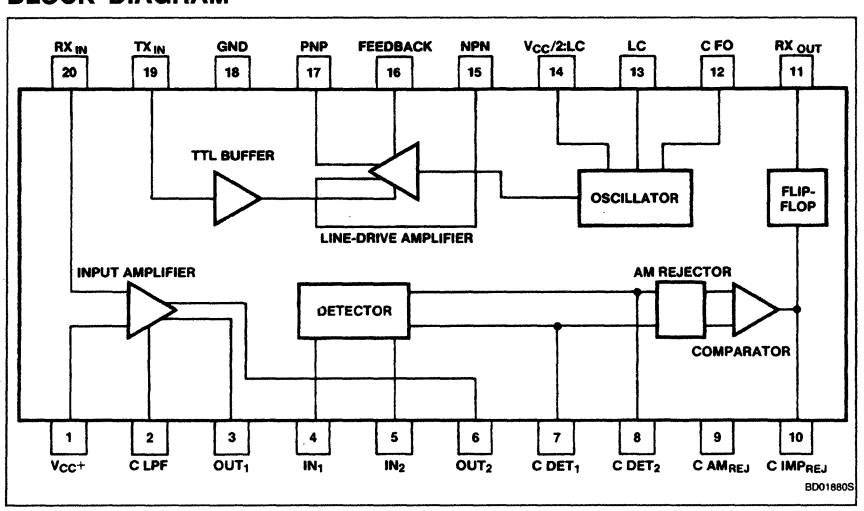
PIN	NAME AND FUNCTION
1	$+V_{CC}$
2	Low-pass filter
3	Amplifier output (+)
4	Detector input (+)
5	Detector input (+)
6	Amplifier output (−)
7	Detector output (−)
8	Detector output (−)
9	AM rejection
10	Impulse filter
11	Receiver output (data out)
12	Oscillator feedback
13	Oscillator I/O
14	Oscillator bias ($+V_{CC}/2$)
15	Transmit carrier (NPN base)
16	Line-drive feedback
17	Transmit carrier (PNP base)
18	Ground
19	Transmitter input (data in)
20	Receiver input (carrier in)

NOTE:
1. SOL — Released in large SO package only.

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
20-Pin Plastic SOL package	0 to 70°C	NE5050D
20-Pin Plastic DIP	0 to 70°C	NE5050N

BLOCK DIAGRAM



Signetics

NE5080
High-Speed FSK Modem Transmitter

Preliminary Specification

Linear Products

DESCRIPTION

The NE5080 is the transmitter chip, of a two-chip set, designed to be the heart of an FSK modem. (The NE5081 is the receiver chip.) The chips are compatible with the IEEE 802.4 standard for a "Single Channel Phase-Continuous-FSK Bus." The specifications shown in this data sheet are those guaranteed when the transmitter is tuned for the frequencies given in the 802 standard. However, both the NE5080 and the NE5081 may be used at other frequencies. The ratio of logic high to logic low frequencies remains fixed at 1.67 to 1.00 at any center frequency.

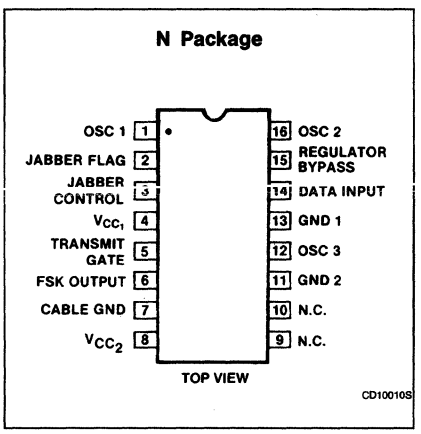
FEATURES

- **Meets IEEE 802.4 standard**
- **Data rates to several Megabaud**
- **Half-or full-duplex operation**
- **Jabber function on-chip**

APPLICATIONS

- **Local Area Networks**
- **Point-to-point communications**
- **Factory automation**
- **Process control**
- **Office automation**

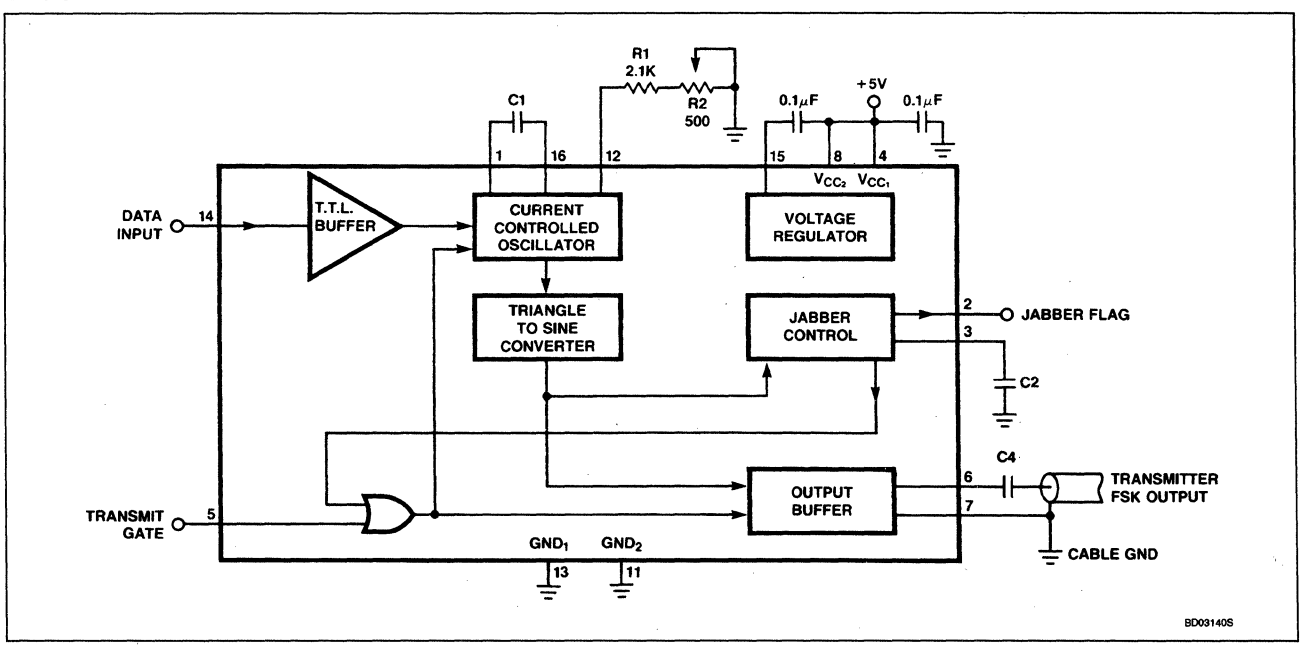
PIN CONFIGURATION



ORDERING CODE

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic DIP		NE5080N

BLOCK DIAGRAM



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NE570/571/SA571
Compandor

Product Specification

Linear Products

DESCRIPTION

The NE570/571 is a versatile low cost dual gain control circuit in which either channel may be used as a dynamic range compressor or expandor. Each channel has a full-wave rectifier to detect the average value of the signal; a linerarized, temperature-compensated variable gain cell; and an operational amplifier.

The NE570/571 is well suited for use in cellular radio and radio communications systems, modems, telephone, and satellite broadcast/receive audio systems.

CIRCUIT DESCRIPTION

The NE570/571 compandor building blocks, as shown in the block diagram, are a full-wave rectifier, a variable gain cell, an operational amplifier and a bias system. The arrangement of these blocks in the IC result in a circuit which can perform well with few external components, yet can be adapted to many diverse applications.

The full-wave rectifier rectifies the input current which flows from the rectifier input, to an internal summing node which is biased at V_{REF}. The rectified current is averaged on an external filter capacitor tied to the C_{RECT} terminal, and the average value of the input current controls the gain of the variable gain cell. The gain will thus be proportional to the average value of the input signal for capacitively coupled voltage inputs as shown in the following equation. Note that for capacitively coupled inputs there is no offset voltage capable of producing a gain error. The only error will come from the bias current of the rectifier (supplied internally) which is less than 0.1μA.

$$G \propto \frac{|V_{IN} - V_{REF}|_{avg}}{R_1}$$

or

$$G \propto \frac{|V_{IN}|_{avg.}}{R_1}$$

FEATURES

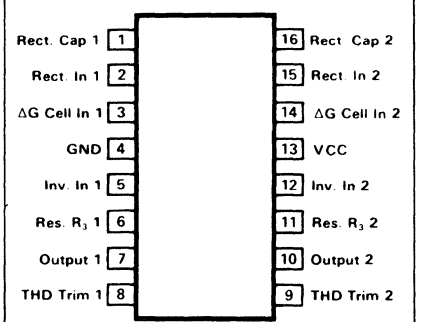
- **Complete compressor and expandor in 1 IC**
- **Temperature compensated**
- **Greater than 110dB dynamic range**
- **Operates down to $6V_{DC}$**
- **System levels adjustable with external components**
- **Distortion may be trimmed out**

APPLICATIONS

- **Cellular radio**
- **Telephone trunk compandor — 570**
- **Telephone subscriber compandor — 571**
- **High level limiter**
- **Low level expandor — noise gate**
- **Dynamic noise reduction systems**
- **Voltage-controlled amplifier**
- **Dynamic filters**

PIN CONFIGURATION

D[1], F, N Packages

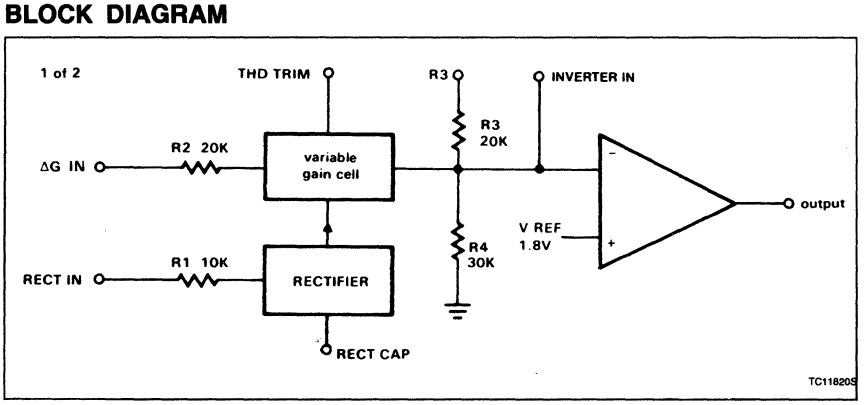


NOTES:
1. SOL - Released in Large SO Package Only.
2. SOL and Non-Standard Pinout.
3. SO and Non-Standard Pinouts.

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-pin Hermetic Cerdip	0 to +70°C	NE570F
16-pin Plastic DIP	0 to +70°C	NE570N
16-pin Plastic SOL	0 to +70°C	NE571D
16-pin Hermetic Cerdip	0 to +70°C	NE571F
16-pin Plastic Cerdip	0 to +70°C	NE571N
16-pin Hermetic Cerdip	-40 to +85°C	SA571F
16-pin Plastic DIP	-40 to +85°C	SA571N

BLOCK DIAGRAM



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SA/NE572

Programmable Analog Compandor

Objective Specification

Linear Products

DESCRIPTION

The NE572 is a dual channel, high performance gain control circuit in which either channel may be used for dynamic range compression or expansion. Each channel has a full wave rectifier to detect the average value of input signal; a linearized, temperature compensated variable gain cell (ΔG) and a dynamic time constant buffer. The buffer permits independent control of dynamic attack and recovery time with minimum external components and improved low frequency gain control ripple distortion over previous compandors.

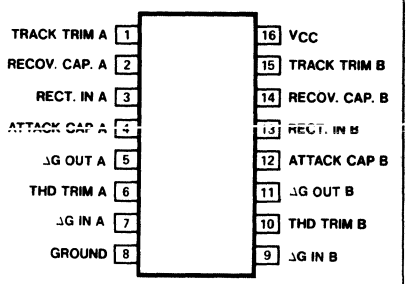
The NE572 is intended for noise reduction in high performance audio systems. It can also be used in a wide range of communication systems and video recording applications.

FEATURES

- **Independent control of attack and recovery time.**
- **Improved low frequency gain control ripple**
- **Complementary gain compression and expansion with external Op Amp**
- **Wide dynamic range—greater than 110dB**
- **Temperature compensated gain control**
- **Low distortion gain cell**
- **Low noise—6μV typical**
- **Wide supply voltage range—6V–22V**
- **System level adjustable with external components.**

PIN CONFIGURATION

D, N PACKAGE



(Top view)

ORDER PART NO.

NE572N SA572N
SA572F NE572D SA572D

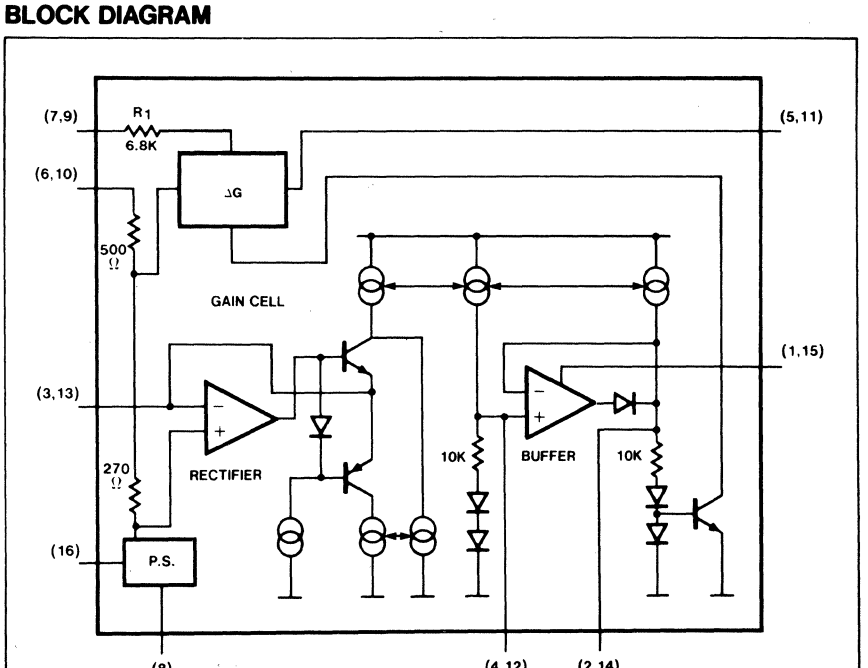
APPLICATIONS

- **Dynamic noise reduction system**
- **Voltage control amplifier**
- **Stereo expandor**
- **Automatic level control**
- **High level limiter**
- **Low level noise gate**
- **State variable filter**

ABSOLUTE MAXIMUM RATINGS

	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	22	VDC
T_A	Operating temperature range NE572	0 to 70	°C
	Operating temperature range SA572	-40 to +85	°C
P_D	Power dissipation	500	mW

BLOCK DIAGRAM



Note:
1. Supplied only in large SO (Small Outline) package.

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SA/NE602
Double Balanced Mixer And Oscillator

Product Specification

Linear Products

DESCRIPTION

The SA/NE602 is a low-power VHF monolithic double balanced mixer with input amplifier, on-board oscillator, and voltage regulator. It is intended for high performance, low power communication systems. The guaranteed parameters of the SA602 make this device particularly well suited for cellular radio applications. The mixer is a "Gilbert cell" multiplier configuration which typically provides 18dB of gain at 45MHz. The oscillator will operate to 200MHz. It can be configured as a crystal oscillator, a tuned tank oscillator, or a buffer for an external L.O. The noise figure at 45MHz is typically less than 5dB. The gain, intercept performance, low-power and noise characteristics make the SA/NE602 a superior choice for high-performance battery operated equipment. It is available in an 8-lead dual-in-line plastic package and an 8-lead SO (surface-mount miniature package).

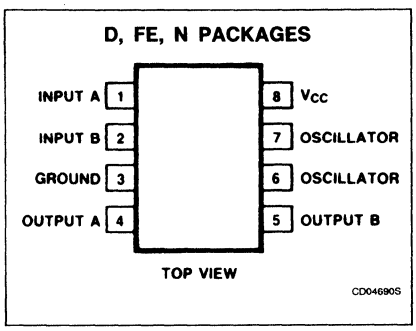
FEATURES

- **Low current consumption: 2.4mA typical**
- **Excellent noise figure: < 5.0dB typical at 45MHz**
- **High operating frequency**
- **Excellent gain, intercept and sensitivity**
- **Low external parts count; suitable for crystal/ceramic filters**
- **SA602 meets cellular radio specifications**

APPLICATIONS

- **Cellular radio mixer/oscillator**
- **Portable radio**
- **VHF transceivers**
- **RF data links**
- **HF/VHF frequency conversion**
- **Instrumentation frequency conversion**
- **Broadband LAN's**

PIN CONFIGURATION



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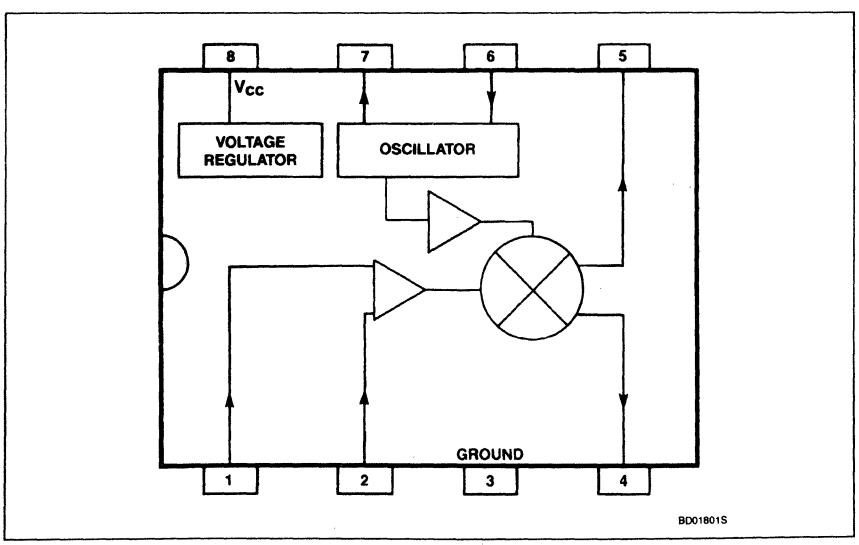

Signetics

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NE612
Double Balanced Mixer And Oscillator

Product Specification

Linear Products

DESCRIPTION

The NE612 is a low-power VHF monolithic double balanced mixer with onboard oscillator and voltage regulator. It is intended for low cost, low power communication systems with signal frequencies to 500MHz and local oscillator frequencies as high as 200MHz. The mixer is a "Gilbert cell" multiplier configuration which provides gain of 14dB or more at 49MHz.

The oscillator can be configured for a crystal, a tuned tank operation, or as a buffer for an external L.O. Noise figure at 49MHz is typically below 6dB and makes the device well suited for high performance cordless telephone. The low power consumption makes the NE612 excellent for battery operated equipment. Networking and other communications products can benefit from very low radiated energy levels within systems. The NE612 is available in an 8- lead dual-in-line plastic package and an 8-lead SO (surface mounted miniature package).

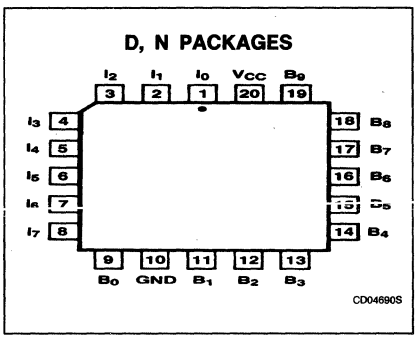
FEATURES

- **Low current consumption**
- **Low cost**
- **Operation to 500MHz**
- **Low radiated energy**
- **Low external parts count; suitable for crystal/ceramic filter**
- **Excellent sensitivity, gain, and noise figure**

APPLICATIONS

- **Cordless telephone**
- **Portable radio**
- **VHF transceivers**
- **RF data links**
- **Sonabuoys**
- **Communications receivers**
- **Broadband LAN's**
- **HF and VHF frequency conversion**

PIN CONFIGURATION



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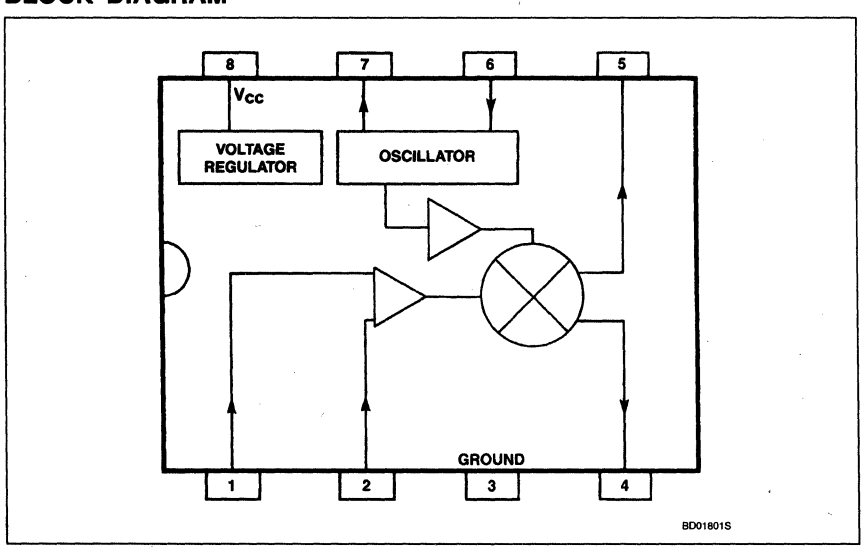

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SA/NE 604
Low Power FM IF System

Product Specification

Linear Products

DESCRIPTION

The SA/NE604 is a monolithic low-power FM IF system incorporating two limiting intermediate frequency amplifiers, quadrature detector, muting, logarithmic signal strength indicator, and voltage regulator. The SA/NE604 is available in a 16-lead dual-in-line plastic and Cerdip packages and 16-lead SO (surface-mounted miniature package).

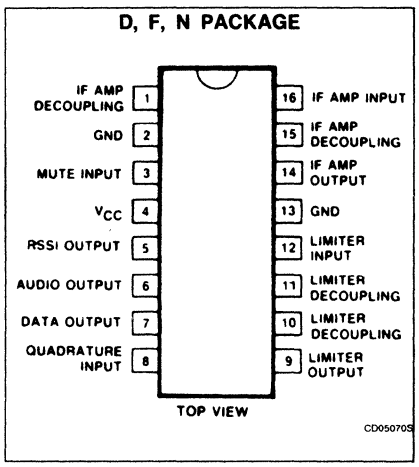
FEATURES

- **Low-power consumption: 2.3mA typical**
- **Logarithmic Received Signal Strength Indicator (RSSI) with a dynamic range in excess of 90dB**
- **Separate data output**
- **Audio output with muting**
- **Low external count; suitable for crystal/ceramic filters**
- **Excellent sensitivity: 1.5μV across input pins (0.27μV into 50Ω matching network) for 12dB SINAD (Signal to Noise and Distortion ratio) at 455kHz**
- **SA604 meets cellular radio specifications**

APPLICATIONS

- **Cellular Radio FM IF**
- **Communications receivers**
- **Intermediate frequency amplification and detection up to 15MHz**
- **RF level meter**
- **Spectrum analyzer**
- **Instrumentation**

PIN CONFIGURATION



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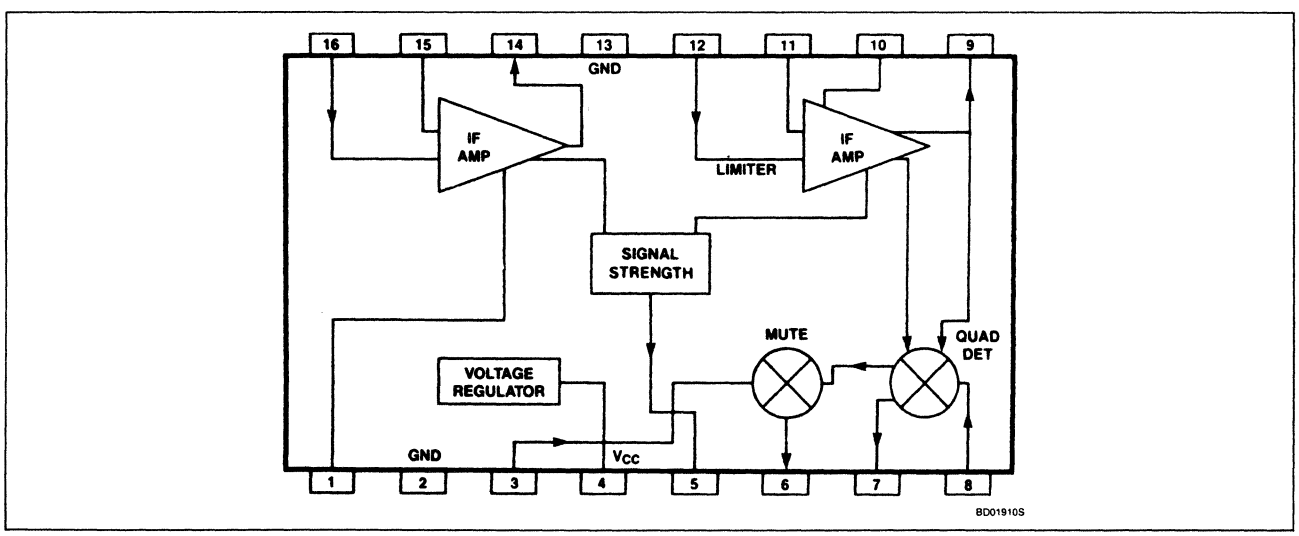


Signetics

Signetics

NE614
Low Power FM IF System

Product Specification

Linear Products

DESCRIPTION

The NE614 is a monolithic low-power FM IF system incorporating two limiting intermediate frequency amplifiers, quadrature detector, muting, logarithmic signal strength indicator, and voltage regulator. The NE614 is available in a 16-lead dual-in-line plastic package and 16-lead SO (surface-mounted miniature package).

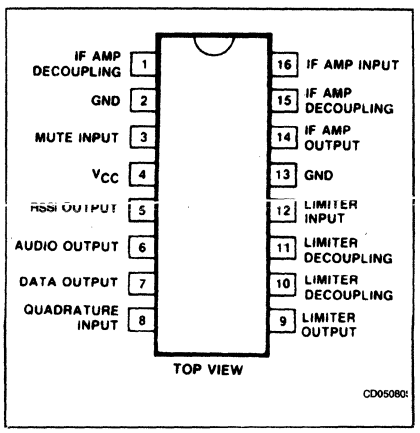
FEATURES

- **Low-power consumption**
- **Logarithmic signal strength indicator**
- **Separate data output**
- **Audio output with muting**
- **Low external count; suitable for crystal/ceramic filters**
- **Excellent sensitivity**

APPLICATIONS

- **Cellular Radio FM IF**
- **Communications receivers**
- **Intermediate frequency amplification and detection up to 15MHz**
- **RF level meter**
- **Spectrum analyzer**
- **Instrumentation**
- **Cordless telephone**
- **Remote control**

PIN CONFIGURATION



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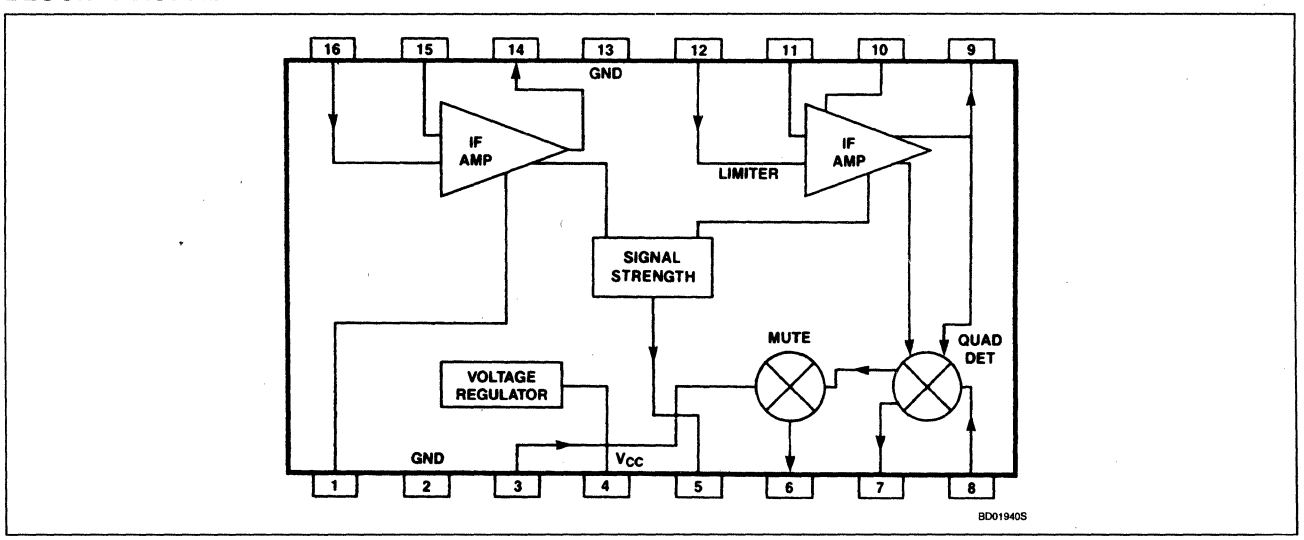

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TDA5030T
VHF Mixer/Oscillator

Linear Products

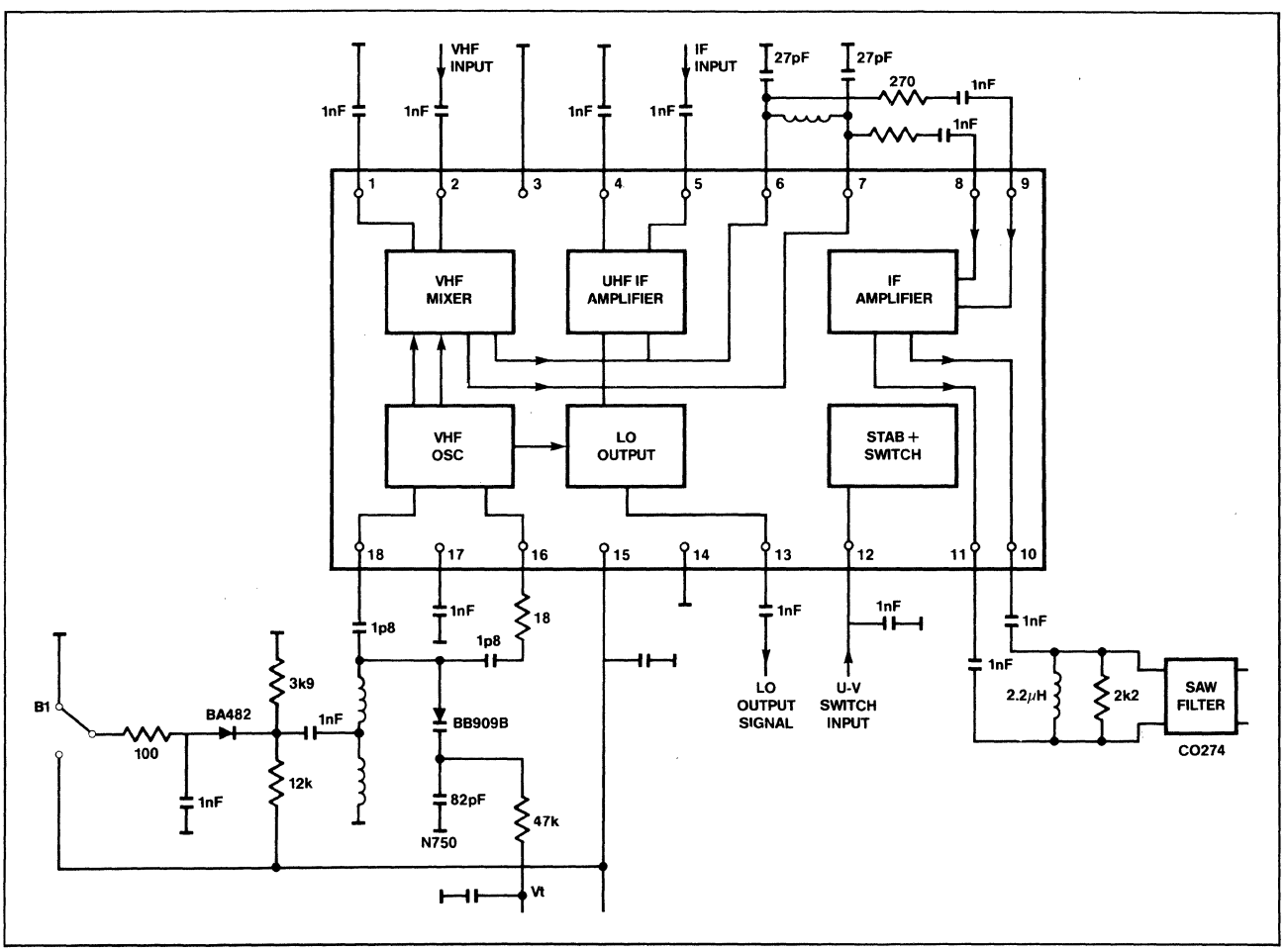
Preliminary Specification

DESCRIPTION
The TDA5030T is a monolithic IC for the VHF mixer/oscillator function in TV tuners.

FEATURES
- **Balanced mixer**
- **Amplitude controlled oscillator**
- **SAW filter preamplifier**
- **UHF IF preamplifier**
- **Buffered stage for drive of a prescaler with the oscillator signal**
- **Voltage stabilizer**
- **U-V switching circuit**

APPLICATIONS
- **Mixer/oscillator**
- **RF receiver**
- **Tuners**
- **CATV**

BLOCK DIAGRAM



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TDD1742T
CMOS Frequency Synthesizer (Lopsy)

Advance Information

Linear Products

DESCRIPTION

The TDD1742T is an oxide-isolated CMOS (LOCMOS) circuit designed specifically for Low Power Frequency Synthesizer applications, especially for VHF and UHF portables.

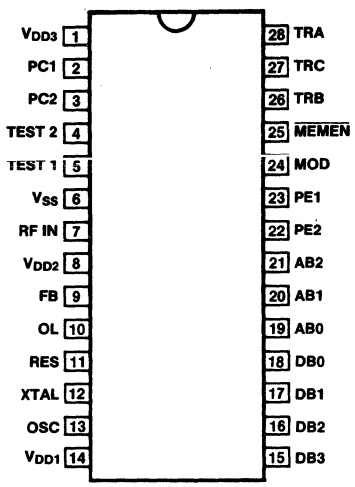
FEATURES

- **Single chip with on-board sample and hold capacitor**
- **Low power requirements**
- **High performance phase comparator with low phase noise and spurious response**
- **Auxiliary digital phase comparator for fast locking**
- **On-board phase modulator**
- **Simple interface to memory**
- **Microprocessor controllable**
- **Power-on reset circuitry**

APPLICATIONS

- **Frequency synthesizers**
- **Radio/TV LO circuit**

PIN CONFIGURATION



TOP VIEW

CD01350S

PIN	SYMBOL	FUNCTION
1	V_{DD3}	Main power supply; +7 to +10V
2	PC1	High-gain phase comparator (analogue)
3	PC2	Low-gain phase comparator (digital)
4	Test 2	Not connected
5	Test 1	Not connected
6	V_{SS}	Positive power supply
7	RF IN	RF input
8	V_{DD2}	Power supply for TTL-compatible stages; +5V ± 10%
9	FB	Feedback to pre-scaler
10	OL	Out-of-lock indication
11	RES	Power-on-reset
12	XTAL	Reference oscillator/buffer output
13	OSC	Reference oscillator/buffer input
14	V_{DD1}	Main power supply; +7 to +10V
15	DB3	Data bus inputs
16	DB2	Data bus inputs
17	DB1	Data bus inputs
18	DB0	Data bus inputs
19	AB0	Address bus
20	AB1	Address bus
21	AB2	Address bus
22	PE2	Program enable 2
23	PE1	Program enable 1
24	MOD	Phase modulation input
25	$\overline{\text{MEMEN}}$	Memory enable
26	TRB	Bias resistor R_B
27	TRC	Bias resistor R_C
28	TRA	Bias resistor R_A

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TDA7000
Single-Chip FM Radio Circuit

Preliminary Specification

Linear Products

DESCRIPTION

The TDA7000 is a monolithic integrated circuit for mono FM portable radios where a minimum of peripheral components is important (small dimensions and low costs).

The IC has an FLL (Frequency-Locked Loop) system with an intermediate frequency of 70kHz. The IF selectivity is obtained by active RC filters. The only function which needs alignment is the resonant circuit for the oscillator, thus selecting the reception frequency. Spurious reception is avoided by means of a mute circuit, which also eliminates too-noisy input signals. Special precautions are taken to meet the radiation requirements.

FEATURES

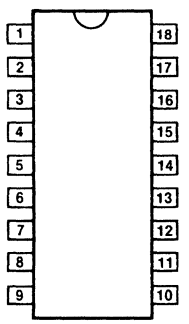
- **RF input stage**
- **Mixer**
- **Local oscillator**
- **IF amplifier/limiter**
- **Phase demodulator**
- **Mute detector**
- **Mute switch**

APPLICATIONS

- **Mono FM Portable Radio**
- **Wireless Telephone**
- **LAN**
- **Data Receivers**
- **SCA Receiver**

PIN CONFIGURATION

N Package



TOP VIEW

CD10150S

PIN DESCRIPTION

PIN NO.	NAME AND FUNCTION
1	Muting capacitor
2	Audio frequency output
3	Noise source
4	Loop filter capacitor
5	Supply Voltage
6	VCO
7	1st integrator capacitor (to Pin 9)
8	2nd integrator capacitor
9	1st integrator capacitor (to Pin 7)
10	IF filter capacitor (to Pin 11)
11	If filter capacitor
12	If limiter capacitor
13	RF input
14	Mixer
15	Current source capacitor
16	Ground
17	Demodulator capacitor
18	Correlator capacitor

ORDERING CODE

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
18-pin Plastic DIP	0°C to +70°C	TDA7000N

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage (Pin 5)	12	V
V_{6-5}	Oscillator voltage (Pin 6)	$V_{CC}-0.5$ to $V_{CC}+0.5$	V
P_{TOT}	Total power dissipation	See derating curve Figure 2	
T_{STG}	Storage temperature range	−55 to +150	°C
T_A	Operating ambient temperature range	0 to +60	°C

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TDA7010T
FM Radio Circuit (SO Package)

Product Specification

Linear Products

DESCRIPTION

The TDA7010T is a monolithic integrated circuit for mono FM portable radios, where a minimum of peripheral components is important (small dimensions and low costs).

The IC has an FLL (Frequency-Locked Loop) system with an intermediate frequency of 70kHz. The IF selectivity is obtained by active RC filters. The only function which needs alignment is the resonant circuit for the oscillator, thus selecting the reception frequency. Spurious reception is avoided by means of a mute circuit, which also eliminates too noisy input signals. Special precautions are taken to meet the radiation requirements.

FEATURES

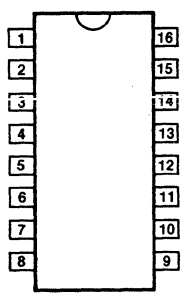
- **RF input stage**
- **Mixer**
- **Local oscillator**
- **IF amplifier/limiter**
- **Phase demodulator**
- **Mute detector**
- **Mute switch**

APPLICATIONS

- **Mono FM Portable Radio**
- **Wireless Telephone**
- **LAN**
- **Data Recievers**
- **SCA Receivers**

PIN CONFIGURATION

D Package



PIN DESCRIPTION

PIN NO.	NAME AND FUNCTION
1	Muting capacitor
2	Audio frequency output
3	Loop filter capacitor
4	Supply Voltage
5	VCO
6	1st integrator capacitor (to Pin 7)
7	2nd integrator capacitor
8	1st integrator capacitor (to Pin 8)
9	IF filter capacitor (to Pin 11)
10	If limiter capacitor
11	RF input
12	Mixer
13	Current source capacitor
14	Ground
15	Demodulator capacitor
16	Correlator capacitor

ORDERING CODE

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic SO DIP	0°C to +70°C	TDA7010TD

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage (Pin 4)	12	V
V_{6-5}	Oscillator voltage (Pin 5)	$V_{CC}-0.5$ to $V_{CC}+0.5$	V
	Total power dissipation	See derating curve Figure 2	
T_{STG}	Storage temperature range	−55 to +150	°C
T_A	Operating ambient temperature range	0 to +60	°C

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TDA7020T
FM Radio Circuit

Product Specification

Linear Products

DESCRIPTION

The TDA7020T integrated circuit is for FM portable radios, stereo as well as mono, where a minimum periphery is important in terms of small dimensions and low cost. The IC has a FLL (Frequency-Locked Loop) system with an intermediate frequency of 76 kHz. The selectivity is obtained by active RC filters. The only function to be tuned is the resonant circuit of the oscillator. Interstation noise as well as noise from receiving weak signals is reduced by a correlation mute system.

Special precautions have been taken to meet local oscillator radiation requirements. Because of the low intermediate frequency, low pass filtering of the MPX signal is required to avoid noise when receiving stereo. 50kHz roll-off compensation, needed because of the low pass characteristic of the FLL, is performed by the integrated LF amplifier. For mono application this amplifier can be used to directly drive an earphone. The field strength detector enables field strength dependent channel separation control.

FEATURES

- **RF input stage**
- **Mixer**
- **Local oscillator**
- **IF amplifier/limiter**
- **Frequency detector**
- **Mute circuit**
- **RF input frequency range to 110MHz**
- **Loop amplifier**
- **Internal reference circuit**
- **LF amplifier for:**
  - **— mono earphone amplifier or**
  - **— MPX filter**
- **Field strength dependent channel separation control facility**

APPLICATIONS

- **FM radios**
- **Stereo**
- **Mono**

ORDERING CODE

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic SO DIP	0°C to +70°C	TDA7020TD

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_P	Supply voltage (Pin 4)	7	V
V_{6-5}	Oscillator voltage (Pin 5)	V_p−0.5 to V_p+0.5	V
P_{TOT}	Total power dissipation (see derating curve, Figure 2)		
T_{STG}	Storage temperature range	−55 to +150	°C
T_A	Operating temperature range	−10 to +70	°C

Signetics

Signetics

NE5900
Call Progress Decoder

Product Specification

Linear Products

DESCRIPTION

The NE5900 call progress decoder (CPD) is a low cost, low power CMOS integrated circuit designed to interface with a microprocessor-controlled smart telephone capable of making preprogrammed telephone calls. The call progress decoder provides information to permit microprocessor decisions whether to initiate, continue, or terminate calls. A tri-state, 3-bit output code indicates the presence of dial tone, audible ringback, busy signal, or reorder tones.

A front-end bandpass filter is accomplished with switched capacitors. The bandshaped signal is detected and the cadence is measured prior to output decoding. In addition to the three data bits, a buffered bandpass output and envelope output are available. All logic inputs and outputs can interface with LSTTL, CMOS, and NMOS.

Circuit features include low power consumption and easy application. Few and inexpensive external components are required. A typical application requires a 3.58MHz crystal or clock, 470kΩ resistor, and two bypass capacitors. The NE5900 is effective where traditional call progress tones, PBX tones, and precision call progress tones must be correctly interpreted with a single circuit.

FEATURES

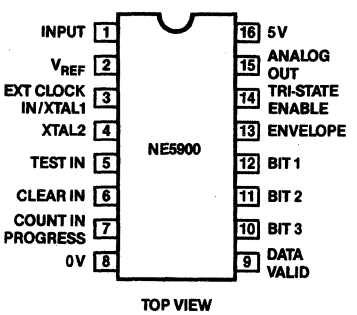
- **Fully decoded tri-state call progress status output**
- **Works with traditional, precision, or PBX call progress tones**
- **Low power consumption**
- **Low cost 3.58MHz crystal or clock**
- **No calibration or adjustment**
- **Interfaces with LSTLL, CMOS, NMOS**
- **Easy application**

APPLICATIONS

- **Modems**
- **PBXs**
- **Security equipment**
- **Auto dialers**
- **Answering machines**
- **Remote diagnostics**
- **Pay telephones**

PIN CONFIGURATION

D[1] and N Packages

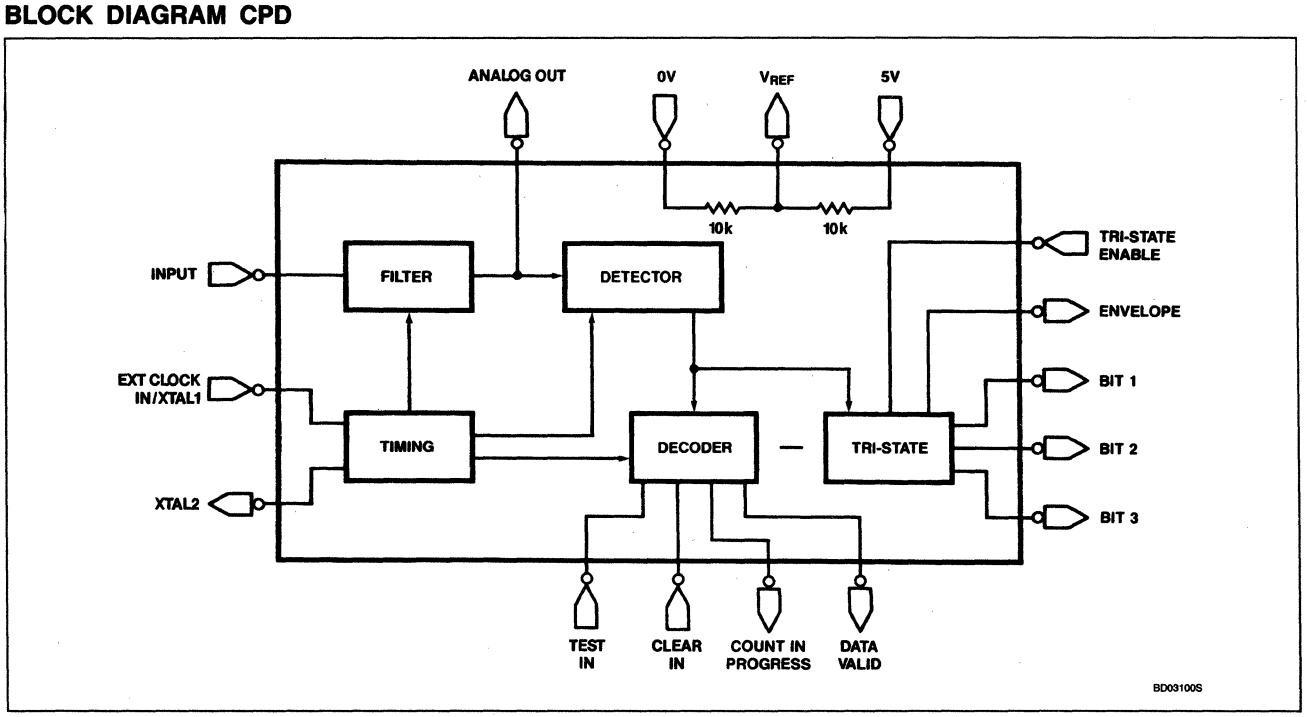


TOP VIEW

CD09970S

NOTES:
1. SOL — Released in large SO package only.

BLOCK DIAGRAM CPD



BD03100S

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PCD3310
Pulse and DTMF Dialer with Redial

Advance Information

Linear Products

DESCRIPTION

The PCD3310 is a single-chip silicon-gate CMOS integrated circuit with an on-chip oscillator for a 3.58MHz crystal. It is a dual-standard dialing circuit for either pulse dialing (PD) or dual tone multi-frequency (DTMF) dialing.

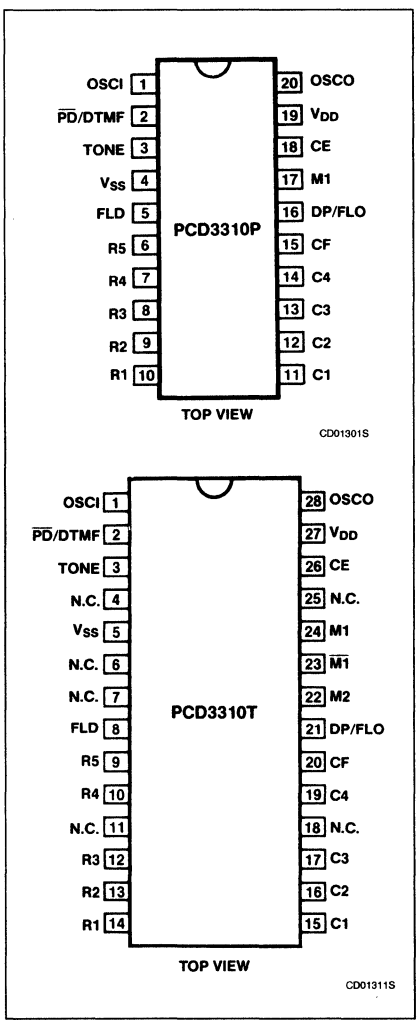
Input data is derived from any standard matrix keypad for dialing in either DP or DTMF mode. Numbers of up to 23 digits can be retained in RAM for redial and notepad facilities.

In DTMF mode, bursts as well as pauses are timed to a minimum in manual dialing, the maximum depending on the key depression time.

FEATURES

- **PD and DTMF dialing.**
- **23-digit capacity for redial operation (cursor method)**
- **Memory clear and electronic notepad**
- **Mixed mode dialing (start with DP and end with DTMF dialing**
- **Dual redial buffers for PABX and public calls**
- **Four extra function keys: program, flash, redial and PD to DTMF (mixed dialing)**
- **DTMF timing:**
  - **manual dialing-minimum duration for bursts and pauses**
  - **redialing-calibrated timing**
- **On-chip voltage reference for supply and temperature independent tone output**
- **On-chip filtering for low output distortion (CEPT CS 203 compatible)**
- **On-chip oscillator with low cost 3.58MHz TV color-burst crystal**
- **Uses standard single-contact or double-contact (common left open) keypad**
- **Keyboard entries fully debounced at both edges**
- **Flash (register recall) output**

PIN CONFIGURATION



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TEA1067
Low Voltage Transmission IC With Dialer Interface

Advance Information

Linear Products

DESCRIPTION

The TEA1067 is a low-voltage bipolar integrated circuit performing all speech and line interface functions required in fully electronic telephone sets. The TEA1067 operates down to 2.0V which facilitates the use of telephone sets in parallel operation. Electronic switching between dialing and speech is performed by internal circuitry. Other specifications similar to TEA1060/61.

FEATURES

- **Low DC line voltage; operates down to 2V excluding polarity guard.**
- **Minimum instantaneous line voltage 0.9V excluding polarity guard.**
- **Voltage regular with adjustable static resistance.**
- **Provides supply with limited current for external circuitry.**
- **Symmetrical high-impedance inputs (64kohm) for dynamic, magnetic or piezoelectric microphones.**
- **Asymmetrical high-impedance input (32kohm) for electret microphone.**
- **DTMF signal input.**
- **Mute input for pulse or DTMF dialing.**
- **Power down input for pulse dial or register recall.**
- **Receiving amplifier for magnetic, dynamic or piezoelectric earpieces.**
- **Large amplification setting range on microphone and earpiece amplifiers.**
- **Line loss compensation facility, line current dependent.**
- **Gain control adaptable to exchange supply.**
- **Possibility to adjust the DC line voltage.**

APPLICATIONS

- **Telephone handsets requiring low operating voltage.**

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TEA1080

Supply IC for Telephone Set Peripherals

Product Specification

Linear Products

DESCRIPTION

The TEA1080 is a bipolar integrated circuit intended for use in line-powered telephone sets to supply peripheral circuits for extended dialing and/or loudspeaking facilities.

The IC uses a part of the surplus of the line current sinked normally in the voltage regulator of the applied speech/transmission circuit.

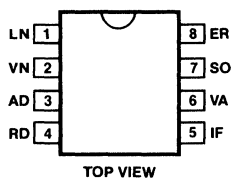
FEATURES

- **High input impedance for audio signals**
- **High output current**
- **Large audio signal handling**
- **Low distortion**
- **Two modes of operation:**
  - **regulated output voltage**
  - **constant DC voltage drop in series with a resistor between line and output terminal**
- **Low number of external components**

APPLICATION

- **Telephone hand sets**

PIN CONFIGURATION



TOP VIEW

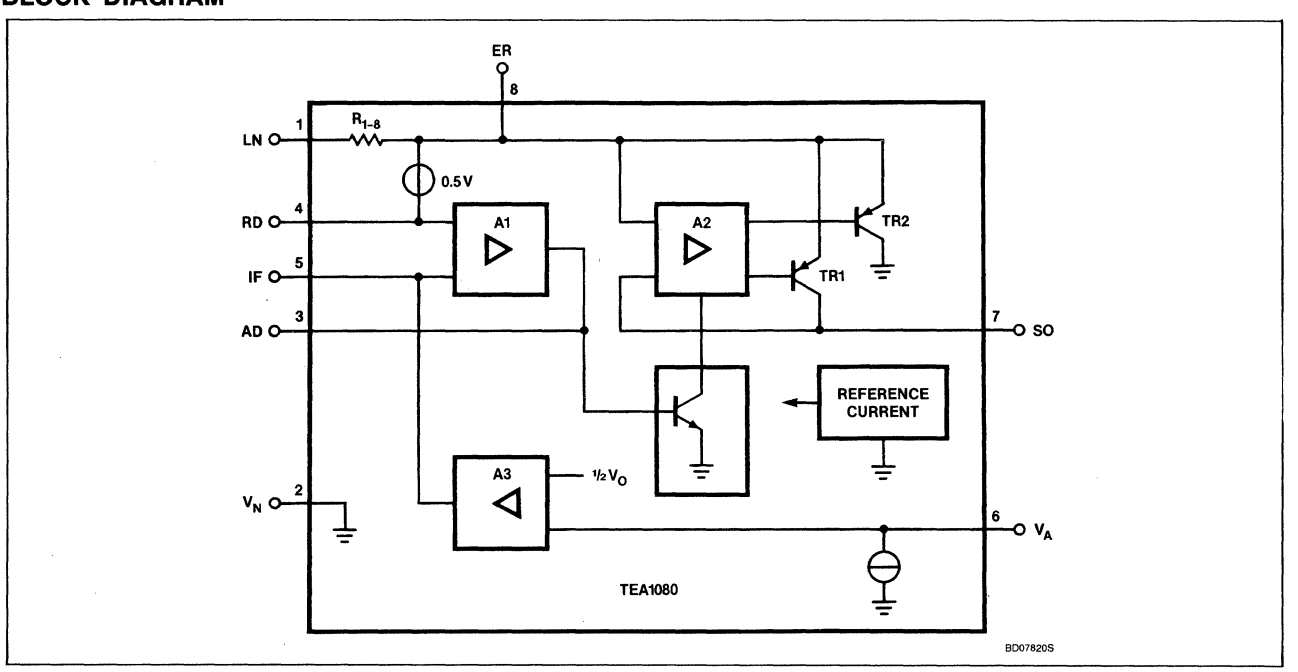
CD01371S

PIN NO.	SYMBOL	DESCRIPTION
1	LN	Positive line terminal
2	VN	Negative line terminal
3	AD	Amplifier decoupling
4	RD	Regulator input
5	IF	Input low-pass filter
6	VA	Output voltage adjustment
7	SO	Supply output
8	ER	Supply terminal of the internal circuit

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic DIP (SOT-97A)	−25°C to +70°C	TEA1080PN

BLOCK DIAGRAM



Signetics

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MEA8000
Voice Synthesizer

Linear Products

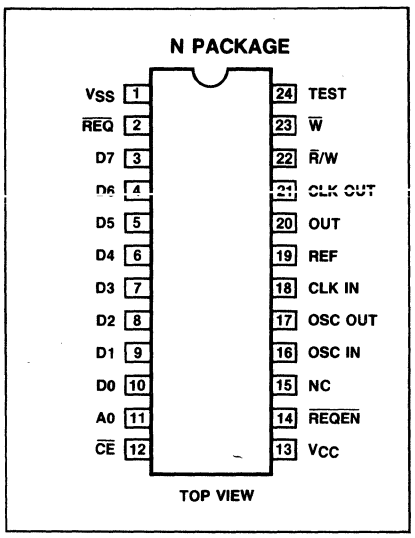
Preliminary Specification

DESCRIPTION
The MEA8000 is a 24-pin N MOS integrated circuit for generating good quality speech from digital code with a programmable bit rate. The circuit is primarily intended for applications in microprocessor controlled systems, where the speech code is stored separately in a Read-Only Memory. An efficient, easy-to-use speech editing and encoding system with EPROM programming capability, has been specially developed.

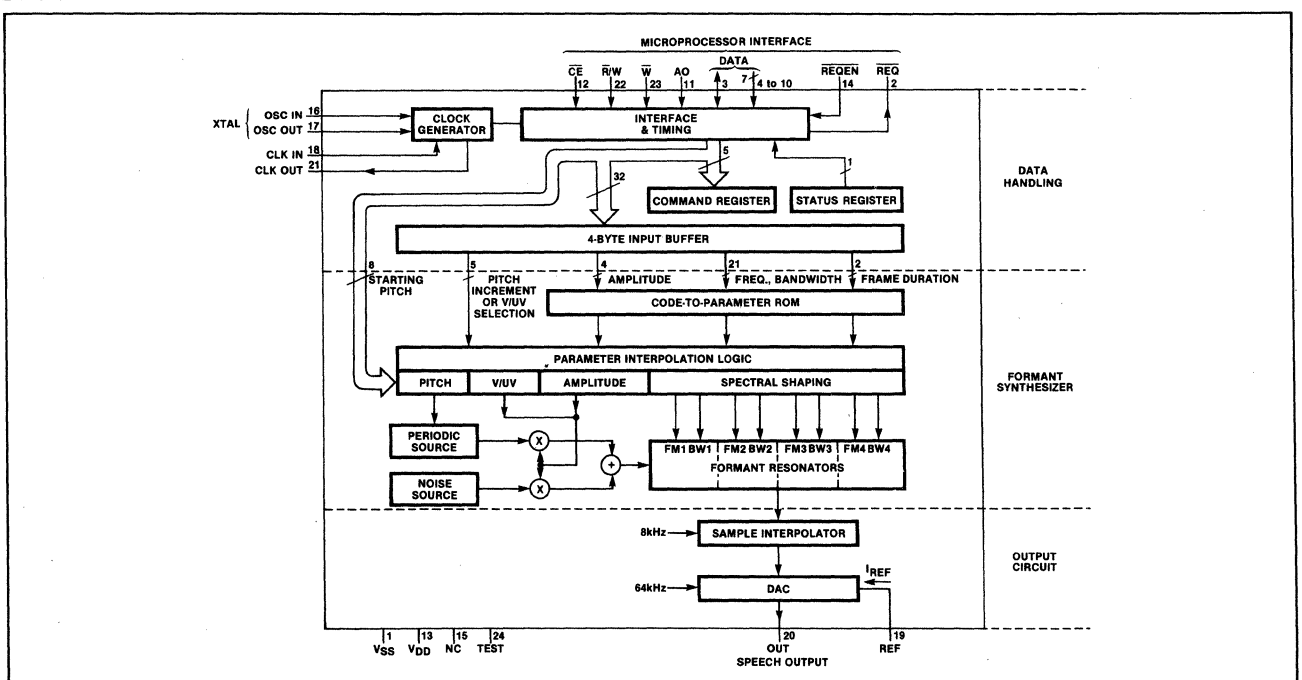
APPLICATIONS
- **Telephony**
- **Automotive**
- **Computer response/prompt.**
- **Video games.**
- **General industrial.**

FEATURES
- **Microprocessor interface capability including an 8-bit data bus, an enable and a read/write input control signals.**
- **32-bit data buffer holding speech frame codes.**
- **Digital filter of 8th order with 3 programmable formant frequencies, one fixed formant frequency, and 4 programmable formant bandwidths. 4 kHz bandwidth.**
- **Programmable amplitudes.**
- **Programmable duration of each frame: 8, 16, 32, or 64 milliseconds.**
- **Low data rate: average 1000 bits/sec.**
- **Operates from standard EPROMs/ROMs.**
- **Minimal external audio filter requirement.**
- **Crystal controlled oscillator or external (TTL) clock.**
- **Single +5 V power supply.**

PIN CONFIGURATION



BLOCK DIAGRAM



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NE5150/5151/5152
Triple 4-Bit RGB D/A Converter with Memory
Triple 4-Bit RGB D/A Converter

Linear Products

Preliminary Specification

DESCRIPTION

The NE5150/5151/5152 are triple 4-bit DACs intended for use in graphic display systems. They are a high performance — yet cost effective — means of interfacing digital memory and a CRT. The NE5150/5152 are single integrated circuit chips containing special input buffers, an ECL static RAM, high-speed latches, and three 4-bit DACs. The input buffers are user-selectable as either ECL or TTL compatible for the NE5150. The NE5152 is similar to the NE5150, but is TTL compatible only, and operates off of a single +5V supply. The RAM is organized as 16 × 12, so that 16 "color words" can be down loaded from the pixel memory into the chip memory. Each 12-bit word represents 4 bits of red, 4 bits of green and 4 bits of blue information. This system gives 4096 possible colors. The RAM is fast enough to completely reload during the horizontal retrace time. The latches resynchronize the digital data to the DACs to prevent glitches. The DACs include all the composite video functions to make the output waveforms meet RS-170 and RS-343 standards, and produce $1V_{P-P}$ into 75Ω. The composite functions (reference white, bright, blank, and sync) are latched to prevent screen-edge distortions generally found on "video DACs." External components are kept to an absolute minimum (bypass capacitors only as needed) by including all reference generation circuitry and termination resistors on-chip, by building in high-frequency PSRR (eliminating separate V_{EE}s and costly power supplies and filtering), and by using a single-ended clock. The guaranteed maximum operating frequency for the NE5150/5152 is 110MHz over the commercial termperature range. The devices are housed in a standard 24-pin package and consume less than 1W of power.

The NE5151 is a simplified version of the NE5150, including all functions except the memory. Maximum operating frequency is 150MHz.

FEATURES

- **Single-chip**
- **On-board ECL static RAM**
- **4096 colors**
- **ECL and TTL compatible**
- **110MHz update rate (NE5150, 5152)**
- **150MHz update rate (NE5151)**
- **Low power and cost**
- **Drives 75Ω cable directly**
- **Internal reference**
- **40dB PSRR**
- **No external components necessary**

APPLICATIONS

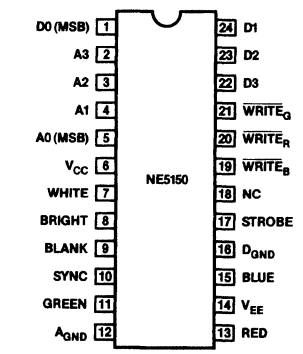
- **Bit-mapped graphics**
- **Super high-speed DAC**
- **Home computers**
- **Raster-scan displays**

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDE CODE
24-Pin Ceramic DIP	0°C to +70°C	NE5150F
24-Pin Ceramic DIP	0°C to +70°C	NE5151F
24-Pin Ceramic DIP	0°C to +70°C	NE5152F

PIN CONFIGURATIONS

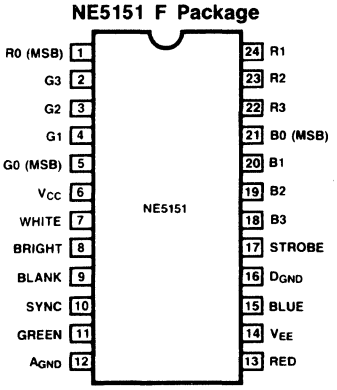
NE5150 F Package



CD09550S

TOP VIEW

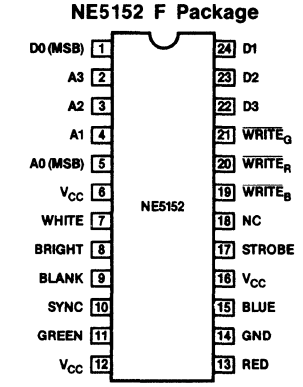
NE5151 F Package



CD09560S

TOP VIEW

NE5152 F Package



CD09570S

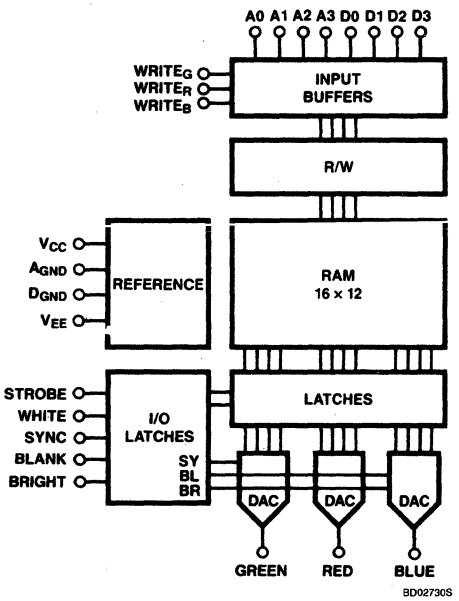
TOP VIEW

Signetics

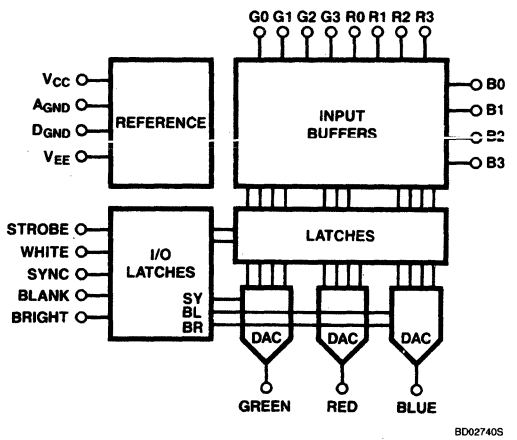
Triple 4-Bit RGB D/A Converter with Memory NE5150/5151/5152

BLOCK DIAGRAMS

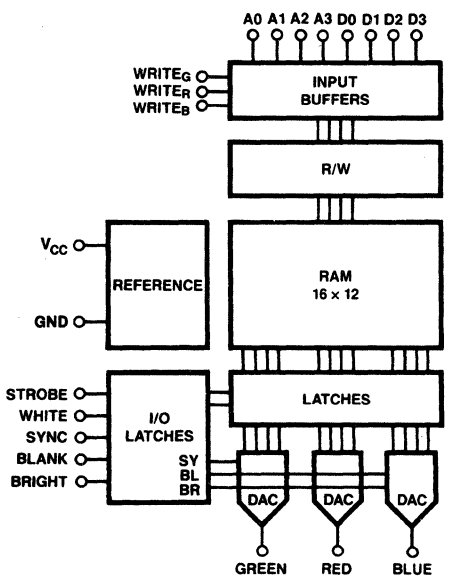
NE5150



NE5151



NE5152



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SE/NE5018
8-Bit μP-Compatible D/A Converter

Product Specification

Linear Products

DESCRIPTION

The NE5018 is a complete 8-bit digital-to-analog converter subsystem on one monolithic chip. The data inputs have input latches, controlled by a latch enable pin. The data and latch enable inputs are ultralow loading for easy interfacing with all logic systems. The latches appear transparent when the $\overline{LE}$ input is in the low state. When $\overline{LE}$ goes high, the input data present at the moment of transition is latched and retained until $\overline{LE}$ again goes low. This feature allows easy compatibility with most microprocessors.

The chip also comprises a stable voltage reference (5V nominal) and high slew ratre buffer amplifier. The voltage reference may be externally trimmed with a potentiometer for easy adjustment of full-scale, while maintaining a low temperature coefficient.

The output of the buffer amplifier may be offset so as to provide bipolar as well as unipolar operation.

FEATURES

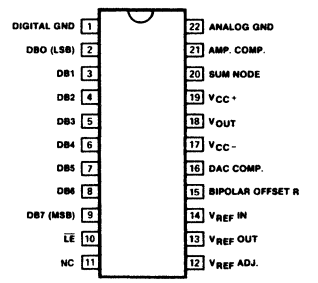
- **8-bit resolution**
- **Input latches**
- **Low-loading data inputs**
- **On-chip voltage reference**
- **Output buffer amplifier**
- **Accurate to ± ½ LSB (0.19%)**
- **Monotonic to 8 bits**
- **Amplifier and reference both shortcircuit protected**
- **Compatible with 8085, 6800 and many other μPs**

APPLICATIONS

- **Precision 8-bit D/A converters**
- **A/D converters**
- **Programmable power supplies**
- **Test equipment**
- **Measuring instruments**
- **Analog – digital multiplication**

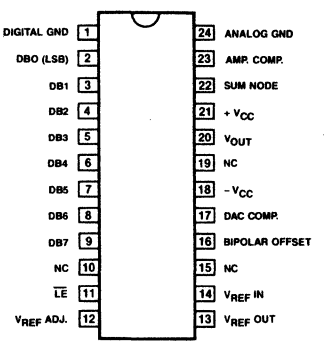
PIN CONFIGURATIONS

F, N Package



CD09820S

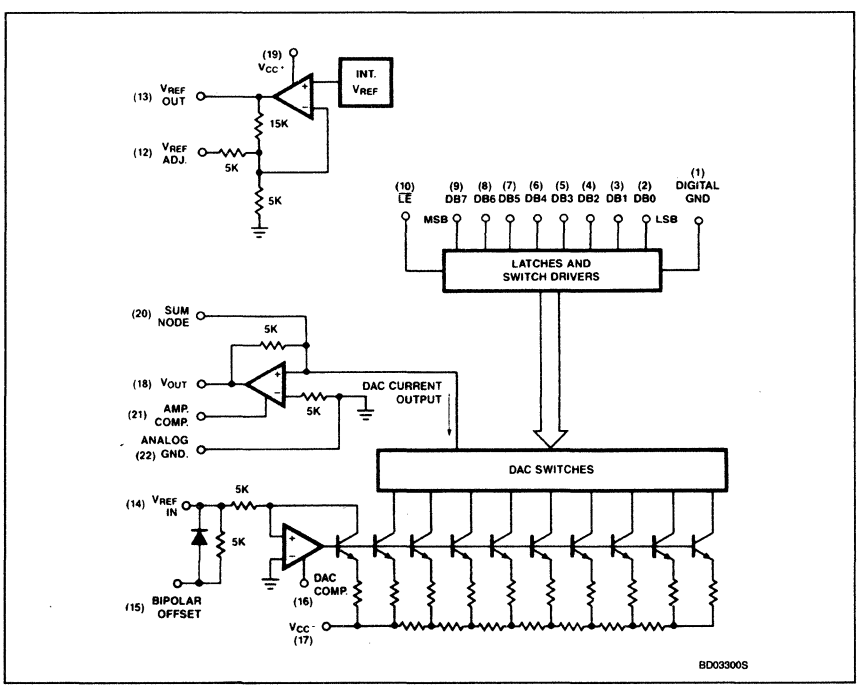
D Package [2]



CD09830S

NOTES:
1. SOL-released in large SO package only.
2. SOL and non-standard pinout.
3. SO and non-standard pinouts.

BLOCK DIAGRAM



BD03300S

Signetics

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PNA7518
8-Bit Multiplying DAC

Product Specification

Linear Products

DESCRIPTION

The PNA7518 is an NMOS 8-bit multiplying digital-to-analog converter (DAC) designed for video applications. The device converts a digital input signal into a voltage-equivalent analog output at a sampling rate of 30MHz.

The input signal is latched, then fed to a decoder which switches a transfer gate array (1 out of 256) to select the appropriate analog signal from a resistor chain. Two external reference voltages supply the resistor chain.

The input latches are positive edge-triggered. The output impedance is approximately 0.5kΩ depending on the applied digital code. An additional operational amplifier is required for the full bandwidth. Two's complement is selected when STC (Pin 11) is HIGH or is not connected.

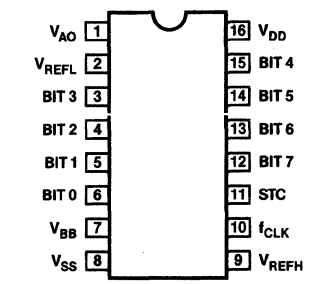
FEATURES

- **TTL input levels**
- **Positive edge-triggered**
- **Analog voltage output at 30MHz sampling rate**
- **Binary or two's complement input**
- **Output voltage accuracy to within ± ½ of the input**

APPLICATIONS

- **Video data conversion**
- **CRT displays**
- **Waveform/test signal generation**
- **Color/black-and-white graphics**

PIN CONFIGURATION



TOP VIEW

CD10200S

1	V_{AO}	analog output voltage
2	V_{refL}	reference voltage LOW
3	bit 3	digital voltage inputs (V_I)
4	bit 2	
5	bit 1	
6	bit 0	least-significant bit (LSB)
7	V_{BB}	back bias
8	V_{SS}	ground
9	V_{refH}	reference voltage HIGH
10	f_{CLK}	clock input
11	STC	select two's complement
12	bit 7	most-significant bit (MSB)
13	bit 6	
14	bit 5	digital voltage inputs (V_I)
15	bit 4	
16	V_{DD}	positive supply voltage

ORDERING CODE

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-pin Plastic DIP	0°C to +70°C	PNA7518N

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TDA5702
8-Bit Digital-To-Analog Converter

Preliminary Specification

Linear Products

DESCRIPTION

The TDA5702 is an 8-bit digital to analog converter (DAC) designed for video and professional applications. The TDA5702 converts the 8-bit binary-coded digital words into an analog output signal at a sampling rate of 25MHz. The design of the TDA5702 has eliminated the need for an operational amplifier, buffer and deglitching circuit at the analog output.

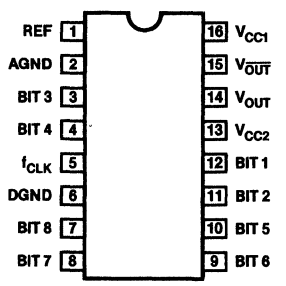
FEATURES

- **8-bit accuracy**
- **Internal input register**
- **TTL compatible digital signals**
- **Two voltage supply connections:**
  analog +5V
  digital +5V
- **Two complementary outputs (V_{OUT}, $V_{\overline{OUT}}$)**
- **No deglitching circuit required**
- **Low power consumption; typically 300 mW**
- **16-lead plastic DIP**

APPLICATIONS

- **Video data conversion**
- **Color/black-and-white graphics**
- **Waveform/test signal generation**
- **Waveform/test signal generation**

PIN CONFIGURATION



TOP VIEW

CD10840S

PIN NO.	SYMBOL	DESCRIPTION
1	REF	current reference loop decoupling
2	AGND	analog ground
3	Bit 3	
4	Bit 4	
5	f_{CLK}	25MHz clock input
6	DGND	digital ground
7	Bit 8	most significant bit (MSB)
8	Bit 7	
9	Bit 6	
10	Bit 5	
11	Bit 2	
12	Bit 1	least significant bit (LSB)
13	V_{P2}	digital supply voltage
14	V_{OUT}	analog voltage output
15	$V_{\overline{OUT}}$	complementary analog voltage output
16	V_{P1}	analog supply voltage

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic DIP	0 to +70°C	TDA5702N

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
	Supply voltages		
V_{P2}	at Pin 13	8	V
V_{P1}	at Pin 16	8	V
	Input voltage		
	at Pins 3, 4, 5, 7		
V_{IN}	8, 9, 10, 11 and 12	8	V
T_{STG}	Storage temperature range	−55 to +150	°C
T_J	Junction temperature	+125	°C
T_A	Operating temperature range	0 to +70	°C

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TDA5703
Analog To Digital Converter

Preliminary Specification

Linear Products

DESCRIPTION

The TDA5703 is an 8-bit analog to digital converter (ADC) designed for video and professional applications. The TDA5703 converts the analog input signal into 8-bit binary coded digital words at a sampling rate of up to 25MHz.

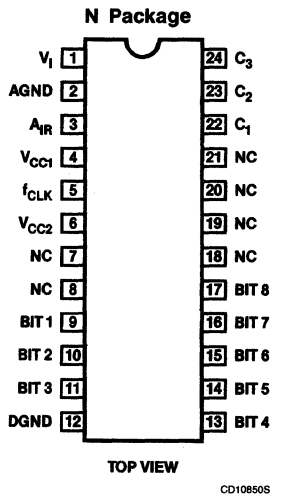
FEATURES

- **8-bit binary coded resolution**
- **Digitizing rates up to 25MHz**
- **Internal reference**
- **Only 3 external capacitors required**
- **Two voltage supply connections: analog +5V digital +5V**
- **1V full-scale analog input (75 Ω external resistor tied to V_{P1})**
- **Full-scale bandwidth; 10.5 MHz at 3 dB**
- **Low power consumption; typically 250 mW**
- **24-lead plastic DIP**

APPLICATIONS

- **Video data conversion**

PIN CONFIGURATION



PIN NO.	SYMBOL	DESCRIPTION
1	V_I	Analog voltage input
2	A GND	Analog ground
3	A_{IR}	Analog input reference
4	V_{P1}	Analog supply voltage
5	f_{CLK}	Clock input
6	V_{P2}	Digital supply voltage
7	NC	Not connected
8	NC	Not connected
9	Bit 1	Least significant bit (LSB)
10	Bit 2	
11	Bit 3	
12	D GND	Digital ground
13	Bit 4	
14	Bit 5	
15	Bit 6	
16	Bit 7	
17	Bit 8	Most significant bit (MSB)
18	NC	Not connected
19	NC	Not connected
20	NC	Not connected
21	NC	Not connected
22	C_1	
23	C_2	Decoupling for internal reference
24	C_3	

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PNA7509
7-Bit Analog-to-Digital Converter

Preliminary Specification

Linear Products

DESCRIPTION

The PNA7509 is a monolithic NMOS 7-bit analog-to-digital converter designed for video applications. The device converts the analog input signal into 7-bit binary coded digital words at a sampling rate of 22MHz.

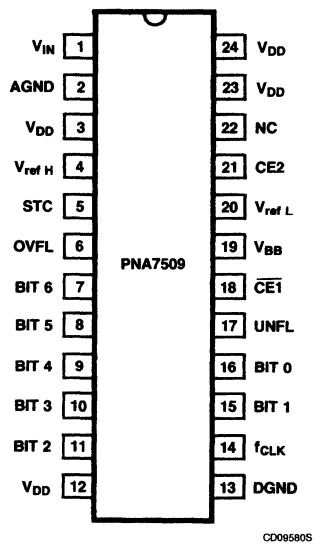
The circuit comprises 129 comparators, a reference resistor chain, combining logic, transcoder stages, and TTL output buffers which are positive edge-triggered and can be switched into 3-state mode. The digital output is selectable in two's complement or binary coding.

The use of separate outputs for overflow and underflow detection facilitates full-scale driving.

FEATURES

- **7-bit resolution**
- **22MHz clock frequency**
- **No external sample and hold required**
- **High input impedance**
- **Binary or two's complement 3-state TTL outputs**
- **Overflow and underflow 3-state TTL outputs**
- **Low reference current (250μA typ.)**
- **Positive supply voltages (+5V, +10V)**
- **Low power consumption (400mW typ.)**
- **Available in SO Package**

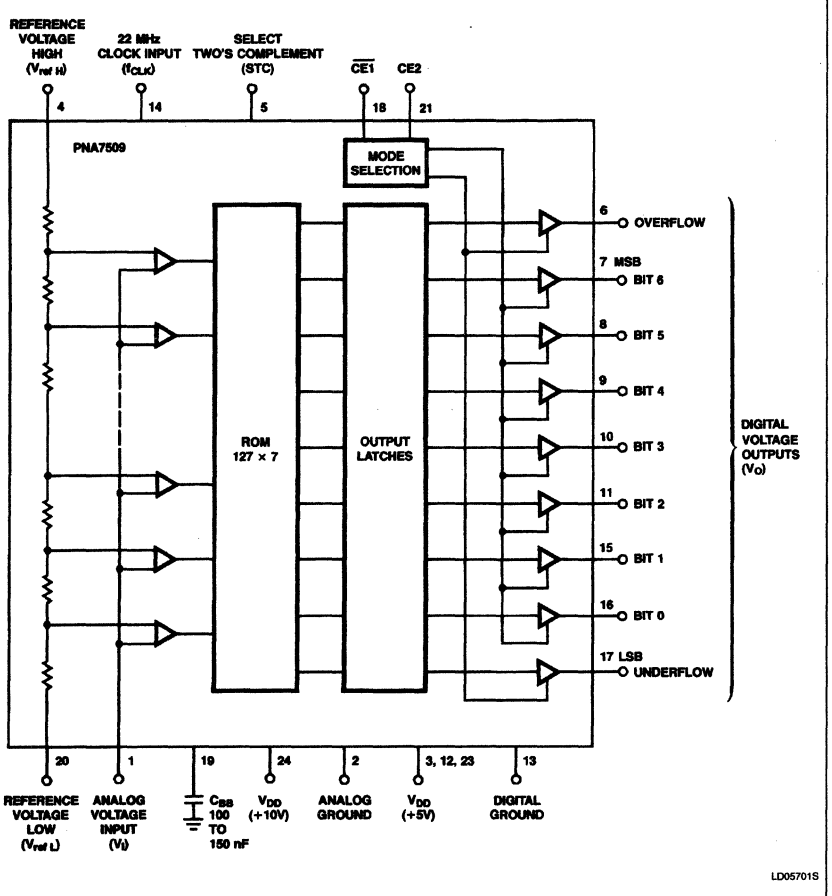
PIN CONFIGURATION



CD09580S

PIN NO.	SYMBOL	DESCRIPTION
1	V_{IN}	analog voltage input
2	AGND	analog ground
3	V_{DD}	positive supply voltage (+5V)
4	V_{refH}	reference voltage HIGH
5	STC	select two's complement
6	OVFL	overflow
7	bit 6	most-significant bit (MSB)
8	bit 5	
9	bit 4	
10	bit 3	
11	bit 2	
12	V_{DD}	positive supply voltage (+5V)
13	DGND	digital ground
14	f_{CLK}	22MHz clock input
15	bit 1	
16	bit 0	least-significant bit (LSB)
17	UNFL	underflow
18	$\overline{CE1}$	chip enable input 1
19	V_{BB}	back bias output
20	V_{refL}	reference voltage LOW
21	CE2	chip enable input 2
22	n.c.	not connected
23	V_{DD}	positive supply voltage (+5V)
24	V_{DD}	positive supply voltage (+10V)

BLOCK DIAGRAM



LD05701S

APPLICATIONS

- **High-speed A/D conversion**
- **Video signal digitizing**
- **Radar pulse analysis**
- **High energy physics research**
- **Transient signal analysis**

Signetics

Signetics

SE/NE521
High-Speed Dual Differential Comparator/Sense AMP

Preliminary Specification

Linear Products

FEATURES

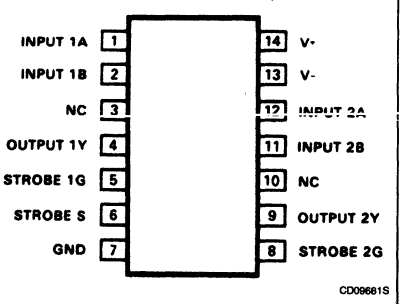
- 12ns max. guaranteed propagation delay
- 20μA max. input bias current
- TTL compatible strobes and outputs
- Large common-mode input voltage range
- Operates from standard supply voltages
- Military qualifications pending

APPLICATIONS

- MOS memory sense amp
- A-to-D conversion
- High-speed line receiver

PIN CONFIGURATION

D, F, N Packages

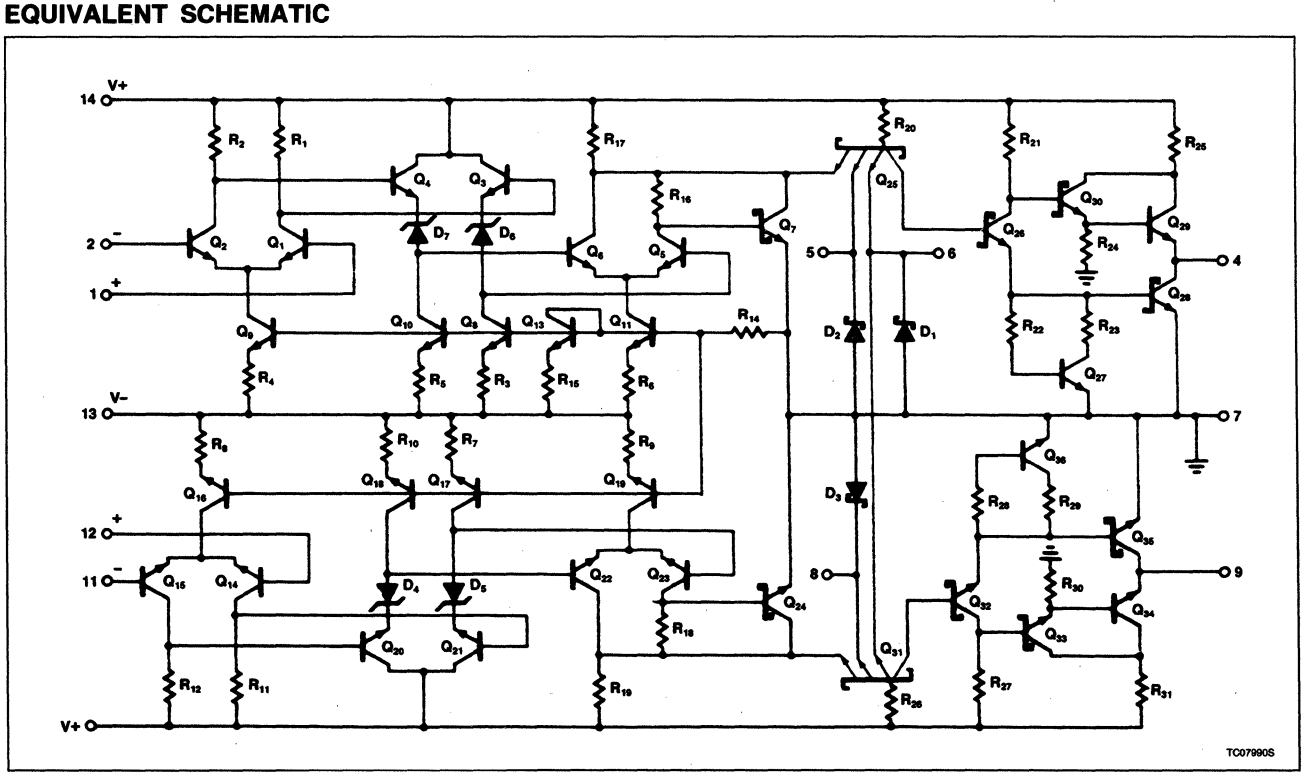


TOP VIEW

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
14-pin Plastic DIP		NE521N
14-pin SO DIP		NE521D
14-pin Cerdip		NE521F
14-pin Cerdip		SE521F

EQUIVALENT SCHEMATIC



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Signetics

SE/NE522
High-Speed Dual Differential Comparator/Sense Amp

Linear Products

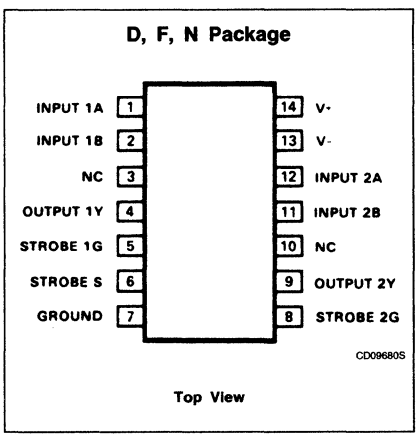
FEATURES

- **15ns maximum guaranteed propagation delay**
- **20μA maximum input bias current**
- **Open collector output for wire-ORed applications**
- **Open collector output for wire-ORed applications**
- **Large common-mode input voltage range**
- **Operates from standard supply voltages**

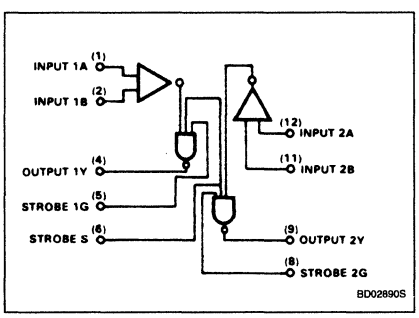
APPLICATIONS

- **MOS memory sense amp**
- **A-to-D conversion**
- **High-speed line receiver**

PIN CONFIGURATION



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
	Supply voltage		V
V+	Positive	+7	
V–	Negative	–7	
V_{IDR}	Differential input voltage	±6	V
V_{IN}	Input voltage		V
	Common-mode	±5	
	Strobe/gate	+5.25	
P_D	Power dissipation	600	mW
T_A	Operating temperature range NE522	0 to 70	°C
	SE522	–55 to +125	
T_{STG}	Storage temperature range	–65 to +150	°C
T_{SOLD}	Lead temperature (solder, 60 sec)	+300	°C

Signetics

Signetics

SE/NE527
Voltage Comparator

Product Specification

Linear Products

DESCRIPTION

The SE/NE527 is a high-speed analog voltage comparator which, in the first time, mates state-of-the-art Schottky diode technology with the conventional linear process. This allows simultaneous fabrication of high speed TTL gates with a precision linear amplifier on a single monolithic chip. The SE/NE527 is similar in design to the Signetics SE/NE529 voltage comparator except that it incorporates an "Emitter-Follower" input stage for extremely low input currents. This opens the door to a whole new range of applications for analog voltage comparators.

FEATURES

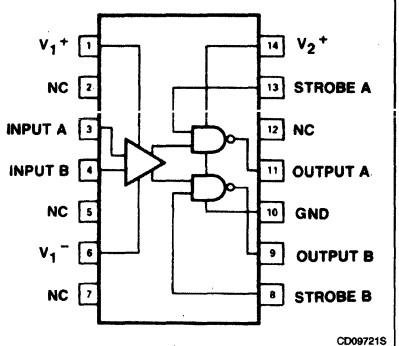
- **15ns propagation delay**
- **Complementary output gates**
- **TTL or ECL compatible outputs**
- **Wide common-mode and differential voltage range**
- **MIL-STD 883A, B, C available**
- **Typical gain of 5000**

APPLICATIONS

- **A/D conversion**
- **ECL-to-TTL interface**
- **TTL-to-ECL interface**
- **Memory sensing**
- **Optical data coupling**

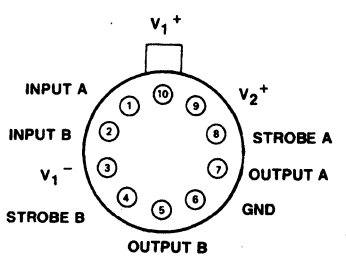
PIN CONFIGURATIONS

D, F, N Packages



CD09721S

H Package*



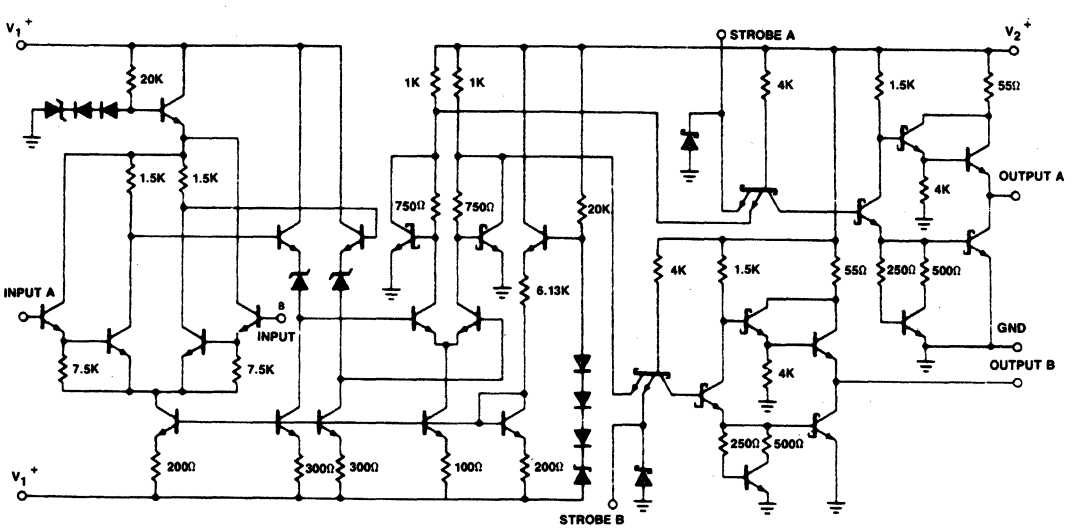
CD09730S

NOTE:
*Metal cans (H) not recommended for new designs.

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
14-pin Plastic DIP		NE527N
14-pin Cerdip		NE527F
14-pin SO DIP		NE527D
14-pin Cerdip		SE527F
10-lead metal can		NE527H
10-lead metal can		SE527H

EQUIVALENT SCHEMATIC



TC08001S

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SE/NE529
Voltage Comparator

Product Specification

Linear Products

DESCRIPTION

The SE/NE529 is a high-speed analog voltage comparator which, for the first time, mates state-of-the-art Schottky diode technology with the conventional linear process. This allows simultaneous fabrication of high speed TTL gates with a precision linear amplifier on a single monolithic chip.

FEATURES

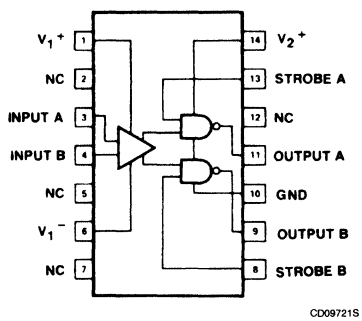
- **10ns propagation delay**
- **Complementary output gates**
- **TTL or ECL compatible outputs**
- **Wide common-mode and differential voltage range**
- **Typical gain 5000**

APPLICATIONS

- **A/D conversion**
- **ECL-to-TTL interface**
- **TTL-to-ECL interface**
- **Memory sensing**
- **Optical data coupling**
- **MIL-STD-883A, B, C available**

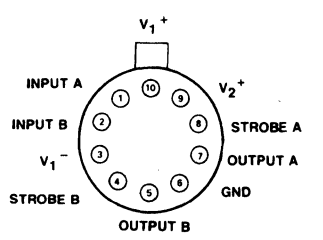
PIN CONFIGURATIONS

D, F, N Packages



TOP VIEW

H Package*

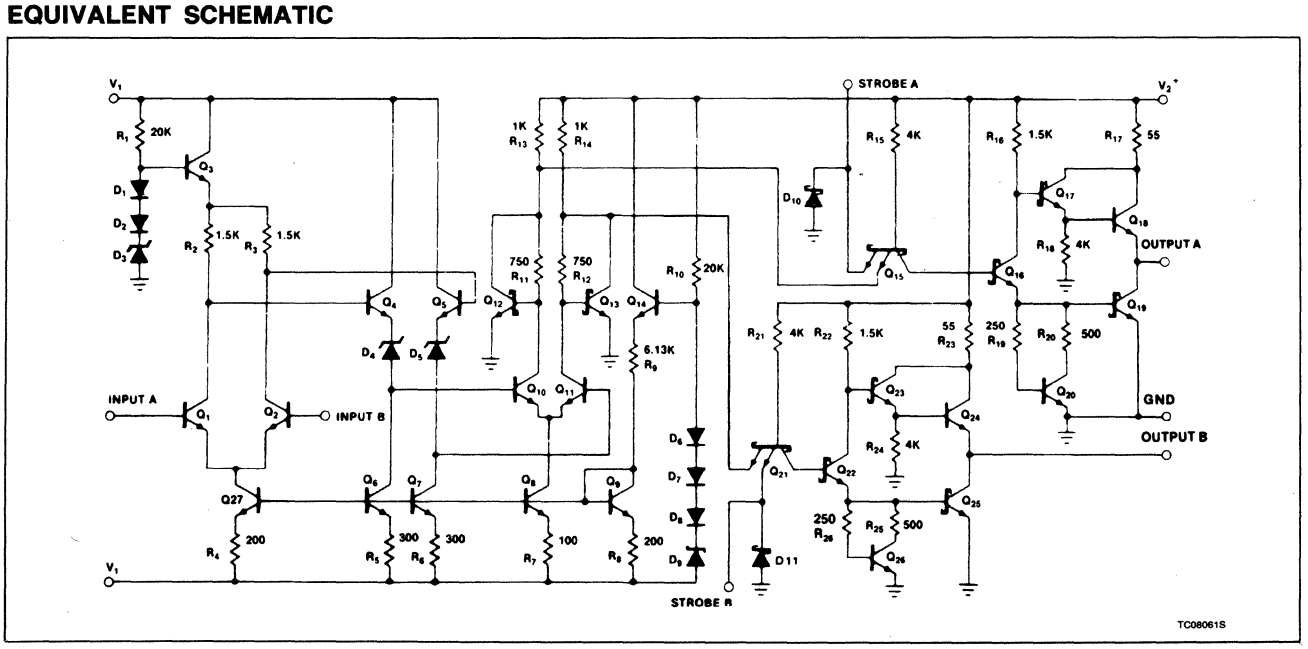


NOTE:
*Metal cans (H) not recommended for new designs.

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
14-pin plastic DIP		NE529N
14-pin Cerdip		NE529F
14-pin Cerdip		SE529F
14-pin SO DIP		NE529D
10-lead metal can		NE529H
10-lead metal can		SE529H

EQUIVALENT SCHEMATIC



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SE/NE5521 LVDT Signal Conditioner

Advance Information

Linear Products

DESCRIPTION

The SE/NE5521 is a signal conditioning circuit for use with Linear Variable Differential Transformers (LDVTs) and Rotary Variable Differential Transformers (RVDTs). The chip includes a low distortion, amplitude-stable sine wave oscillator with programmable frequency to drive the primary of the LVDT/RVDT, a synchronous demodulator to convert the LVDT/RVDT output amplitude and phase to position information, and an output amplifier to provide amplification and filtering of the demodulated signal.

FEATURES

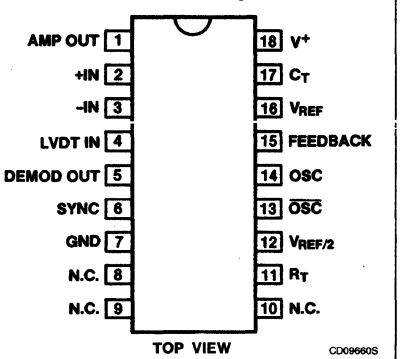
- **Low distortion**
- **Single supply 5V to 20V, or dual supply ±2.5V to ±10V**
- **Oscillator frequency 1kHz to 20kHz**
- **Capable of ratiometric operation**
- **Low power consumption (177mV typ)**

APPLICATIONS

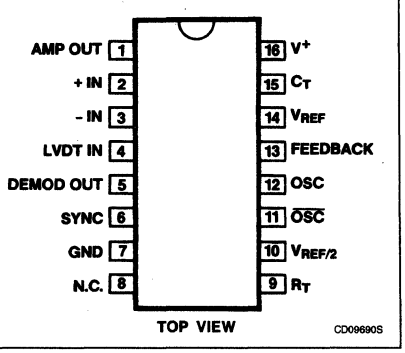
- **LVDT signal conditioning**
- **RVDT signal conditioning**
- **LPDT signal conditioning**
- **Bridge circuits**

PIN CONFIGURATIONS

F, N Package



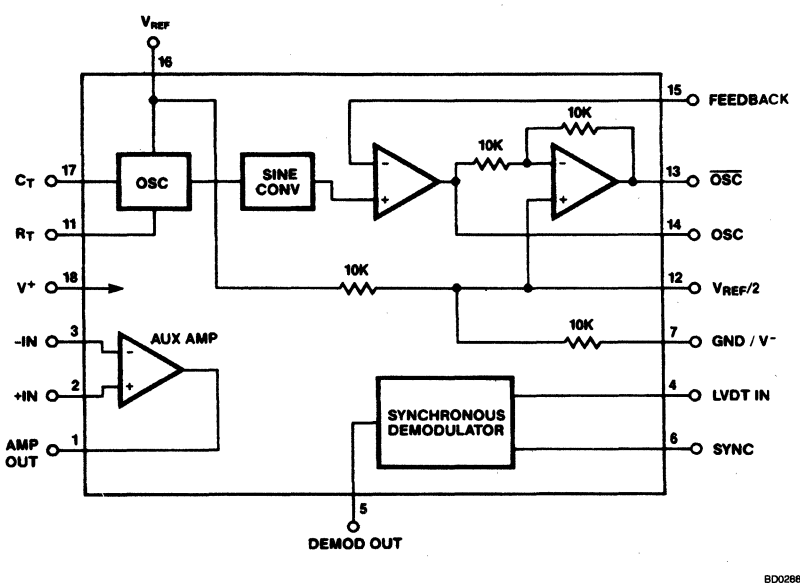
D Package



ORDERING CODE

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
18-Pin Plastic DIP		NE5521N
18-Pin Cerdip		NE5521F
18-Pin SO DIP		NE5521D
18-Pin Plastic DIP		SA5521N
18-Pin Cerdip		SE5521F

BLOCK DIAGRAM



NOTE:
Pin numbers are for F, N packages.

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PCF8576
Universal LCD Driver for Low Multiplex Rates

Linear Products

Preliminary Specification

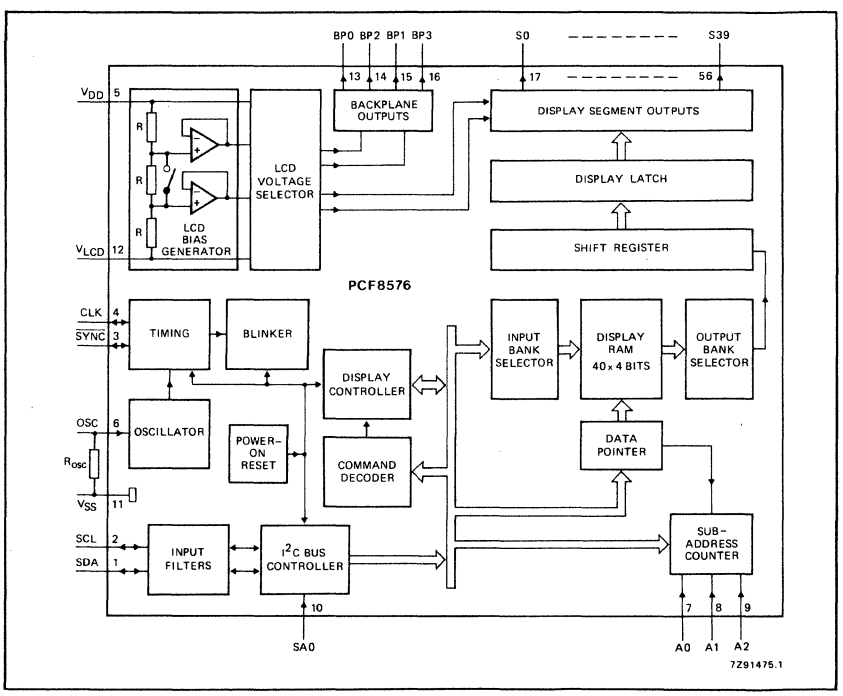
DESCRIPTION

The PCF8576 is a peripheral device which interfaces to almost any liquid crystal display (LCD) having low multiplex rates. It generates the drive signals for any static or multiplexed LCD containing up to four backplanes and up to 40 segments and can easily be cascaded for larger LCD applications. The PCF8576 is compatible with most microprocessors and communicates via a two-line bidirectional bus (I^2C). Communication overheads are minimized by a display RAM with auto-incremented addressing, by hardware subaddressing and by display memory switching (static and duplex drive modes).

FEATURES

- **Single-chip LCD controller/driver**
- **Selectable backplane drive configuration: static or 2/3/4 backplane multiplexing**
- **Selectable display bias configuration: static, 1/2 or 1/3**
- **40 segment drives: up to twenty 8-segment numeric characters; up to ten 15-segment alphanumeric characters; or any graphics of up to 160 elements**
- **40 x 4-bit RAM for display data storage**
- **Auto-incremented display data loading across device subaddress boundaries**
- **display memory bank switching in static and duplex drive modes**
- **Versatile blinking modes**
- **LCD and logic supplies may be separated**
- **Wide power supply range: from 2V for low-threshold LCDs and up to 9V for guest-host LCDs and high-threshold (automobile) twisted nematic LCDs**
- **Low power consumption**
- **Power-saving mode for extremely low power consumption in battery-operated and telephone applications**
- **I^2C bus interface**
- **TTL/CMOS compatible**
- **Compatible with any 4-bit, 8-bit or 16-bit microprocessors**
- **May be cascaded for large LCD applications (up to 2560 segments possible)**
- **Optimized pinning for single plane wiring in both single and multiple PCF8576 applications**
- **Space-saving 56-lead plastic mini-pack (VSO-56)**
- **Very low external component count (at most one resistor, even in multiple device applications)**
- **Compatible with Philips/Videlec chip-on-glass technology**
- **Manufactured in silicon gate CMOS process**

BLOCK DIAGRAM



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TEA1017
13-Bit Series – Parallel Converter

Product Specification

Linear Products

DESCRIPTION

The TEA1017 is a bipolar integrated circuit intended to drive displays, triacs and relays and small stepper motors. The data is serially shifted into the device and is stored in 13 latches that drive the outputs.

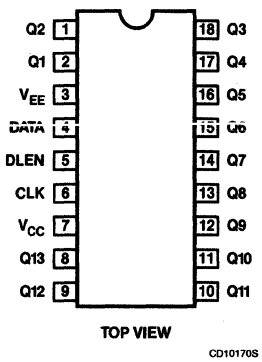
FEATURES

- **TTL and CMOS compatible inputs**
- **Outputs drive load in both directions**
- **Power-on reset makes outputs floating**
- **Wide supply voltage range**

APPLICATIONS

- **Driving Stepper Motors**
- **Driving Triacs**
- **Used as a Simple Switch**
- **Driving Mosaic Printhead**
- **Electronic Appliances; i.e. Washing Machines**
- **Electronic Equipment; i.e. Typewriters**
- **Relays**
- **Automotive Industry**

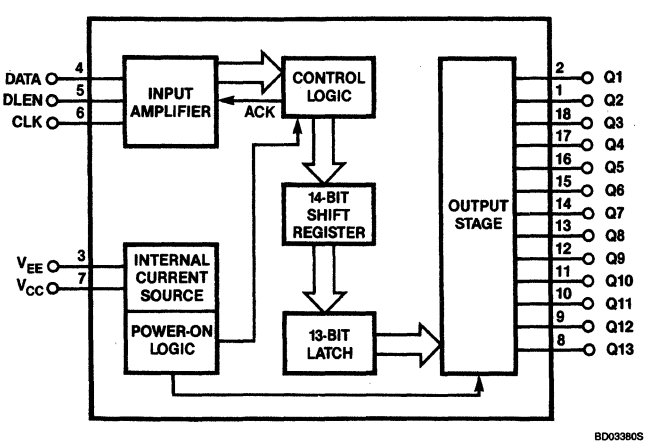
PIN CONFIGURATION



ORDERING CODE

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
18-Pin Plastic DIP	−20°C to +80°C	TEA1017N

BLOCK DIAGRAM



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SE/NE5560
Switched-Mode Power Supply Control Circuit

Product Specification

Linear Products

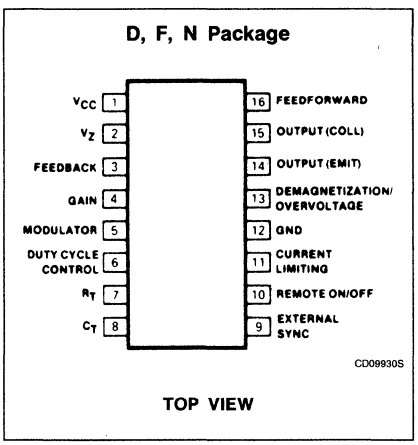
DESCRIPTION

The SE/NE5560 is a control circuit for use in switched-mode power supplies. This single monolithic chip incorporates all the control and housekeeping (protection) functions required in switched-mode power supplies, including an internal temperature-compensated reference source, internal Zener references, sawtooth generator, pulse-width modulator, output stage and various protection circuits.

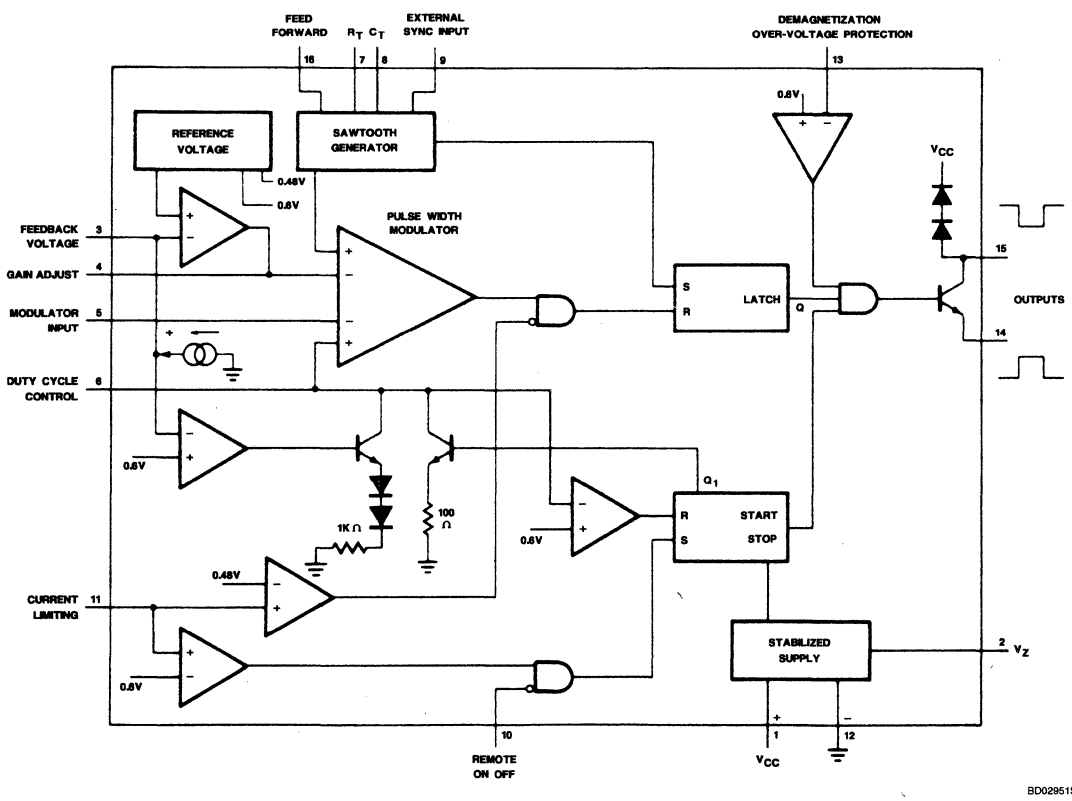
FEATURES

- **Stabilized power supply**
- **Temperature-compensated reference source**
- **Sawtooth generator**
- **Pulse-width modulator**
- **Remote on/off switching**
- **Current limiting**
- **Low supply voltage protection**
- **Loop fault protection**
- **Demagnetization/overvoltage protection**
- **Maximum duty cycle clamp**
- **Feed-forward control**
- **External synchronization**

PIN CONFIGURATION



BLOCK DIAGRAM



NOTE:
1. See Voltage/Current fed supply characteristic curve.

Signetics

Signetics

SE/NE5561
Switched-Mode Power Supply Control Circuit

Product Specification

Linear Products

DESCRIPTION

The NE5561/SE5561 is a control circuit for use in switched-mode power supplies. It contains an internal temperature-compensated supply, PWM, sawtooth oscillator, overcurrent sense latch, and output stage. The device is intended for low cost SMPS applications where extensive housekeeping functions are not required.

FEATURES

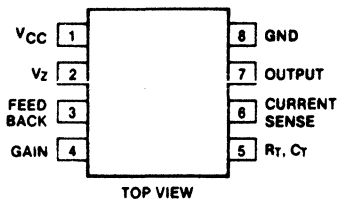
- **Micro-miniature (D) package**
- **Pulse-width modulator**
- **Current limiting (cycle-by-cycle)**
- **Sawtooth generator**
- **Stabilized power supply**
- **Double pulse protection**
- **Internal temperature-compensated reference**

APPLICATIONS

- **Switched-mode power supplies**
- **D/C motor controller inverter**
- **DC/DC converter**

PIN CONFIGURATION

D, FE, N Packages



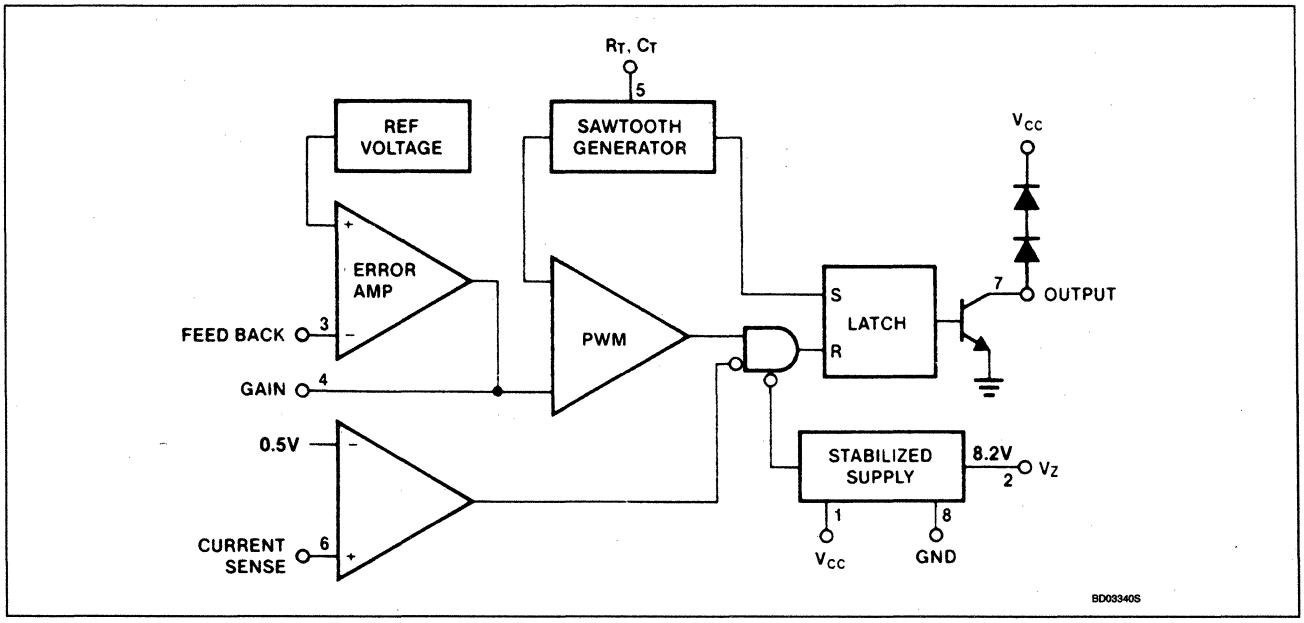
TOP VIEW

CD10190S

ORDERING CODE

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-pin Plastic DIP		NE5561N
8-pin Plastic DIP		SE5561N
8-pin Cerdip		NE5561FE
8-pin Cerdip		SE5561FE
8-pin SO DIP		NE5561D

BLOCK DIAGRAM



BD03340S

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SE/NE5562
Switched-Mode Power Supply Control Circuit

Preliminary Specification

Linear Products

DESCRIPTION

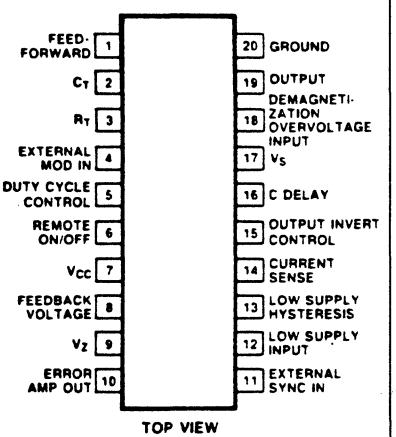
The SE/NE5562 is a single-output control circuit for Switched-Mode Power Supplies. This single monolithic IC contains all control and protection features needed for full-featured Switched-Mode Power Supplies.

FEATURES

- **Stabilized power supply**
- **Temperature-compensated reference source**
- **Sawtooth generator**
- **Pulse-width modulator**
- **Remote on/off switching**
- **Current limiting (2 levels)**
- **Low supply voltage, with adjustable hysteresis**
- **Loop fault protection**
- **Demagnetization/overvoltage protection**
- **Duty cycle adjust and clamp**
- **Feed-forward control**
- **External synchronization**
- **Total shutdown after adjustable number of overcurrent faults**

PIN CONFIGURATION

D, F, N Packages



TOP VIEW

ORDERING CODE

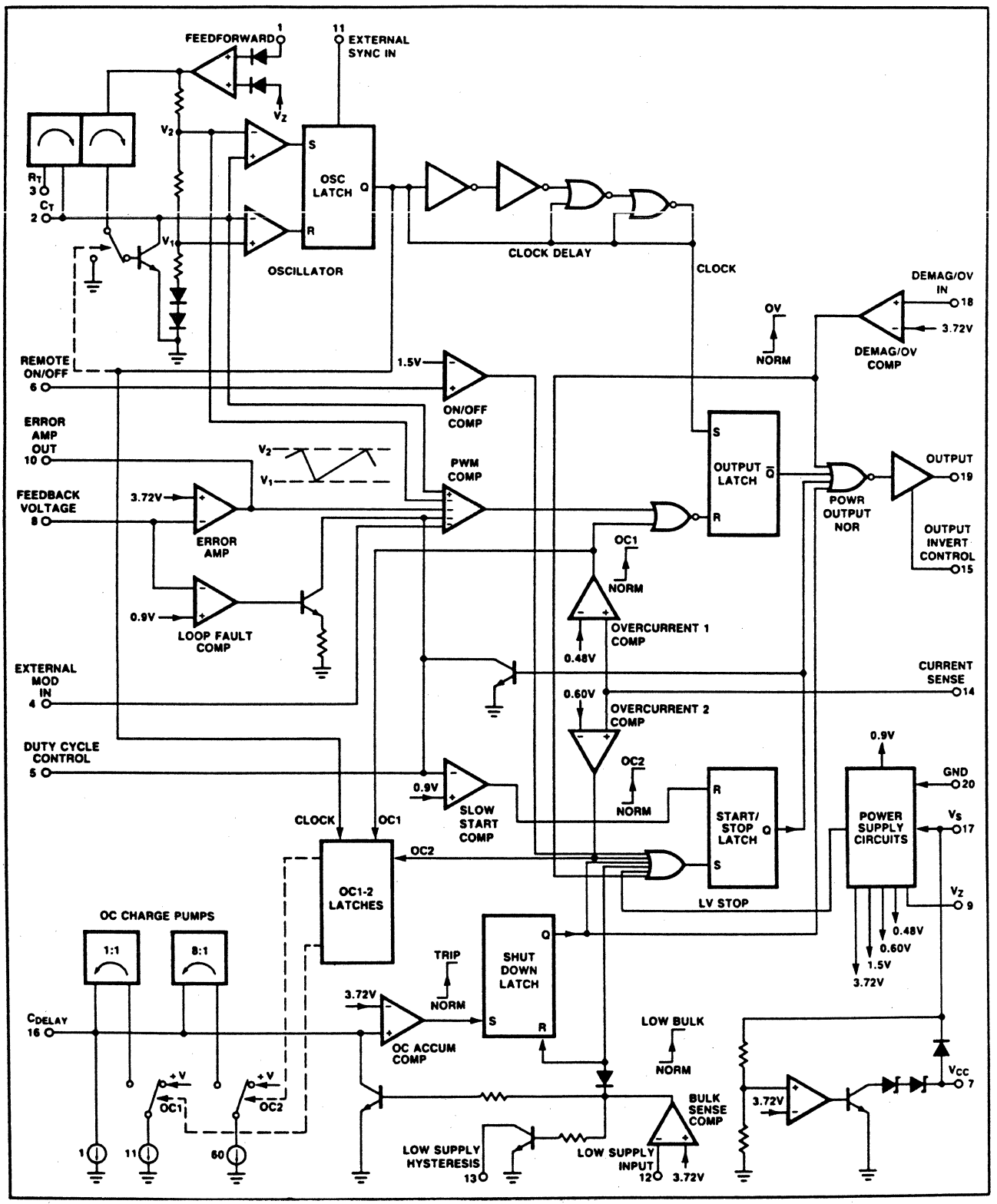
DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
20-pin Plastic DIP		NE5562N
20-pin Plastic DIP		SE5562N
20-pin Cerdip		NE5562F
20-pin Cerdip		SE5562F
20-pin SOL DIP		NE5562D

Signetics

Switched-Mode Power Supply Control Circuit

SE/NE5562

BLOCK DIAGRAM



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NE5568
Switched-Mode Power Supply Controller

Product Specification

Linear Products

DESCRIPTION

The NE5568 is a control circuit for use in switched mode power supplies. It contains an internal temperature-compensated supply, PWM, sawtooth oscillator, over-current sense latch, and output stage. The device is intended for low-cost SMPS applications where extensive housekeeping functions are not required. The NE5568 is a selected version of the NE5561.

FEATURES

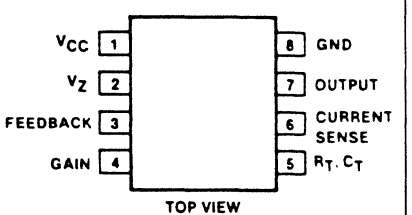
- **Micro-miniature (D) package**
- **Pulse width modulator**
- **Current limiting (cycle by cycle)**
- **Sawtooth generator**
- **Stabilized power supply**
- **Double pulse protection**
- **Internal temperature-compensated reference**

APPLICATIONS

- **Switch mode power supplies**
- **DC motor controller inverter**
- **DC/DC converter**

PIN CONFIGURATION

D, FE, N Packages

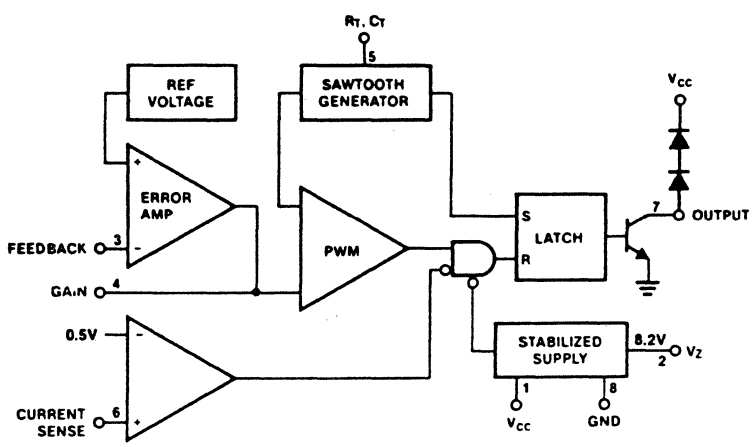


TOP VIEW

ORDERING CODE

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-pin Plastic DIP		NE5568N
8-pin Cerdip		NE5568FE
8-pin SO DIP		NE5568D

BLOCK DIAGRAM



Signetics

Signetics

TEA1039
Control Circuit For Switched-Mode Power Supply

Product Specification

Linear Products

DESCRIPTION

The TEA1039 is a bipolar integrated circuit intended for the control of a switched-mode power supply. Together with an external error amplifier and a voltage regulator (e.g., a regulator diode) it forms a complete control system. The circuit is capable of directly driving the SMPS power transistor in small SMPS systems.

FEATURES

- **Wide frequency range**
- **Adjustable input sensitivity**
- **Adjustable minimum frequency or maximum duty factor limit**
- **Adjustable overcurrent protection limit**
- **Supply voltage out-of-range protection**
- **Slow-start facility**

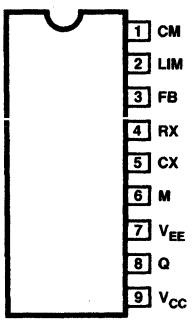
APPLICATIONS

- **Home appliances**
- **Frequency regulation**
- **Flyback converters**
- **Forward converters**

ORDERING CODE

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
9-pin Plastic SIP Power Package	−25°C to +125°C	TEA1039U

PIN CONFIGURATION



TOP VIEW

CD10370S

PINNING

1	CM	overcurrent protection input
2	LIM	limit setting input
3	FB	feedback input
4	RX	external resistor connection
5	CX	external capacitor connection
6	M	mode input
7	V_{EE}	common
8	Q	output
9	V_{CC}	positive supply connection

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TDA2595
Horizontal Combination

Linear Products

DESCRIPTION

The TDA2595 is a monolithic integrated circuit intended for use in color television receivers.

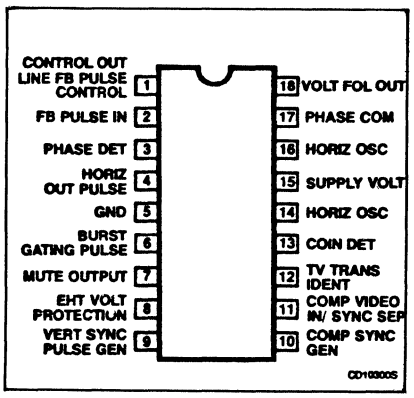
FEATURES

- Positive video input; capacitively coupled (source impedance < 200Ω)
- Adaptive sync separator; slicing level at 50% of sync amplitude
- Internal vertical pulse separator with double slope integrator
- Output stage for vertical sync pulse or composite sync depending on the load; both are switched off at muting
- φ_1 phase control between horizontal sync and oscillator
- Coincidence detector φ_3 for automatic time constant switching; overruled by the VCR switch
- Time constant switch between two external time constants for loop gain; both controlled by the coincidence detector φ_3
- φ_1 gating pulse controlled by coincidence detector φ_3
- Mute circuit depending on TV transmitter identification
- φ_2 phase control between line flyback and oscillator; the slicing levels for φ_2 control and horizontal blanking can be set separately
- Burst keying and horizontal blanking pulse generation, in combination with clamping of the vertical blanking pulse (three-level sandcastle)
- Horizontal drive output with constant duty cycle inhibited by the protection circuit or the supply voltage sensor
- Detector for too low supply voltage
- Protection circuit for switching off the horizontal drive output continuously if the input voltage is below 4V or higher than 8V
- Line flyback control causing the horizontal blanking level at the sandcastle output continuously in case of a missing flyback pulse
- Spot suppressor controlled by the line flyback control

APPLICATIONS

- Television receivers
- Video receivers

PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
18-Pin Plastic DIP SOT102CS	−20 to +70°C	TDA2595N

TDA2653A
Vertical Deflection

Product Specification

Linear Products

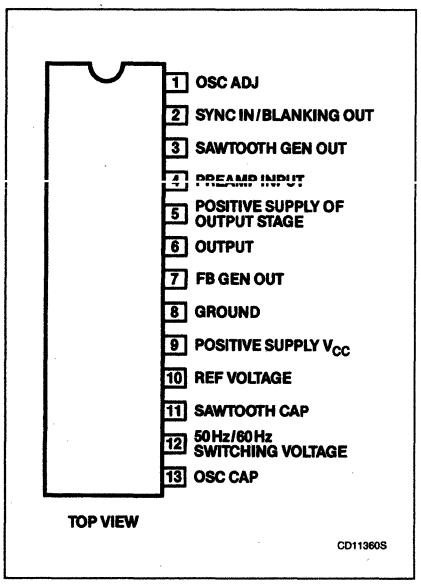
DESCRIPTION

The TDA2653A is a monolithic integrated circuit for vertical deflection in video monitors and large screen color television receivers, e.g. 30AX and PIL-S4 systems.

FEATURES

- **Oscillator; switch capability for 50Hz/60Hz operation**
- **Synchronization circuit**
- **Blanking pulse generator with guard circuit**
- **Sawtooth generator with buffer stage**
- **Preamplifier with fed-out inputs**
- **Output stage with thermal and short-circuit protection**
- **Flyback generator**
- **Voltage stabilizer**

PIN CONFIGURATION



1, 13 Oscillator

The oscillator frequency is determined by a potentiometer at Pin 1 and a capacitor at Pin 13.

2 Sync input/blanking output

Combination of sync input and blanking output. The oscillator has to be synchronized by a positive-going pulse between 1V and 12V. The integrated frequency detector delivers a switching level at Pin 12.

The blanking pulse amplitude is 20V with a load of 1mA.

3 Sawtooth generator output

The sawtooth signal is fed via a buffer stage to Pin 3. It delivers the signal which is used for linearity control, and drive of the preamplifier. The sawtooth is applied via a shaping network to Pin 11 (linearity) and via a resistor to Pin 4 (preamplifier).

4 Preamplifier input

The DC voltage is proportional to the output voltage (DC feedback). The AC voltage is proportional to the sum of the buffered sawtooth voltage at Pin 3 and the voltage, with opposite polarity, at the feedback resistor (AC feedback).

5 Positive supply of output stage

This supply is obtained from the flyback generator. An electrolytic capacitor between Pins 7 and 5, and a diode between Pins 5 and 9 have to be connected for proper operation of the flyback generator.

6 Output of class-B power stage

The vertical deflection coil is connected to this pin, via a series connection of a coupling capacitor and a feedback resistor, to ground.

7 Flyback generator output

An electrolytic capacitor has to be connected between Pins 7 and 5 to complete the flyback generator.

8 Negative supply (ground)

Negative supply of output stage and small signal part.

9 Positive supply

The supply voltage at this pin is used to supply the flyback generator, voltage stabilizer, blanking pulse generator and buffer stage.

10 Reference voltage of preamplifier

External adjustment and decoupling of reference voltage of the preamplifier.

11 Sawtooth capacitor

This sawtooth capacitor has been split to realize linearity control.

12 50Hz/60Hz switching level

This pin delivers a LOW voltage level for 50Hz and a HIGH voltage level for 60Hz. The amplitudes of the sawtooth signals can be made equal for 50Hz and 60Hz with these levels.

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TDA2579
Synchronization Circuit

Product Specification

Linear Products

DESCRIPTION

The TDA2579 generates and synchronizes horizontal and vertical signals. The device has a 3-level sandcastle output, a transmitter identification signal and also 50/60Hz identification.

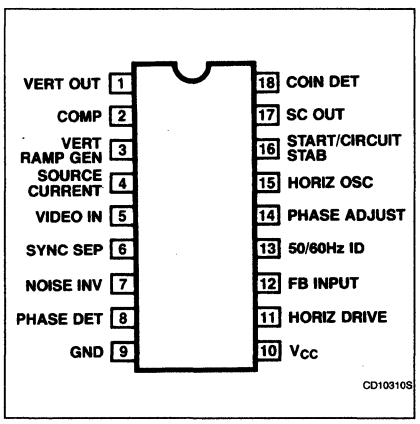
FEATURES

- **Horizontal phase detector, (sync to osc), sync separator and noise inverter**
- **Triple current source in the phase detector with automatic selection**
- **Inhibit of horizontal phase detector and video transmitter identification**
- **Second phase detector for storage compensation of the horizontal output stage**
- **Stabilized direct starting of the horizontal oscillator and output stage**
- **Horizontal output pulse with constant duty cycle value of 29μs**
- **Duty factor of the horizontal output pulse is 50% when horizontal flyback pulse is absent**
- **Internal vertical sync separator and two integration selection times**
- **Divider system with three different reset enable windows**
- **Synchronization is set to 628 divider ratio when no vertical sync pulses and no video transmitter is identified**
- **Vertical comparator with a low DC feedback signal**
- **50/60Hz identification output combined with mute function**
- **Automatic amplitude adjustment for 50 and 60Hz and blanking pulse duration**

APPLICATIONS

- **Video Terminals**
- **Television**
- **Video Tape Recorder**

PIN CONFIGURATION



ORDERING CODE

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-pin Plastic DIP	0°C to +70°C	TDA2579N

Signetics

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TDA3651A/AQ/3653
Vertical Deflection

Product Specification

Linear Products

DESCRIPTION

The TDA3651A/AQ is a vertical deflection output circuit for drive of various deflection systems with deflector currents up to 2A peak-to-peak.

FEATURES

- **Driver**
- **Output stage**
- **Thermal protection and output stage protection**
- **Flyback generator**
- **Voltage stabilizer**

APPLICATIONS

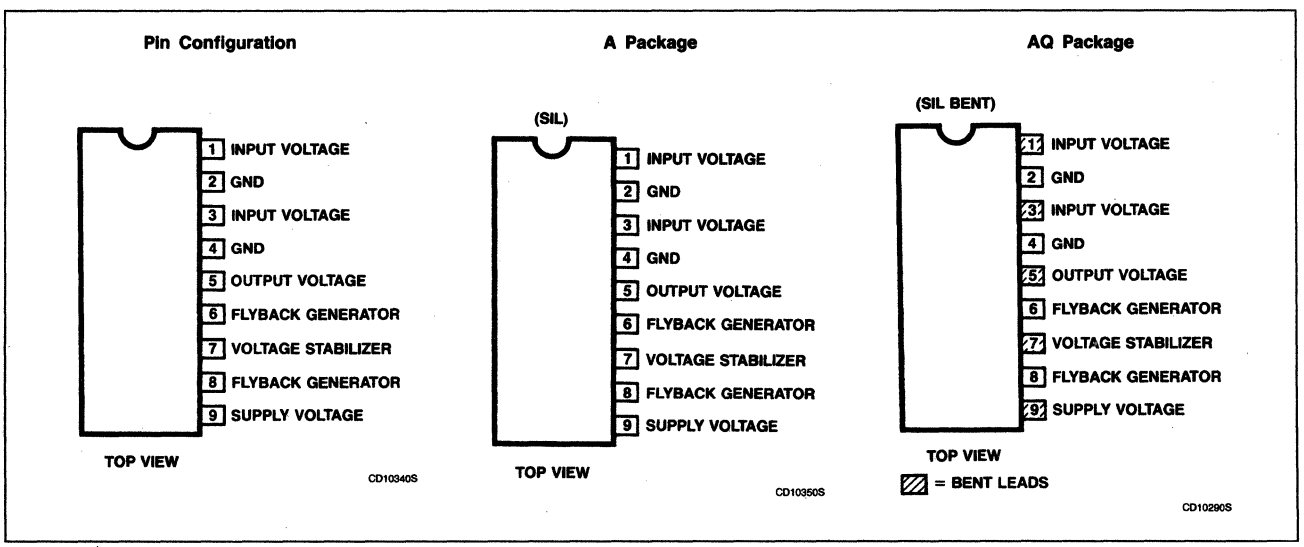
- **Video terminals**
- **Television**

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
9-Pin Plastic SIP	0 to 70°C	TDA3651A TDA3653A
9-Pin Plastic SIP BENT to DIP	0 to 70°C	TDA3651AQ TDA3653AQ

PIN CONFIGURATION

Signetics



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PCF8573
Clock/Calendar With Serial I/O

Product Specification

Linear Products

DESCRIPTION

The PCF8573 is a low threshold, monolithic CMOS circuit that functions as a real-time clock/calendar in the Inter IC (I^2C) bus-oriented microcomputer systems. The device includes an addressable time counter and an addressable alarm register, both for minutes, hours, days and months. Three special control/status flags, COMP, POWF and NODA, are also available. Information is transferred serially via a two-line bidirectional bus (I^2C). Back-up for the clock during supply interruptions is provided by a 1.2V nickel cadmium battery. The time base is generated from a 32.768kHz crystal-controlled oscillator.

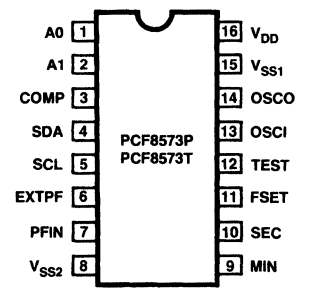
FEATURES

- **Serial input/output has (I^2C) interface for minutes, hours, days and months**
- **Additional pulse outputs for seconds and minutes**
- **Alarm register for presetting a time for alarm or remote switching functions**
- **Battery back-up for clock function during supply interruption**
- **Crystal oscillator control (32.768kHz)**

APPLICATIONS

- **Automotive**
- **Telephony**

PIN CONFIGURATION



TOP VIEW

CD10260S

PIN NO.	SYMBOL	DESCRIPTION
1	A0	Address input
2	A1	Address input
3	COMP	Comparator output
4	SDA	Serial data line (I^2C bus)
5	SCL	Serial clock line (I^2C bus)
6	EXTPF	Enable power fail flag input
7	PFIN	Power fail flag input
8	V_{SS2}	Negative supply 2 (I^2C interface)
9	MIN	One pulse per minute output
10	SEC	One pulse per second output
11	FSET	Oscillator tuning output
12	TEST	Test input; must be connected to V_{SS2} when not in use
13	OSCI	Oscillator input
14	OSCO	Oscillator input/output
15	V_{SS1}	Negative supply 1 (clock)
16	V_{DD}	Common positive supply

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-pin Plastic DIP	−40°C to +85°C	PCF8573PN
16-pin Plastic SO	−40°C to +85°C	PCF8573TD

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{DD}	Supply voltage range (clock)	−0.3 to 8	V
V_{SS2}	Supply voltage range (I^2C interface)	−0.3 to 8	V
I_{IN}	Input current	10	mA
I_{OUT}	Output current	10	mA
P_D	Total Power Dissipation per package	200	mW
T_A	Operating Ambient Temperature	−40 to 85	°C
T_{STG}	Storage Temperature	−55 to 125	°C

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SAF3019P
Clock/Timer

Product Specification

Linear Products

DESCRIPTION

The SAF3019 is a CMOS integrated circuit comprising a digital clock for minutes, hours, days and months, as well as an additional register for resetting. The time counter provides cycles of 28, 30 or 31 days automatically, depending on the length of the month.

The time reference is the 50 Hz mains frequency or a 32.768 Hz on-chip reference oscillator with an external crystal. If the 50 Hz mains frequency is interrupted, the circuit is automatically switched to crystal oscillator operation.

The circuit can be controlled by a microcomputer. The data transmission (e.g., TIME SET and TIME READ of the time counter and time register) is achieved via the CBUS. A microcomputer then controls the data processing and the display unit drive.

The circuit uses a 5V supply for data transmission. If the 5V supply is interrupted, the clock function is maintained by a 1.5V battery. The clock can then continue to function for an extended period, because the battery load current is only a few microamperes.

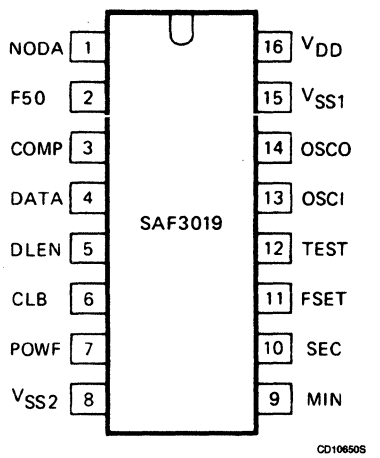
FEATURES

- **Serial bidirectional CBUS interface for input/output of minutes, hours, day and month**
- **Additional pulse outputs for seconds and minutes**
- **Time register for presetting a time for alarm or remote switching functions**
- **Battery back-up for clock function during supply interruption**
- **Controlled either by the 50Hz mains frequency or a crystal oscillator (automatic switch)**

APPLICATIONS

- **Clock displays**
- **Timers**
- **Appliances**
- **Control Systems**

PIN CONFIGURATION



PIN NO.	SYMBOL	DESCRIPTION
16	V_{DD}	common positive supply (5V; V_B = 1.5V)
15	V_{SS1}	negative battery supply (V_B)
8	V_{SS2}	ground (V_{DD})
4	DATA	data input/output
5	DLEN	data line enable input CBUS (bidirectional)
6	CLB	clock burst input
1	NODA	comparator mode select input
12	TEST	test mode input (normally ground)
2	F50	50Hz mains frequency input
13	OSCI	input and output of the on-chip oscillator
14	OSCO	
10	SEC	1 pulse per second output
9	MIN	1 pulse per minute output
3	COMP	comparator output
7	POWF	power failure output
11	FSET	frequency setting signal output (128Hz)

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-pin Plastic DIP	−40 to 85°C	SAF3019P

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PIN-FOR-PIN FUNCTIONALLY-COMPATIBLE CROSS REFERENCE BY COMPETITOR

Linear Products

COMPETITOR	COMPETITOR PART NUMBER	SIGNETICS PART NUMBER	TEMPERATURE (°C)	PACKAGE
AMD	AM6012DC	AM6012F	0 to +70	Ceramic
	DAC08AQ	DAC08AF	−55 to +125	Ceramic
	DAC08CN	DAC08CN	0 to +70	Plastic
	DAC08CQ	DAC08CF	0 to +70	Ceramic
	DAC08EN	DAC08EN	0 to +70	Plastic
	DAC08EQ	DAC08EF	0 to +70	Ceramic
	DAC08HN	DAC08HN	0 to +70	Plastic
	DAC08HQ	DAC08HF	0 to +70	Ceramic
	DAC08Q	DAC08F	−55 to +125	Ceramic
	LF198H	SE5537H	−55 to +125	Metal can
	LF398H	NE5537H	0 to +70	Metal can
	LF398L	NE5537D	0 to +70	SO
	LF398N	NE5537N	0 to +70	Plastic
Datel	AM4532	NE5534AF	0 to +70	Ceramic
	AM4532C	NE5534AF	0 to +70	Ceramic
	AM4532M	SE5534AF	−55 to +125	Ceramic
	DACUP10BC	NE5020N	0 to +70	Plastic
	DACUP8BC	NE5018N	0 to +70	Plastic
	DACUP8BM	SE5019F	−55 to +125	Ceramic
	DACUP8BQ	SE5018F	−55 to +125	Ceramic
Exar	XR5532/A N	NE5532/AF	0 to +70	Ceramic
	XR5532/A P	NE5532/AN	0 to +70	Plastic
	XRL567CN	NE567F	0 to +70	Ceramic
	XRL567CP	NE567N	0 to +70	Plastic
	XR5534/A CN	NE5534/AF	0 to +70	Ceramic
	XR5534/A CP	NE5534/AN	0 to +70	Plastic
	XR5534/A M	SE5534/AF	−55 to +125	Ceramic
	XR558CN	NE558F	0 to +70	Ceramic
	XR558CP	NE558N	0 to +70	Plastic
	XR558M	SE558F	−55 to +125	Ceramic
	XR1524N	SG3524F	0 to +70	Ceramic
	XR1524P	SG3524N	0 to +70	Plastic
	XR2524P	SG3524N	0 to +70	Plastic
	XR3524N	SG3524F	0 to +70	Ceramic
	XR3524P	SG3524N	0 to +70	Plastic
Fairchild	μA080/DA	DAC08F	0 to +70	Ceramic
	μA0801CDC	MC1408F	0 to +70	Ceramic
	μA0801CPC	MC1408N	0 to +70	Plastic
	μA0801EDC	DAC08EF	0 to +70	Ceramic
	μA0801EPC	DAC08AF	0 to +70	Ceramic
	μA1458HC	MC1458H	0 to +70	Metal can
	μA1458TC	MC1458N	0 to +70	Plastic
	μA1488DC	MC1488F	0 to +70	Ceramic
	μA1488PC	MC1488N	0 to +70	Plastic
	μA1489/A DC	MC1489/AF	0 to +70	Ceramic

Pin-for-Pin Functionally-Compatible Cross Reference by Competitor

COMPETITOR	COMPETITOR PART NUMBER	SIGNETICS PART NUMBER	TEMPERATURE (°C)	PACKAGE
Fairchild (Cont.)	μA1489/A PC	MC1489/AN	0 to +70	Plastic
	μA198HM	NE5537H	0 to +70	Metal can
	μA198RM	NE5537N	0 to +70	Plastic
	μA2901DC	LM2901F	−40 to +85	Ceramic
	μA2901PC	LM2901N	−40 to +85	Plastic
	μA311RC	LM311F	0 to +70	Ceramic
	μA324DC	LM324F	0 to +70	Ceramic
	μA324PC	LM324N	0 to +70	Plastic
	μA3302DC	MC3302F	−40 to +85	Ceramic
	μA3302PC	MC3302N	−40 to +85	Plastic
	μA339/A DC	LM339/AF	0 to +70	Ceramic
	μA339/A PC	LM339/AN	0 to +70	Plastic
	μA3403DC	MC3403F	0 to +70	Ceramic
	μA3403PC	MC3403N	0 to +70	Plastic
	μA398HC	SE5537H	−55 to +125	Metal Can
	μA398RC	SE5537N	−55 to +125	Plastic
	μA555TC	NE555N	0 to +70	Plastic
	μA556PC	NE556-1N	0 to +70	Plastic
		NE556N	0 to +70	Plastic
	μA723DC	μA723CF	0 to +70	Ceramic
	μA723DM	μA723F	−55 to +125	Ceramic
	μA723HC	μA723CH	0 to +70	Metal Can
	μA723HM	μA723H	−55 to +125	Metal Can
	μA723PC	μA723CN	0 to +70	Plastic
	μA733DC	μA733F	0 to +70	Ceramic
	μA733DM	μA733F	−55 to +125	Ceramic
	μA733PC	μA733N	0 to +70	Plastic
	μA741HC	NE530H	0 to +70	Metal can
	μA741HM	SE530H	−55 to +125	Metal can
	μA741NM	μA741N	−55 to +125	Plastic
	μA741RC	μA741CF	0 to +70	Ceramic
	μA741TC	μA741CN	0 to +70	Plastic
	μA747DC	μA747CF	0 to +70	Ceramic
	μA747PC	μA747CN	0 to +70	Plastic
	μA9667DC	ULN2003F	0 to +70	Ceramic
	μA9667PC	ULN2003N	0 to +70	Plastic
	μA9668DC	ULN2004F	0 to +70	Ceramic
	μA9668PC	ULN2004N	0 to +70	Plastic
Harris	HA2539	NE5539	0 to +70	Plastic
	HA15102-2	SE5532/AF	−55 to +125	Ceramic
	HA15102-5	NE5532/AF	0 to +70	Ceramic
	HA15135-2	SE5534/AF	−55 to +125	Ceramic
	HA15135-5	NE5534/AF	0 to +70	Ceramic
	HA35102-5	NE5532/AN	0 to +70	Plastic
Intersil	ADC0803LCD	ADC0803-1LCF	−40 to +85	Ceramic
	ADC0804	ADC0804-1C	0 to +70	Plastic
	ADC0805	ADC0805-1LC	−40 to +85	Plastic
Motorola	DAC08CD	DAC08CN	0 to +70	Plastic
	DAC08CQ	DAC08CF	0 to +70	Ceramic
	DAC08ED	DAC08EN	0 to +70	Plastic
	DAC08EF	DAC08EF	0 to +70	Ceramic
	DAC08HQ	DAC08HF	0 to +70	Ceramic

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Pin-for-Pin Functionally-Compatible Cross Reference by Competitor

COMPETITOR	COMPETITOR PART NUMBER	SIGNETICS PART NUMBER	TEMPERATURE (°C)	PACKAGE
Motorola (Cont.)	DAC08Q	DAC08F	−55 to +125	Ceramic
	LM2901N	LM2901N	−40 to +85	Plastic
	LM311J-8	LM311F	0 to +70	Ceramic
	LM311N	LM311N	0 to +70	Plastic
	LM324J	LM324F	0 to +70	Ceramic
	LM324N	LM324N	0 to +70	Plastic
	LM339/A J	LM339/AF	0 to +70	Ceramic
	LM339/A N	LM339/AN	0 to +70	Plastic
	LM358H	LM358H	0 to +70	Metal can
	LM358N	LM358N	0 to +70	Plastic
	LM393A/J	LM393/AF	0 to +70	Ceramic
	LM393A/N	LM393/AN	0 to +70	Plastic
	MC1408L	MC1408F	0 to +70	Ceramic
	MC1408P	MC1408N	0 to +70	Plastic
	MC1488L	MC1488F	0 to +70	Ceramic
	MC1488P	MC1488N	0 to +70	Plastic
	MC1489/A L	MC1489/AF	0 to +70	Ceramic
	MC1489/A P	MC1489/AN	0 to +70	Plastic
	MC1496L	MC1496F	0 to +70	Ceramic
	MC1496P	MC1496N	0 to +70	Plastic
	MC3302L	MC3302F	−40 to +85	Ceramic
	MC3302P	MC3302N	−40 to +85	Plastic
	MC3403L	MC3403F	0 to +70	Ceramic
	MC3403P	MC3403N	0 to +70	Plastic
	MC3410CL	MC3410CN	0 to +70	Ceramic
	MC3410L	MC3410N or NE5410N	0 to +70	Ceramic
	MC3510L	SE5410F	−55 to +125	Ceramic
	NE592F	NE592F	0 to +70	Ceramic
	NE592N	NE592N	0 to +70	Plastic
	NE565N	NE565N	0 to +70	Plastic
	SE592F	SE592F	−55 to +125	Ceramic
	SE592H	SE592H	−55 to +125	Metal can
National	ADC0803F	ADC0803-1LCF	−40 to +85	Ceramic
	ADC0803N	ADC0803-1LCN	−40 to +85	Plastic
	ADC0805	ADC0805-1LC	−40 to +85	Plastic
	DAC08AQ	DAC08AF	−55 to +125	Ceramic
	DAC08CD	DAC08CN	0 to +70	Plastic
	DAC08CQ	DAC08CF	0 to +70	Ceramic
	DAC08ED	DAC08EN	0 to +70	Plastic
	DAC08HQ	DAC08HF	0 to +70	Ceramic
	DAC08Q	DAC08F	−55 to +125	Ceramic
	DAC0808LCJ	MC1408F	0 to +70	Ceramic
	DAC0808LCN	MC1408N	0 to +70	Plastic
	DAC0808LD	MC1408F	0 to +70	Ceramic
	LF198/A H	SE5537H	−55 to +125	Metal can
	LF398/A H	NE5537H	0 to +70	Metal can
	LF398/A N	NE5537N	0 to +70	Plastic
	LM13600AN	NE5517N	0 to +70	Plastic
	LM13600N	NE5517N	0 to +70	Plastic
	LM1458H	MC1458H	0 to +70	Metal can

Pin-for-Pin Functionally-Compatible Cross Reference by Competitor

COMPETITOR	COMPETITOR PART NUMBER	SIGNETICS PART NUMBER	TEMPERATURE (°C)	PACKAGE
National (Cont.)	LM1458N	MC1458N	0 to +70	Plastic
	LM161H	SE529H	−55 to +125	Metal can
	LM161J	SE529F	−55 to +125	Ceramic
	LM2524J	SG3524F	0 to +70	Ceramic
	LM2524N	SG3524N	0 to +70	Plastic
	LM2901N	LM2901N	−40 to +85	Plastic
	LM2903N	LM2903N	−40 to +85	Plastic
	LM3089	CA3089N	−55 to +125	Plastic
	LM319H	LM119H	0 to +70	Metal can
	LM319J	LM319F	0 to +70	Ceramic
	LM319N	LM319N	0 to +70	Plastic
	LM324J	LM324F	0 to +70	Ceramic
	LM324N	LM324N	0 to +70	Plastic
	LM339/AJ	LM339/AF	0 to +70	Ceramic
	LM339/AN	LM339/AN	0 to +70	Plastic
	LM3524J	SG3524F	0 to +70	Ceramic
	LM3524N	SG3524N	0 to +70	Plastic
	LM358H	LM358H	0 to +70	Metal can
	LM358N	LM358N	0 to +70	Plastic
	LM361H	NE529H	0 to +70	Metal can
	LM361J	NE529D	0 to +70	SO
	LM361N	NE529N	0 to +70	Plastic
	LM393/A N	LM393/AN	0 to +70	Plastic
	LM555J	NE555F	0 to +70	Ceramic
	LM555N	NE555N	0 to +70	Plastic
	LM556J	SE556-1F	−55 to +125	Ceramic
	LM556N	SE556-1N	−55 to +125	Plastic
	LM556CJ	NE556-1F	0 to +70	Ceramic
	LM556CN	NE556-1N	0 to +70	Plastic
	LM565CN	NE565N	0 to +70	Plastic
	LM566N	SE566N	−55 to +125	Plastic
	LM566CN	NE566N	0 to +70	Plastic
	LM567CN	NE567N	0 to +70	Plastic
	LM592	NE592N	0 to +70	Plastic
	LM733CN	μA733CN	0 to +70	Plastic
	LM741CJ	μA741CF	0 to +70	Ceramic
	LM741CN	μA741CN	0 to +70	Plastic
	LM741J	μA741F	−55 to +125	Ceramic
	LM741N	μA741N	−55 to +125	Plastic
	LM747CJ	μA747CF	0 to +70	Ceramic
	LM747CN	μA747CN	0 to +70	Plastic
	LM747J	μA747F	−55 to +125	Ceramic
	LM747N	μA747N	−55 to +125	Plastic
PMI	DAC1408-8P	MC1408N	0 to +70	Plastic
	DAC1408-8Q	MC1408F	0 to +70	Ceramic
	PM747Y	μA747N	−55 to +125	Plastic
Raytheon	RC5532/A DE	NE5532/AF	0 to +70	Ceramic
	RC5532/A NB	NE5532/AN	0 to +70	Plastic
	RC5534/A DE	NE5534/AF	0 to +70	Ceramic
	RC5534/A NB	NE5534/AN	0 to +70	Plastic
	RM5532/A DE	SE5532/AF	−55 to +125	Ceramic
	RM5534/A DE	SE5534/AF	−55 to +125	Ceramic

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Pin-for-Pin Functionally-Compatible Cross Reference by Competitor

COMPETITOR	COMPETITOR PART NUMBER	SIGNETICS PART NUMBER	TEMPERATURE (°C)	PACKAGE
Silicon General	SG3524J	SG3524F	0 to +70	Ceramic
Sprague	UDN6118A	SA594N	−40 to +85	Plastic
	UDN6118R	SA594F	−40 to +85	Ceramic
	ULN8160A	NE5560N	0 to +70	Plastic
	ULN8160R	NE5560F	0 to +70	Ceramic
	ULN8161M	NE5561N	0 to +70	Plastic
TI	ADC0803	ADC0803-1LCN	−40 to +85	Plastic
	ADC0804CN	ADC0804-1C	0 to +70	Plastic
	ADC0805	ADC0805-1LC	−40 to +85	Plastic
	LM324D	LM324N	0 to +70	Plastic
	LM324J	LM324F	0 to +70	Ceramic
	LM339/AJ	LM339/AF	0 to +70	Ceramic
	LM339/AN	LM339/AN	0 to +70	Plastic
	LM358P	LM358N	0 to +70	Plastic
	LM358U	LM358H	0 to +70	Metal can
	LM393/A P	LM393/AN	0 to +70	Plastic
	MC1458P	MC1458N	0 to +70	Plastic
	MC1458U	MC1458H	0 to +70	Metal can
	NE5532/A JG	NE5532/AF	0 to +70	Ceramic
	NE5532/A P	NE5532/AN	0 to +70	Plastic
	NE5534/A JG	NE5534/AF	0 to +70	Ceramic
	NE5534/A P	NE5534/AN	0 to +70	Plastic
	NE555JG	NE555N	0 to +70	Plastic
	NE555P	NE555N	0 to +70	Plastic
	NE556D	NE556N	0 to +70	Plastic
	NE556J	NE556-1F	0 to +70	Ceramic
	NE556N	NE556-1N	0 to +70	Plastic
	NE592	NE592N14	0 to +70	Plastic
	NE592A	NE592F14	0 to +70	Ceramic
	NE592J	NE592F	0 to +70	Ceramic
	NE592N	NE592N	0 to +70	Plastic
	SA556D	SA556N	−40 to +85	Plastic
	SE5534/A JG	SE5534/AF	−55 to +125	Ceramic
	SE555JG	SE555N	−55 to +125	Plastic
	SE556J	SE556-1F	−55 to +125	Ceramic
	SE556N	SE556-1N	−55 to +125	Plastic
	SE592	SE592N14	−55 to +125	Plastic
	SE592J	SE592F	−55 to +125	Ceramic
	SE592N	SE592N	−55 to +125	Plastic
	TL592A	NE592F14	0 to +70	Ceramic
	TL592P	NE592N8	0 to +70	Plastic
	μA723CJ	μA723CF	0 to +70	Ceramic
	μA723CN	μA723CN	0 to +70	Plastic
	μA723MJ	μA723F	−55 to +125	Ceramic
	μA723MU	μA723D	−55 to +125	SO
Unitrode	UC3524J	SG3524F	0 to +70	Ceramic
	UC3524N	SG3524N	0 to +70	Plastic

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Interface / Data Conversion Products

Part Number	Description	Available in SO
Analog-to-Digital Converters		
ADC0801/2/3/4/5	8-bit CMOS A/D converter	
SE/NE5030	10-bit high-speed microprocessor-compatible A/D converter	
NE5034	8-bit high-speed A/D converter	
NE5036	6-bit A/D converter, serial output	x
NE5037	6-bit A/D converter, parallel output	x
PCF8591	8-bit A/D and D/A converter	
PNA7507	7-bit A/D converter, 15MHz (Flash)	
TDA1534A	14-bit A/D converter, serial output	
Digital-to-Analog Converters		
AM6012	12-bit high-speed multiplying D/A converter	
DAC-08 Series	8-bit high-speed multiplying D/A converter	x
DAC800	12-bit D/A converter	
MC1508-8/1408-8/1408-7	8-bit multiplying D/A converter	x
MC3410/3510/3410C	10-bit high-speed multiplying D/A converter	
NE5020	10-bit microprocessor-compatible D/A converter	
NE5150/5151	RGB video D/A converter	
PCF8591	8-bit A/D and D/A converter	
PNA7518	8-bit D/A converter, 30MHz	
SAB3013	Six-function analog memory (6-bit D/A converter)	
SE/NE5018	8-bit microprocessor-compatible D/A converter	x
SE/NE5019	8-bit microprocessor-compatible D/A converter	x
SE/NE5118	8-bit microprocessor-compatible D/A converter, current output	
SE/NE5119	8-bit microprocessor-compatible D/A converter, current output	
SE/NE5410	10-bit high-speed multiplying D/A converter	
TDA1540P,D	14-bit D/A converter, serial output	
Comparators		
LM111/211/311	Voltage comparator	x
LM119/219/319	Dual voltage comparator	x
LM139/A/239/A/339/A	Quad voltage comparator	x
LM193/A/239/A/393/A	Low power dual voltage comparator	x
LM2901	Quad voltage comparator	x
LM2903	Low power dual voltage comparator	x
MC3302	Quad voltage comparator	x
SE/NE521	High-speed dual differential comparator/sense amplifier	x
SE/NE522	High-speed dual differential comparator/sense amplifier	x
SE/NE527	Voltage comparator	x
SE/NE529	Voltage comparator	x
PCF1251T	Micropower voltage detector	x
Position Measurement		
NE5520	LVDT signal conditioner	x
SE/NE5521	LVDT signal conditioner	
Sample and Hold		
LF198/298/398	Monolithic sample and hold circuit	x
SE/NE5537	Sample and hold amplifier	x
TDA1535	High performance sample and hold amplifier with resolution to 16 bits	

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Interface/Data Conversion Products

Part Number	Description	Available in SO
Drivers		
MC1488	Quad line driver	x
MC1489/A	Quad line receiver	x
NE5090	Addressable relay driver	x
NE5170	Octal line driver	
NE5180/81	Octal line receiver	
NE587	LED decoder/driver	x
NE589	LED decoder/driver	x
NE590	Addressable peripheral driver	
NE591	Addressable peripheral driver	
SA/NE594	Vacuum fluorescent display driver	x
PCF2100	40-segment LCD duplex driver	x
PCF2110	60-segment LCD duplex driver	x
PCF2111	64-segment LCD duplex driver	x
PCF1303	18-segment LCD bar graph driver	
PCF2112	32-segment LCD static driver	x
PCF8576	Universal LCD driver for low multiplex rates	x
PCF8577	32/64-segment LCD driver	x
SAA1060	32-segment LED driver	
SAA1061	16-segment LED driver	
SAA1062A	20-segment LCD driver	x
SAA1063	Vacuum fluorescent display driver (17-bit)	
ULN2003	High voltage/current Darlington transistor array	x
ULN2004	High voltage/current Darlington transistor array	x

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Communications Products

Part Number	Description	Available in SO
Analog and Audio Processing		
NE570	Compandor	
SA/NE571	Compandor	x
SA/NE572	Programmable analog compandor	x
SAA7000	Compact disc circuit	
SAA7010	Demodulator for compact disc	
SAA7020	Error corrector for compact disc	
SAA7030	Filter circuit for compact disc	
Audio/Stereo		
LM1870	Stereo demodulator with blend	x
NE5240	Dolby digital audio decoder	
NE542	Dual low-noise preamplifier	
NE645/646	Dolby B-type noise reduction circuit	
NE648/649	Low voltage Dolby B-type noise reduction circuit	
NE650	Dolby B-type noise reduction circuit	
NE660	Dolby B-type noise reduction circuit	
NE670	Low voltage Dolby B/C-type noise reduction circuit	
TDA1029	Stereo audio switch	
TDA1074A	DC-controlled dual potentiometers	
TDA1522	Stereo cassette preamplifier (dual)	
TDA1524A	Stereo, DC-controlled audio control	
TDA1578A	PLL stereo decoder	
TDA3810	Spatial, stereo, pseudo-stereo processor	
TDA3806	TV-stereo sound decoder (Zenith format)	
TDA3807	Second audio program (SAP) FM decoder	
TEA5580	PLL stereo decoder	
μA758	FM stereo multiplex decoder phase locked loop	
AM Radio		
SAA1057	PLL radio tuning circuit	
TDA1072	AM radio circuit	
TDD1742T	CMOS frequency synthesizer	x
TEA5550	AM radio circuit	
TEA5570	AM/FM radio receiver circuit	
FM Radio		
CA3089	FM I.F. system	
MC1496	Balanced modulator/demodulator	
SA/NE602	Double-balanced mixer and oscillator	x
SA/NE612	Double-balanced mixer and oscillator	x
SA/NE604	Low power narrow-band FM I.F.	x
SA/NE614	Low power narrow-band FM I.F.	x
SAA1057	PLL radio tuning circuit	
TDA0820T	Balanced modulator/demodulator	x
TDA1001B,T	FM noise suppression circuit	x
TDA1571	FM mixer stage	
TDA1574	FM front end IC	
TDA1576	FM/I.F. (quadrature detector)	
TDA1596	FM/I.F. amplifier	
TDA7000	Single-chip FM radio	
TDA7010T	Single-chip FM radio, SO package	x
TDA7020T	FM radio (stereo receiver)	x
TDD1742T	CMOS frequency synthesizer	x
TEA5560	FM radio circuit	
TEA5570	AM/FM radio receiver circuit	
TEA6000	FM/I.F. system and computer interface circuit	

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Communications Products

Part Number	Description	Available in SO
FSK Modems		
NE5050	Power line modem	x
NE5080	2-Megabaud FSK transmitter, IEEE 802.4	
NE5081	FSK receiver, IEEE 802.4	
IR Remote Control Transmitters and Receivers		
SAA3004	I/R transmitter (448 commands)	x
SAA3006	I/R transmitter (2K commands, low voltage)	
SAA3028	I/R receiver	
SAF1032P	Remote control receiver	
SAF1039P	Remote control transmitter	
TDA3047	I/R preamplifier	
TDA3048	I/R preamplifier	
Phase Locked Loops		
SE/NE564	High frequency phase locked loop	x
SE/NE565	Phase locked loop	x
SE/NE566	Function generator	x
SE/NE567	Tone decoder/phase locked loop	x
SE/NE568	150MHz phase locked loop	
Speech/Music Synthesis		
MEA8000	Speech synthesizer	
OM8000	Speech evaluation P.C. board	
OM8001	Speech demonstrator	
OM8010/8011	Speech encoding system	
PCD3311/3312	DTMF/MODEM/Musical tone generator	x
PCF8200	Single-chip CMOS male/female speech synthesizer	
SAA1099	Stereo sound generator for sound effects and music synthesis	
UAA2183	Sound generator IC for organs	
Telephony		
NE5900	Call progress decoder	
PCD3310	Pulse and DTMF dialer with redial	
PCD3311/3312	DTMF/MODEM/Musical tone generator	x
PCD3315	CMOS redial and repertory dialer	x
PCD3343	CMOS microcontroller for telephone sets	x
PCD3360/61	Programmable multi-tone telephone ringer	x
PM4300/4337	Low-cost, stand-alone microcomputer development system for MAB84xx family of microcomputers	
SA/NE602	Double-balanced mixer and oscillator (cellular/portable for telephone)	x
SA/NE612	Double-balanced mixer and oscillator (cellular/portable for telephone)	x
SA/NE604	Low power narrow-band FM I.F. (cellular/portable for telephone)	x
SA/NE614	Low power narrow-band FM I.F. (cellular/portable for telephone)	x
TDA7000	Single-chip FM radio (for cordless telephone)	
TDA7050T	Low voltage mono/stereo power amplifier (for cordless telephone)	x
TEA1042	Transmission interface with loudspeaking ability	
TEA1046/A	Transmission interface with DTMF	
TEA1060/61	Telephone transmission circuit	
TEA1067	Low voltage transmission IC with dialer interface	
TEA1075	DTMF generator for telephone dialing	
TEA1080	Supply IC for telephone peripherals	
Timers		
PCF8573	Clock/Timer with I^2C interface	x
SA/SE/NE556/-1/SE556-1C	Dual timer	x
SA/SE/NE558	Quad timer	x
SAF3019P	Clock/Timer	
SE/NE555/SE555C	Timer	x

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Amplifier Products

Part Number	Description	Available in SO
Companding		
NE570	Compandor	
SA/NE571	Compandor	
SA/NE572	Programmable analog compandor	x
Operational		
LM124/224/324/SA534	Low power quad operational amplifier	x
LM158/258/358	Low power dual operational amplifier	x
MC/SA1458/MC1558	General purpose operational amplifier	x
MC3303/3403/3503	Quad low power operational amplifier	x
NE1012	Low noise operational amplifier	
NE1037	Low noise, high-speed precision operational amplifier	
SE/NE4558	Dual general purpose operational amplifier	x
NE5230	Low voltage operational amplifier	x
SE/NE530	High slew rate operational amplifier	
SE/NE531	High slew rate operational amplifier	
SA/SE/NE532	Low power dual operational amplifier	x
SE/NE538	High slew rate operational amplifier	
SE/NE5512	Dual high performance operational amplifier	x
SE/NE5514	Quad high performance operational amplifier	x
SE/NE5532/A	Internally compensated dual low noise operational amplifier	x
NE5533/A/SA/SE/NE5534A	Single and dual low noise operational amplifier	x
SE/NE5535	Dual high slew rate operational amplifier	x
μA741/741C/SA741C	General purpose operational amplifier	x
μA747/747C/SA747C	Dual operational amplifier	x
Power		
OM200/S2	Hearing aid amplifier	
TDA1010A	6W audio amplifier	
TDA1013A	4W audio amplifier with DC volume control	
TDA1015	1 to 4W audio amplifier	
TDA1020	12W audio amplifier	
TDA1510	2×12W audio amplifier	
TDA1512	12 to 20W audio amplifier	
TDA1515	24W BTL audio amplifier	
TDA1520A	20W Hi-Fi audio amplifier	
TDA2611A	5W audio output for TV	
TDA7050T	Low voltage mono/stereo power amplifier	x
Transconductance		
NE5517/A	Dual operational transconductance amplifier	x
Video		
NE5205	Wideband high frequency amplifier	x
SE/NE5539	Ultra high frequency operational amplifier	x
SE/NE5592	Video amplifier	x
SE/NE592	Video amplifier	x
μA733/C	Differential video amplifier	

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Video Products

Part Number	Description	Available in SO
Tuning		
MAB84xx	Single-chip 8-bit microcontroller family	
PCD8571	1K serial RAM	x
PCF8570	256×8 static RAM	x
PCF8573	Clock/timer with I^2C Interface	x
PCF8574	8-bit remote I/O expander	
SAA1300	Video switch (5-output switch)	
SAB1164	1GHz divide by 64 (prescaler)	
SAB1165	1GHz divide by 64 (prescaler)	
SAB1256	1GHz divide by 256 (prescaler)	
SAB3013	Six-function analog memory (6-bit D/A converter)	
SAB3035	FLL tuning circuit (eight D/A converters)	
SAB3036	FLL tuning circuit	
SAB3037	FLL tuning circuit (four D/A converters)	
TDA0820T	Balanced modulator/demodulator	x
TDA5030	VHF mixer-oscillator	
TDD1742T	CMOS frequency synthesizer	x
Video I.F.		
TDA2540	Video I.F. amplifier demodulator, AFT, NPN tuners	
TDA2541	Video I.F. amplifier demodulator, AFT, PNP tuners	
TDA3540/41	Video I.F./AFT	
TDA3806	TV-stereo sound decoder (Zenith format)	
TDA3807	Second audio program (SAP) FM detector	
TDA4501	Complete video and sound I.F. IC with vertical and horizontal outputs	
TDA4502	Complete video I.F. IC with vertical and horizontal sync	
TDA4503	Small signal combination for B/W TV without castle generator	
Sound I.F. and Special Audio Decoding		
TBA120U	I.F. amplifier and demodulator	
TDA2545A	Quasi-split sound I.F.	
TDA2546A	Quasi-split sound I.F. and sound demodulator	
TDA2555	Dual TV sound demodulator	
Sync Processing and Generation		
TDA2577A	Sync circuit with vertical oscillator and driver (with negative horizontal output)	
TDA2578A	Sync circuit with vertical oscillator and driver (with negative horizontal output)	
TDA2579	Sync circuit with vertical oscillator and driver (with horizonta output)	
TDA2593	Horizontal combination	
TDA2594	Horizontal combination	
TDA2595	Horizontal combination	
SAA1043	Universal sync generator	
SAA1044	Subcarrier coupler (used with SAA1043)	
Color Decoding and Encoding		
NE5150/5151	RGB video D/A converter	
TDA2501	PAL or NTSC encoder	
TDA3505	Chroma control circuit	
TDA3562A	PAL/NTSC decoder	
TDA3563	NTSC decoder with RGB inputs	
TDA3564	NTSC decoder	
TDA3568	Monolithic integrated delay line and filter combination for NTSC television receivers	
TDA4555/4556	Multistandard color decoder	
TDA4560	Color transient improvement circuit (CTI)	
TDA4580	Video control with two RGB and color difference inputs	
TEA2000	RGB to NTSC/PAL encoder	

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Video Products

Part Number	Description	Available in SO
Vertical Deflection		
TDA2653A	Vertical deflection	
TDA3651A/AQ	Vertical deflection	
TDA3651A/AQ/3653	Vertical deflection	
TDA3652	Vertical deflection	
TDA3654	Vertical deflection	
Videotex/Teletext		
SAA5025D	525-line teletext timing chain	
SAA5030	Teletext video input processor	
SAA5040	Teletext acquisition and control circuit	
SAA5045	Gearing and address logic array (GALA)	
SAA5050/55	Teletext character generator	
SAA5230	Advanced video processor	
SAA5240	Microprocessor controlled teletext circuit	
SAA5350	Advanced display controller (625-line system)	

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Small Area Networks (I^2C) Products

Part Number	Description	Available in SO
MAB84xx	Single-chip 8-bit microcontroller family	
NE5036	6-bit A/D converter-serial output	x
PCB8573	Clock/timer with I^2C interface	
PCD8571	1K serial RAM	
PCD8572	1024-bit EEROM	
PCF2100	4-segment LCD duplex driver	x
PCF2110	60-segment LCD duplex driver	x
PCF2111	64-segment LCD duplex driver	x
PCF2112	32-segment LCD static driver	x
PCF8200	Single-chip CMOS high performance speech synthesizer	
PCF8570	256×8 static RAM	x
PCF8574	8-bit remote I/O expandor	x
PCF8576	Universal LCD driver for low multiplex rates	x
PCF8577	32/64-segment LCD driver for automotive	x
PCF8591	8-bit A/D and D/A converter	
SAA1057	PLL radio tuning circuit	
SAA1060	32-segment LED driver	
SAA1061	16-segment LED driver	
SAA1063	Vacuum fluorescent display driver (17-bit)	
SAA1300	Video switch (5-output switch)	
SAA3028	I/R receiver	
SAA5240	Microprocessor controlled teletext circuit	
SAB3013	6-function analog memory (6-bit D/A converter)	
SAB3035	FLL TV tuning circuit (eight D/A converters)	
SAB3036	FLL TV tuning circuit	
SAB3037	FLL TV tuning circuit (four D/A converters)	
SAF3019P	Clock/timer with I^2C interface	
SCC84Cxx	CMOS 8-bit microcontroller family	
SCC83C351	CMOS serial bus microcontroller	
SCC80C351	CMOS serial bus microcontroller	
TDA1534A	14-bit A/D converter-serial output	
TDA1540P,D	14-bit D/A converter-serial output	
TDA8400	Frequency synthesizer (Cypress)	
TDA8440	Audio/video switch	
TDA8442	I/O expandor	
TDA8443	RGB/YUV matrix switch	
TDD1742T	CMOS frequency synthesizer	x
TEA6000	FM I.F. system and computer interface circuit	

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Signetics Programmable Logic Device Selection Guide

Signetics P/N	Architecture	Package	Total Inputs (#Dedicated)	Product Terms	Internal State Registers	Outputs C, I/O, R, R I/O	T_{PD}† (Typical Values)	I_{CC} (Typical Values)
FPGA								
PLS103	16 × 9 × 9	28-Pin	16	9	0	9 C	20ns	120mA
PLS151	18 × 15 × 12	20-Pin	18 (6)	15	0	12 I/O	15ns	130mA
FPAD								
PLS162	16 × 5	24-Pin	16	5	0	5 C	20ns	120mA
PLS163	12 × 9	24-Pin	12	9	0	9 C	20ns	120mA
FPLA								
PLS100	16 × 48 × 8	28-Pin	16	48	0	8 C	35ns	120mA
PLS153	18 × 42 × 10	20-Pin	18 (8)	42	0	10 I/O	30ns	130mA
PLS153A	18 × 42 × 10	20-Pin	18 (8)	42	0	10 I/O	20ns	130mA
PLUS153**	18 × 42 × 10	20-Pin	18 (8)	42	0	10 I/O	10ns	150mA
PLC153**	18 × 42 × 10	20-Pin	18 (8)	42	0	10 I/O	TBD	TBD
PLS161	12 × 48 × 8	24-Pin	12	48	0	8 C	35ns	120mA
PLS173	22 × 42 × 10	24-Pin	22 (12)	42	0	10 I/O	20ns	150mA
PLC173**	22 × 42 × 10	24-Pin	22 (12)	42	0	10 I/O	TBD	TBD
PLUS173**	22 × 42 × 10	24-Pin	22 (12)	42	0	10 I/O	10ns	150mA
PLHS473**	20 × 24 × 11	24-Pin	20 (11)	24	0	2 C & 9 I/O	15ns	140mA
PLC473**	20 × 24 × 11	24-Pin	20 (11)	24	0	2 C & 9 I/O	35ns	40mA
PLHS18P8A**	18 × 72 × 8	20-Pin	18 (10)	72	0	8 I/O	14ns	120mA
FPLS								
PLS105	16 × 48 × 8	28-Pin	16	48	6	8 R	60ns	120mA
PLS105A	16 × 48 × 8	28-Pin	16	48	6	8 R	45ns	120mA
PLC105**	16 × 48 × 8	28-Pin	16	48	6	8 R	45ns	40mA
PLUS405**	16 × 64 × 8	28-Pin	16	64	8	8 R	20ns	190mA
PLS155	16 × 45 × 12	20-Pin	16 (4)	45	4*	8 I/O & 4 R I/O	55ns	150mA
PLS157	16 × 45 × 12	20-Pin	16 (4)	45	6*	6 I/O & 6 R I/O	55ns	150mA
PLS159	16 × 45 × 12	20-Pin	16 (4)	45	8*	4 I/O & 8 R I/O	55ns	150mA
PLS167	14 × 48 × 6	24-Pin	14	48	6 plus 2*	6 R	60ns	120mA
PLS167A	14 × 48 × 6	24-Pin	14	48	6 plus 2*	6 R	45ns	120mA
PLS168	12 × 48 × 8	24-Pin	12	48	6 plus 4*	8 R	60ns	120mA
PLS168A	12 × 48 × 8	24-Pin	12	48	6 plus 4*	8 R	45ns	120mA
PLS179	20 × 45 × 12	24-Pin	20 (8)	45	8*	4 I/O & 8 R I/O	45ns	145mA

Outputs:
C = Combinatorial output
I/O = Combinatorial I/O
R = Registered output
R I/O = Registered I/O

Notes:
*State registers shared with output registers
**Under development
†$T_{PD} = T_{IS} + T_{CKO}$ for registered devices

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PLS105
Field Programmable Logic Sequencer (16 × 48 × 8)

Signetics Programmable Logic
Product Specification

Application Specific Products
- **Series 28**

DESCRIPTION

The PLS105 is a bipolar programmable state machine of the Mealy type. It contains logic AND-OR gate arrays with user programmable connections which control the inputs of on-chip State and Output Registers. These consist respectively of 6 Q_P, and 8 Q_F edge-triggered, clocked S/R flip-flops, with an asynchronous Preset option. All flip-flops are unconditionally preset to "1" during power turn on.

The AND array combines 16 external inputs I_{0-15} with six internal inputs P_{0-5} fed back from the State Register to form up to 48 transition terms (AND terms). All transition terms can include True, False, or Don't Care states of the controlling variables, and are merged in the OR array to issue next-state and next-output commands to their respective registers on the LOW-to-HIGH transition of the Clock pulse. Both True and Complement transition terms can be generated by optional use of the internal input variable (C) from the Complement Array. Also, if desired, the Preset input can be converted to $\overline{\text{Output Enable}}$ function, as an additional user-programmable option.

Order codes are contained on the pages following.

FEATURES

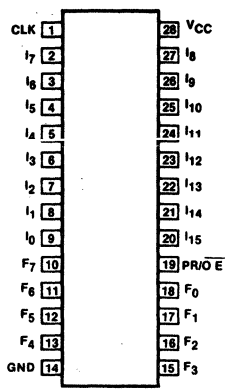
- **Field programmable (Ni-Cr link)**
- **16 input variables**
- **8 output functions**
- **48 transition terms**
- **6-bit State Register**
- **8-bit Output Register**
- **Transition Complement Array**
- **Positive edge trigger clock**
- **Programmable asynchronous preset or Output Enable**
- **Power-on preset to all "1" of internal registers**
- **f_{MAX} = 13.9MHz**
- **650mW power dissipation (typical)**
- **TTL compatible**
- **Single +5V supply**
- **Tri-state outputs**

APPLICATIONS

- **Interface protocols**
- **Sequence detectors**
- **Peripheral controllers**
- **Timing generators**
- **Sequential circuits**
- **Elevator controllers**
- **Security locking systems**
- **Counters**
- **Shift registers**

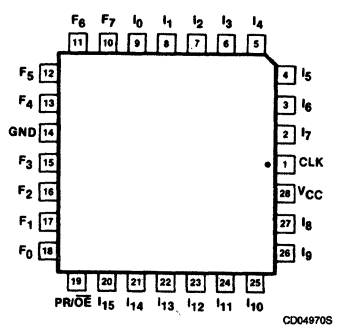
PIN CONFIGURATION

N PACKAGE



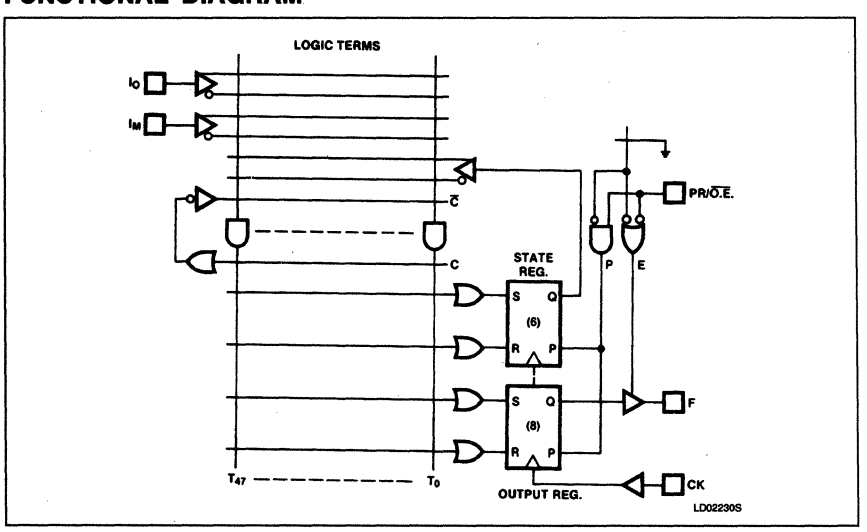
N = Plastic

A PACKAGE



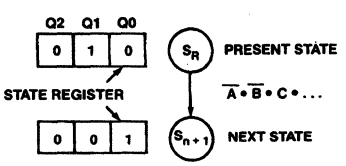
A = Plastic Leaded Chip Carrier

FUNCTIONAL DIAGRAM



LOGIC FUNCTION

Typical State Transition:



SET Q_0: $S_0 = (\overline{Q_2} \bullet Q_1 \bullet \overline{Q_0}) \bullet \overline{A} \bullet \overline{B} \bullet C \ldots$
$R_0 = 0$

RESET Q_1: $S_1 = 0$
$R_1 = (\overline{Q_2} \bullet Q_1 \bullet \overline{Q_0}) \bullet \overline{A} \bullet \overline{B} \bullet C \ldots$

HOLD Q_2: $S_2 = 0$
$R_2 = 0$

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Signetics

PLS105A
Field Programmable Logic Array (16 × 48 × 8)

Signetics Programmable Logic
Product Specification

Application Specific Products
- **Series 28**

DESCRIPTION

The PLS105A is a bipolar programmable state machine of the Mealy type. It contains logic AND-OR gate arrays with user programmable connections which control the inputs of on-chip State and Output Registers. These consist respectively of 6 Q_P, and 8 Q_F edge-triggered, clocked S/R flip-flops, with an asynchronous Preset option. All flip-flops are unconditionally preset to "1" during power turn on.

The AND array combines 16 external inputs I_{0-15} with 6 internal inputs P_{0-5} fed back from the State Register to form up to 48 Transition terms (AND terms). All Transition terms can include True, False, or Don't Care states of the controlling variables, and are merged in the OR array to issue next-state and next-output commands to their respective registers on the Low to High transition of the Clock pulse. Both True and Complement Transition terms can be generated by optional use of the internal input variable (C) from the Complement Array. Also, if desired, the Preset input can be converted to Output-Enable function, as an additional user programmable option.

Order codes are contained on the pages following.

FEATURES

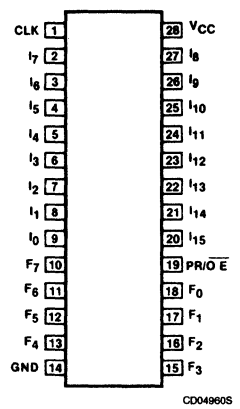
- **Field programmable (Ni-Cr link)**
- **16 input variables**
- **8 output functions**
- **48 transition terms**
- **6-bit State Register**
- **8-bit Output Register**
- **Transition complement array**
- **Positive edge trigger clock**
- **Programmable asynchronous preset or output enable**
- **Power-on preset to all "1" of internal registers**
- **$f_{(MAX)}$ = 20MHz**
- **650mW power dissipation (typical)**
- **TTL compatible**
- **Single +5V supply**
- **Tri-state outputs**

APPLICATIONS

- **Interface protocols**
- **Sequence detectors**
- **Peripheral controllers**
- **Timing generators**
- **Sequential circuits**
- **Elevator controllers**
- **Security locking systems**
- **Counters**
- **Shift registers**

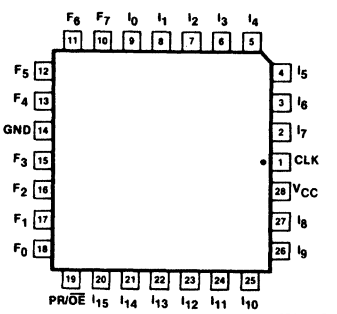
PIN CONFIGURATION

N PACKAGE



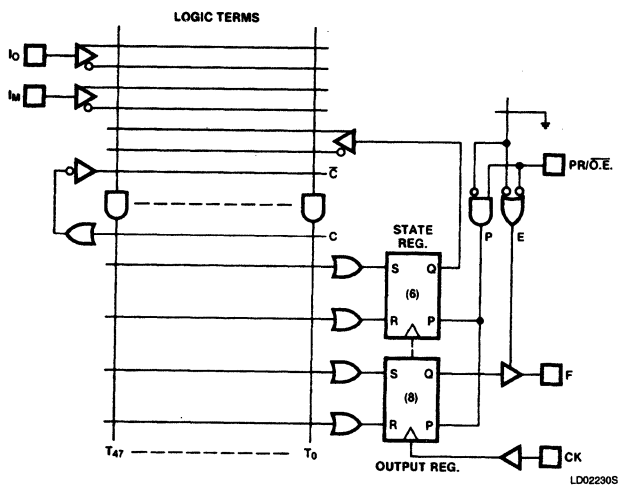
N = Plastic

A PACKAGE



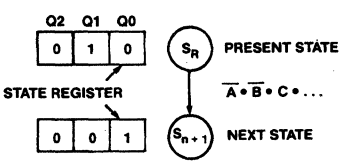
A = Plastic Leaded Chip Carrier

FUNCTIONAL DIAGRAM



LOGIC FUNCTION

Typical State Transition:



SET Q_0: $S_0 = (\overline{Q_2} \cdot Q_1 \cdot \overline{Q_0}) \cdot \overline{A} \cdot \overline{B} \cdot C \ldots$

$R_0 = 0$

RESET Q_1: $S_1 = 0$

$R_1 = (\overline{Q_2} \cdot Q_1 \cdot \overline{Q_0}) \cdot \overline{A} \cdot \overline{B} \cdot C \ldots$

HOLD Q_2: $S_2 = 0$

$R_2 = 0$

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Signetics

PLS155
Field-Programmable Logic Sequencer (16 × 45 × 12)

Signetics Programmable Logic
Product Specification

Application Specific Products
- **Series 20**

DESCRIPTION

The PLS155 is a Tre-state output, registered logic element combining AND/OR gate arrays with clocked J-K flip-flops. These J-K flip-flops are dynamically convertible to D-type via a "fold-back" inverting buffer and control gate F_C. It features 4 registered I/O outputs (F) in conjunction with 8 bidirectional I/O lines (B). These yield variable I/O gate and register configurations via control gates (D, L) ranging from 16 inputs to 12 outputs.

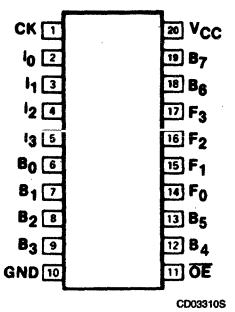
The AND/OR arrays consist of 32 logic AND gates, 13 control AND gates, and 21 OR gates with fusible link connections for programming I/O polarity and direction. All AND gates are linked to 4 inputs (I), bidirectional I/O lines (B), internal flip-flop outputs (Q), and Complement Array output ($\overline{C}$). The Complement Array consists of a NOR gate optionally linked to all AND gates for generating and propagating complementary AND terms.

FEATURES

- **Field-programmable (Ni-Cr link)**
- **4 dedicated inputs**
- **13 control gates**
- **32 AND gates**
- **21 OR gates**
- **45 product terms:**
  - **32 logic terms**
  - **13 control terms**
- **8 bidirectional I/O lines**
- **4 bidirectional registers**
- **J-K, T, or D-type flip-flops**
- **Asynchronous Preset/Reset**
- **Complement Array**
- **Active HIGH or LOW outputs**
- **Programmable $\overline{OE}$ control**
- **Positive edge-triggered clock**
- **Clock frequency: 15MHz (max.)**
- **Input loading: −100μA (max.)**
- **Power dissipation: 750mW (typ.)**
- **TTL compatible**
- **Tri-state outputs**

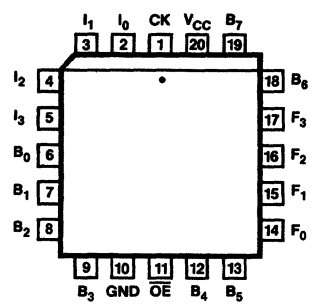
PIN CONFIGURATION

N Package



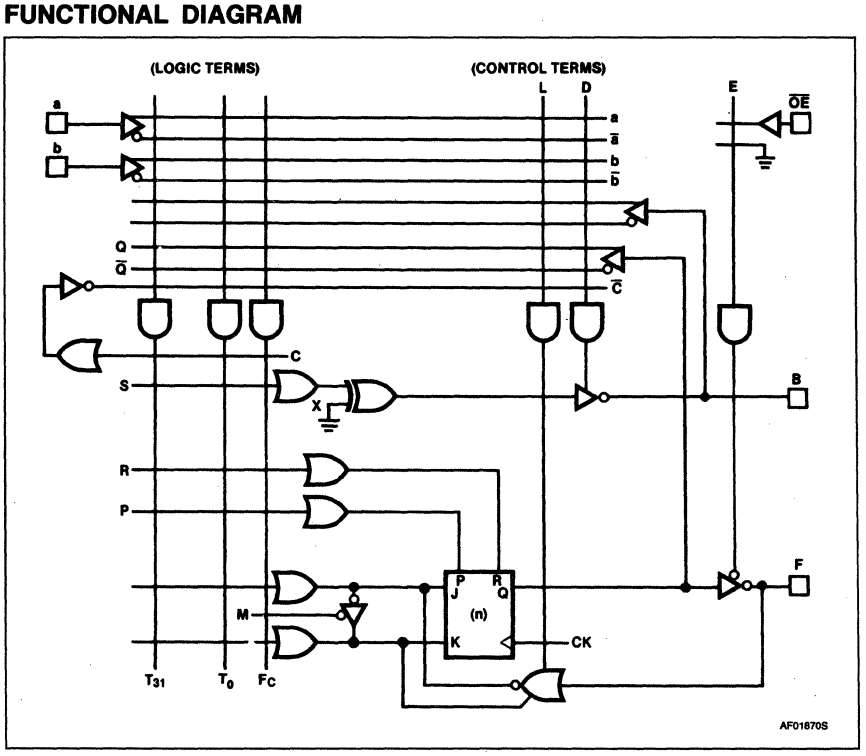
N = Plastic

A Package



A = Plastic Leaded Chip Carrier

FUNCTIONAL DIAGRAM



APPLICATIONS

- **Random sequential logic**
- **Synchronous up/down counters**
- **Shift registers**
- **Bidirectional data buffers**
- **Timing function generators**
- **System controllers/synchronizers**
- **Priority encoder/registers**

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Signetics

PLS157
Field Programmable Logic Sequencer (16 × 45 × 12)

Signetics Programmable Logic
Product Specification

Application Specific Products
- **Series 20**

DESCRIPTION

The PLS157 is a Three-State output, registered logic element combining AND/OR gate arrays with clocked J-K flip-flops. These J-K flip-flops are dynamically convertible to D-type via a "fold-back" inverting buffer and control gate F_C. It features 6 registered I/O outputs (F) in conjunction with 6 bidirectional I/O lines (B). These yield variable I/O gate and register configurations via control gates (D, L) ranging from 16 inputs to 12 outputs.

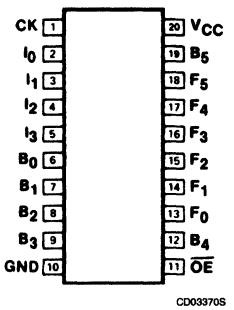
The AND/OR arrays consist of 32 logic AND gates, 13 control AND gates, and 21 OR gates with fusible link connections for programming I/O polarity and direction. All AND gates are linked to 4 inputs (I), bidirectional I/O lines (B), internal flip-flop outputs (Q), and Complement Array output ($\overline{C}$). The Complement Array consists of a NOR gate optionally linked to all AND gates for generating and propagating complementary AND terms.

FEATURES

- **Field programmable (Ni-Cr link)**
- **4 dedicated inputs**
- **13 control gates**
- **32 AND gates**
- **21 OR gates**
- **45 product terms:**
  - **32 logic terms**
  - **13 control terms**
- **6 bidirectional I/O lines**
- **6 bidirectional registers**
- **J-K, T, or D-type flip-flops**
- **Three-State Outputs**
- **Asynchronous Preset/Reset**
- **Complement Array**
- **Active HIGH or LOW outputs**
- **Programmable $\overline{OE}$ control**
- **Positive edge-triggered clock**
- **Clock frequency: 15MHz (max)**
- **Input loading: −100μA (max)**
- **Power dissipation: 750mW (typ)**
- **TTL compatible**

PIN CONFIGURATION

N PACKAGE



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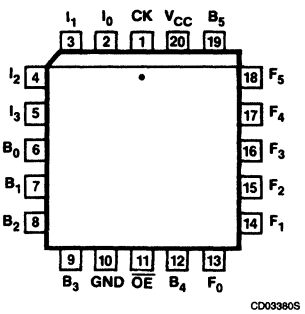
N = Plastic

A PACKAGE



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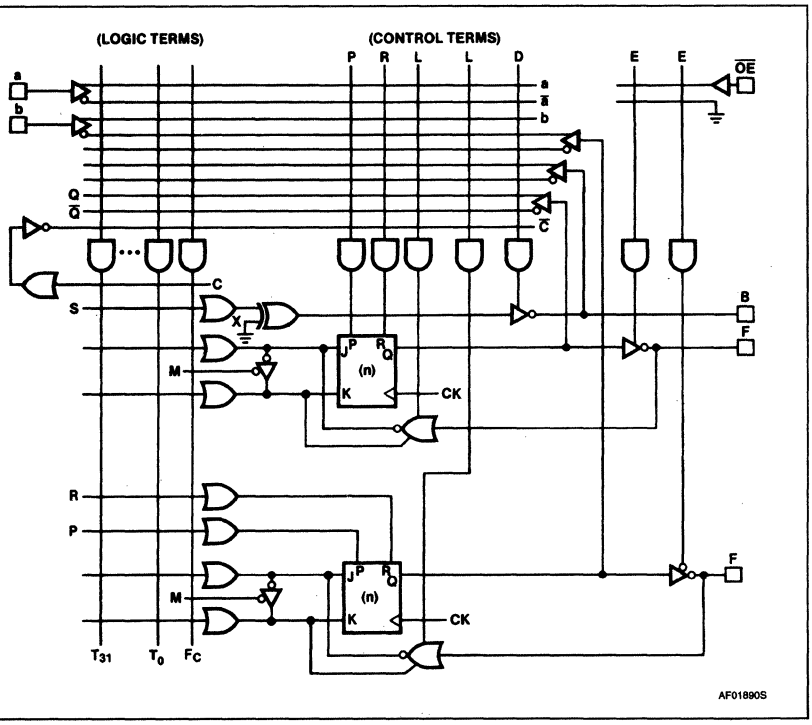
A = Plastic Leaded Chip Carrier

FUNCTION DIAGRAM



APPLICATIONS

- **Random sequential logic**
- **Synchronous up/down counters**
- **Shift registers**
- **Bidirectional data buffers**
- **Timing function generators**
- **System controllers/synchronizers**
- **Priority encoder/registers**

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Signetics

PLS159
Field Programmable Logic Sequencer (16 × 45 × 12)

Signetics Programmable Logic
Product Specification

Application Specific Products
- **Series 20**

DESCRIPTION

The PLS159 is a Three-State output, registered logic element combining AND/OR gate arrays with clocked J-K flip-flops. These J-K flip-flops are dynamically convertible to D-type via a "fold-back" inverting buffer and control gate F_C. It features 8 registered I/O outputs (F) in conjunction with 4 bidirectional I/O lines (B). These yield variable I/O gate and register configurations via control gates (D, L) ranging from 16 inputs to 12 outputs.

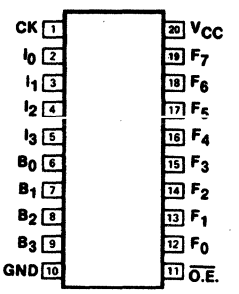
The AND/OR arrays consist of 32 logic AND gates, 13 control AND gates, and 21 OR gates with fusible link connections for programming I/O polarity and direction. All AND gates are linked to 4 inputs (I), bidirectional I/O lines (B), internal flip-flop outputs (Q), and Complement Array output ($\overline{C}$). The Complement Array consists of a NOR gate optionally linked to all AND gates for generating and propagating complementary AND terms.

FEATURES

- **Field programmable (Ni-Cr link)**
- **4 dedicated inputs**
- **13 control gates**
- **32 AND gates**
- **21 OR gates**
- **45 product terms:**
  - **32 logic terms**
  - **13 control terms**
- **4 bidirectional I/O lines**
- **8 bidirectional registers**
- **J/K, T, or D-type flip-flops**
- **Asynchronous Preset/Reset**
- **Complement Array**
- **Active high or low outputs**
- **Programmable $\overline{O.E.}$ control**
- **Positive edge trigger clock**
- **Clock frequency: 15MHz (max)**
- **Input loading: −100μA (max)**
- **Power dissipation: 750mW (typ)**
- **TTL compatible**
- **Three-State Outputs**

PIN CONFIGURATION

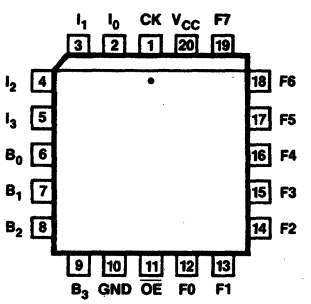
N PACKAGE



CD03350S

N = Plastic

A PACKAGE



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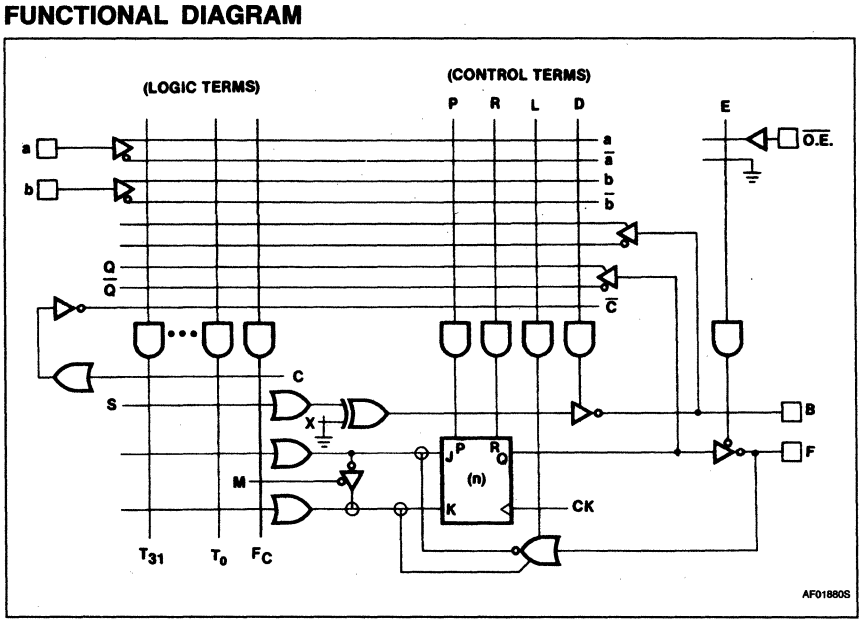
A = Plastic Leaded Chip Carrier

FUNCTIONAL DIAGRAM



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APPLICATIONS

- **Random sequential logic**
- **Synchronous up/down counters**
- **Shift registers**
- **Bidirectional data buffers**
- **Timing function generators**
- **System controllers/synchronizers**
- **Priority encoder/registers**

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Signetics

PLS159A
Field Programmable Logic Sequencer (16 × 45 × 12)

Signetics Programmable Logic
Objective Specification

Application Specific Products
- **Series 20**

DESCRIPTION

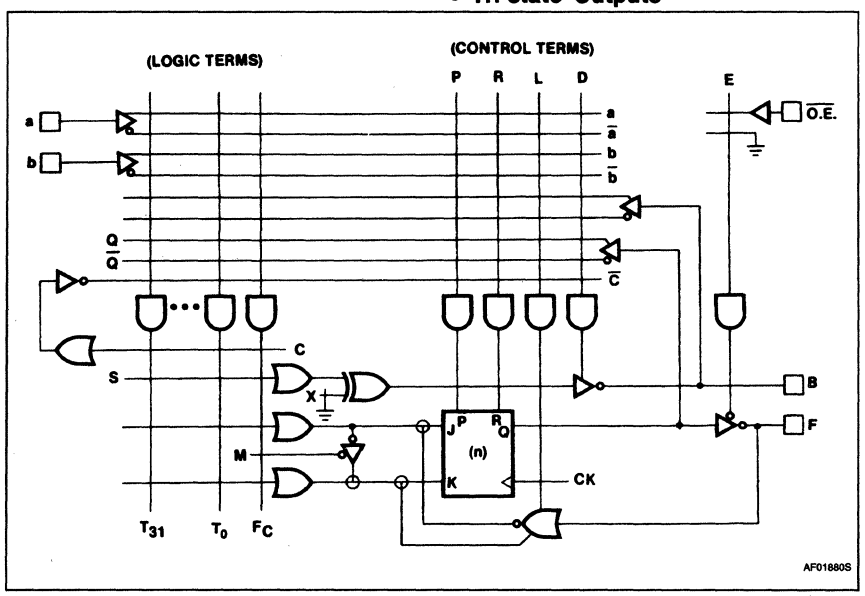
The PLS159A is a Tri-state output, registered logic element combining AND/OR gate arrays with clocked J-K flip-flops. These J-K flip-flops are dynamically convertible to D-type via a "fold-back" inverting buffer and control gate F_C. It features 8 registered I/O outputs (F) in conjunction with 4 bidirectional I/O lines (B). These yield variable I/O gate and register configurations via control gates (D, L) ranging from 16 inputs to 12 outputs.

The AND/OR arrays consist of 32 logic AND gates, 13 control AND gates, and 21 OR gates with fusible link connections for programming I/O polarity and direction. All AND gates are linked to 4 inputs (I), bidirectional I/O lines (B), internal flip-flop outputs (Q), and Complement Array output ($\overline{C}$). The Complement Array consists of a NOR gate optionally linked to all AND gates for generating and propagating complementary AND terms.

FEATURES

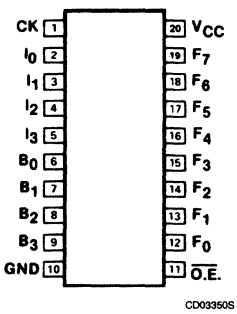
- **Field programmable (Ni-Cr link)**
- **4 dedicated inputs**
- **13 control gates**
- **32 AND gates**
- **21 OR gates**
- **45 product terms:**
  - **32 logic terms**
  - **13 control terms**
- **4 bidirectional I/O lines**
- **8 bidirectional registers**
- **J/K, T, or D-type flip-flops**
- **Power on reset feature on all flip-flops ($F_n = 1$)**
- **Asynchronous Preset/Reset**
- **Complement Array**
- **Active high or low outputs**
- **Programmable $\overline{O.E.}$ control**
- **Positive edge-trigger clock**
- **Clock frequency: 18MHz (max)**
- **Input loading: −100μA (max)**
- **Power dissipation: 725mW (typ)**
- **TTL compatible**
- **Tri-state Outputs**

FUNCTIONAL DIAGRAM



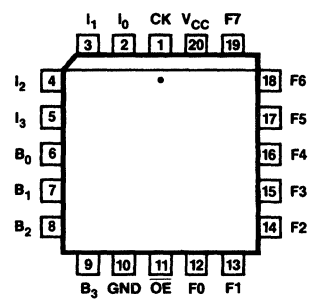
PIN CONFIGURATION

N PACKAGE



N = Plastic

A PACKAGE



A = Plastic Leaded Chip Carrier

APPLICATIONS

- **Random sequential logic**
- **Synchronous up/down counters**
- **Shift registers**
- **Bidirectional data buffers**
- **Timing function generators**
- **System controllers/synchronizers**
- **Priority encoder/registers**

Signetics

PLS167
Field Programmable Logic Sequencer (14 × 48 × 6)

Signetics Programmable Logic
Product Specification

Application Specific Products
- **Series 24**

DESCRIPTION

The PLS167 is a bipolar, programmable state machine of the Mealy type. The Field Programmable Logic Sequencer (FPLS) contains logic AND-OR gate arrays with user programmable connections which control the inputs of on-chip state and output registers. These consist respectively of 8 Q_p, and 4 Q_f edge-triggered, clocked S/R flip-flops, with an asynchronous preset option.

All flip-flops are unconditionally preset to "1" during power turn-on.

The AND Array combines 14 external inputs, $I_{0\text{-}13}$, with 8 internal inputs, $P_{0\text{-}7}$, fed back from the State Register to form up to 48 transition terms (AND terms). In addition, P_0 and P_1 of the internal state register are brought off-chip to allow extending the Output Register to 6 bits, if so desired.

All transition terms can include True, False, or Don't Care states of the controlling variables, and are merged in the OR Array to issue next-state and next-output commands to their respective registers on the Low to High transition of the Clock pulse.

Both True and Complement transition terms can be generated by optional use of the internal variable (C) from the Complement Array. Also, if desired, the Preset input can be converted to output-enable function, as an additional user programmable option.

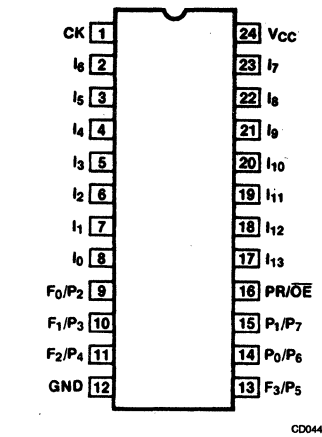
Order codes are contained on the pages following.

FEATURES

- **Field programmable (Ni-Cr link)**
- **14 True/Complement buffered inputs**
- **48 programmable AND gates**
- **25 programmable OR gates**
- **8-bit State Register**
- **2-bit shared State/Output Register**
- **4-bit Output Register**
- **Transition Complement Array**
- **Programmable asynchronous preset/output enable**
- **Positive edge-trigger clock**
- **Power-on preset to logic "1" of all registers**
- **Automatic logic "HOLD" state via S/R flip-flops**
- **On-chip Test Array**
- **$f_{(max)}$: 13.9MHz**
- **Power: 650mW (typ)**
- **TTL compatible**
- **Tri-state outputs**
- **Single +5V supply**
- **300 mil wide 24-pin DIP**

PIN CONFIGURATION

N PACKAGE



N = Plastic

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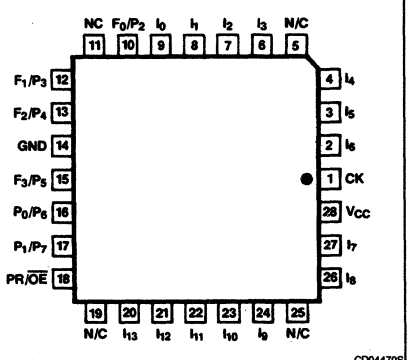
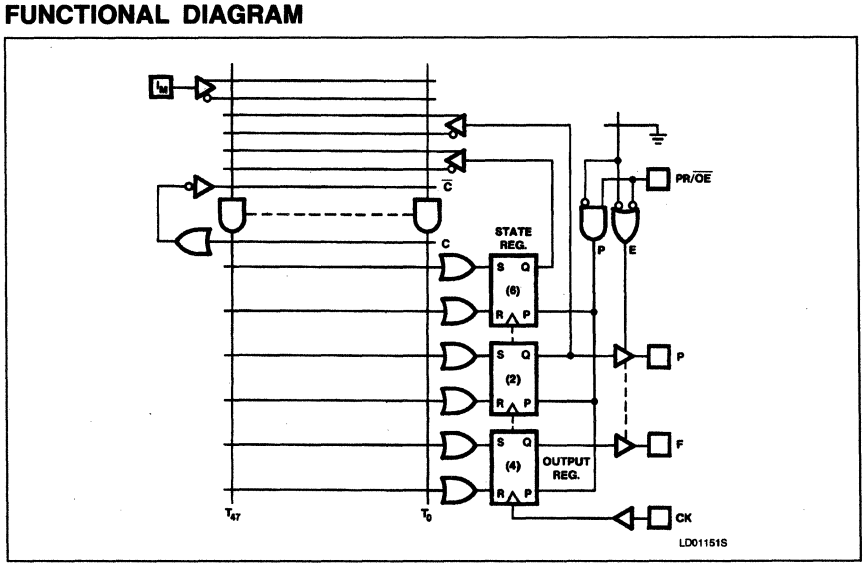


A = Plastic Leaded Chip Carrier

FUNCTIONAL DIAGRAM



APPLICATIONS

- **Interface protocols**
- **Sequence detectors**
- **Peripheral controllers**
- **Timing generators**
- **Sequential circuits**
- **Security locking systems**

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Signetics

PLS167A
Field Programmable Logic Sequencer (14 × 48 × 6)

Signetics Programmable Logic
Product Specification

Application Specific Products
- **Series 24**

DESCRIPTION

The PLS167A is a bipolar, programmable state machine of the Mealy type.The Field Programmable Logic Sequencer (FPLS) contains logic AND-OR gate arrays with user programmable connections which control the inputs of on-chip state and output registers. These consist respectively of 8 Q_p, and 4 Q_f edge-triggered, clocked S/R flip-flops, with an asynchronous preset option.

All flip-flops are unconditionally preset to "1" during power turn-on.

The AND array combines 14 external inputs, $I_{0\text{-}13}$, with 8 internal inputs, $P_{0\text{-}7}$, fed back from the State register to form up to 48 transition terms (AND terms). In addition, P_0 and P_1 of the internal state register are brought off-chip to allow extending the output register to 6 bits, if so desired.

All transition terms can include True, False, or Don't Care states of the controlling variables, and are merged in the OR array to issue next-state and next-output commands to their respective registers on the low to high transition of the Clock pulse.

Both True and Complement transition terms can be generated by optional use of the internal variable (C) from the complement array. Also, if desired, the Preset input can be converted to output-enable function, as an additional user programmable option.

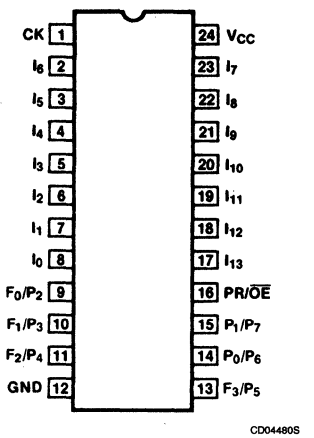
Order codes are contained on the pages following.

FEATURES

- **Field programmable (Ni-Cr link)**
- **14 True/Complement buffered inputs**
- **48 programmable AND gates**
- **25 programmable OR gates**
- **8-bit state register**
- **2-bit shared state/output register**
- **4-bit output register**
- **Transition complement array**
- **Programmable asynchronous preset/output enable**
- **Positive edge-trigger clock**
- **Power-on preset to logic "1" of all registers**
- **Automatic logic "HOLD" state via S/R flip-flops**
- **On/chip test array**
- **$f_{(max)}$: 20MHz**
- **Power: 650mW (typ)**
- **TTL compatible**
- **Tri-state outputs**
- **Single +5V supply**
- **300 mil wide 24-pin DIP**

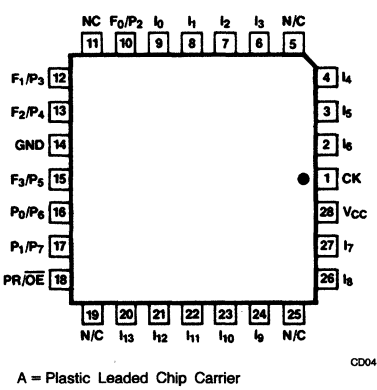
PIN CONFIGURATION

N PACKAGE



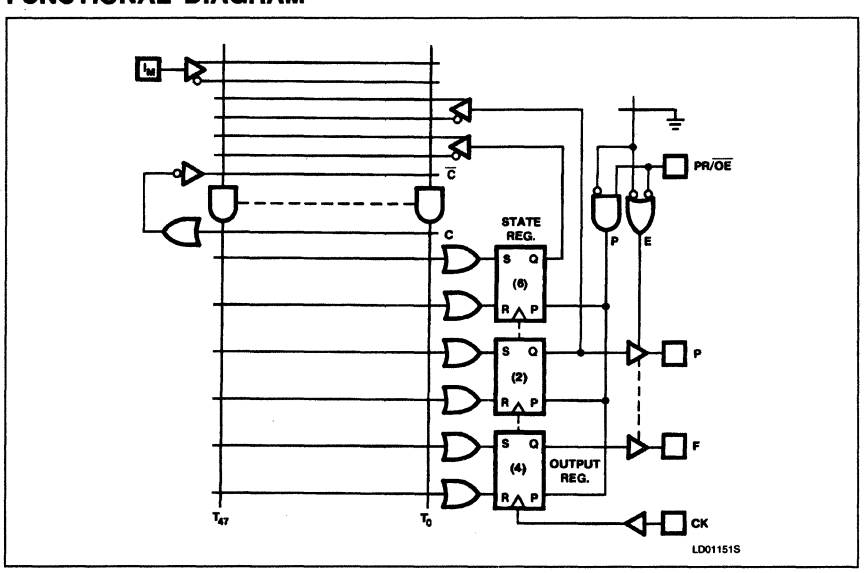
N = Plastic

A PACKAGE



A = Plastic Leaded Chip Carrier

FUNCTIONAL DIAGRAM



APPLICATIONS

- **Interface protocols**
- **Sequence detectors**
- **Peripheral controllers**
- **Timing generators**
- **Sequential circuits**
- **Security locking systems**

853-0315 80117

Signetics

Signetics

PLS168
Field Programmable Logic Sequencer (12 × 48 × 8)

Signetics Programmable Logic
Product Specification

Application Specific Products
- **Series 24**

DESCRIPTION

The PLS168 is a bipolar, programmable state machine of the Mealy type. It contains logic AND-OR gate arrays with user programmable connections which control the inputs of on-chip state and output registers. These consist respectively of 10 Q_p, and 4 Q_f edge-triggered, clocked S/R flip-flops, with an asynchronous preset option.

All flip-flops are unconditionally preset to "1" during power turn-on.

The AND array combines 12 external inputs, I_{0-11}, with 10 internal inputs, P_{0-9}, fed back from the State register to form up to 48 transition terms (AND terms). In addition, P_0-P_3 of the internal state register are brought off-chip to allow extending the output register to 8 bits, if so desired.

All transition terms can include True, False, or Don't Care states of the controlling variables, and are merged in the OR array to issue next-state and next-output commands to their respective registers on the low to high transition of the Clock pulse.

Both True and Complement transition terms can be generated by optional use of the internal variable (C) from the complement array. Also, if desired, the Preset input can be converted to output-enable function, as an additional user programmable option.

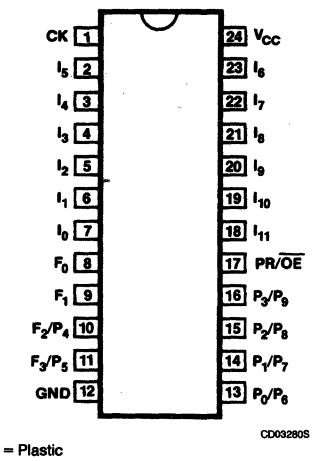
Order codes for this device are contained on the pages following.

FEATURES

- **Field programmable (Ni-Cr link)**
- **12 True/Complement buffered inputs**
- **48 programmable AND gates**
- **29 programmable OR gates**
- **10-bit state register**
- **4-bit shared state/output register**
- **4-bit output register**
- **Transition complement array**
- **Programmable asynchronous preset/output enable**
- **Positive edge-trigger clock**
- **Power-on preset to logic "1" of all registers**
- **Automatic logic "HOLD" state via S/R flip-flops**
- **On/chip test array**
- **$f_{(max)}$: 13.9MHz**
- **Power: 600mW**
- **TTL compatible**
- **Three-state outputs**
- **Single +5V supply**
- **300 mil wide 24-pin DIP**

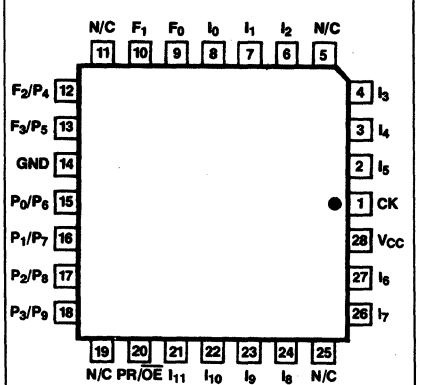
PIN CONFIGURATION

N PACKAGE



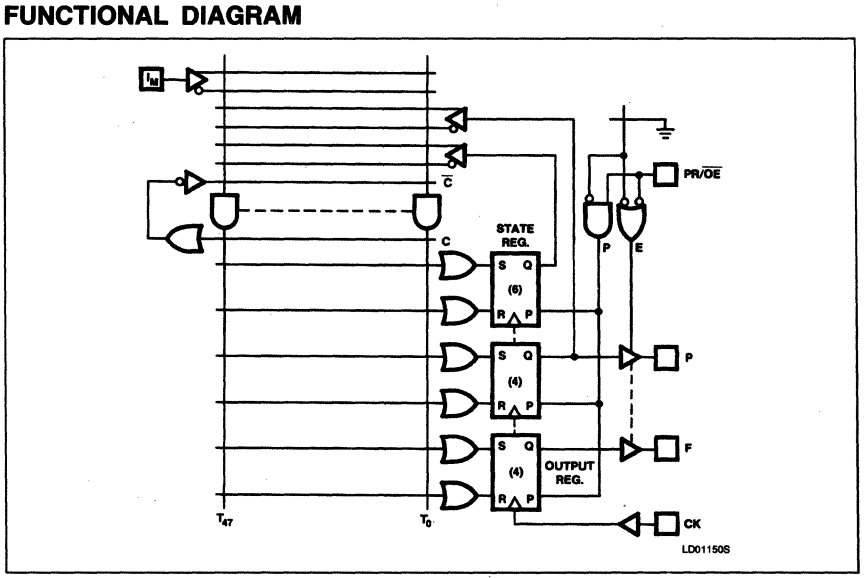
N = Plastic

A PACKAGE



A = Plastic Leaded Chip Carrier

FUNCTIONAL DIAGRAM



APPLICATIONS

- **Interface protocols**
- **Sequence detectors**
- **Peripheral controllers**
- **Timing generators**
- **Sequential circuits**
- **Elevator controllers**
- **Security locking systems**
- **Counters**
- **Shift registers**

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PLS168A
Field Programmable Logic Sequencer (12 × 48 × 8)

Signetics Programmable Logic
Product Specification

Application Specific Products
- **Series 24**

DESCRIPTION

The PLS168A is a bipolar, programmable state machine of the Mealy type. It contains logic AND-OR gate arrays with user programmable connections which control the inputs of on-chip state and output registers. These consist respectively of 10 Q_p, and 4 Q_f edge-triggered, clocked S/R flip-flops, with an asynchronous preset option.

All flip-flops are unconditionally preset to "1" during power turn-on.

The AND array combines 12 external inputs, $I_{0\text{-}11}$, with 10 internal inputs, $P_{0\text{-}9}$, fed back from the State register to form up to 48 transition terms (AND terms). In addition, P_0-P_3 of the internal state register are brought off-chip to allow extending the output register to 8 bits, if so desired.

All transition terms can include True, False, or Don't Care states of the controlling variables, and are merged in the OR array to issue next-state and next-output commands to their respective registers on the low to high transition of the Clock pulse.

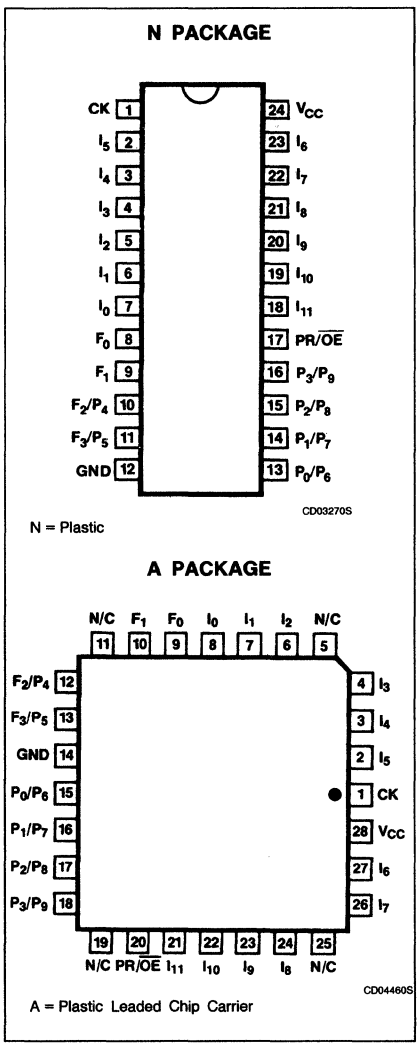
Both True and Complement transition terms can be generated by optional use of the internal variable (C) from the complement array. Also, if desired, the Preset input can be converted to output-enable function, as an additional user programmable option.

Order codes for this device are contained on the pages following.

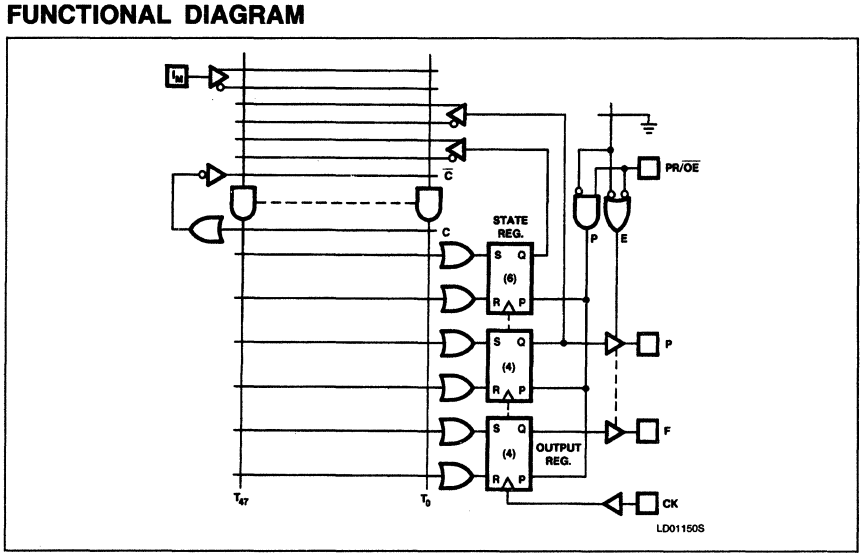
FEATURES

- **Field programmable (Ni-Cr link)**
- **12 True/Complement buffered inputs**
- **48 programmable AND gates**
- **29 programmable OR gates**
- **10-bit state register**
- **4-bit shared state/output register**
- **4-bit output register**
- **Transition complement array**
- **Programmable asynchronous preset/output enable**
- **Positive edge-trigger clock**
- **Power-on preset to logic "1" of all registers**
- **Automatic logic "HOLD" state via S/R flip-flops**
- **On/chip test array**
- **$f_{(max)}$: 20MHz**
- **Power: 600mW typ**
- **TTL compatible**
- **Three-state outputs**
- **Single +5V supply**
- **300 mil wide 24-pin DIP**

PIN CONFIGURATION



FUNCTIONAL DIAGRAM



APPLICATIONS

- **Interface protocols**
- **Sequence detectors**
- **Peripheral controllers**
- **Timing generators**
- **Sequential circuits**
- **Elevator controllers**
- **Security locking systems**
- **Counters**
- **Shift registers**

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Signetics

Signetics

PLS179
Field Programmable Logic Sequencer (20 X 45 X 12)

Signetics Programmable Logic
Product Specification

Application Specific Products
- **Series 24**

DESCRIPTION

The PLS179 is a 3-State output, registered logic element combining AND/OR gate arrays with clocked J-K flip-flops. These J-K flip-flops are dynamically convertible to D-type via a "foldback" inverting buffer and control gate F_C. It features 8 registered I/O outputs (F) in conjunction with 4 bidirectional I/O lines (B). There are 8 dedicated inputs. These yield variable I/O gate and register configurations via control gates (D, L) ranging from 20 inputs to 12 outputs.

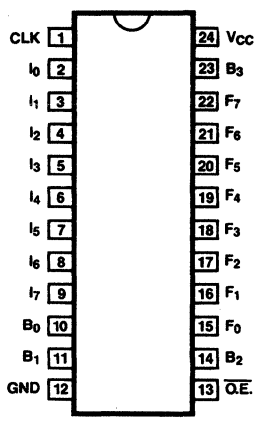
The AND/OR arrays consist of 32 logic AND gates, 13 control AND gates, and 21 OR gates with fusible link connections for programming I/O polarity and direction. All AND gates are linked to 8 inputs (I), bidirectional I/O lines (B), internal flip-flop outputs (Q), and Complement Array output ($\overline{C}$). The Complement Array consists of a NOR gate optionally linked to all AND gates for generating and propagating complementary AND terms.

FEATURES

- **Field programmable (Ni-Cr link)**
- **8 dedicated inputs**
- **13 control gates**
- **32 AND gates**
- **21 OR gates**
- **45 product terms:**
  - **32 logic terms**
  - **13 control terms**
- **4 bidirectional I/O lines**
- **8 bidirectional registers**
- **J/K, T, or D-type flip-flops**
- **Asynchronous Preset/Reset**
- **Complement Array**
- **Active high or low outputs**
- **Programmable $\overline{O.E.}$ control**
- **Positive edge trigger clock**
- **Power-on reset on flip-flop (Fn = "1")**
- **Clock frequency: PLS179: 18MHz (max)**
- **Input loading: PLS179: – 100μA (max)**
- **Power dissipation: 725mW (typ)**
- **TTL Compatible**

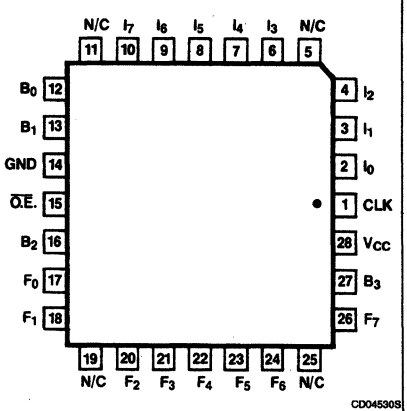
PIN CONFIGURATION

N PACKAGE



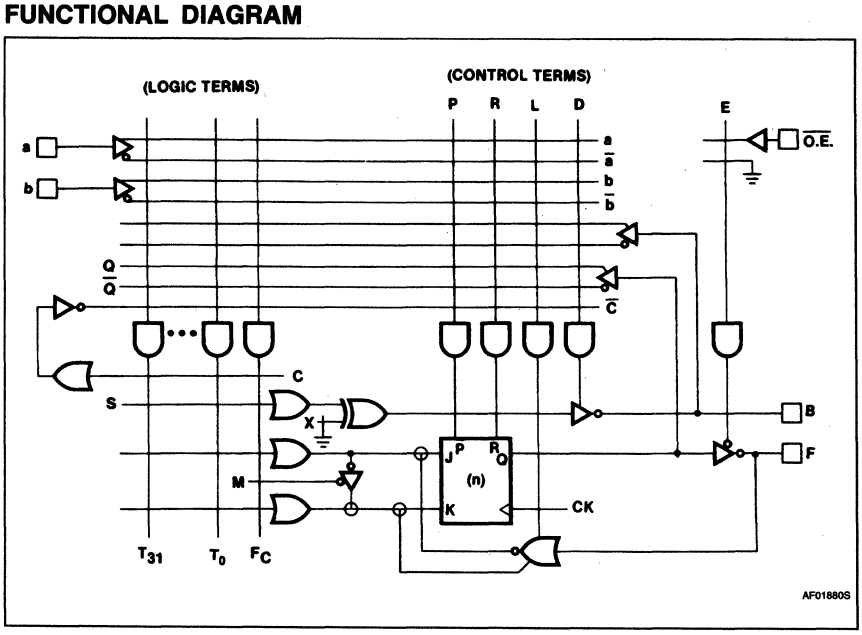
N = Plastic

A PACKAGE*



A = Plastic Leaded Chip Carrier

FUNCTIONAL DIAGRAM



APPLICATIONS

- **Random sequential logic**
- **Synchronous up/down counters**
- **Shift registers**
- **Bidirectional data buffers**
- **Timing function generators**
- **System controllers/synchronizers**
- **Priority encoder/registers**

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Signetics

PLS100/PLS101
Field Programmable Array (16 × 48 × 8)

Signetics Programmable Logic
Product Specification

Application Specific Products
- **Series 28**

DESCRIPTION

The PLS100 (Three-State) and PLS101 (Open Collector) are bipolar, fuse Programmable Logic Arrays (FPLAs). Each device utilizes the standard AND/OR/Invert architecture to directly implement custom sum of product logic equations.

Each device consists of 16 dedicated inputs and 8 dedicated outputs. Each output is capable of being actively controlled by any or all of the 48 product terms. The true, complement, or don't care condition of each of the 16 inputs ANDed together comprise one P-term. All 48 P-terms are selectively ORed to each output. The user must then only select which P-terms will activate an output by disconnecting terms which do not affect the output. In addition, each output can be fused as active HIGH (H) or active-LOW (L).

The PLS100 and PLS101 are fully TTL compatible, and include chip enable control for expansion of input variables and output inhibit. They feature either Open Collector or Three-State outputs for ease of expansion of product terms and application in bus-organized systems.

Order codes are contained on the pages following.

FEATURES

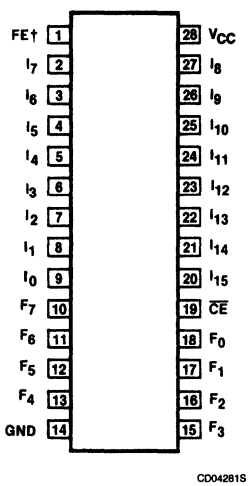
- **Field programmable (Ni-Cr link)**
- **Input variables: 16**
- **Output functions: 8**
- **Product terms: 48**
- **I/O propagation delay: 50ns max**
- **Power dissipation: 600mW typ**
- **Input loading: −100μA max**
- **Chip enable input**
- **Output option:**
  - **PLS100: Three-state**
  - **PLS101: Open Collector**
- **Output disable function:**
  - **Three-state: Hi-Z**
  - **Open Collector: Hi**
- **Separate I/O architecture**

APPLICATIONS

- **CRT display systems**
- **Code conversion**
- **Peripheral controllers**
- **Function generators**
- **Look-up and decision tables**
- **Microprogramming**
- **Address mapping**
- **Character generators**
- **Data security encoders**
- **Fault detectors**
- **Frequency synthesizers**
- **16-bit to 8-bit bus interface**
- **Random logic replacement**

PIN CONFIGURATION

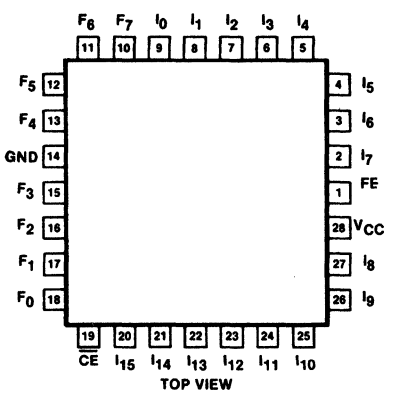
N PACKAGE



CD04281S

N = Plastic
†Open or grounded during normal operation.

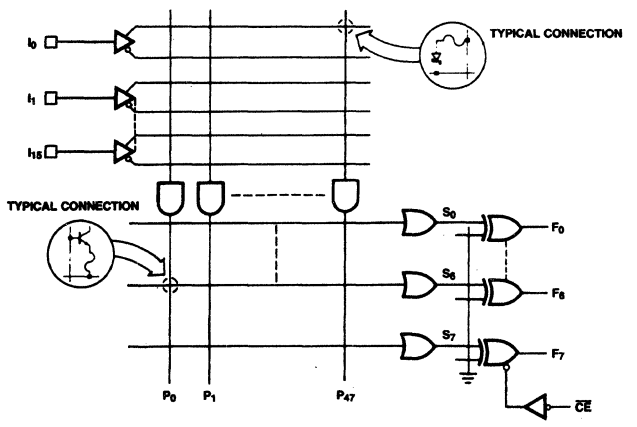
A PACKAGE



CD04271S

A = Plastic Leaded Chip Carrier

FUNCTIONAL DIAGRAM



LD01480S

Fusible Ni-Cr links are initially intact at all array cross-points.

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PLS151
Field-Programmable Gate Array (18 × 15 × 12)

Signetics Programmable Logic
Product Specification

Application Specific Products
- **Series 20**

DESCRIPTION

The PLS151 is a single level logic element, consisting of 15 AND gates with fusible link connections for programming I/O polarity, I/O direction and output enable control.

All gates are linked to 6 inputs (I) and 12 bidirectional I/O lines (B). These yield variable I/O gate configurations via 3 direction control gates (D), ranging from 18 inputs to 12 outputs.

On chip T/C buffers couple either True (I, B) or Complement ($\overline{I}$, $\overline{B}$) input polarities to each AND gate. The polarity of all gate outputs is individually programmable through a set of EX-OR gates for implementing AND/NAND logic functions. Alternately, if desired, OR/NOR logic functions can also be realized by programming for each gate the complement of its inputs and outputs (DeMorgan's Theorem).

The PLS151 is field programmable, enabling the user to quickly generate custom patterns using standard programming equipment.

Order codes are contained on the pages following.

FEATURES

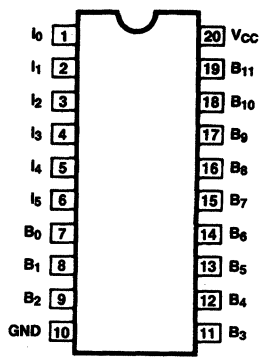
- **Field-Programmable (Ni-Cr link)**
- **6 inputs**
- **15 product terms:**
  - **12 logic terms**
  - **3 control terms**
- **12 bidirectional I/O lines**
- **Active high or low outputs**
- **Programmable output enable**
- **Power dissipation: 575mW (typ.)**
- **I/O propagation delay: 25ns (max.)**
- **Input loading: −100μA (max.)**
- **TTL compatible**
- **Tri-state outputs**

APPLICATIONS

- **Random gating functions**
- **Address decoding**
- **Code detectors**
- **Memory mapped I/O**
- **Fault monitors**
- **I/O port decoders**

PIN CONFIGURATION

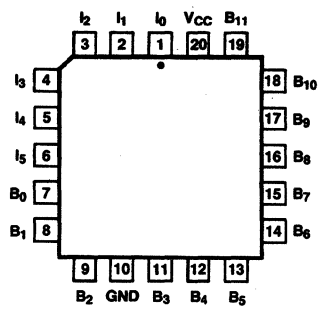
N Package



CD04540S

N = Plastic

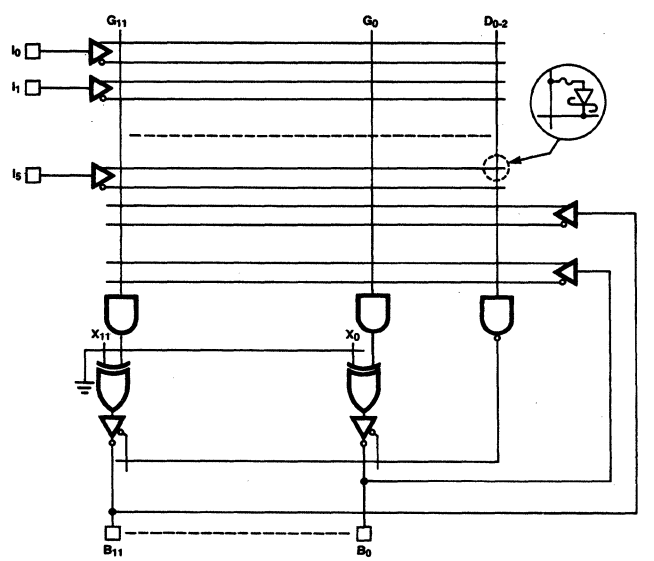
A Package



CD04550S

A = Plastic Leaded Chip Carrier

FUNCTIONAL DIAGRAM



LD01710S

All Ni-Cr links are initially intact.

LOGIC FUNCTION

TYPICAL OUTPUT FUNCTIONS:

ACTIVE-HIGH

$X = A \cdot \overline{B} \cdot C \cdot \ldots$

ACTIVE-LOW

$\overline{X} = A \cdot \overline{B} \cdot C \cdot \ldots$

$X = \overline{A} + B + \overline{C} + \ldots$

NOTES:
1. For each of the 12 outputs, either function X (Active-High) or $\overline{X}$ (Active-Low) is available, but not both. The desired output polarity is programmed via the EX-OR gates.
2. X, A, B, C, etc. are user defined connections to fixed inputs (I) and bidirectional pins (B).

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Signetics

PLS153
Field-Programmable Logic Array (18 × 42 × 10)

Signetics Programmable Logic
Product Specification

Application Specific Products
- **Series 20**

DESCRIPTION

The PLS153 is a two-level logic element, consisting of 42 AND gates and 10 OR gates with fusible link connections for programming I/O polarity and direction.

All AND gates are linked to 8 inputs (I) and 10 bidirectional I/O lines (B). These yield variable I/O gate configurations via 10 direction control gates (D), ranging from 18 inputs to 10 outputs.

On chip T/C buffers couple either True (I, B) or Complement ($\bar{I}$, $\bar{B}$) input polarities to all AND gates, whose outputs can be optionally linked to all OR gates. Their output polarity, in turn, is individually programmable through a set of EX-OR gates for implementing AND/OR or AND/NOR logic functions.

The PLS153 is field programmable, enabling the user to quickly generate custom patterns using standard programming equipment.

Order codes are contained on the pages following.

FEATURES

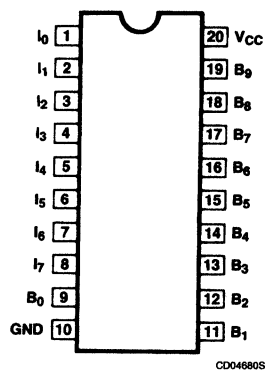
- **Field-Programmable (Ni-Cr links)**
- **8 inputs**
- **42 AND gates**
- **10 OR gates**
- **10 bidirectional I/O lines**
- **Active high or low outputs**
- **42 product terms:**
  - **32 logic terms**
  - **10 control terms**
- **I/O propagation delay: 40ns (max.)**
- **Input loading: −100μA (max.)**
- **Power dissipation: 650mW (typ.)**
- **Tri-state outputs**
- **TTL compatible**

APPLICATIONS

- **Random logic**
- **Code converters**
- **Fault detectors**
- **Function generators**
- **Address mapping**
- **Multiplexing**

PIN CONFIGURATION

N Package



N = Plastic

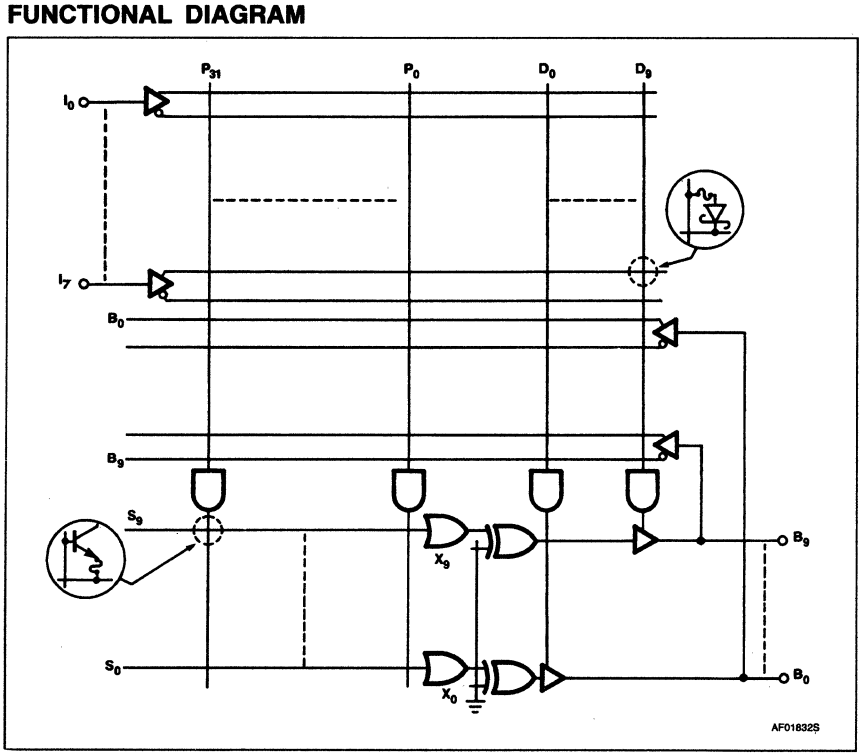
LOGIC FUNCTION

TYPICAL PRODUCT TERM:
$Pn = A \cdot B \cdot C \cdot D \cdot \ldots$
TYPICAL LOGIC FUNCTION:
AT OUTPUT POLARITY = H
$Z = P0 + P1 + P2 \ldots$

AT OUTPUT POLARITY = L
$Z = \overline{P0 + P1 + P2 + \ldots}$
$Z = \overline{P0} \cdot \overline{P1} \cdot \overline{P2} \cdot \ldots$

NOTES:
1. For each of the 10 outputs, either function Z (Active-High) or $\bar{Z}$ (Active-Low) is available, but not both. The desired output polarity is programmed via the EX-OR gates.
2. Z, A, B, C, etc. are user defined connections to fixed inputs (I) and bidirectional pins (B).

FUNCTIONAL DIAGRAM



Signetics

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Signetics

PLS162
Field Programmable Address Decoder (16 × 5)

Signetics Programmable Logic
Product Specification

Application Specific Products
- **Series 24**

DESCRIPTION

The PLS162 is a bipolar, Field Programmable Address Decoder. The device consists of five AND/NAND gates which share 16 common inputs. The type of gate is selected by programming the output as active-HIGH (H) or active-LOW (L). Each of the 16 inputs $I_0 - I_{15}$ can be programmed to provide the True (H), Complement (L), or Don't Care (—) state to each of the five AND/NAND gates. OR/NOR logic functions can also be implemented by complementing the inputs and outputs via on-chip inverting buffers.

The device is field programmable, which means that custom patterns are immediately available.

The PLS162 includes chip-enable control for output strobing and inhibit. It features Tri-State outputs for ease of expansion of input variables and application in bus-organized systems.

Order codes are contained on the following pages.

FEATURES

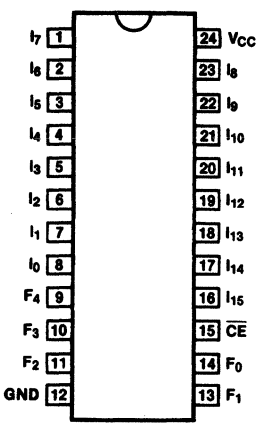
- **Field programmable (Ni-Cr link)**
- **16 input variables**
- **5 output functions**
- **Chip enable input**
- **I/O propagation delay: 30ns max**
- **Power dissipation: 500mW typ**
- **Input loading: −100μA max**
- **Output: Tri-State**
- **Output disable function: Hi-Z**
- **Fully TTL compatible**

APPLICATIONS

- **Random logic**
- **Address decoders**
- **Code detectors**
- **Peripheral selectors**
- **Fault monitors**
- **Machine state decoders**

PIN CONFIGURATION

N PACKAGE*



CD03340S

*N = Plastic

LOGIC FUNCTION

TYPICAL OUTPUT FUNCTIONS:

ACTIVE-HIGH

$X = A \cdot \overline{B} \cdot C \cdot \ldots$

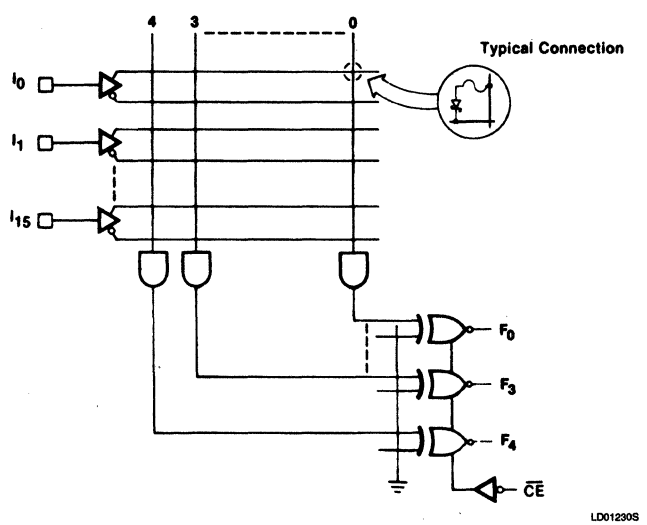
ACTIVE-LOW

$\overline{X} = A \cdot \overline{B} \cdot C \cdot \ldots$

$X = \overline{A} + B + \overline{C} + \ldots$

NOTES:
1. For each of the 5 outputs, either function X (active-high) or $\overline{X}$ (active-low) is available, but not both. The desired output polarity is programmed via the EX-OR gates.
2. X, A, B, C, etc. are user defined connections to fixed inputs (I) and output pins (F).

FUNCTIONAL DIAGRAM



LD01230S

Fusible Ni-Cr links are initially intact at all array cross-points.

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Signetics

PLS163
Field Programmable Address Decoder (12 × 9)

Signetics Programmable Logic
Product Specification

Application Specific Products
- **Series 24**

DESCRIPTION

The PLS163 is a bipolar, Field Programmable Address Decoder. The device consists of nine AND/NAND gates which share 12 common inputs. The type of gate is selected by programming the output as active-HIGH (H) or active-LOW (L). Each of the 12 inputs $I_0 - I_{11}$ can be programmed to provide the True (H), Complement (L), or Don't Care (—) state to each of the nine AND/NAND gates. OR/NOR logic functions can also be implemented by complementing the inputs and outputs via on-chip inverting buffers.

The device is field programmable, which means that custom patterns are immediately available.

The PLS163 includes chip-enable control for output strobing and inhibit. It features Tri-State outputs for ease of expansion of input variables and application in bus-organized systems.

Order codes are contained on the following pages.

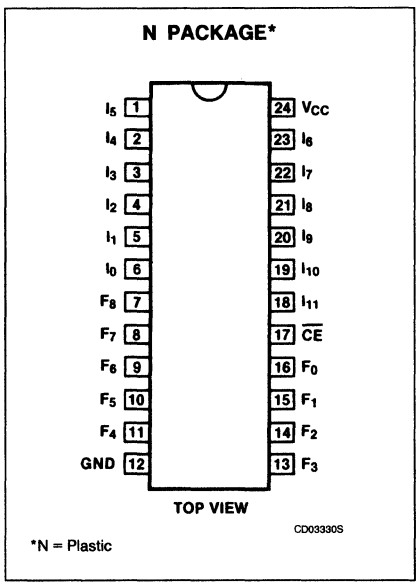
FEATURES

- **Field programmable (Ni-Cr link)**
- **12 input variables**
- **9 output functions**
- **Chip enable input**
- **I/O propagation delay: 30ns max**
- **Power dissipation: 600mW typ**
- **Input loading: −100μA max**
- **Output: Tri-State**
- **Output disable function: Hi-Z**
- **Fully TTL compatible**

APPLICATIONS

- **Random logic**
- **Address decoders**
- **Code detectors**
- **Peripheral selectors**
- **Fault monitors**
- **Machine state decoders**

PIN CONFIGURATION



*N = Plastic

LOGIC FUNCTION

TYPICAL OUTPUT FUNCTIONS:

ACTIVE-HIGH

$X = A \cdot \overline{B} \cdot C \cdot \ldots$

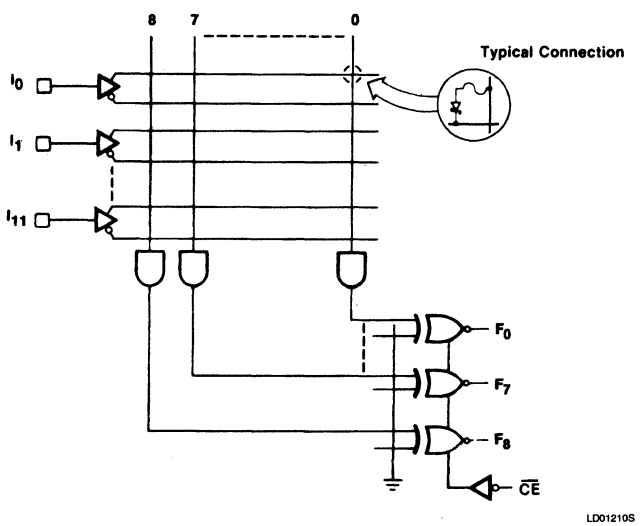
ACTIVE-LOW

$\overline{X} = A \cdot \overline{B} \cdot C \cdot \ldots$

$X = \overline{A} + B + \overline{C} + \ldots$

NOTES:
1. For each of the 9 outputs, either function X (active-high) or $\overline{X}$ (active-low) is available, but not both. The desired output polarity is programmed via the EX-OR gates.
2. X, A, B, C, etc. are user defined connections to fixed inputs (I) and output pins (F).

FUNCTIONAL DIAGRAM



Fusible Ni-Cr links are initially intact at all array cross-points.

853-0321 80118

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Signetics

PLS173
Field Programmable Logic Array (22 × 42 × 10)

Signetics Programmable Logic
Product Specification

Application Specific Products
- **Series 24**

DESCRIPTION

The PLS173 is a two-level logic element consisting of 42 AND gates and 10 OR gates with fusible link connections for programming I/O polarity and direction.

All AND gates are linked to 12 inputs (I) and 10 bidirectional I/O lines (B). These yield variable I/O gate configurations via 10 direction control gates (D), ranging from 22 inputs to 10 outputs.

On chip T/C buffers couple either True (I, B) or Complement ($\overline{I}$, $\overline{B}$) input polarities to all AND gates, whose outputs can be optionally linked to all OR gates. Their output polarity, in turn, is individually programmable through a set of EX-OR gates for implementing AND/OR or AND/NOR logic functions.

The PLS173 is field programmable, enabling the user to quickly generate custom patterns using standard programming equipment.

Order codes for this device are contained in the pages following.

FEATURES

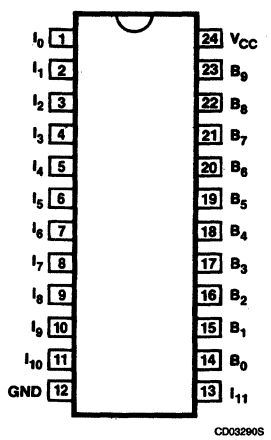
- **Field Programmable (Ni-Cr links)**
- **12 inputs**
- **42 AND gates**
- **10 OR gates**
- **10 bidirectional I/O lines**
- **Active high or low outputs**
- **42 Product Terms:**
  - **32 Logic Terms**
  - **10 Control Terms**
- **I/O propagation delay: 30 nSec (max)**
- **Input loading: −100μA max**
- **Power dissipation: 750mW typ**
- **Output: three-state**
- **TTL compatible**

APPLICATIONS

- **Random logic**
- **Code converters**
- **Fault detectors**
- **Function generators**
- **Address mapping**
- **Multiplexing**

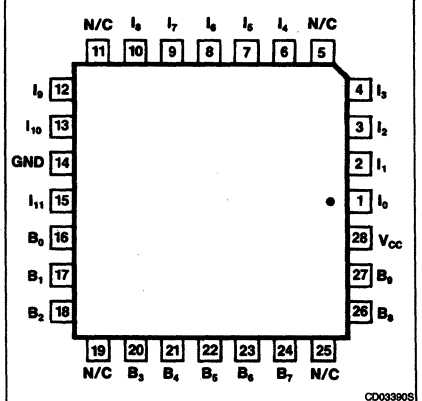
PIN CONFIGURATION

N PACKAGE



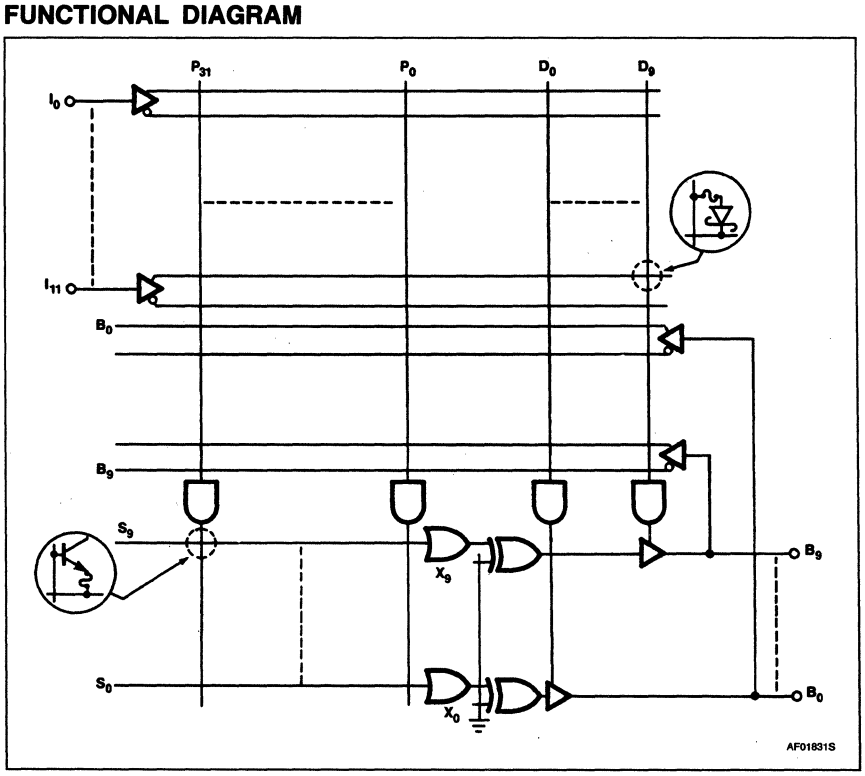
N = Plastic

A PACKAGE



A = Plastic Leaded Chip Carrier

FUNCTIONAL DIAGRAM



LOGIC FUNCTION

TYPICAL PRODUCT TERM:
$Pn = A \cdot \overline{B} \cdot C \cdot D \cdot \ldots$

TYPICAL LOGIC FUNCTION:
AT OUTPUT POLARITY = H
$Z = P0 + P1 + P2 \ldots$

AT OUTPUT POLARITY = L
$Z = \overline{P0 + P1 + P2 + \ldots}$
$Z = \overline{P0} \cdot \overline{P1} \cdot \overline{P2} \cdot \ldots$

NOTES:
1. For each of the 10 outputs, either function Z (active-high) or $\overline{Z}$ (active-low) is available, but not both. The desired output polarity is programmed via the EX-OR gates.
2. Z, A, B, C, etc. are user defined connections to fixed inputs (I) and bidirectional pins (B).

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Signetics

PLHS18P8
Programmable AND Array Logic (18 × 72 × 8)

Signetics Programmable Logic
Product Specification

Application Specific Products
- **Series 20**

DESCRIPTION

The PLHS18P8 is a two-level logic element consisting of 72 AND gates and 8 OR gates with fusible connections for programming I/O polarity and direction.

All AND gates are linked to 10 inputs (I) and 8 bidirectional I/O lines (B). These yield variable I/O gate configurations via 8 direction control gates, ranging from 18 inputs to 8 outputs.

On-chip T/C buffers couple either True (I, B) or Complement ($\bar{I}$, $\bar{B}$) input polarities to all AND gates. The 72 AND gates are separated into 8 groups of 9 each. Each group of 9 is associated with one bidirectional pin. In each group, eight of the AND terms are ORed together, while the ninth is used to establish I/O direction. All outputs are individually programmable via an EX-OR gate to allow implementation of AND/OR or NAND/NOR logic functions.

In the virgin state, the AND array fuses are back-to-back CB-EB diode pairs which will act as open connections. Current is avalanched across individual diode pairs during fusing, which essentially short circuits the EB diode and provides the connection for the associated product term.

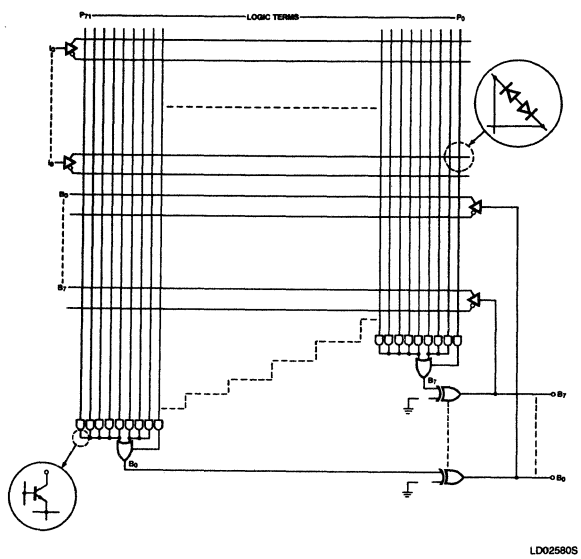
The PLHS18P8 is field-programmable, allowing the user to quickly generate custom pattern using standard programming equipment.

Order codes are contained in the pages following.

FEATURES

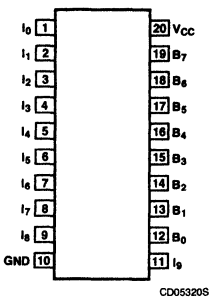
- **100% functionally compatible with AmPAL18P8**
- **Field-programmable**
- **10 inputs**
- **8 bidirectional I/O lines**
- **72 AND gates/product terms**
  - **configured into eight groups of nine**
- **Programmable output polarity (Tri-state output)**
- **I/O propagation delay: 15ns (max)**
- **Power dissipation: 750mW (nominal)**
- **TTL compatible**
- **Verify Lock Fuse**
- **On-chip test features for extensive AC and DC parametric testing**

FUNCTIONAL DIAGRAM



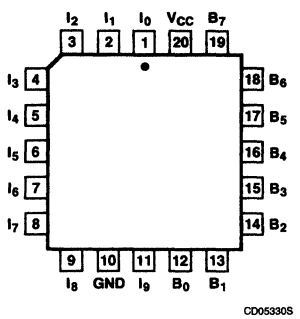
PIN CONFIGURATION

N PACKAGE



N = Plastic

A PACKAGE



A = Plastic Leader Chip Carrier

LOGIC FUNCTION

TYPICAL PRODUCT TERM:
$Pn = A \cdot \bar{B} \cdot C \cdot D \cdot \ldots$

TYPICAL LOGIC FUNCTION:

AT OUTPUT POLARITY = H
$Z = P0 + P1 + P2 \ldots$

AT OUTPUT POLARITY = L
$Z = \overline{P0 + P1 + P2 + \ldots}$
$Z = \overline{P0} \cdot \overline{P1} \cdot \overline{P2} \cdot \ldots$

NOTES:
1. For each of the 8 outputs, either function Z (active-high) or $\bar{Z}$ (active-low) is available, but not both. The desired output polarity is programmed via the EX-OR gates.
2. Z, A, B, C, etc. are user defined connections to fixed inputs (I) and bidirectional pins (B).

APPLICATIONS

- **100% functional replacement for all 20-pin combinatorial PALs***
- **Random logic**
- **Code converters**
- **Fault detectors**
- **Function generators**
- **Address mapping**

*PAL is a registered trademark of Monolithic Memories, Inc.

853-0683 84172

Signetics

Signetics

PLUS405A
Field Programmable Logic Sequencer (16 X 64 X 8)

Signetics Programmable Logic
Preliminary Specification

Application Specific Products
- **Series 28**

DESCRIPTION

The PLUS405A is a bipolar, programmable state machine of the Mealy type. Both the AND and the OR array are user programmable. All 64 AND gates are connected to the 16 external dedicated inputs ($I_0 - I_{15}$) and to the feedback paths of the 8 on-chip state registers ($Q_{P0} - Q_{P7}$). Both true and complement transition terms can be generated via optional use of the two internal Complement Arrays (input variables C_0, C_1).

All transition terms can include True, False and Don't Care states of the controlling state variables. All AND gates are merged into the programmable OR array to issue the next-state and next-output commands to their respective registers. Because the OR array is programmable, any one or all of the 64 transition terms can be connected to any or all of the state and output registers.

All state ($Q_{P0 - P7}$) and output ($Q_{F0 - F7}$) registers are edge triggered, clocked J-K/S-R flip-flops, with asynchronous preset and reset options. The PLUS405A architecture provides the added flexibility of the J-K toggle function which is not allowed in the S-R mode. All 16 flip-flops may be individually programmed for operation in either the J-K or S-R configuration. Each register may be individually programmed such that a specific Preset-Reset pattern is initialized when the initialization pin is raised to a logic level "I". (Note: Upon power-up, all registers are unconditionally preset to "I"). If desired, the initialization input pin (INIT) can be converted to an Output Enable ($\overline{OE}$) function as an additional user programmable feature.

Availability of two user programmable clocks allows the user to design an independently clocked, buried state machine.

Order codes are contained on the pages following.

FEATURES

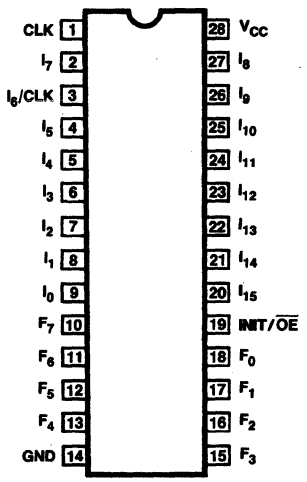
- **Field programmable (Ni-Cr link)**
- **16 input variables**
- **8 output functions**
- **64 transition terms**
- **8-bit State Register**
- **8-bit Output Register**
- **2 Transition complement array term**
- **Multiple clocks**
- **Programmable asynchronous Preset/Reset or Output Enable**
- **Power-on preset to "1" of registers**
- **f_{MAX} = 40MHz**
- **1000mW power dissipation (typical)**
- **TTL compatible**
- **J-K or S-R flip-flop functions**
- **Tri-state outputs**
- **Functional superset of PLS105/105A**

APPLICATIONS

- **Interface protocols**
- **Sequence detectors**
- **Peripheral controllers**
- **Timing generators**
- **Sequential circuits**
- **Elevator controllers**
- **Security locking systems**
- **Counters**
- **Shift registers**

PIN CONFIGURATION

N Package

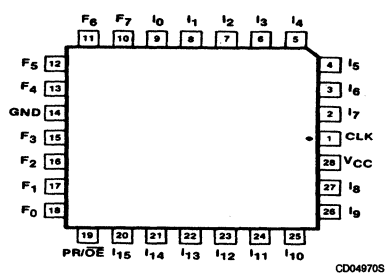


TOP VIEW

CD11461S

NOTE:
N = Plastic

A Package

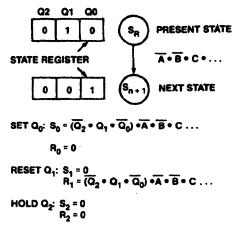


CD04970S

NOTE:
A = Plastic Leaded Chip Carrier

LOGIC FUNCTION

Typical State Transition:



TB00900S

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Signetics

PLHS473
Field Programmable Logic Array (20 × 24 × 11)

Signetics Programmable Logic
Preliminary Specification

Application Specific Products
- **Series 24**

DESCRIPTION

The PLHS473 is a two level logic device consisting of 24 AND gates and 22 OR gates with fusible link connections for programming I/O polarity and direction. The Signetics state of the art Oxide Isolated Bipolar process is used to produce performance not yet achieved in devices of this complexity.

All AND gates are linked to 11 input pins, 9 bidirectional I/O pins, and 2 dedicated output pins. The bidirectional pins are controlled via the OR array. Using these features, the PLHS473 can be configured with up to 20 inputs and as many as 11 outputs.

On chip True/Complement buffers couple either the true or complement of all inputs ($I_0 - I_{10}$)) and bidirectional pins ($B_0 - B_8$) to all AND gates. All 24 AND gates may be optionally linked to any OR gate feeding a bidirectional pin or output pin ($O_A - O_B$). The output polarity is controlled by using the fuse option on the EX-OR gates found on all bidirectional and output pins. This makes the implementation of AND/OR and AND/NOR functions possible.

The PLHS473 contains two new features of significance. A code verification lock has been incorporated to improve user security. The addition of three test columns and one test row enables the user to test the device in an unprogrammed state.

The PLHS473 is field programmable using Vertical Avalanche Migration Programmed (VAMP)™ fuses to program the cells. This enables the generation of custom logic patterns using standard programming equipment.

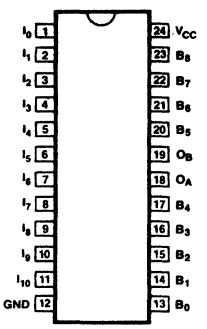
Order codes for this device are contained in the pages following.

FEATURES

- **Field programmable**
- **11 dedicated inputs**
- **2 dedicated outputs**
- **9 bi-directional I/O lines**
- **24 Product Terms**
- **22 OR gates**
- **I/O direction decoded in OR array**
- **Output enable decoded in OR array**
- **I/O propagation delay: 20nSec (max)**
- **Input loading: −100μA (max)**
- **Power dissipation: 700mW (typ)**
- **Security fuse**
- **Testable in unprogrammed state**
- **Output: Programmable as Tri-State or Open Collector.**
- **TTL compatible**

PIN CONFIGURATION

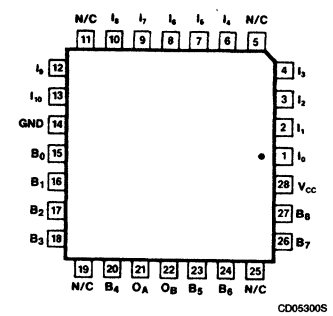
N PACKAGE



CD05290S

N = Plastic

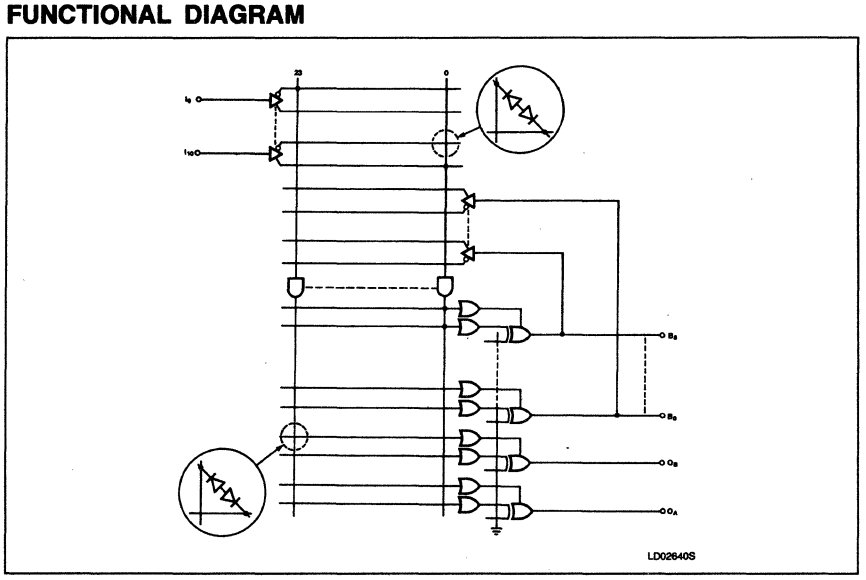
A PACKAGE



CD05300S

A = Plastic Leaded Chip Carrier

FUNCTIONAL DIAGRAM



LD02640S

LOGIC FUNCTION

TYPICAL PRODUCT TERM:
$Pn = A \cdot \overline{B} \cdot C \cdot D \cdot \ldots$

TYPICAL LOGIC FUNCTION:
AT OUTPUT POLARITY = H
$Z = P0 + P1 + P2 \ldots$

AT OUTPUT POLARITY = L
$Z = \overline{P0 + P1 + P2 + \ldots}$
$Z = \overline{P0} \cdot \overline{P1} \cdot \overline{P2} \cdot \ldots$

NOTES:
1. For each of the 11 outputs, either function Z (active-high) or $\overline{Z}$ (active-low) is available, but not both. The desired output polarity is programmed via the EX-OR gates.
2. Z, A, B, C, etc. are user defined connections to fixed inputs (I), fixed output pins (0) and bidirectional pins (B).

APPLICATIONS

- **Random logic**
- **Code converters**
- **Fault detectors**
- **Function generators**

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Selection Guide

Bipolar Memory Products

DEVICE[5]	ORGANIZATION	OUTPUT CIRCUIT[1]	OUTPUT LOGIC[2]	ACCESS TIME[3]	PACKAGE[4]	PINS	MAX I_{CC}
RAMs							
82S25	16 × 4	OC	B	50	N	16	105
3101A	16 × 4	OC	B	35	N	16	105
74S189	16 × 4	TS	B	35	N	16	110
74F189A	16 × 4	TS	—	20	N, A	16, 20	55
82S16	256 × 1	TS	T	50	N	16	115
74S301	256 × 1	OC	B	50	N	16	130
82LS16	256 × 1	TS	T	40	N	16	70
74LS301	256 × 1	OC	B	40	N	16	70
82S09	64 × 9	OC	T	45	A, N	28	190
82S09A	64 × 9	OC	T	35	A, N	28	190
82S19	64 × 9	OC	B	35	N	28	190
82S212	256 × 9	TS	B	45	N	22	185
82S212A	256 × 9	TS	B	35	N	22	185
8X350	256 × 8	TS	B	N/A	N	22	185
PROMs							
82S23	32 × 8	OC	—	50	N, A	16, 20	96
82S23A	32 × 8	OC	—	25	N, A	16, 20	96
82US23[6]	32 × 8	OC	—	10	N, A	16, 20	115
82S123	32 × 8	TS	—	50	N, A	16, 20	96
82S123A	32 × 8	TS	—	25	N, A	16, 20	96
82US123[6]	32 × 8	TS	—	10	N, A	16, 20	115
82S126	256 × 4	OC	—	50	N, A	16, 20	120
82S126A	256 × 4	OC	—	30	N, A	16, 20	120
82S129	256 × 4	TS	—	50	N, A	16, 20	120
82S129A	256 × 4	TS	—	27	N, A	16, 20	120
10149	256 × 4	OE	—	20	F	16	150
10149A	256 × 4	OE	—	10	F	16	160
100149	256 × 4	OE	—	20	F	16	150
100149A	256 × 4	OE	—	10	F	16	160
82S130	512 × 4	OC	—	50	N, A	16, 20	140
82S130A	512 × 4	OC	—	33	N, A	16, 20	140
82S131	512 × 4	TS	—	50	N, A	16, 20	140
82S131A	512 × 4	TS	—	30	N, A	16, 20	140
82LS135	256 × 8	TS	—	100	A, N	20	100
82S135	256 × 8	TS	—	45	A, N	20	150
82S115	512 × 8	TS	—	60	N	24	175
82S137	1024 × 4	TS	—	60	N, A	18, 20	140
82S137A	1024 × 4	TS	—	45	N, A	18, 20	140
82S137B	1024 × 4	TS	—	35	N, A	18, 20	140
82S137C[6]	1024 × 4	TS	—	25	N, A	18, 20	140
82S147	512 × 8	TS	—	60	A, N	20	155
82S147A	512 × 8	TS	—	45	A, N	20	155
82S147B[6]	512 × 8	TS	—	25	N, A	20	155
82LS181	1024 × 8	TS	—	120	A, N	24	80
82S181	1024 × 8	TS	—	70	N	24	175
82S181A	1024 × 8	TS	—	55	N, A	24, 28	175
82S181C	1024 × 8	TS	—	35	N, N3, A	24, 28	175
82S183	1024 × 8	TS	—	60	N, A	24, 28	175
82S185	2048 × 4	TS	—	100	N	18	120

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Selection Guide

DEVICE[5]	ORGANIZATION	OUTPUT CIRCUIT[1]	OUTPUT LOGIC[2]	ACCESS TIME[3]	PACKAGE[4]	PINS	MAX I_{CC}
PROMs							
82S185A	2048 × 4	TS	—	50	N	18	155
82S185C[6]	2048 × 4	TS	—	25	N, A	18, 20	155
82HS187	1024 × 8	TS	R	55	N, A	24, 28	175
82HS187A	1024 × 8	TS	R	45	N, A	24, 28	175
82HS189	1024 × 8	TS	R	55	N, A	24, 28	175
82HS189A	1024 × 8	TS	R	45	N, A	24, 28	175
82HS191	2048 × 8	TS	—	20	N, N3, A	24, 28	175
82S191	2048 × 8	TS	—	80	N, A	24, 28	175
82S191A	2048 × 8	TS	—	55	N, A	24, 28	175
82S191C	2048 × 8	TS	—	35	A, N, N3	24	175
82HS195	4096 × 4	TS	—	45	N	20	145
82HS195A	4096 × 4	TS	—	35	N	20	145
82HS195B	4096 × 4	TS	—	25	N	20	145
82HS197[6]	2048 × 8	TS	R	65	N	24	175
82HS199[6]	2048 × 8	TS	R	65	N	24	175
82HS321	4096 × 8	TS	—	45	N, A	24, 28	175
82HS321A	4096 × 8	TS	—	35	N, A	24, 28	175
82HS321B	4096 × 8	TS	—	30	N, A	24, 28	175
82HS641	8192 × 8	TS	—	55	N	24, 28	175
82HS641A	8192 × 8	TS	—	45	N	24, 28	175
82HS641B	8192 × 8	TS	—	35	N	24, 28	175
82HS1281[6]	16384 × 8	TS	—	45	N	24	185

NOTES:

1. Output circuit
   OE = Open Emitter
   OC = Open Collector
   TS = 3-State
2. Output logic
   T = Transparent — input data appears on output during Write
   B = Blanked — output is blanked during Write
   R = Registers
   I/O = Programmable input/output option
3. Commercial (0°C to +75°C)
4. Packages:
   N = Plastic Dual In Line (N3 = 300mil-wide)*
   A = Plastic Square Leaded Chip Carrier
   D = Small Outline Large (SO-L)
   *Whenever a single device is offered in both 300mil-wide and 600mil-wide packages, designate either N3 (300mil) or N (600mil) to assure proper order entry and shipment.
5. Part numbers:
   82Sxxx Junction-Isolated
   82HSxxx Oxide-Isolated
   82USxxx Oxide-Isolated TiW fuse
6. Objective specification (under product development)

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Signetics

82HS187
82HS187A
8K-Bit TTL Bipolar PROM

Product Specification

Bipolar Memory Products

Signetics

DESCRIPTION

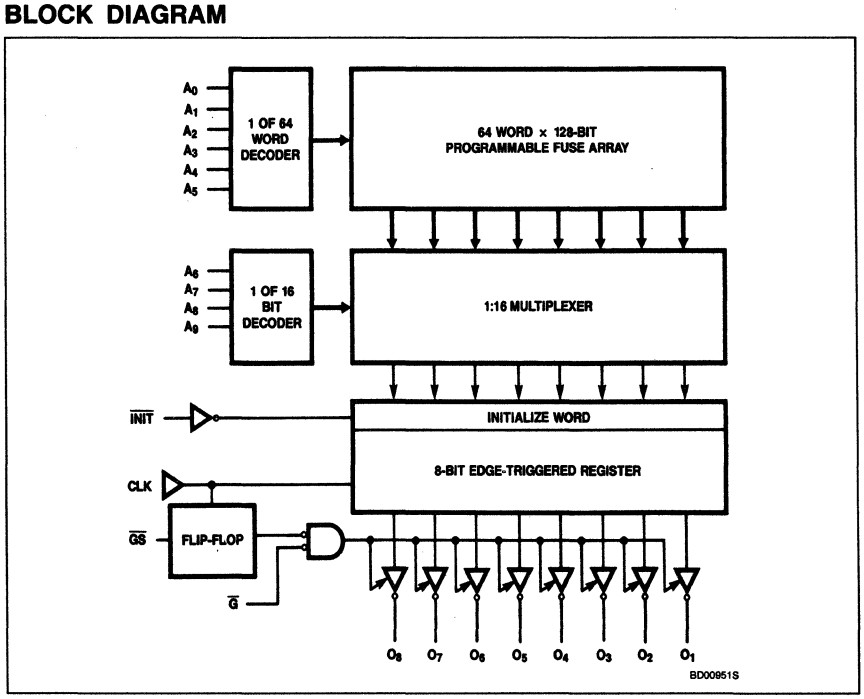
The 82HS187 is a programmable read only memory containing D-type, master-slave data registers. The 82HS187 contains 1024 words of 8 bits each. The unprogrammed state is with all outputs at a High level and can be selectively programmed to a Low level by following the Signetics Generic II programming method. The output structure is Three-state for ease in connection to bus-organized systems. The combination of on-chip registers and Three-state outputs will substantially reduce cost and size of pipelined microprogrammed systems and other designs where accessed PROM data is temporarily stored in a register.

All outputs will go into the third state or Hi-Z condition whenever the asynchronous chip enable ($\overline{G}$) is High. The outputs are enabled when ($\overline{GS}$) is brought Low before the rising edge of the clock and ($\overline{G}$) is held Low. The ($\overline{GS}$) flip-flop is designed to power-up in the third state or Hi-Z condition with the application of V_{CC}.

The 82HS187 also features an initialize function, $\overline{INIT}$. The initialize function provides the user with an extra word of programmable memory which is accessed with single-pin control by applying a Low on $\overline{INIT}$. The initialize function is asynchronous and is loaded into the output register and will appear at the outputs upon an application of a Low on $\overline{INIT}$ if the outputs are enabled, and will control the state of the data registers independent of all other inputs. The unprogrammed state of $\overline{INIT}$ is all ones.

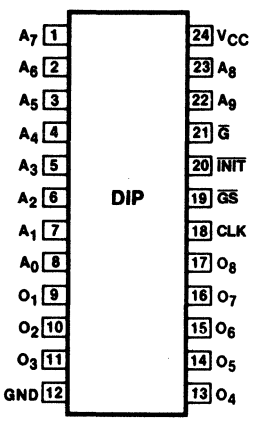
Data is read from the PROM by first applying an address to inputs A_0 to A_9. During the setup time the output of the array is loaded into the master flip-flop of the data register. During the rising edge (Low-to-High transition) of the clock, the data is transferred to the slave of the flip-flop and will appear on the output if the output is enabled. Following the rising edge clock transition, the addresses and synchronous chip enable can be removed and the output data will remain stable.

BLOCK DIAGRAM



PIN CONFIGURATION

N PACKAGE



TOP VIEW

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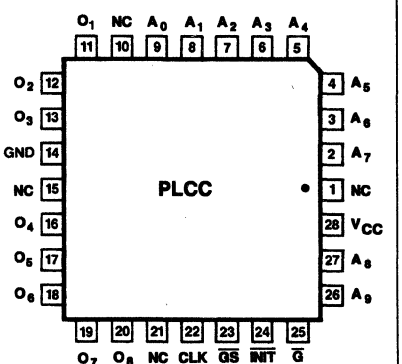

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FEATURES

- **On-chip edge-triggered registers**
- **Programmable register with asynchronous Initialize function**
- **24-pin 300mil-wide DIP package**
- **Read cycle "Address setup plus clock to output delay"**
  - **N82HS187: 55ns max**
  - **N82HS187A: 45ns max**
- **Outputs: Three-state**
- **Unprogrammed outputs are High level**
- **Synchronous and asynchronous enables for word expansion**

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Signetics

82HS189
82HS189A
8K-Bit TTL Bipolar PROM

Product Specification

Bipolar Memory Products

DESCRIPTION

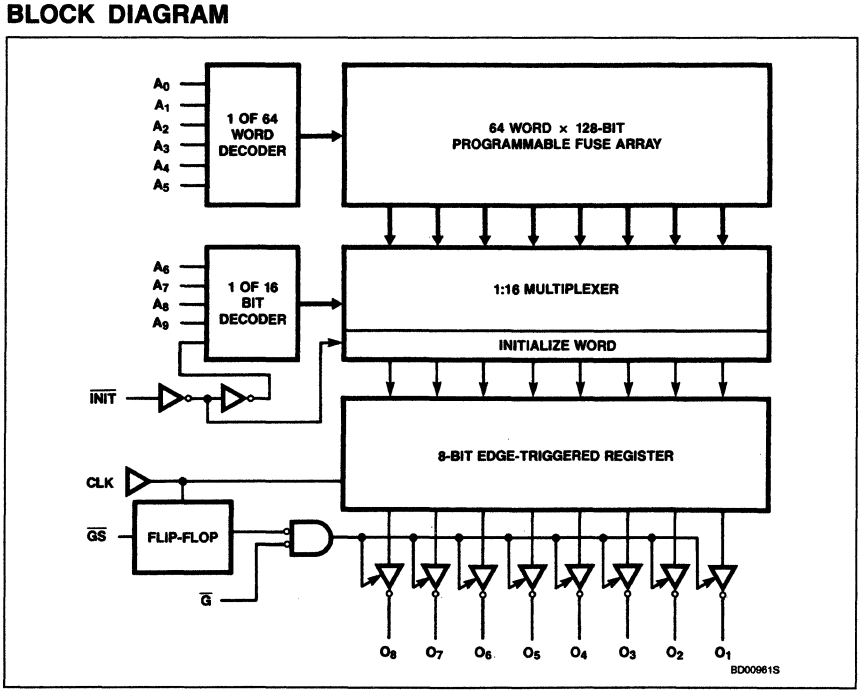
The 82HS189 is a programmable read only memory containing D-type, master-slave data registers. The 82HS189 contains 1024 words of 8 bits each. The unprogrammed state is with all outputs at a High level and can be selectively programmed to a Low level by following the Signetics Generic II programming method. The output structure is Three-state for ease in connection to bus-organized systems. The combination of on-chip registers and Three-state outputs will substantially reduce cost and size of pipelined microprogrammed systems and other designs where accessed PROM data is temporarily stored in a register.

All outputs will go into the third state or Hi-Z condition if the asynchronous chip enable ($\overline{G}$) is held High. The outputs are enabled when ($\overline{GS}$) is brought Low before the rising edge of the clock and ($\overline{G}$) is held Low. The ($\overline{GS}$) flip-flop is designed to power-up in the third state or Hi-Z condition with the application of V_{CC}.

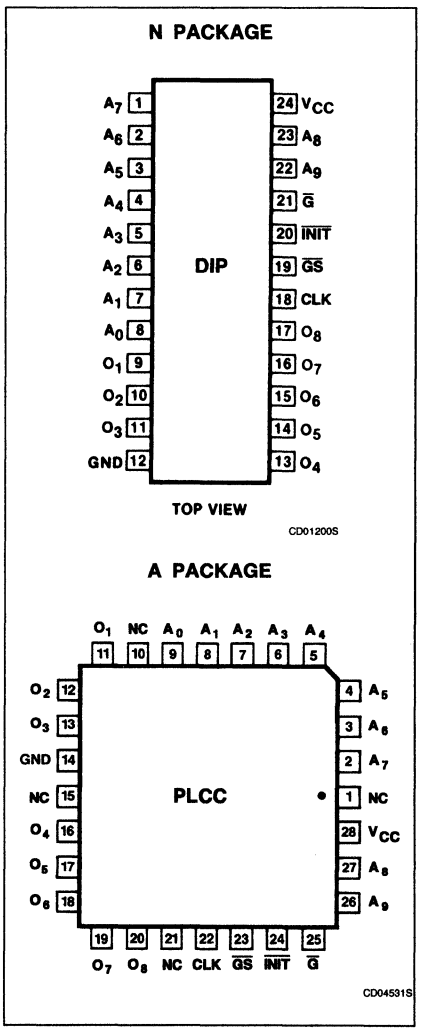
The 82HS189 also features an initialize function, $\overline{INIT}$. The initialize function provides the user with an extra word of programmable memory which is accessed with single-pin control by applying a Low on $\overline{INIT}$. The initialize function is synchronous and is loaded into the output register on the next rising edge of the clock. The unprogrammed state of $\overline{INIT}$ is all ones.

Data is read from the PROM by first applying an address to inputs A_0 to A_9. During the setup time the output of the array is loaded into the master flip-flop of the data register. During the rising edge (Low-to-High transition) of the clock, the data is transferred to the slave of the flip-flop and will appear on the output if the output is enabled. Following the rising edge clock transition, the addresses and synchronous chip enable can be removed and the output data will remain stable.

BLOCK DIAGRAM



PIN CONFIGURATION



FEATURES

- **On-chip edge-triggered registers**
- **Asynchronous and synchronous enables for word expansion**
- **Programmable register with synchronous initialize function**
- **24-pin 300mil package**
- **Read cycle "Address Setup plus Clock to Output Delay"**
  - **N82HS189: 55ns max**
  - **N82HS189A: 45ns max**
- **Unprogrammed outputs are High level**
- **Outputs: Three-state**

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Signetics

Signetics

82HS321
82HS321A
82HS321B
32K-Bit TTL Bipolar PROM

Bipolar Memory Products

Product Specification

DESCRIPTION

The 82HS321 is field programmable, which means that custom patterns are immediately available by following the Signetics Generic II fusing procedure. The 82HS321 is supplied with all outputs at a logical High. Outputs are programmed to a logic Low level at any specified address by fusing a programmable matrix.

This device includes on-chip decoding and 2 chip enable inputs for ease of memory expansion. It features Three-state outputs for optimization of word expansion in bused organizations.

Ordering information can be found on the following page.

This device is also processed to military requirements for operation over the military temperature range. For specifications and ordering information consult the Signetics Military Data Book.

FEATURES

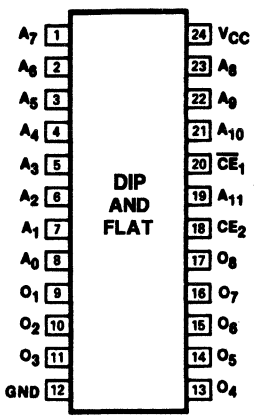
- **Address access time:**
  N82HS321: 45ns max
  N82HS321A: 35ns max
  N82HS321B 30ns max
- **Power dissipation: 20μW/bit typ**
- **Input loading: −100μA max**
- **2 chip enable inputs**
- **On-chip address decoding**
- **No separate fusing pins**
- **Unprogrammed outputs are High level**
- **Fully TTL compatible**
- **Outputs: Three-state**

APPLICATIONS

- **Prototyping/volume production**
- **Sequential controllers**
- **Microprogramming**
- **Hardwired algorithms**
- **Control store**
- **Random logic**
- **Code conversion**

PIN CONFIGURATION

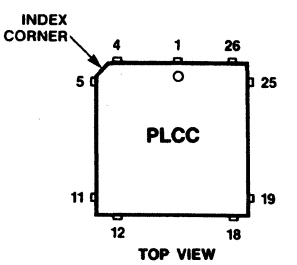
N PACKAGE



TOP VIEW

CD00951S

A PACKAGE

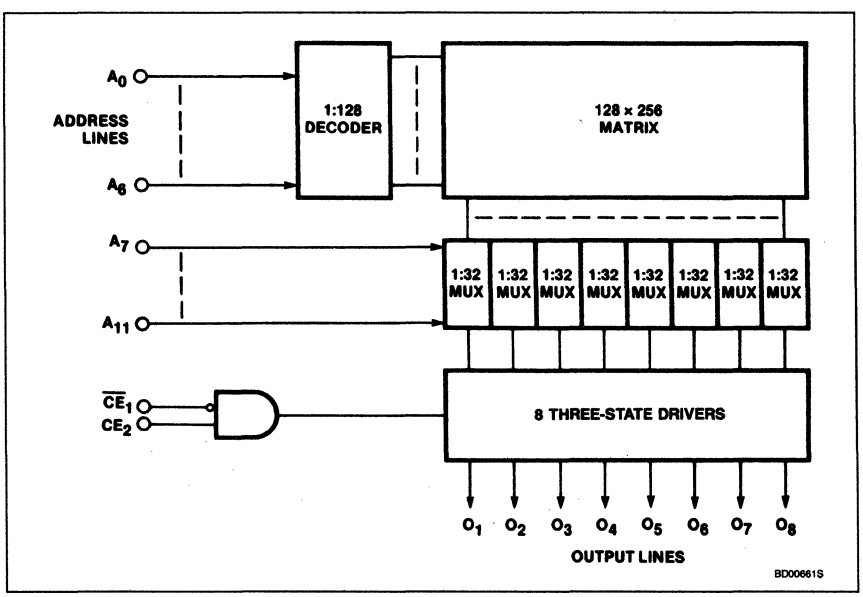


TOP VIEW

CD0028PS

Pin	Function	Pin	Function
1	NC	15	NC
2	A_7	16	O_4
3	A_6	17	O_5
4	A_5	18	O_6
5	A_4	19	O_7
6	A_3	20	O_8
7	A_2	21	NC
8	A_1	22	CE_2
9	A_0	23	A_{11}
10	NC	24	$\overline{CE}_1$
11	O_1	25	A_{10}
12	O_2	26	A_9
13	O_3	27	A_8
14	GND	28	V_{CC}

BLOCK DIAGRAM



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32K-Bit TTL Bipolar PROM (4096 × 8) 82HS321, 82HS321A, 82HS321B

ORDERING CODE

PACKAGE DESCRIPTION	ORDER CODES
Plastic Dual Inline 600mil wide 24-pin	N82HS321 N • N82HS321A N • N82HS321B N
Ceramic Dual Inline 600mil wide 24-pin	N82HS321 F • N82HS321A F • N82HS321B F
Plastic Leaded Chip Carrier 450mil sq 28-pin	N82HS321 A • N82HS321A A • N82HS321B A

ABSOLUTE MAXIMUM RATINGS

	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	V_{dc}
V_{IN}	Input voltage	+5.5	V_{dc}
V_O	Output voltage Off-state	+5.5	V_{dc}
T_A	Temperature range Operating	0 to +75	°C
T_{STG}	Storage	−65 to +150	

DC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +75°C,\ 4.75V \leq V_{CC} \leq 5.25V$

PARAMETER		TEST CONDITIONS[1,2]	LIMITS Min	LIMITS Typ[5]	LIMITS Max	UNIT
Input voltage						
V_{IL}	Low[3]				0.8	V
V_{IH}	High[3]		2.0			
V_{IC}	Clamp	$I_{IN} = -12mA$		−0.8	−1.2	
Output voltage		$\overline{CE}_1$ = Low, CE_2 = High				
V_{OL}	Low	$I_{OUT} = 9.6mA$			0.45	V
V_{OH}	High	$I_{OUT} = -2mA$	2.4			
Input current						
I_{IL}	Low	$V_{IN} = 0.45V$			−100	μA
I_{IH}	High	$V_{IN} = 5.5V$			40	
Output current						
I_{OZ}	Hi-Z state	$\overline{CE}_1$ = High, CE_2 = Low, $V_{OUT} = 0.5$			−40	μA
		$\overline{CE}_1$ = High, CE_2 = Low, $V_{OUT} = 5.5$			40	
I_{OS}	Short circuit[4]	$\overline{CE}_1$ = Low, CE_2 = High, $V_{OUT} = 0V$	−15		−70	mA
Supply current						
I_{CC}		$V_{CC} = 5.25V$		130	175	mA
Capacitance						
		$\overline{CE}_1$ = High, CE_2 = Low, $V_{CC} = 5.0V$				
C_{IN}	Input	$V_{IN} = 2.0V$		5		pF
C_{OUT}	Output	$V_{OUT} = 2.0V$		8		

Signetics

Signetics

82HS641
82HS641A
82HS641B
64K-Bit TTL Bipolar PROM

Bipolar Memory Products

Product Specification

The 82HS641 is field programmable, which means that custom patterns are immediately available by following the Signetics Generic II fusing Procedure. The 82HS641 is supplied with all outputs at a logical High. Outputs are programmed to a logic low level at any specified address by fusing the vertical junction matrix.

This device includes on-chip address decoding with 1 chip enable input for ease of memory expansion. It features Three-state outputs for optimization of word expansion in bused applications.

Ordering information can be found on the following page.

This device is also processed to military requirements for operating over the military temperature range. For specifications and ordering information consult the Signetics Military Data Book.

FEATURES

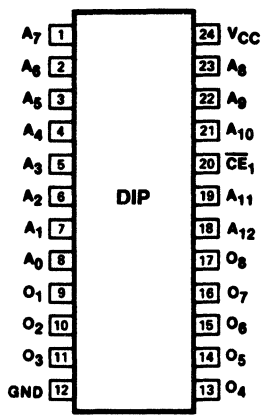
- **Address access time:**
  - **N82HS641 55ns max**
  - **N82HS641A 45ns max**
  - **N82HS641B 35ns max**
- **Power dissipation: 10μW/bit typ**
- **Input loading: −100μA max**
- **One chip enable input**
- **On-chip address decoding**
- **No separate fusing pins**
- **Unprogrammed outputs are High level**
- **Fully TTL compatible**
- **Outputs: Three-state**

APPLICATIONS

- **Prototyping/volume production**
- **Sequential controllers**
- **Microprogramming**
- **Hardwired algorithms**
- **Control store**
- **Random logic**
- **Code conversion**

PIN CONFIGURATION

N PACKAGE



TOP VIEW

CD00960S

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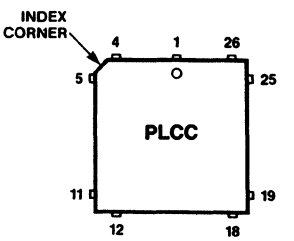
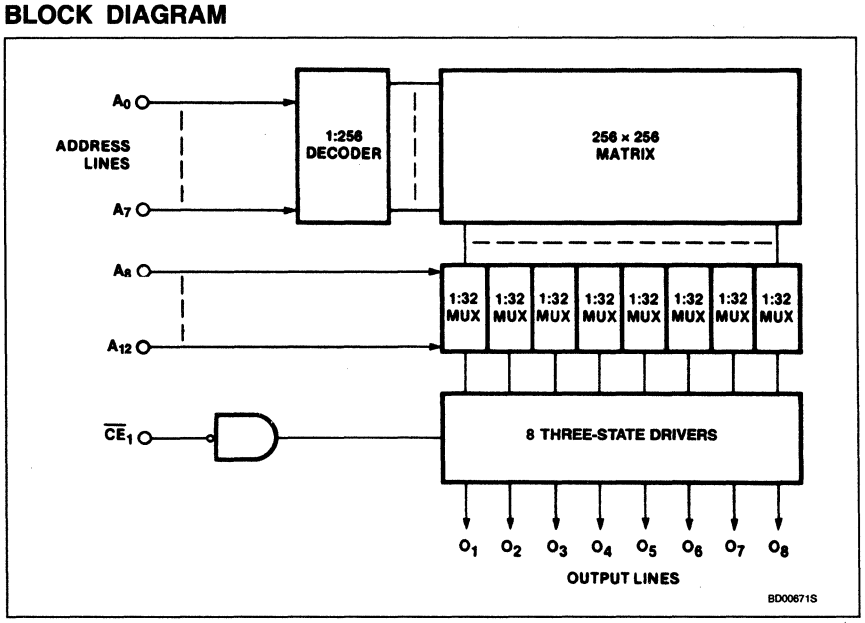


TOP VIEW

CD0028PS

Pin	Function	Pin	Function
1	NC	15	NC
2	A_7	16	O_4
3	A_6	17	O_5
4	A_5	18	O_6
5	A_4	19	O_7
6	A_3	20	O_8
7	A_2	21	NC
8	A_1	22	A_{12}
9	A_0	23	A_{11}
10	NC	24	$\overline{CE}_1$
11	O_1	25	A_{10}
12	O_2	26	A_9
13	O_3	27	A_8
14	GND	28	V_{CC}

BLOCK DIAGRAM



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64K-Bit TTL Bipolar PROM (8192 × 8) — 82HS641, 82HS641A, 82HS641B

ORDERING CODE

PACKAGE DESCRIPTION	ORDER CODES
Plastic Dual Inline 600mil wide 24-pin	N82HS641 N • N82HS641A N • N82HS641B N
Ceramic Dual Inline 600mil wide 24-pin	N82HS641 F • N82HS641A F • N82HS641B F
Plastic Leaded Chip Carrier 450mil sq 28-pin	N82HS641 A • N82HS641A A • N82HS641B A

ABSOLUTE MAXIMUM RATINGS

	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	V_{dc}
V_{IN}	Input voltage	+5.5	V_{dc}
V_O	Output voltage Off-state	+5.5	V_{dc}
T_A T_{STG}	Temperature range Operating Storage	0 to +75 −65 to +150	°C

DC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +75°C,\ 4.75V \leq V_{CC} \leq 5.25V$

PARAMETER		TEST CONDITIONS[1,2]	LIMITS Min	LIMITS Typ[5]	LIMITS Max	UNIT
Input voltage						
V_{IL}	Low[3]				0.8	V
V_{IH}	High[3]		2.0			
V_{IC}	Clamp	$I_{IN} = -12mA$		−0.8	−1.2	
Output voltage		$\overline{CE}_1$ = Low				
V_{OL}	Low	$I_{OUT} = 9.6mA$			0.45	V
V_{OH}	High	$I_{OUT} = -2mA$	2.4			
Input current						
I_{IL}	Low	$V_{IN} = 0.45V$			−100	μA
I_{IH}	High	$V_{IN} = 5.5V$			40	
Output current						
I_{OZ}	Hi-Z State	$\overline{CE}_1$ = High, $V_{OUT} = 0.5V$			−40	μA
		$\overline{CE}_1$ = High, $V_{OUT} = 5.5V$			40	
I_{OS}	Short circuit[4]	$\overline{CE}_1$ = Low, $V_{OUT} = 0V$	−15		−70	mA
Supply current						
I_{CC}		$V_{CC} = 5.25V$		130	175	mA
Capacitance		$\overline{CE}_1$ = High, $V_{CC} = 5.0V$				
C_{IN}	Input	$V_{IN} = 2.0V$		5		pF
C_{OUT}	Output	$V_{OUT} = 2.0V$		8		

Signetics

Signetics

82S191C
16K-Bit TTL Bipolar PROM

Product Specification

Bipolar Memory Products

DESCRIPTION

The 82S191C is field programmable, which means that custom patterns are immediately available by following the Signetics Generic I fusing procedure. The 82S191C is supplied with all outputs at a logical Low. Outputs are programmed to a logic High level at any specified address by fusing the Ni-Cr link matrix.

This device includes on-chip decoding and 3 chip enable inputs for ease of memory expansion. It features Three-state outputs for optimization of word expansion in bused organizations.

Ordering information can be found on the following page.

The 82S191C devices are also processed to military requirements for operation over the military temperature range. For specifications and ordering information consult the Signetics Military Data Book.

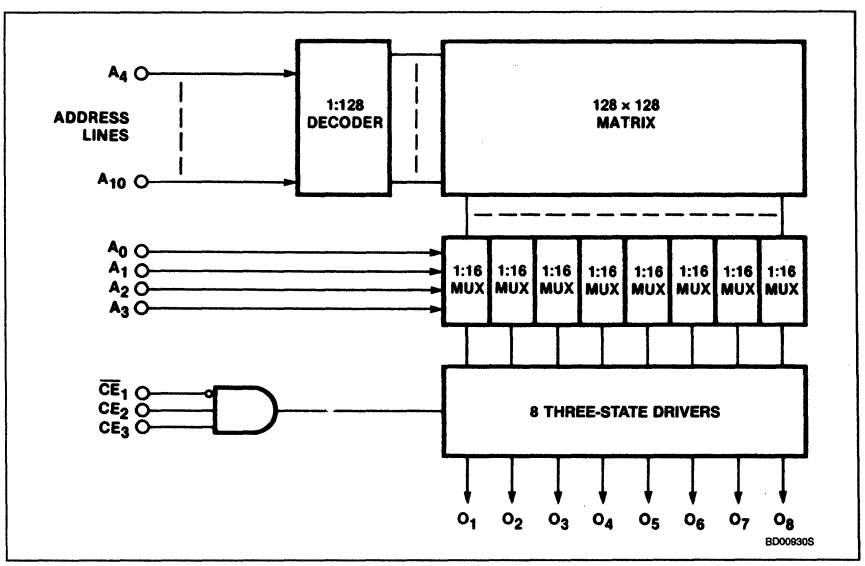
FEATURES

- **Address access time: 35ns max**
- **Power dissipation: 40μW/bit typ**
- **Input loading: −100μA max**
- **Three chip enable inputs**
- **On-chip address decoding**
- **No separate fusing pins**
- **Unprogrammed outputs are Low level**
- **Fully TTL compatible**
- **Outputs: Three-state**

APPLICATIONS

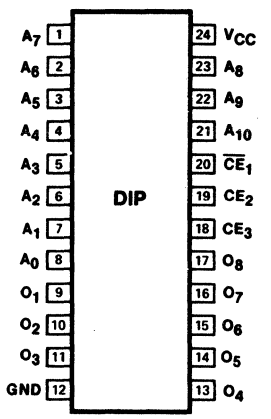
- **Prototyping/volume production**
- **Sequential controllers**
- **Microprogramming**
- **Hardwired algorithms**
- **Control store**
- **Random logic**
- **Code conversion**

BLOCK DIAGRAM



PIN CONFIGURATION

N PACKAGE



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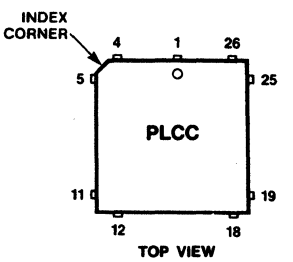

Pin	Function	Pin	Function
1	NC	15	NC
2	A_7	16	O_4
3	A_6	17	O_5
4	A_5	18	O_6
5	A_4	19	O_7
6	A_3	20	O_8
7	A_2	21	NC
8	A_1	22	CE_3
9	A_0	23	CE_2
10	NC	24	$\overline{CE}_1$
11	O_1	25	A_{10}
12	O_2	26	A_9
13	O_3	27	A_8
14	GND	28	V_{CC}

Signetics

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10149
1K-Bit ECL Bipolar PROM

Product Specification

Bipolar Memory Products

DESCRIPTION

The 10149 is field programmable, meaning that custom patterns are immediately available by following the ECL fusing procedure. The device is supplied with all outputs at logical Low. Outputs are programmed to a logic High level at any specified address by fusing the Ni-Cr link matrix.

The 10149 is suitable for use in high performance ECL systems. The outputs are capable of driving 50Ω loads.

A chip enable input is provided for ease of memory expansion.

Ordering information can be found on the folowing page.

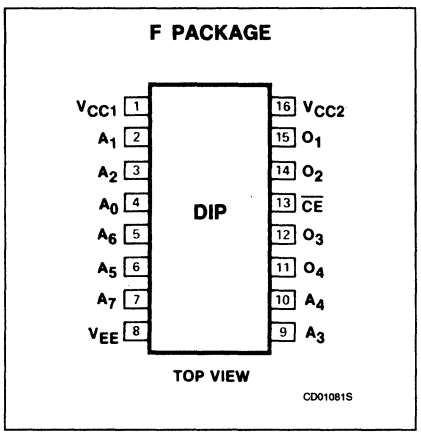
FEATURES

- **Address access time: 20ns max**
- **Power dissipation: 0.66mW/bit typ**
- **High impedance inputs (50kΩ pulldown)**
- **Open emitter outputs (50Ω drive)**
- **On-chip address decoding**
- **No separate fusing pins**
- **Fully compatible with ECL 10K series**

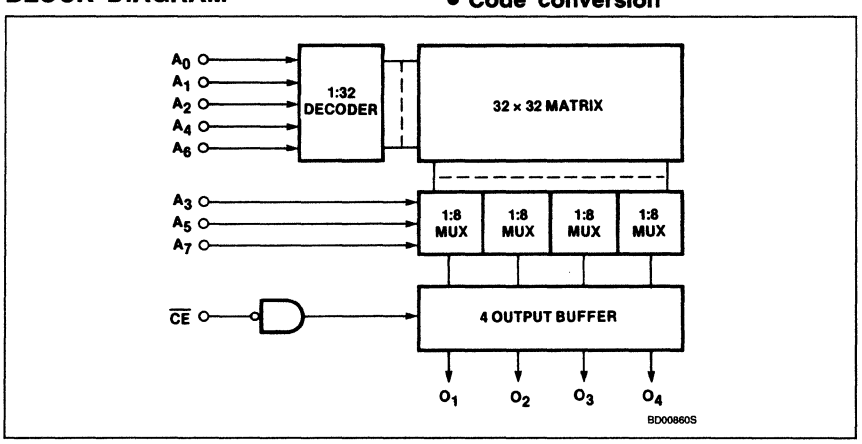
APPLICATIONS

- **Sequential controllers**
- **Microprogramming**
- **Hardwired algorithms**
- **Control store**
- **Random logic**
- **Code conversion**

PIN CONFIGURATION



BLOCK DIAGRAM



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74F764/765
DRAM Dual-Ported Controllers

Logic Products

Preliminary Specification

FEATURES

- **Allows two microprocessors to access the same bank of dynamic RAM**
- **Replaces 25 discrete devices**
- **Performs arbitration, signal timing, address multiplexing, and refresh**
- **9 address output pins allow direct control of up to 256K dynamic RAMS**
- **External address multiplexing enables control of 1 Mbit (or more) dynamic RAMS**
- **Separate refresh clock allows adjustable refresh timing**
- **F764 has on-chip 18-bit address input latch**
- **100 MHz Maximum clock rate**
- **Allows control of dynamic RAMs with row access times down to 40 ns**

Signetics

DESCRIPTION

The 74F764/765 DRAM Dual-Ported Controller is a high speed synchronous dual-port arbiter and timing generator that allows two microprocessors, microcontrollers, or any other memory accessing devices to share the same block of DRAM. The device performs arbitration, signal timing, address multiplexing, and refresh address generation, replacing up to 25 discrete devices.

The 74F764 contains an on-chip address input latch which latches the address inputs at the start of a memory access cycle.

The 74F765 is an unlatched option of the 74F764, designed for use in systems that provide latched address lines i.e. processors with non-multiplexed address and data bus.

Both devices are available in 40-pin plastic DIP or 44-pin PLCC with pinouts designed to allow convenient placement of microprocessors, DRAMs, and other support chips.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F764/765	150 MHz	150 mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$, $T_A = 0°C$ to $+70°C$
Plastic DIP	N74F764N, N74F765N
PLCC-44	N74F764A, N74F765A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$\overline{REQ1}$, $\overline{REQ2}$	Request inputs (Active LOW)	1.0/1.0	20μA/0.6mA
CP	Clock input	1.0/1.0	20μA/0.6mA
RCP	Refresh clock input	1.0/1.0	20μA/0.6mA
A1–A18	Address inputs	1.0/1.0	20μA/0.6mA
GNT	Grant output	1750/100	35mA/60mA
$\overline{SEL1}$, $\overline{SEL2}$	Select outputs (Active LOW)	1750/100	35mA/60mA
DTACK	Data Transfer Acknowledge output	1750/100	35mA/60mA
$\overline{RAS}$	Row Address Strobe (output active LOW)	1750/100	35mA/60mA
WG	Write Gate output	1750/100	35mA/60mA
$\overline{CASEN}$	Column Address Strobe Enable output (Active LOW)	1750/100	35mA/60mA
MA0–MA8	Address outputs	1750/100	35mA/60mA

NOTE: One (1.0) FAST Unit Load is defined as; 20μA in the HIGH state and 0.6mA in the LOW state.

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74LS765
DRAM Controller

DRAM Dual-Ported Controller
Preliminary Specification

Products

FEATURES

- **Allows two microprocessors to access the same bank of DRAM**
- **Replaces 25 TTL devices to perform arbitration, signal timing, multiplexing, and refresh generation**
- **9 address output pins allow control of up to 256K DRAMS**
- **Separate refresh clock allows adjustable refresh timing**
- **Same as LS764 but without input latch**
- **30MHz Maximum Clock rate**

DESCRIPTION

The 74LS765 DRAM Dual-Ported Controller is a high speed, clocked dual port arbiter and timing generator that allows two microprocessors, microcontrollers, or any other memory accessing devices to share the same block of memory. The device performs arbitration, signal timing, address multiplexing and refresh, replacing up to 25 discrete TTL devices.

The 'LS765 unlatched option eliminates the address input latch to facilitate use with latched address outputs.

The device is available in a 40-pin plastic DIP or 44-pin PLCC with pinouts designed to allow convenient placement of microprocessors, DRAMs, and other support chips.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74LS765	45ns	215mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ± 5%; T_A = 0°C to +70°C
Plastic DIP	N74LS765N*
PLCC-44	N74LS765A**

NOTE:
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74LS
$\overline{REQ}_1$, $\overline{REQ}_2$	Request inputs (active LOW)	1LSUL
CP	Clock input	1LSUL
RCP	Refresh clock input	1LSUL
A1 – A18	Address inputs	1LSUL
GNT	Grant output	60LSUL
$\overline{SEL}_1$, $\overline{SEL}_2$	Select outputs (active LOW)	60LSUL
DTACK	Data transfer acknowledge output	60LSUL
$\overline{RAS}$	Row address strobe (output active LOW)	60LSUL
WG	Write gate output	60LSUL
$\overline{CASEN}$	Column address strobe enable output (active LOW)	
MA0 – MA8	Address outputs	60LSUL

NOTE:
One 74LS Unit Load (LSUL) is defined as: 20μA in the HIGH state and 0.4mA in the LOW state.

Signetics

8X60
FIFO RAM Controller (FRC)

Product Specification

Products

FEATURES

- **12-Bit FIFO Address Generator**
- **Data Rate Exceeding 8MHz**
- **Asynchronous Read/Write Operations**
- **Three-State Address Outputs**
- **User-Defined Word Width**
- **Specifically Designed for Use with High-Speed Bipolar RAMs (Adaptable for Use with MOS RAMs)**
- **TTL Input and Output**
- **16mA Address-Drive Capability**

USE AND APPLICATION

- **Interface Between Independently-Clocked Systems**
- **Buffer Memories for Disk and/or Tape**
- **Data Communication Concentrators**
- **CPU/Terminal Buffering**
- **DMA Applications**
- **CRT Terminals**

PRODUCT DESCRIPTION

The Signetics 8 × 60 FIFO RAM Controller (FRC) is an address and status generator designed to implement a high-speed/high-capacity First-In/First-Out (FIFO) stack utilizing standard off-the-shelf RAMs — see **Applications** on the last page of this data sheet. The FRC can control up to 4096 words of buffer memory; intermediate buffer sizes can be selected — refer to the memory length table on the next page. Built-in arbitration logic handles read/write operations on a first-come/first-served basis.

As shown in Figure 1, the FRC consists of:

- A 12-Bit Write Address Generation Counter (Counter #1) and a 12-Bit Read Address Generation Counter (Counter #2).
- A 12-Bit Up/Down Status Counter (Counter #3).
- Twelve Three-State Address Drivers.
- Control Logic.

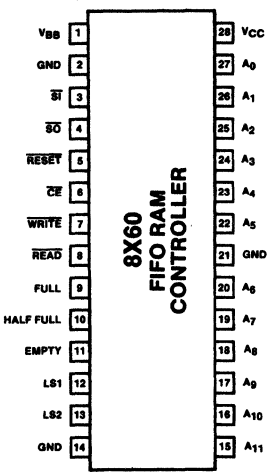
The two address counters, #1 and #2, respectively, are used to generate write and read addresses; the outputs of these counters are multiplexed to the three-state address drivers. Counter #3 generates **full, empty,** and **half full** status.

FUNCTIONAL OPERATION

The FRC operates in either of two basic modes — **write** into the FIFO buffer memory or **read** from the FIFO buffer memory. These two operations are described in subsequent paragraphs and the complete sequence is summarized in Table 1. Typical Write/Read timing relationships, arbitration logic, and chip-enable control are shown in the Timing Diagrams.

PIN CONFIGURATION

N, F PACKAGE



PIN NO.	IDENTIFIER	FUNCTION
1	V_{BB}	Supply voltage for internal circuits.
2, 14, 21	GND	Circuit ground.
3	$\overline{SI}$	Shift-In request for write cycle; active-low input.
4	$\overline{SO}$	Shift-Out request for read cycle; active-low input.
5	$\overline{RESET}$	Active-low master reset input.
6	$\overline{CE}$	Active-low chip enable input.
7	$\overline{WRITE}$	Write cycle address valid; active-low output.
8	$\overline{READ}$	Read cycle address valid; active-low output.
9	FULL	Memory full status output; also, override input capability. Active when **high.**
10	HALF FULL	Memory half-full status output; active-high.
11	EMPTY	Memory empty status output; also, override input capability. Active when **high.**
12	LS1	Least significant bit (LSB) of the memory length select input.
13	LS2	Most significant bit (MSB) of the memory length select input.
15 – 20 22 – 27	$A_{11} - A_0$	Three-state address outputs: A_0 = LSB.
28	V_{CC}	Supply voltage.

ORDERING CODE

PACKAGES	COMMERCIAL RANGES $V_{CC} = 5V \pm 10\%$; $T_A = 0°C$ to $+70°C$
Plastic DIP	N8X60N
Hermetic CERDIP	N8X60F

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Signetics SMD Products

Standard Products

Signetics Corporation, and it's parent N. V. Philips are the world leaders in SMD Technology. Philips developed both the SOT for Transistors in the 1960s, and the SO for ICs in the early 1970s. Signetics, through it's Philips connection, has offered SMD components longer than any other IC manufacturer in the US and has the most experience and broadest line of products and packages available. In addition to SMD IC's, Philips offers a broad line of other components in SMD format, including capacitors, resistors, transistors, and diodes. Philips offers an excellent line of automatic pick-and-place equipment. Through it's own assembly factories worldwide, Philips also has the broadest experience in SMD Manufacturing Technology. Signetics' and Philips' SMD leadership is a result of being able to help customers use this technology through a more thorough understanding of the relationships between devices, placement equipment, and manufacturing technology, as well as having the broadest range of SMD components, equipment, and services available in the world.

The purpose of this pocket guide is to provide users with details of the SMD IC packages offered through Signetics, including mechanical outlines, standardization, footprint information, and a complete list of available parts and their appropriate packages, as well as a tentative list of parts to be released in the near future.

Since the part list grows almost daily, this pocket guide is updated and published quarterly. DO NOT USE OUTDATED POCKET GUIDES. ASK YOUR LOCAL SALES OFFICE FOR A CURRENT ONE.

Further, if you need a component not listed in this guide, please CHECK WITH YOUR LOCAL SIGNETICS SALES REPRESENTATIVE.

Table 1

No. of Pins	SO (0.150" Wide)	SOL (0.300" Wide)	PLCC
8	X		
14	X		
16	X	X	
20		X	X
24		X	
28		X	X
32			X
44			X
52			X
68			X
84			X

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SMD Products

SMD PACKAGES

Commercial SMD packages fall into two general categories: Small Outline (both the 0.150 inch wide SO and the 0.300 inch wide SOL) and the PLCC (Plastic Leaded Chip Carrier, also referred to as a PCC). Both of these packages use the same materials and assembly technology as used for the standard plastic DIL. Both have 0.050 inch lead spacing. The SO/SOL is dual-in-line with a Gull-Wing lead bend, while the PLCC is square or rectangular with a J-Bend lead bend. Both lead bends are designed for mounting directly to the surface of a printed circuit board. The SO/SOL packages are for the smaller pin count devices, i.e., those up to 28 pins, while the PLCC is for those parts with up to 84 pins. There is, however, some overlap due to the need to accomodate larger die in smaller pin counts (see Table 1).

MILITARY PACKAGES

To support the implementation of defense and aerospace systems in surface mount technology Signetics Military Division offers products processed to MIL-M-38510, DESC selected item drawings, and MIL-STD-883 Revision C in the following packages:

Ceramic leadless chip carriers; triple laminated with metal lid and gold plated terminals in 20 to 68 leads.

Ceramic flat packages; frit glass sealed alumina CERPAC in 14 to 28 leads, and brazed leaded ceramic in 52 leads.

All military package case outlines and physical dimensions conform with the current revision MIL-M-38510, Appendix C, except for package types which are not included in that specification.

For more information on Signetics military SMD ICs please refer to the military products data manual or contact the Signetics Military Division, Sacramento, California, 916-924-6010.

SEMICUSTOM

The full complement of SMD packaging including both SO's and PLCC's is available for designing with Signetics Semicustom products.

STANDARDIZATION

All Signetics small outline packages (SO-8, SO-14, SO-16, SOL-16, SOL-20, SOL-24, SOL-28) meet the specifications detailed in the *JEDEC STANDARD* #MS-012AA-AC and #MS-013AA-AE. All Signetics PLCC packages (20, 28, 44, 52, 68, and 84 pins) meet the specifications covered in the *JEDEC Registered Outline* #MS-047AA-AH. The PLCC-32 meets the specifications covered in *JEDEC Registered Outline* #MO-052-AE.

SPECIFICATIONS

Below are the specific dimensions of each of our packages.

Pinouts for devices in SO packages are the same as all standard DIPs except for a few linear devices identified with an asterisk(*). Pin configurations for each of the PLCC formats are indicated in the drawings below. **THESE ARE THE MOST CURRENT DRAWINGS. DISCARD PREVIOUS POCKET GUIDE.**

SMD Products

THERMAL CHARACTERISTICS

For complete thermal resistance data including both Θ_{JA} and Θ_{JC} of SO, SOL and PLCC packages see "SMD Thermal Considerations."

ASSUMPTIONS

- Junction temperature (T_J) is the temperature of a powered IC measured at the substrate diode. When the device is powered, the heat generated causes the T_J to rise above the ambient temperature (T_A).
- Prior to 1985, SO packages were assembled with Alloy-42 leadframes. Currently, all SMD packages use Copper lead frames with the exception of the very low power devices (CMOS and High Speed CMOS) and the analog parts in SO-8. Although the power is low enough in these exceptions that Θ_{JA} is adequate with Alloy-42, they will gradually be shifted into copper leadframes.
- The ability of the package to conduct heat from the chip to the environment is expressed in terms of thermal resistance, normally called Theta JA (Θ_{JA}). Θ_{JA} is the total resistance from the junction to ambient and is often separated into two components: Θ_{JC} (junction to case) and Θ_{CA} (case to ambient) $\Theta_{JA} = \Theta_{JC} + \Theta_{CA}$.
- Θ_{JA} values for SMD packages with copper leadframes are listed in Table #2. Test conditions for these values follow:
  Test Ambient — Still air
  Test Fixture — Glass epoxy test board
  Test Board Size
  — SO — 1.12″ × 0.75″ × 0.059″
  — SOL — 1.58″ × 0.75″ × 0.059″
  — PLCC — 2.24″ × 2.24″ × 0.062″
- Calculate power (P) by multiplying V_{CC} nominal × I_{CC} at T_A.
  $P = IE$
- Calculate rise in (T_J) by multiplying Power by Θ_{JA}

$$\Delta T_J = (P \times \Theta_{JA})$$

Signetics

Table 2 Typical Θ_{JA} Values for SMD Packages*

No. of Pins	Die Size (sq mils)	Average Θ_{JA} (°C/W)		
		SO	SOL	PLCC
8	3k	159	—	—
14	5k	118	—	—
16	5k	110	—	—
16	12k	—	97	—
20	12k	—	87	73
24	12k	—	75	—
28	12k	—	71	—
32	30k	—	—	60
44	30k	—	—	47
52	50k	—	—	42
68	50k	—	—	44
84	50k	—	—	34

*(Values express in °C/W)

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SHIPPING

SO/SOL and PLCC packages can be shipped in either Tubes or in Tape & Reel.

PLCC Tubes are 19.33″ long and the number of components/tube are listed below. The SO tubes are being modified to use an improved turn-lock end-stop developed by Philips and will be shortened from the present 20.12″ to 19.5″. Both the current and the new quantities are indicated in Table 3 below.

Signetics' Tape & Reel meets the requirements specified in proposed specification #EIA-481-A using 13 inch reels. Tape sizes and quantity/reel are indicated in Table 3. Note: As more customers move into high volume production, the quantities/reel will be increased to fill the reels. This will be in the second half of 1986 and exact quantities will be provided at that time.

Table 3

Package Description	Tube Specification	Qty Per Tube	Tape Specification	Tape Size (mm) Width x Pitch	Qty Per Reel
SO-8, 0.15 Body	D570-0004	96	EIA-481-A	12 x 8	2500
SO-14, 0.15 Body	D570-0004	55	EIA-481-A	16 x 8	2500
SO-16, 0.15 Body	D570-0004	48	EIA-481-A	16 x 12	1000
SO-16, 0.30 Body	D570-0002	46	EIA-481-A	24 x 12	1000
SO-20, 0.30 Body	D570-0002	37	EIA-481-A	24 x 12	1000
SO-24, 0.30 Body	D570-0002	31	EIA-481-A	24 x 12	1000
SO-28, 0.30 Body	D570-0002	26	EIA-481-A	24 x 12	1000
PLCC-20, Square	D570-0020	45	EIA-481-A	16 x 12	1000
PLCC-28, Square	D570-0020	36	EIA-481-A	24 x 16	750
PLCC-44, Square	D570-0020	26	EIA-481-A	32 x 24	500
PLCC-52, Square	D570-0020	22	EIA-481-A	32 x 24	500
PLCC-68, Square	D570-0020	18	EIA-481-A	44 x 32	250
PLCC-84, Square	D570-0020	15	EIA-481-A	44 x 36	250
PLCC-32, Rect	D570-0020	36	EIA-481-A	24 x 16	750

NOTES: EIA-481-A (taping of surface mount components for automatic placement) is the electronic industry standard.

SMD Products

FOOTPRINTS

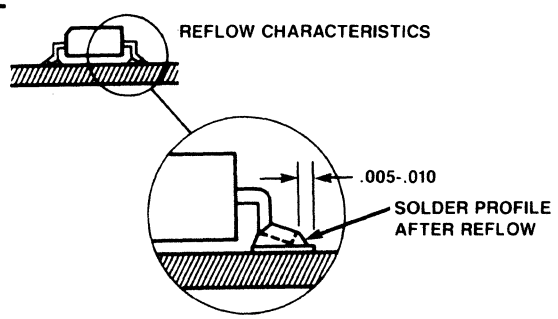
The suggested footprints should work in most manufacturing environments for Signetics and Philips packages (as well as other manufacturers' packages that meet the JEDEC standard).

These pad widths allow 0.008-inch traces between footprints while still keeping an 0.008-inch gap between trace and footprint.

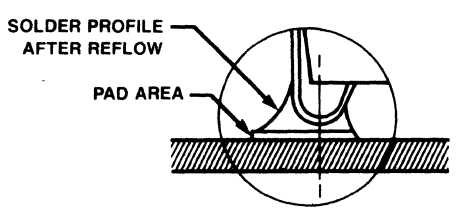
Experienced designers stress that pad length can be important for SO packages. They should be long enough to provide a solder fillet of 0.005- to 0.10-inch after reflow, but not long enough to allow the device to float off centerline during the reflow operation. For the PLCC, care must be taken not to run the footprint too far under the package, but rather, extend it out approximately 0.050-inch to the outside. This will help reduce solder bridges under the package where they cannot be seen during visual inspection.

SOLDERING CRITERIA

FOR SO/SOL



FOR PLCC



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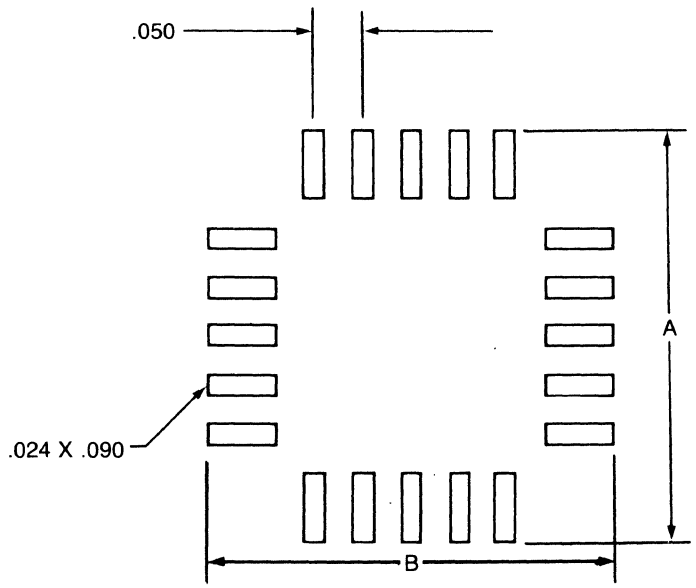
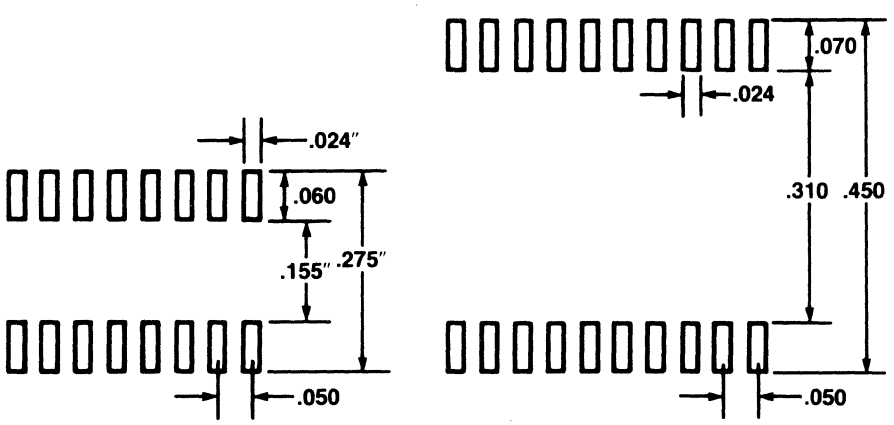
FOOTPRINTS FOR PLCC



	A	B
20	.440	.440
28	.540	.540
32	.540	.460
44	.740	.740
52	.840	.840
68	1.040	1.040
84	1.240	1.240

FOOTPRINTS FOR SO/SOL



Dimensions in inches.

SMD Products

SMD LITERATURE

SMD Pocket Guide	Published Quarterly
SMD Reliability Data	Available
SMD Thermal Considerations	Available
SMD Substrate Design Guidelines	Available
SMD Fluxing & Cleaning	Available
SMD Adhesive Application & Curing	Available
SMD Test and Repair	Available
SMD Soldering Techniques	Q4 '86
SMD Solder Joint Criteria	Q4 '86
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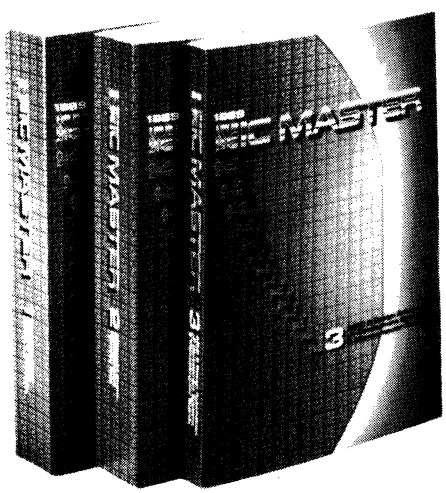

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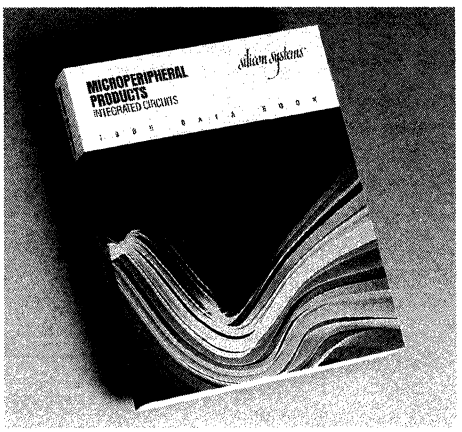

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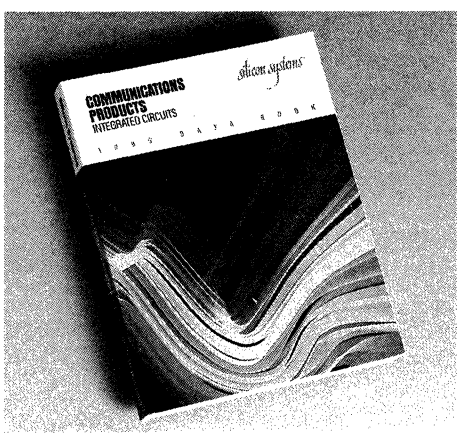

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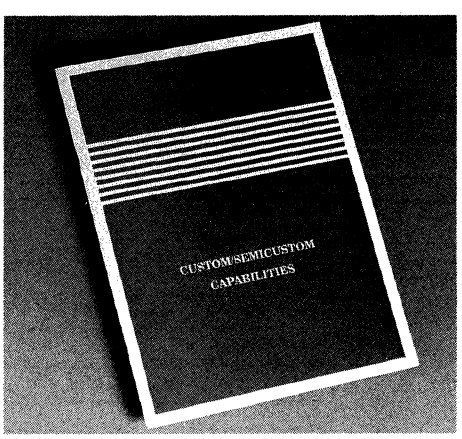

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HDD READ/WRITE AMPLIFIERS								
SSI 32R104C	Ferrite	4	2.4	23	35	15 to 45	+6V,-4V	Differential, Bi-directional
SSI 32R104CLN	Ferrite	4	1.7	23	35	15 to 45	+6V,-4V	Differential, Bi-directional
SSI 32R114	Thin Film	4	1.1	65	123	55 to 110	±5V	Differential/Differential
SSI 32R115	Ferrite	2, 4, 5	1.8	20	40	30 to 50	±5V	Differential, Bi-directional
SSI 32R117	Ferrite	2, 4, 6	2.1	23	100	10 to 50	+5V,+12V	Differential/TTL
SSI 32R117A	Ferrite	2, 4, 6	1.7	20	100	10 to 50	+5V,+12V	Differential/TTL
SSI 32R188	Ferrite	4	2.4	18	43	35 to 70	+6V,-5V	Differential, Bi-directional
SSI 32R501	Ferrite	4, 6, 8	1.5	23	100	10 to 50	+5V,+12V	Differential/TTL
SSI 32R510A	Ferrite	2, 4, 6	1.5	20	100	10 to 40	+5V,+12V	Differential/TTL
SSI 32R511	Ferrite	4, 6, 8	1.5	20	100	10 to 40	+5V,+12V	Differential/TTL
SSI 32R512	Thin Film	8, 9	0.9	32	150	10 to 40	+5V,+12V	Differential/TTL
SSI 32R514	Ferrite	2, 4, 6	1.5	20	150	10 to 40	+5V,+12V	Differential/TTL
SSI 32R515	Ferrite	9, 10	1.5	20	100	10 to 50	+5V, +12V	Differential/TTL
SSI 32R520	Thin Film	4	0.9	65	123	30 to 75	±5V	Differential/Differential
SSI 32R521	Thin Film	6	0.9	65	100	20 to 70	+5V,+12V	Differential/TTL
SSI 32R522	Thin Film	4, 6	1.0	32	100	6 to 35	+5V,+12V	Differential/TTL
SSI 32R524R	Thin Film	8	0.8	56	100	20 to 60	+5V, +12V	Differential/Differential
SSI 32R525	Thin Film	4	0.8	35	150	25 to 40	+5V, -5V	Differential/Differential

SSI Device Number	Circuit Function	Features
HDD PULSE DETECTION		
SSI 32P540	Read Data Processor	Time Domain Filter
SSI 32P541	Read Data Processor	AGC, Amplitude & Time Pulse Qualification, RLL Compatible
SSI 32P544	Pulse Detector	32P541-type pulse detector with embedded servo electronics
SSI 32P546	Pulse Detector	32P541-type pulse detector with pulse slimming compatibility
HDD DATA RECOVERY		
SSI 32D531	Data Synchronizer	Data Synchronizer/Write Precompensation
SSI 32D5321	Data Separator	Data Synchronizer/2, 7 RLL ENDEC
SSI 32D534	Data Separator	Data Synchronizer/MFM ENDEC/Write Precompensation
SSI 32D535	Data Separator	Data Synchronizer/2, 7 RLL ENDEC/Write Precompensation
SSI 32D536	Data Separator	Data Synchronizer/1, 7 RLL ENDEC/Write Precompensation
HDD HEAD POSITIONING		
SSI 32H101A	Preamplifier-Ferrite Head	AV = 93, BW = 10MHZ, e_n = 7.0 nV/√Hz
SSI 32H116	Preamplifier-Thin Film Head	AV = 250, BW = 20MHz, e_n = 0.94 nV/√Hz
SSI 32H523R	Servo Read/Write	Single-channel thin-film read/write device
SSI 32H566	Servo Read/Write	Single-channel ferrite read/write device
SSI 32H567	Servo Demodulator	Di-bit Quadrature Servo Pattern: PLL Synchronization
SSI 32H568	Servo Controller	Track & Seek Mode Operation; Microprocessor Interface
SSI 32H569	Servo Motor Driver	Head Parking, Spindle Motor Braking
HDD SPINDLE MOTOR CONTROL		
SSI 32M590	2-Phase Motor Speed Control	±0.035% Speed Accuracy; Unipolar Operation
SSI 32M591	3-Phase Motor Speed Control	±0.05% Speed Accuracy; Unipolar Operation
SSI 32M593	3-Phase Motor Speed Control	±0.037% Speed Accuracy; Bipolar Operation, 5-1/4" Drives
SSI 32M594	Motor Speed Control	±0.037% Speed Accuracy; Bipolar Operation, 3-1/2", 5-1/4" Drives
HDD CONTROLLER/INTERFACE		
SSI 32B450A	SCSI Controller	Async transfer to 2 MBPS; Initiate/Target Modes; Internal Drivers; CMOS
SSI 32B451	SCSI Controller	Async transfer to 1.5 MBPS; Internal Drivers; AIC 500L compatible
SSI 32C452	Storage Controller	20Mbits/sec; CMOS; Programmable; AIC-010 Compatible
SSI 32C452A	Storage Controller	15Mbits/sec; CMOS; Programmable; AIC-010F Compatible
SSI 32C453	Buffer Controller	Non-mux addressing to 16K; CMOS; AIC-300 Compatible
SSI 32B545	Support Logic	Includes ST506 Bus Drivers/Receivers
FLOPPY DISK DRIVES		
SSI 34D441	Data Separator	High Performance Analog Data Separator, NEC 765 Compatible
SSI 34P570	Read Data Path	2 Channel Read/ Write With Read Data Path
SSI 34R575	Read/Write	2, 4 Channel Read/Write Circuit
SSI 34B580	Support Logic	Port Expander, Includes SA400 Interface Drivers/Receivers
TAPE DRIVER CIRCUITS		
SSI 35P550	Read Data Path	4 Channel Read/Write With Read Data Path

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K-SERIES SINGLE CHIP MODEM FAMILY						
SSI 73K212	X			1200/300 BPS, Bell 212A/103 compatible	12V	28, 22 DIP, 28 PLCC
SSI 73K212L	X			Low power 73K212, 40mW, +5V single supply	5V	28, 22 DIP, 28 PLCC
SSI 73K212U	X			73K212 with integral 16C450 UART	5V	40 DIP
SSI 73K221		X		1200/600 BPS, CCITT V.22/V.21 compatible	12V	28, 22 DIP, 28 PLCC
SSI 73K221L		X		Low power 73K221, 40mW, +5V single supply	5V	28, 22 DIP, 28 PLCC
SSI 73K221U		X		73K221 with integral 16C450 UART	5V	40 DIP
SSI 73K222	X	X		1200/600/300 BPS Bell 212/103, CCITT V.22/V.21	12V	28, 22 DIP, 28 PLCC
SSI 73K222L	X	X		Low power 73K222, 40mW, +5V single supply	5V	28, 22 DIP, 28 PLCC
SSI 73K222U	X	X		73K222 with integral 16C450 UART	5V	40 DIP
SSI 73K322		X		73K221 with V.23 mode for European applications	12V	28, 22 DIP, 28 PLCC
SSI 73K322L		X		Low power 73K322, 40mW, +5V single supply	5V	28, 22 DIP, 28 PLCC
SSI 73K324		X	X	2400/1200/300 BPS, V.22 bis/V.22/V.21 with V.23 mode for European applications		
SSI 73K324L		X	X	Low power, 73K324, 120mW, +5V single supply		
SSI 73K224	X	X	X	2400/1200/300/ BPS, V.22 bis, V.22/V.21, Bell 212/103 compatible	12V	28, 44 PLCC
SSI 73K224L	X	X	X	Low power 73K224, 100mW, +5V single supply	5V	28, 44 PLCC
MODEM/MODEM SUPPORT						
SSI 73D2404	X	X	X	2400 BPS intelligent modem device set	±5V	44, 28 PLCC, 28, 40 DIP
SSI 73M223				1200 BPS half-duplex V.23 FSK modem	5V	16 DIP
SSI 73M3522	X	X		Hi-performance filter for 1200 BPS modems	±5V	16 DIP
SSI 73M450				16C450 pin compatible UART	5V	40 DIP, 44 PLCC
SSI 73M450F				Fast version of 73M450 UART	5V	40 DIP, 44 PLCC

SSI Device Number	Circuit Function	Features	Power Supplies	Available Packages
TONE SIGNALING PRODUCTS				
SSI 75T201	Integrated DTMF Receiver	Binary of 2-of-8 output	12V	22 DIP
SSI 75T202	Integrated DTMF Receiver	Low-power, binary output	5V	18 DIP
SSI 75T203	Integrated DTMF Receiver	Binary output, early detect	5V	18 DIP
SSI 75T204	Integrated DTMF Receiver	Low-power, binary output	5V	14 DIP, 16 SO
SSI 75T2089	Integrated DTMF Transceiver	Generator and Receiver, µP interface	5V	22 DIP
SSI 75T2090	Integrated DTMF Transceiver	Like 75T2089 plus Call Progress Detect	5V	22 DIP
SSI 75T2091	Integrated DTMF Transceiver	Like 75T2090 plus Early Detect	5V	28 DIP, PLCC
SSI 75T957	Integrated DTMF Receiver	Early Detect, Dial Tone reject	5V	22 DIP, 24 SO
SSI 75T980	Imprecise Call Progress Detector	Energy detect in 305-640 Hz band, Teltone	5V	8 DIP
SSI 75T981	Precise Call Progress Detector	Detects 350, 400, 440, 480 Hz, Teltone second-source	5V	22 DIP
SSI 75T982	Precise Call Progress Detector	Detects 350, 440, 480, 620 Hz, Teltone second-source	5V	22 DIP
TELEPHONY/DIGITAL TELECOM				
SSI 78P233	DS-1 Line Interface	T1 Clock/Data Recovery, Transmit Equalization	5V	24 DIP, SO, SDIP
SSI 78P234	2048 KB/S PCM Interface	Receive Clock & Data Recovery;Transmit Drivers	5V	20 DIP, SO
SSI 78P8050	T1 Transmitter	CMOS version of Rockwell 8050	5V	28 DIP, PLCC
SSI 78P8060	T1 Receiver	CMOS version of Rockwell 8060	5V	28 DIP, PLCC
SSI 78A093A/B	12x8x1 Crosspoint Switch	Low ON resistance, two versions	5-12V	40 DIP, 44 PLCC
SSI 78A207	Integrated MF Receiver	Detects central office toll signals	5V	20 DIP
SSI 78A400	4-Wire Loopback	2713 Hz detector, failsafe timeouts	±5V	16 DIP, 18 SO
SSI 78A420	4-Wire Loopback	2713 Hz detector, failsafe timeouts, gain/loss block	±5V	22 DIP

For a copy of the literature, contact Silicon Systems or your local representative.

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Silicon Systems, Inc. 14351 Myford Road, Tustin, CA 92680 (714) 731-7110, TWX 910-595-2809

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Silicon Systems Custom and Semicustom Circuits

MIX FULL-CUSTOM AND SEMICUSTOM DESIGN ON A SINGLE CHIP

Due to the interlocking nautre of SSi's design approaches, full-custom and semicustom design can be mixed on the electrical and/or physical design of any given IC.

CHOOSE THE OPTIMUM DESIGN APPROACH BASED ON TRADE-OFFS

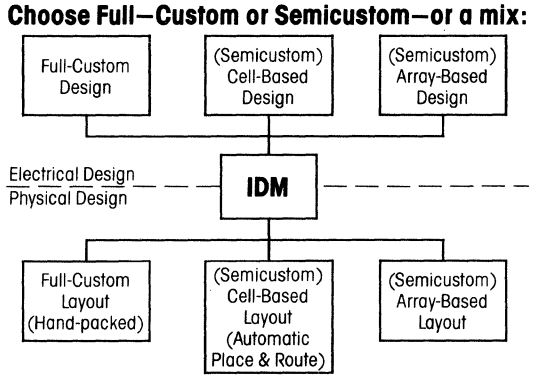
Each IDM design approach offers unique cost, time, and performance tradeoffs.

CONVERT SEMI-CUSTOM DESIGN INTO FULL CUSTOM DESIGN

With its unique integrated design automation system, SSi can easily convert a semicustom design into full-custom circuitry. This capability allows SSi's customers to reduce production costs by converting an area-inefficient semicustom design into a high-performance full-custom design.

IDM—INTEGRATED DESIGN METHODOLOGY

Choose Full—Custom or Semicustom—or a mix:



CUSTOM / SEMICUSTOM TRADE-OFFS

Choose Optimum Design Approach Based on Trade-Offs:

	Full-Custom Design	(Semicustom) Cell-Based Design	(Semicustom) Array-Based Design
Design Parameters			
Cost (Non-Recurring Expense)	1.0	.40–.70	.20–.40
Time (Schedule)	1.0	.40–.60	.20–.40
Production Parameters			
Piece Price (Production Cost)	1.0	1.5–2.0	2.0–2.5
Die Size (Silicon Area)	1.0	1.3–1.6	1.6–2.0

All comparisons are normalized to a full-custom design.

CHOOSE OPTIMUM CMOS OR BIPOLAR PROCESS FOR DESIGNING AND FABRICATING CIRCUITS:

CMOS PROCESS CHART

Process	Type / Features	Production	New Designs	Gate Size (microns)	Digital	Analog	Interconnect Layers: Pitch (microns)	Application Voltage
CB	High Voltage Metal Gate	Yes	No	7.2	Y	Y	Metal 1: 12.5	18V
CF	Supports SSi 6600 Array Family Only	Yes	No	4.0	Y	Y	Metal 1: 10.0 Poly 1: 8.0	7V
CE	Digital CMOS, Supports Controller Group	Yes	Yes	2.0	Y	N	Metal 1: 4.6 Metal 2: 6.0 Poly 1: 4.8	5V
CD	Silicon Gate CMOS, High ohms/square Poly Option, Epi Substrate Available	Yes	Yes	3.5	Y	Y	Metal 1: 8.8 Poly 1: 5.8 Poly 2: 6.4	12V
CH	Silicon Gate CMOS, Same Features as CD Plus Plasma (Dry) Metal Etch	Yes	Yes	3.5	Y	Y	Metal 1: 6.4 Poly 1: 5.8 Poly 2: 6.4	12V
CG	Dual Poly, Dual Metal Silicon Gate	(Development)	Yes	1.5	Y	Y	Metal 1: 5.0 Metal 2: 7.0 Poly 1: 3.6 Poly 2: 5.0	5V

BIPOLAR PROCESS CHART

Process	Type / Features	Production	New Designs	Emitter Size (microns)	Digital	Analog	NPN F_T	Interconnect Layers: Pitch (microns)	BV_{CEO} (volts)
BC	"Standard" Cut Emitter Process	Yes	No	6.0	Y	Y	1 GHz	Metal 1: 14.0 Metal 2: 24.0	12
BJ	High Performance Polysilicon Emitter Structure	Yes	Yes	3.0	Y	Y	3 GHz	Metal 1: 9.0 Metal 2: 14.0	9
BK	Base and Collector Plugs, Improved Lateral PNP's	Yes	Yes	2.5	Y	Y	3 GHz	Metal 1: 9.0 Metal 2: 14.0	12

For a copy of the literature, contact: Silicon Systems or your local representative.

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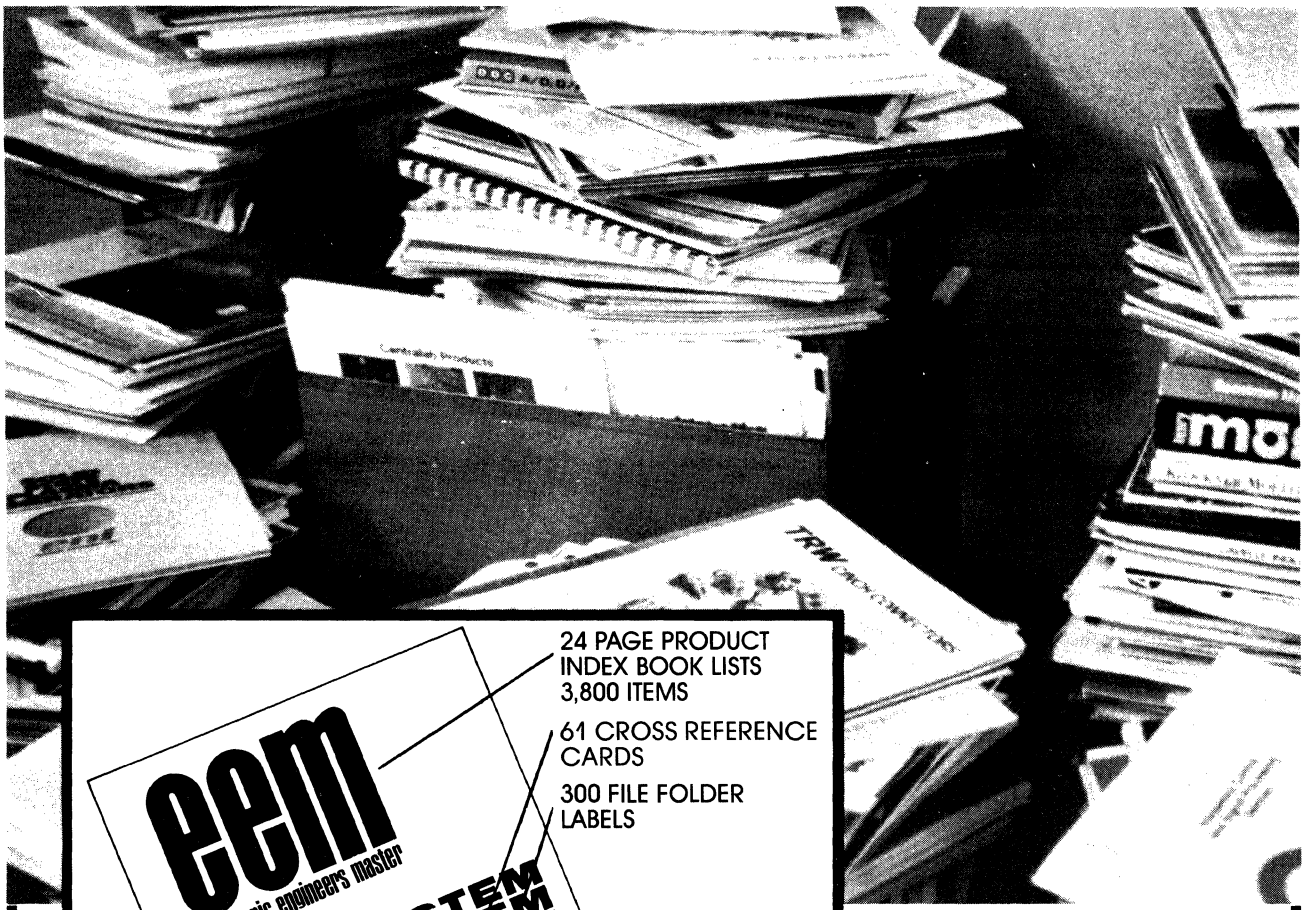

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SPRAGUE PERIPHERAL POWER & DISPLAY DRIVERS

in order of (1) output current, (2) output voltage, and (3) number of drivers

OUTPUTS*			FEATURES							
mA	V	#	SERIAL INPUT	LATCHED DRIVERS	DIODE CLAMP	SAT. OUT.	INTERNAL PROTECT.	PART NUMBER	HERM. AVAIL.	SMD AVAIL.
SINK DRIVERS										
10	20	8	–	X	X	X	–	UCN5881EP	–	X
100	**30**	**32**	**X**	**X**	**–**	**–**	**–**	**UCN5833A**	**–**	**X**
40	**8**	**–**	**–**	**–**	**X**	**–**	**UDN2595A†**	**–**	**X**
40	**32**	**X**	**X**	**–**	**X**	**–**	**UCN5832A**	**–**	**X**
250	70	4	–	–	X	X	–	SERIES UHP400†	X	–
	150	7	–	–	X	–	–	SERIES ULN7003/04A	–	–
300	**50**	**8**	**–**	**–**	**X**	**X**	**–**	**UDN2596/98A**	**–**	**–**
80	**2**	**–**	**–**	**–**	**X**	**–**	**SERIES UDN3160M**	**X**	**–**
80	**2**	**–**	**–**	**X**	**X**	**–**	**SERIES UDN5710M**	**–**	**–**
80	**4**	**–**	**–**	**X**	**X**	**–**	**SERIES UDN5700A**	**X**	**X**
350	50	4	–	X	X	–	–	UCN5800A	X	X
	50	7	–	–	X	–	–	SERIES ULN2000A	X	X
	50	8	–	–	X	–	–	SERIES ULN2800A	X	X
	50	8	–	X	X	–	–	UCN5801A	X	X
	60	16	4 TO 16-LINE LATCHED DECODER/DRIVER					UCN5816A	–	X
	95	7	–	–	X	–	–	SERIES ULN2020A	X	X
	95	8	–	–	X	–	–	SERIES ULN2820A	X	X
	100	8	X	X	–	–	–	SERIES UCN5820A	X	X
	100	8	X	X	X	–	–	SERIES UCN5840A	–	X
	150	4	–	X	X	–	–	UCN5900A	X	–
	150	8	–	X	X	–	–	UCN5901A	X	–
500	**50**	**7**	**–**	**–**	**X**	**–**	**–**	**SERIES ULN2010A**	**X**	**–**
50	**8**	**–**	**–**	**X**	**–**	**–**	**SERIES ULN2810A**	**X**	**–**
600	70	2	–	–	X	X	–	SERIES UDN5740/50M	–	–
700	**60**	**4**	**–**	**–**	**X**	**X**	**X**	**UDN2543B**	**–**	**–**
750	50	8	–	–	X	X	–	UDN2597A	–	–
1000	**70**	**2**	**–**	**–**	**X**	**X**	**–**	**UDN5725M**	**–**	**X**
1250	20	4	STEPPER MOTOR TRANSLATOR/DRIVER				X	UCN4204B	–	–
	50	4	STEPPER MOTOR TRANSLATOR/DRIVER				X	UCN5804B	–	–
	50	4	–	–	X	X	–	UDN2540B	–	–
	80	4	–	X	X	–	–	UCN5813/14B†	–	–
1500	**80**	**2**	**–**	**–**	**X**	**–**	**–**	**ULN2061/62M**	**–**	**X**
80	**4**	**–**	**–**	**X**	**–**	**–**	**SERIES ULN2064/65B**	**X**	**X**
1700	80	3	X	X	X	–	X	UCN5929B	–	–
1750	**80**	**4**	**X**	**X**	**X**	**–**	**X**	**UCN5825/26B**	**–**	**–**
1800	50	4	–	–	X	–	–	UDN2544B	–	–
4000	**80**	**4**	**–**	**–**	**X**	**–**	**–**	**UDN2878/79W**	**–**	**–**
SOURCE DRIVERS										
–25	80	8	–	X	–	–	–	UCN5815A†	X	X
	80	10	X	X	–	–	–	UCN5810AF†	X	X
	80	12	X	X	–	–	–	UCN5811A†	–	–
	80	20	X	X	–	–	–	UCN5812AF†	X	X
	80	32	X	X	–	–	–	UCN5818AF†	X	X
	115	6	–	–	–	–	–	UDN6116A†	–	–
	115	8	–	–	–	–	–	UDN6118/28A†	–	X
–120	**±25**	**8**	**–**	**–**	**X**	**X**	**–**	**UDN2585A**	**–**	**X**
30	**8**	**–**	**–**	**X**	**X**	**–**	**UDN2985A**	**–**	**–**
50	**8**	**X**	**X**	**X**	**X**	**–**	**UCN5895A**	**–**	**X**
–350	35	8	–	–	X	–	X	UDN2987A	–	–
	–80	8	–	–	X	–	–	UDN2580/88A†	X	X
	80	8	–	–	X	–	–	UDN2981-84A	X	X
	80	8	X	X	X	–	–	UCN5890/91A	–	–
–1400	**45**	**1**	**PROTECTED HIGH-SIDE DRIVER**				**X**	**UDN2901Z**	**–**	**–**
–4000	60	4	–	–	X	–	–	UDN2944W	–	–
SOURCE/SINK DRIVERS										
±40	**135**	**10**	**X**	**X**	**–**	**–**	**–**	**UCN5910A**	**X**	**–**
±500	40	4	DUAL FULL-BRIDGE		X	–	–	UDN2993B	–	X
	45	4	DUAL PWM BRIDGE		X	X	X	UDN2916B	–	X
±800	**30**	**3**	**HALF-BRIDGE**		**X**	**X**	**–**	**UDN2933/34B**	**X**	**X**
±1000	28	1	POWER OP AMP		X	–	–	ULN3751Z	–	–
	40	2	DUAL POWER OP AMP		X	–	–	ULN3753/55B/W	–	–
	45	4	STEPPER MOTOR/TRANSLATOR DRIVER				X	UCN5871B	–	X
±2000	**15**	**3**	**HALF-BRIDGE**		**X**	**X**	**X**	**UDN2906W**	**–**	**X**
15	**3**	**HALF-BRIDGE**		**X**	**X**	**X**	**UDN2931B/W**	**–**	**X**
30	**1**	**HALF-BRIDGE**		**X**	**–**	**X**	**UDN2935/50Z**	**–**	**–**
50	**2**	**PWM FULL-BRIDGE**		**X**	**–**	**X**	**UDN2953B/54W**	**X**	**–**
50	**4**	**DUAL FULL-BRIDGE**		**X**	**–**	**X**	**UDN2998W**	**X**	**–**
±3000	45	2	PWM CONTROL		X	–	X	UDN2962B/W	–	X
	45	2	–	–	X	–	X	UDN2974W	–	–
	45	3	3-PHASE BRUSHLESS CONTROL/DRIVER				X	UDN2936/37W	X	–
±4000	**50**	**2**	**PWM CONTROL**		**X**	**–**	**X**	**UDN2965W-2**	**–**	**–**
±8000	50	1	HALF-BRIDGE		X	–	X	UDN2951Z/55W	–	–

**Current is maximum tested condition, voltage is absolute maximum rating.*
†Output ratings shown are for selected units (suffix –1).

For application engineering assistance, write or call
Sprague Semiconductor Group, 115 Northeast Cutoff, Box 15036,
Worcester, MA 01615. Tel. (508) 853-5000.

SPRAGUE

Sprague Electric

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SPRAGUE HALL-EFFECT AND OPTOELECTRONIC SENSORS

UNIPOLAR HALL-EFFECT SWITCHES

Switch Points Max. Operate	Min. Release	Max. Output Ratings	Device Type	Ext. Temp. Available
200 G	50 G	25 mA/25 V	UGN3040T/U	yes
200 G	50 G	25 mA/25 V	UGN3140T/U	yes
350 G	50 G	2x25 mA/17 V	UGN3220K	—
350 G	50 G	25 mA/25 V	UGN3020T/U	yes
350 G	50 G	25 mA/25 V	UGN3120T/U	yes
450 G	25 G	25 mA/25 V	UGN3013T/U	—
450 G	30 G	25 mA/25 V	UGN3113T/U	—
500 G	125 G	25 mA/25 V	UGN3119T/U	yes
500 G	125 G	25 mA/25 V	UGN3019T/U	yes
750 G	100 G	2x25 mA/20 V	UGN3201K	—

BIPOLAR HALL-EFFECT SWITCHES

Switch Points Operate	Release	Max. Output Ratings	Device Type	Ext. Temp. Available
−75/+95 G	−95/+75 G	25 mA/30 V	UGN3131T/U	yes
−130/+150 G	−150/+130 G	25 mA/25 V	UGN3130T/U	yes
−230/+250 G	−250/+230 G	25 mA/25 V	UGN3030T/U	yes

BIPOLAR HALL-EFFECT LATCHES

Switch Points Max. Operate	Max. Output Ratings	Device Type	Ext. Temp. Available
±50 G	25 mA/25 V	UGN3035U	—
±150 G	50 mA/25 V	UGN3077T/U	yes
±150 G	2x50 mA/25 V*	UGN3277K	yes
±150 G	2x1.0 A/14 V*	UDN3625L/M	—
±150 G	2x450 mA/26 V*	UDN3626L/M	—
±150 G	2x500 mA/30 V*	UGN5277K	—
±250 G	2x50 mA/25 V*	UGN3275K	yes
±250 G	50 mA/25 V	UGN3075T/U	yes
±250 G	2x500 mA/30 V*	UGN5275K	—
±350 G	50 mA/25 V	UGN3076T/U	yes
±350 G	2x50 mA/25 V*	UGN3276K	yes
±350 G	2x500 mA/30 V*	UGN5276K	—

**Complementary outputs for brushless dc motor control.*

LINEAR HALL-EFFECT SENSORS

Description	Device Type	Ext. Temp. Available
Differential output 0.06 mV/gauss typ.	UGN3604K	—
Differential output 0.06 mV/gauss typ.	UGN3605K	—
Single-ended output 0.7 mV/gauss typ.	UGN3501T/U	—
Single-ended output 1.3 mV/gauss typ.	UGN3503U	yes
Differential output 1.4 mV/gauss typ.	UGN3501K/L	—

OPTOELECTRONIC SWITCHES

Description	Device Type
Twilight sensor turns ON at 10 uW/cm² typ.	ULN3390D/T
Twilight sensor turns ON at 55 uW/cm² typ.	ULN3330D/T
Twilight sensor turns ON at 55 uW/cm² typ.	ULN3360D/T
Twilight sensor turns OFF at 55 uW/cm² typ.	ULN3363D/T

LINEAR OPTOELECTRONIC SENSORS

Description	Device Type
240 nA/uW/cm² min.	ULN3311D
280 nA/uW/cm² min.	ULN3311T
280 nA/uW/cm² min.	ULN3312D
350 nA/uW/cm² min.	ULN3312T

For application engineering assistance, write or call Sprague Semiconductor Group, 70 Pembroke Rd., Concord, NH 03301. Tel. (603) 224-1961.

SPRAGUE

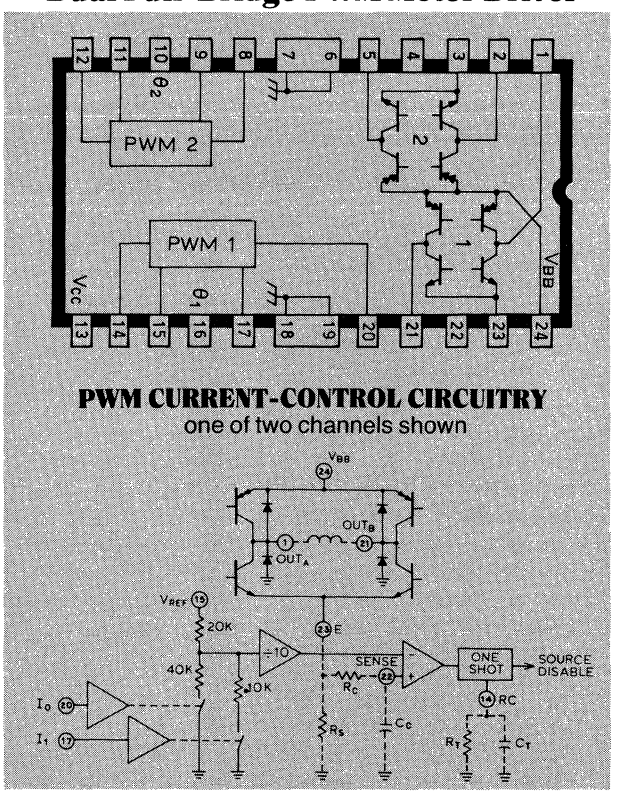
SMART POWER ICs

For Motor Driver Applications

SMART POWER integrated circuits from Sprague Electric combine low-power CMOS, I^2L, or bipolar logic with bipolar or DMOS power drivers. Many devices are specifically intended for driving various types of motors (and other inductive loads) with ratings to ±8 A or 90 V (sustaining) and include current sensing, thermal shutdown, and PWM current control. All motor drivers from Sprague Electric Co. include internal high-current clamp diodes.

UDN2916B

Dual Full-Bridge PWM Motor Driver



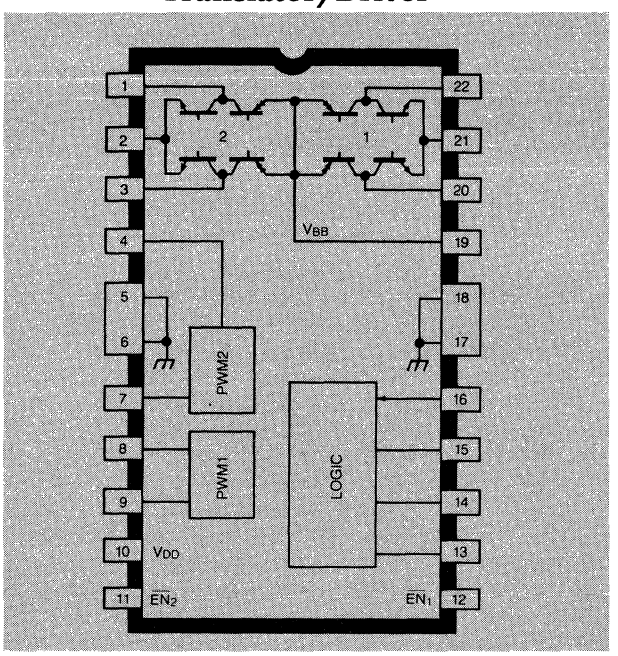
Features:

- ±750 mA continuous output current
- 45 V sustaining
- Internal clamp & flyback diodes
- Internal PWM current control
- Low output saturation voltage
- Crossover-current protected
- Internal thermal shutdown
- Power surface-mount package available
- Similar to dual PBL3717, UC3770

The UDN2916B is designed to drive both windings of a bipolar stepper motor or bidirectionally control two independent dc motors with peak start-up currents to 1 A. With PWM control, load current levels can be digitally-set at 0, 33, 67, or 100% of the user-determined maximum value.

UCN5871B

BiMOS II Stepper-Motor Translator/Driver



Features:

- To ±1 A per phase
- 45 V sustaining
- Wave drive, two-phase, & half-step
- Internal PWM Current Control
- Internal clamp diodes
- Power-ON reset
- Internal thermal shutdown
- Power surface-mount package available

The UCN5871B provides complete control and drive for a two-phase bipolar stepper-motor with continuous output current ratings to ±1 A per phase (1.5 A startup) and will sustain 45 V. The low-power CMOS logic section provides the sequencing logic, direction and output enable control, and the power-ON reset function. Three stepper-motor drive formats are externally selectable. Internal PWM current is user-controllable.

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For application engineering assistance, write or call
Sprague Semiconductor Group, 115 Northeast Cutoff, Box 15036,
Worcester, MA 01615. Tel. (508) 853-5000.

Sprague Electric

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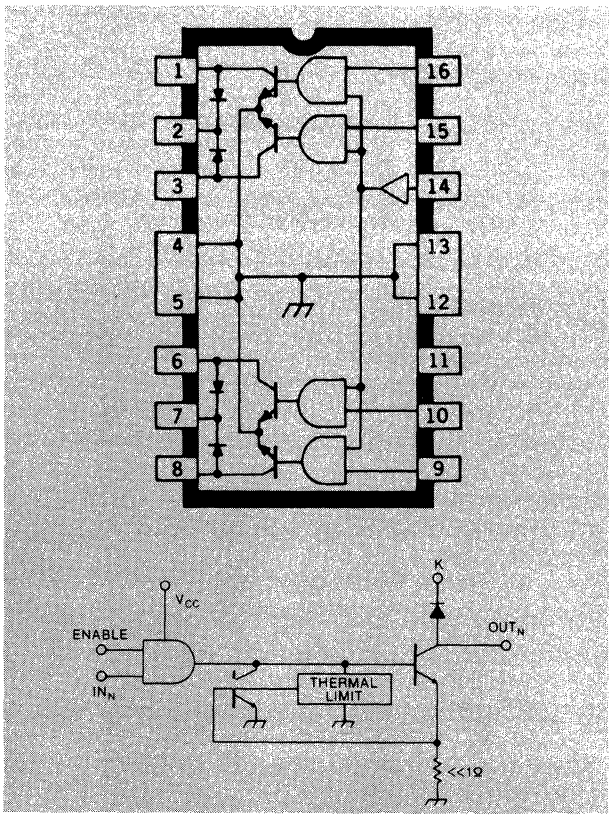
POWER INTERFACE ICs

Sprague power interface ICs provide economical monolithic solutions to interfacing between low-power logic levels and peripheral power loads to 225 V or ±8 A. Many devices include internal clamp diodes for use with inductive loads such as motors, relays, or solenoids; internal logic for serial-to-parallel conversion, decoders, latches, input or output enabling, and commutation or stepping logic for motors; and protection features such as thermal shutdown and current sensing/limiting.

UDN2543B

Quad Nand-Gate Power Driver for Incandescent or Inductive Loads



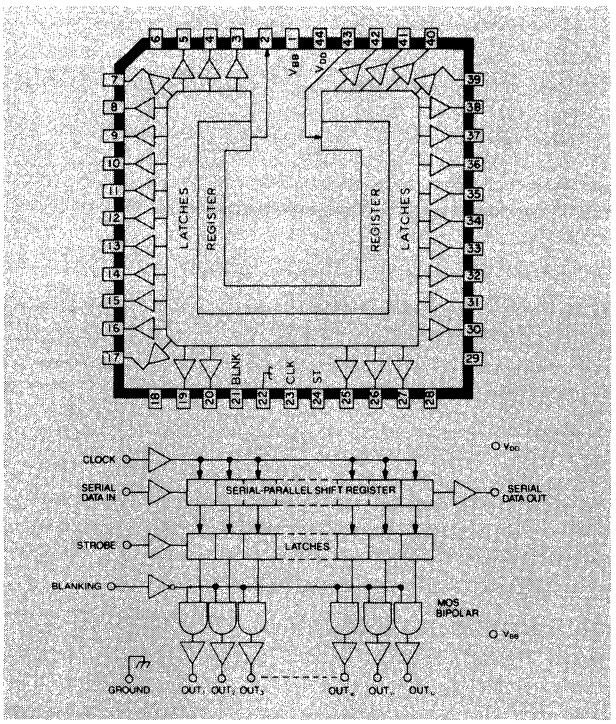
Features:

- To 1 A and 60 V per output
- Over-current limited
- Internal clamp diodes
- Individual thermal limiting

The UDN2543B is a 4-channel driver for use with incandescent lamps, relays, motors, or solenoids. Each channel is independently current and temperature limited to protect the load and driver against turn-on/in-rush current, a stalled motor or shorted filament. Internal high-current clamp diodes and a 35 V sustaining rating provide protection against inductive load transients. In the OFF state, the outputs will withstand up to 60 V.

BiMOS II

High-Speed Serial-Input Latched Drivers with Active DMOS Pulldowns



Features:

- 10-Bit UCN5810AF/LWF (DIP/SOIC)
- 12-Bit UCN5811A (DIP)
- 20-Bit UCN5812AF/EPF (DIP/PLCC)
- 32-Bit UCN5818AF/EPF (DIP/PLCC)
- −25 mA/80 V source outputs
- 15 mA active DMOS pulldowns

"Smart power" BiMOS II drivers combine low-power, high-speed CMOS logic and control circuitry with bi-polar power drivers for load ratings from 25 mA (64 channels) to 2 A (4 channels) or 150 V, or DMOS drivers for operation to 225 V. Typical applications include VF, TFEL, or LED displays; thermal, ink-jet, or impact print heads; stepper motors, and reed relays. Drivers intended for use with inductive loads include internal clamp diodes. Active DMOS pulldowns provide high-speed turn-off and reduced power requirements in display applications.

For application engineering assistance, write or call
Sprague Semiconductor Group, 115 Northeast Cutoff, Box 15036,
Worcester, MA 01615. Tel. (508) 853-5000.

SPRAGUE

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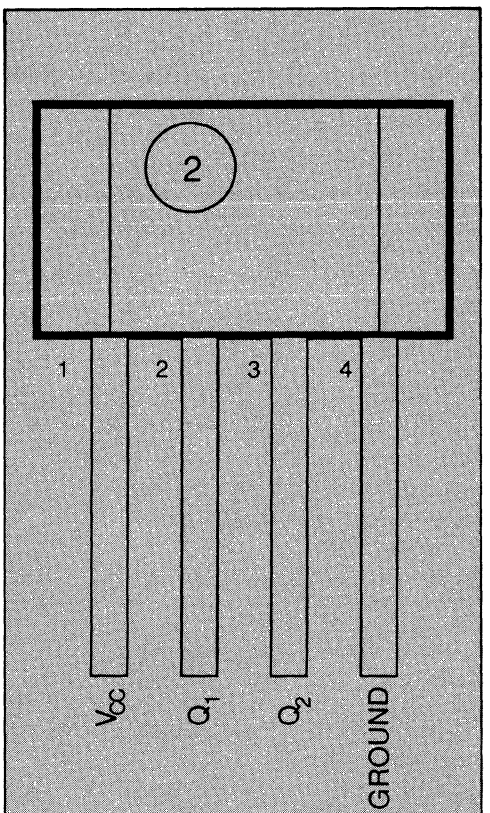
SENSOR INTEGRATED CIRCUITS

UGN3235K AND UGS3235K

DUAL OUTPUT HALL EFFECT SWITCHES



ABSOLUTE MAXIMUM RATINGS
at T_A = +25°C

Power Supply, V_{CC}	29 V
Magnetic Flux Density, B	Unlimited
Output OFF Voltage	25 V
Reverse Polarity Voltage	−30 V
Output ON Current, I_{SINK}	50 mA
Operating Temperature Range,	
T_A UGN3235K	−20°C to +85°C
UGS3235K	−50°C to +125°C
Storage Temperature Range	
T_S	−65°C to +150°C

Sprague Type UGN3235K and UGS3235K Hall effect sensors are bipolar integrated circuits designed for commutation of brushless dc motors, and other rotary encoding applications using multi-pole ring magnets. The devices feature dual outputs which are independently activated by magnetic fields of opposite polarity. The two types share many common characteristics, differing in that the UGN3235K delivers rated performance over a temperature range of −20°C to +85°C, the UGS3235K over −40°C to +125°C.

Each sensor IC includes a Hall voltage generator, two Schmitt triggers, a voltage regulator, dual bipolar-junction output transistors, and on-board reverse polarity protection. The regulator enables these devices to operate from voltages ranging between 4.5 V and 24 V. On-chip compensation circuitry stabilizes the switch points over temperature.

Each open-collector output is independently operated by the proper amount and polarity of incident magnetic flux. Output Q1 responds only to the positive flux from the south pole of a magnet, Output Q2 to the negative flux from the north pole of a magnet. When the sensor experiences the field of a south magnetic pole greater than the maximum operate point of Output Q1, that output switches to the LOW state and Output Q2 is unaffected. When the incident flux falls below the minimum release point for Q1, that output returns to the HIGH state and Output Q2 remains unchanged.

Both the UGN3235K and UGS3235K are supplied in a four-pin plastic single in-line package (SIP) measuring just 0.200 wide × 0.130 high × 0.60 inch thick (5.08 × 3.3 × 1.54 mm).

FEATURES

- Reliable and Rugged Magnetic Sensing Switch
- Dual Outputs Independently Switched by North and South Poles
- Independent Actuation of Outputs Minimizes Inductive-Load Reactive Transient
- Built-in Hysteresis Minimizes Interference from Stray Fields
- Operates from 4.5 V to 24 V
- Outputs Compatible with All Logic Levels
- On-Board Reverse Polarity Protection
- Open Collector, Active Low Outputs

Sprague Electric

SPRAGUE

For application engineering assistance, write or call Sprague Semiconductor Group, 70 Pembroke Rd., Concord, NH 03301. Tel. (603) 224-1961.

When contacting suppliers, say you saw it in IC MASTER

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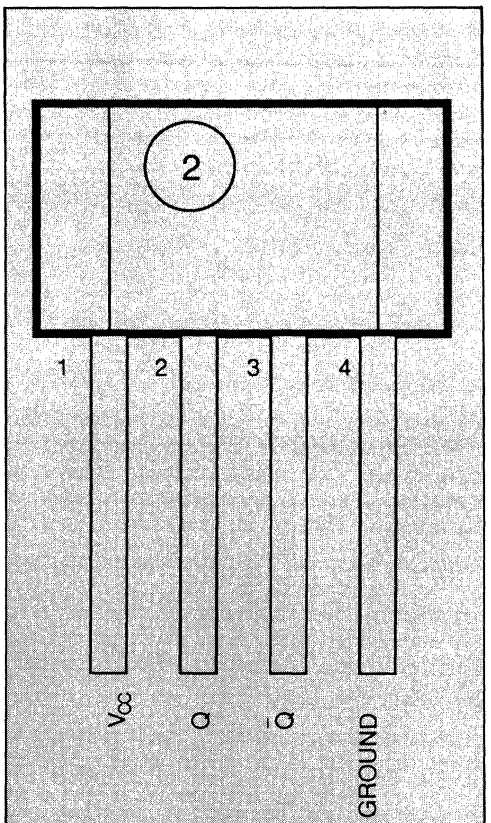
SENSOR INTEGRATED CIRCUITS

UGN5275K THROUGH UGN5277K
COMPLEMENTARY OUTPUT POWER HALL™ LATCHES



ABSOLUTE MAXIMUM RATINGS
at T_A = +25°C

Supply Voltage	14 V
Magnetic Flux Density	Unlimited
Output OFF Voltage	60 V
Output ON Current, I_{SINK}	
Continuous	0.5 A
Peak (Start Up)	0.9 A
Operating Temperature Range, T_A	−20°C to +85°C
Storage Temperature Range, T_S	−65°C to +150°C
Package Power Dissipation, P_D	750 mW

Sprague Type UGN5275K, UGN5276K and UGN5277K latching Hall effect sensors are bipolar integrated circuits designed for electronic commutation of brushless dc motors. All three types feature open-collector complementary power outputs that are capable of sinking up to 300 mA continuously. Increased current ratings, complementary outputs, and sensitive switching points that are stable over temperature and time ideally suit these devices for minimum-component brushless dc motor designs.

This family provides users with the following choice of magnetic response:

Device Type	UGN5275K	UGN5276K	UGN5277K
Operate Point, B_{op}	50 G min 250 G max	50 G min 350 G max	25 G min 150 G max
Release Point, B_{rp}	−250 G min −50 G max	−350 G min −50 G max	−150 G min −25 G max

Each sensor IC includes a Hall voltage generator, an operational amplifier, a Schmitt trigger, a voltage regulator, and large-area dual NPN output transistors. The regulator enables the IC to operate with supply voltages ranging from 4.5 V to 14 V. On-chip compensation circuitry stabilizes switch point performance over temperature. The large bipolar junction output transistors are fed by a unique driver stage which minimizes power dissipation within the IC. The magnetic operation of this device is similar to that of the UGN3275K complementary-output Hall effect latch.

Output Q of the IC switches to the LOW state when the internal Hall generator experiences a magnetic field that exceeds the rated operate point. Output $\bar{Q}$ switches HIGH within one μs of the Output Q change of state. When the device is exposed to a sufficient magnetic field of opposite polarity, Output Q returns to the HIGH state, and Output $\bar{Q}$ returns to the LOW state.

All three devices are rated for operation over a temperature range of −20°C to +85°C, and are supplied in an environmentally rugged, four-pin miniature plastic SIP. Please consult the factory for alternate packaging and custom magnetic requirements.

FEATURES

- High Sink-Current Capability
- Magnetic Sensing, Complementary-Output Latch
- On-Chip Schmitt Trigger Provides Hysteresis
- Temperature-Compensated Switch Points
- Rugged, Low-Profile SIP

Sprague Electric

For application engineering assistance, write or call
Sprague Semiconductor Group, 70 Pembroke Rd.,
Concord, NH 03301. Tel. (603) 224-1961.

SPRAGUE

Stanford Telecommunications

THE STEL-1172B CMOS NCO

(Numerically Controlled Oscillator) is a pin compatible upgrade of the ST-1172A incorporating new performance features.

FEATURES

- ❑ Operates at up to 50 MHz
- ❑ Expanded sine and cosine look-up tables (10 bits of phase resolution)
- ❑ 8-bit sine and cosine or 12-bit phase output
- ❑ Reduced spur levels (-55 dBc)

THE STEL-1173 (48-bit) AND STEL-1174 (16-Bit) CMOS NCOs

generate digital sine or cosine signals with higher precision in every respect than ever before!

FEATURES

- ❑ 50-MHz clock frequency
- ❑ 48-bit or 16-bit frequency resolution
- ❑ 13-bit on-chip phase look-up table
- ❑ 12-bit amplitude resolution
- ❑ Spur levels as low as -70 dBc
- ❑ Selectable sine or cosine output.

THE STEL-1272B AND STEL-1273 SYNTHESIZER BOARDS

use the STEL-1172B and STEL-1173 to drive high-speed, low glitch ECL DACs to generate output signals which are then low-pass filtered to give continuous output waveforms.

FEATURES

- ❑ Anti-aliasing filter (up to 7-poles) can be designed to suit any clock frequency
- ❑ Up to 50 MHz clock frequency (0-70°C)
- ❑ Up to 23 MHz output frequency with 50 MHz clock

THE STEL-2110 BIT SYNCHRONIZER/PSK DEMODULATOR

provides bit timing to control the sampling of the signal in a receiver as well as a feedback signal to control the frequency of the local oscillator. It can be used in high speed coherent PSK, QPSK and DPSK modems in either continuous carrier or burst carrier environments. Soft decision output data is provided to facilitate the inclusion of Forward Error Correction (FEC) using convolutional coding and Viterbi decoding into the system.

FEATURES

- ❑ Up to 6 Mbps operation in BPSK mode and 12 Mbps in QPSK mode
- ❑ Carrier tracking feedback with PLL or AFC outputs
- ❑ Bit timing driven by NCO
- ❑ Programmable 2nd order loop
- ❑ Programmable data rates
- ❑ DPSK output available

THE STEL-2210 BLOCK PHASE ESTIMATOR

provides a phase reference for demodulating BPSK (binary PSK) or QPSK (quadrature PSK) data in the presence of phase roll (frequency offset). The device generates an averaged phase reference without using a phase-locked loop, so that the phase acquisition time is very short. This makes the device ideal for use in burst-mode systems. The device operates on 6-bit soft decision data and is suitable for use with Forward Error Correction (FEC) systems using convolutional coding and Viterbi decoding.

FEATURES

- ❑ Up to 6 Mbps operation in BPSK mode and 12 Mbps in QPSK mode
- ❑ Compensates for frequency offset of up to 0.6% of symbol rate at E_b/N_o of up to 4 dB

THE STEL-1023 C/A CODER

generates the C/A (Clear/Aquisition) codes and other timing information required in GPS (Global Positioning System) receivers. Two outputs are available, one of which can be dithered independently of the other. Timing outputs are available at 1.023 MHz, 1 KHz, 50 Hz and 2/3 Hz. The 1 KHz and 50 Hz output phasing may be synchronized to external inputs.

FEATURES

- ❑ Generates C/A and PRN codes
- ❑ Generates all timing

OTHER CUSTOM PRODUCTS AVAILABLE:

STEL-2172	ECL Numerically Controlled Oscillator
STEL-9172	NCO Evaluation Board
STEL-9272	130 MHz Digital Direct Synthesizer
STI-2003	Complex Multiplier/Accumulator
STI-2010	Viterbi Decoder
STEL-2012	Convolutional Encoder
STI-5268	Convolutional Encoder/Viterbi Decoder
STEL-9268	Serial Viterbi Decoder
STEL-68020	MultiBus Single Board Computer

For further information on any of these products, call or write:

Patti Laakso
STANFORD TELECOMMUNICATIONS
2421 Mission College Blvd.
Santa Clara, CA 95054-1298
Telephone: (408) 980-5684
FAX: (408)980-1066

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Dual High Speed MOSFET Driver TSC1426/1427/1428

General Description

The TSC142X series of MOSFET drivers are low power consumption CMOS MOSFET drivers designed for low cost and increased latch-up protection. This family of drivers is made using an epitaxial layer to effectively short the intrinsic CMOS parasitic PNP transistor responsible for SCR latch-up. Compatible with the bipolar DS0026, quiescent current is five times lower. The high input impedance TSC142X series drivers are CMOS/TTL input compatible so speed-up capacitors are not required. These units come in inverting and non-inverting configurations.

Features

- **Low Cost**
- **Latch Up Protected. Will Withstand 500 mA Reverse Output Current**
- **High Peak Output Current ..... 1.2 A peak**
- **High Capacitive Load Drive Capability ..... 1000 pF in 35 nS**
- **Wide Operating Range ..... 4.75 V to 18 V**
- **Low Delay Time ..... 80 nS max.**
- **Logic Input Threshold Independent of Supply Voltage**
- **Output Voltage Swing to Within 25 mV of Ground or V_{S+}**
- **Low Output Impedance ..... 8 Ω**
- **Pin Compatible to DS0026 & MMH0026**
- **TTL/CMOS Input Compatible**
- **Low Supply Current & Low Quiescent Current ..... 8 mA with Logic "1" Input ..... 400 μA with Logic "0" Input**
- **Low Output Impedance**
- **Available in Inverting & Non-Inverting Configurations**
- **ESD Protected ..... ±2 KV**

Selecting MOSFET Drivers

Device	Peak Drive Current (Amp)	-OUTPUTS- No.	Type Invert	Type Non-Invert	Test Load (pF)	Rise Time†† (nS)	Fall Time†† (nS)	Delay Low to High (nS)	Delay High to Low (nS)	Latch-Up Proof	Input Voltage Range	Surface Mount Package Option	Avail.
TSC1426	1.2	2	■		1000	30	20	55	80	YES	Gnd to V^+	Yes	NOW
TSC1427	1.2	2		■	1000	30	20	55	80	Yes	Gnd to V^+	Yes	NOW
TSC1428	1.2	2	■	■	1000	30	20	55	80	YES	Gnd to V^+	Yes	NOW
TSC426;*	1.5	2	■		1000	30	20	40	75	4Q88	Gnd to V^+	Yes	NOW
TSC427;*	1.5	2		■	1000	30	20	40	75	4Q88	Gnd to V^+	Yes	NOW
TSC428;*	1.5	2	■	■	1000	30	20	40	75	4Q88	Gnd to V^+	Yes	NOW
TSC4426	1.5	2	■		1000	25	25	18	38	YES	-6V to V^+	Yes	4 Qtr. 88
TSC4427	1.5	2		■	1000	25	25	18	38	YES	-6V to V^+	Yes	4 Qtr. 88
TSC4428	1.5	2	■	■	1000	25	25	18	38	YES	-6V to V^+	Yes	4 Qtr. 88
TSC00C26	1.5	2	■		1000	20	20	7.5	12	YES	Gnd to V^+	Yes	1 Qtr. 89
TSC4423	3.0	2	■		2200	25	25	18	38	YES	-6V to V^+	Yes	4 Qtr. 88
TSC4424	3.0	2		■	2200	25	25	18	38	YES	-6V to V^+	Yes	4 Qtr. 88
TSC4425	3.0	2	■	■	2200	25	25	18	38	YES	-6V to V^+	Yes	4 Qtr. 88
TSC430	3.0	1	†		2200	35	35	15	15	YES	Gnd to V^+	Yes	NOW
TSC429*	6.0	1	■		10000	70	80	53	60	2Q89	Gnd to V^+	No	NOW
TSC4420	6.0	1		■	10000	70	80	18	38	YES	-6V to V^+	Yes	4 Qtr. 88
TSC4429	6.0	1	■		10000	70	80	18	38	YES	-6V to V^+	Yes	4 Qtr. 88

*Available with 883 processing **Available to DESC drawing †Complimentary outputs ††At test load

Teledyne Semiconductor

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TSC38C42/TSC38C43
TSC172/TSC173

CMOS Current Mode SMPS Controller

General Description

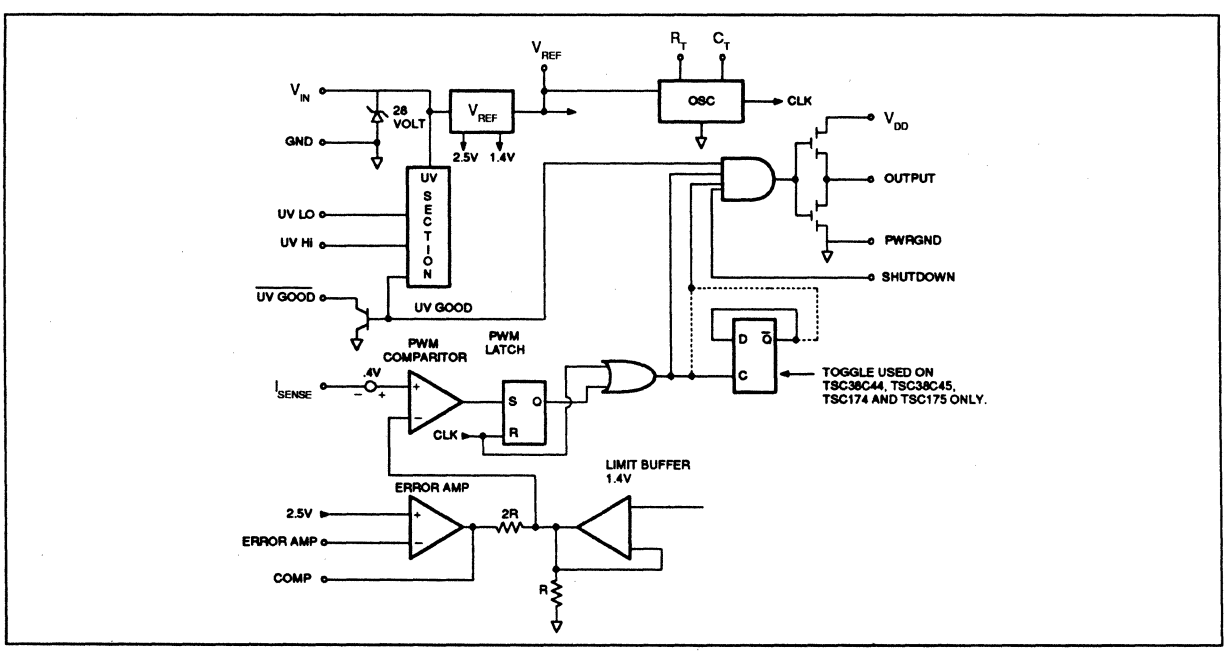
The TSC38C42/43 and TSC172/173 are current mode CMOS PWM control ICs. With a low 1.5 mA supply current along with the high drive currents, 1.2 A typical, the TSC38C42/43 provide a low cost solution for many PWM needs since they can be driven without a 50-60 Hz transformer and can directly drive MOSFETs up to HEX 3 size.

The TSC38C42/43 are pin compatible with earlier bipolar products so that designers can easily update older designs. A number of improvements have been added though. For example, clock ramp reset current is specified at 1 mA ±10% for accurate deadtime control.

The TSC172/173 adds additional features. The TSC172/173 comes in an 14 pin package instead of an 8 pin. This allows a linear timing ramp for the clock (instead of exponential), user adjustable undervoltage start and hysterisis levels as well as separate output drive and control grounds. In addition the TSC172 offers a separate shutdown pin for fast output shutdown while the TSC173 offers an open collector output pin that pulls low when the user adjusted under voltage lockout drops out.

Features

- **Low Power CMOS Construction**
- **Low Supply Current ..... 1.5 mA Typ**
- **Wide Supply Voltage Operation 8.0 to 28 Volts**
- **Latch-Up Immunity ..... 500 mA on Outputs**
- **Above and Below Rail Input Protection 6 Volts**
- **High Output Drive ..... 1.2 A Peak**
- **Current Mode Control**
- **Fast Rise/Fall Time ..... 30 nS @ 1000 pf**
- **High Frequency Operation ..... 500 KHz**
- **Clock Ramp Reset Current ..... 1 mA 10%**
- **Fixed UV Lockout TSC38C42/43 ..... 16 V/8 V**
- **Adjustable UV Lockout TSC172/173**
- **Adjustable UV Hysterisis TSC172/173**
- **Shutdown Pin Available on TSC172**
- **UV Lockout Pin Available on TSC173 ..... 30 V Open Collector**
- **99% Duty Cycle Limited**
- **Soft Start**
- **Low Prop Delay Current Amp to Output ..... < 250 nS Typ**
- **Low Prop Delay Shutdown to Output ..... < 200 nS Typ**
- **TSC38C42/43 Pin Compatible with Unitrode UC3842/3843**



TSC38C42–45/TSC172–175 Block Diagram

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Single High Speed High Current MOSFET Driver

TSC4420/4429

General Description

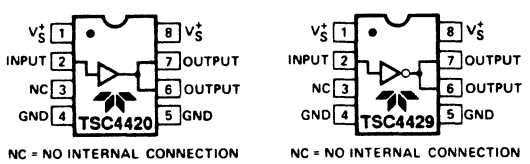
The TSC4420/29 series of MOSFET Drivers are the latest generation of low power consumption single high current CMOS drivers. Tough CMOS™ Drivers are tough, efficient and easy to use. Important features of this new series are:

- Latch-up Protection,
- Input Protection to 6 volts below rail,
- Matched Rise and Fall times,
- Reduced Delay time,
- ESD Protected to 2 KV.

These drivers are fabricated in CMOS for low power consumption, and high efficiency. They are easy to drive, and do not need speed-up ceps or register divider strings needed by other devices.

The TSC4420/29 can drive even the largest MOSFET with low rise and fall times for high power supply efficiency.

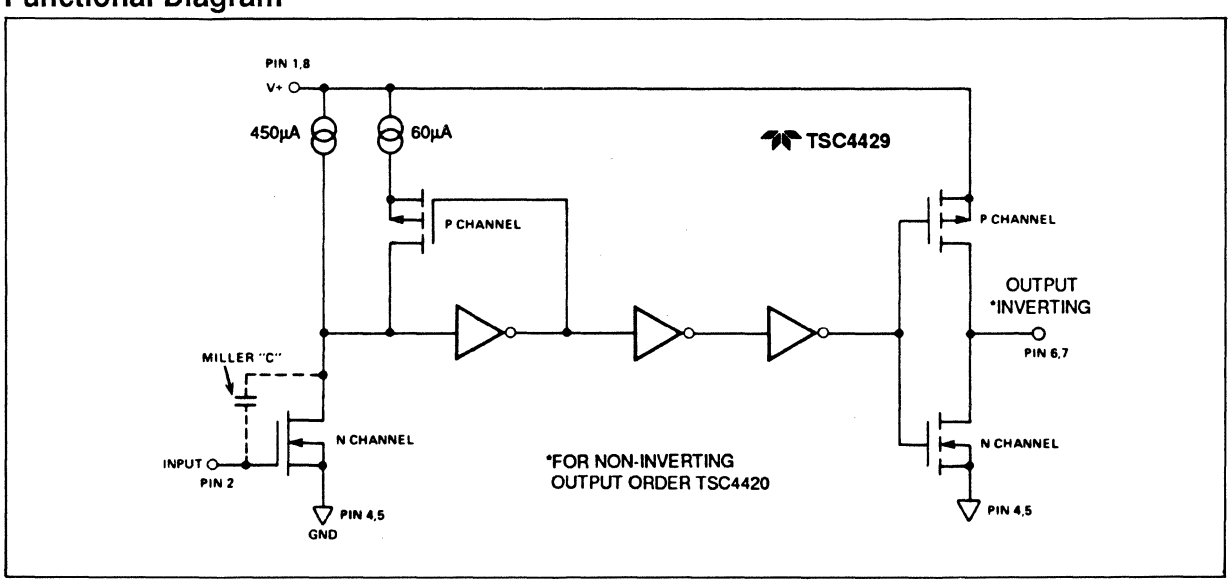
Pin Configurations



Features

- **Latch up protected. Will withstand 500 mA reverse output current**
- **Below Rail Input Transient Protection 6 V, Max.**
- **ESD Protected ..... ±2 KV**
- **Matched Rise and Fall times ..... 25 nS**
- **High peak output current ..... 6.0 A peak**
- **High Capacitive Load Drive Capability ..... 10000 pF in 60 nS**
- **Wide Operating Range ..... 4.5 V to 18 V**
- **Low Delay Time ..... 50 nS max.**
  –Rise Time, Typ ..... 18 nS
  –Fall Time, Typ ..... 38 nS
- **Consistant delay times with changes in voltage drain source**
- **High Impedance TTL/CMOS Input Compatible**
- **Logic Input Threshold Independent of Supply Voltage**
- **Low Supply Current**
  –5 mA with logic 1 input
  –350 µA with logic 0 input
- **Low Output Impedance ..... 2.5 Ω**
- **Output Voltage Swing to Within 25 mV of Ground or V_S+**
- **Available in Inverting & Non-Inverting Configurations**

Functional Diagram



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TSC170/171 CMOS Current Mode SMPS Controller

General Description

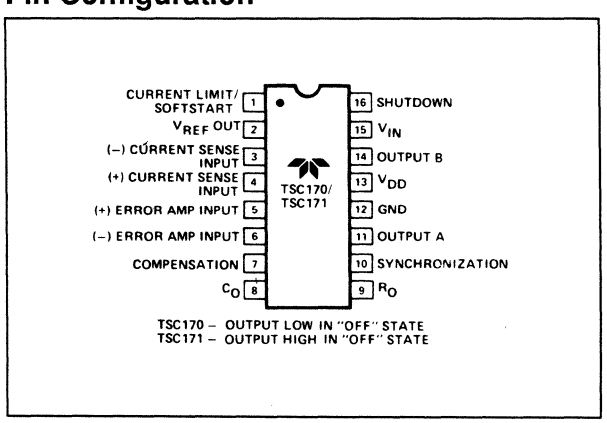
The TSC170/171 brings low power CMOS technology to the current mode switching power supply controller market. Maximum supply current is 3.8 mA. Bipolar current mode control integrated circuits require five times more operating current. Low power supply current eliminates auxiliary power transformers. In off line powering schemes where a simple zener diode circuit provides device supply voltage, power dissipation is greatly reduced. CMOS technology decreases system cost, increases power efficiency, reduces heat generation, and increases total system reliability.

The dual totem pole CMOS outputs drive power MOSFET or biploar transistors. The 50 nS typical output rise and fall times with a 1000 pF capacitive load minimize power MOSFET transition power dissipation. Output peak current is 300 mA.

The TSC170/171 contains a full array of system protection circuits. The undervoltage lockout circuit forces outputs OFF if the supply voltage drops below 7.0 Volts. A soft start feature is also available. The soft start option forces the PWM outputs to initially operate at a minimum duty cycle and low peak output current. The TSC170/171 can be directly turned OFF through a remote shutdown control pin. The shutdown mode can be latched (power must be turned OFF to restart system) or nonlatched. The soft start feature can also be used in system shutdown application. Double output pulse suppression guarantees output drive pulses always alternate from one output driver to the other. Peak current is adjustable by the user.

Current mode control lets users parallel power supply modules. Two or more TSC170/171 controllers can be slaved together for parallel operation. Circuits can operate from a master TSC170/171 internal oscillator or an external system oscillator.

Pin Configuration



The TSC170/171 operates from an 8 V to 16 V power supply. An internal 2% 5.1 V reference minimizes external component count. The TSC170/171 is pin compatible with the Unitrode UC1846/2846/3846 and UC1847/2847/3847 bipolar controllers.

Other advantages inherent in current mode control include superior line and load regulation and automatic symmetry correction in push-pull converters.

Features

- **Low Supply Current with CMOS Technology .. .. 3.8 mA Max**
- **Current Mode Control**
- **Internal Reference ..... 5.1 V**
- **Fast Output Rise/Fall Time (C_L = 1000 pF) ..... 50 nS**
- **Dual Push-Pull Outputs**
- **Direct Power MOSFET Drive**
- **High Totem Pole Output Drive ..... 300 mA**
- **Differential Current Sense Amplifier**
- **Programmable Current Limit**
- **Soft Start Operation**
- **Double Pulse Suppression**
- **Under-Voltage Lockout**
- **Wide Supply Voltage Operation ..... 8 to 16 V**
- **High Frequency Operation ..... 200 kHz**
- **Plastic and CerDIP Package**
- **Available with Low (TSC170) or High (TSC171) "OFF" State Outputs**
- **Low Power, Pin Compatible Replacement for UC3846/3847**

Ordering Information

Part No.	Package	Temp. Range
TSC170CPE	16-Pin Plastic DIP	0 to 70°C
TSC170IJE	16-Pin CerDIP	-25 to 85°C
TSC170MJE	16-Pin CerDIP	-55 to 125°C
TSC171CPE	16-Pin Plastic DIP	0 to 70°C
TSC171IJE	16-Pin CerDIP	-25 to 85°C
TSC171MJE	16-Pin CerDIP	-55 to 125°C
TSC170Y	Chip	-
TSC171Y	Chip	-

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High Current DC-DC Converter

TSC962

General Description

The TSC962 is an advanced version of the industry standard 7662 high voltage DC to DC converter. Using improved design techniques and CMOS construction, the TSC962 can source as much as 80 mA vs the 7662 20 mA capability.

As an inverter, the TSC962 can put out voltages as high as 18 volts and as low as 3.5 volts without the need for external diodes. The output impedance of the device is a low 28Ω (with the proper capacitors), voltage conversion efficiency is 99.9% and power conversion efficiency is 97%.

The low voltage terminal, pin 6, required in some 7662 applications has been eliminated. Grounding this terminal will double the oscillator frequency from 12 to 24 kHz. This will allow the use of smaller capacitors for the same output current and ripple in most applications. Only two external capacitors are required for inverter applications. In the event an external clock is needed to drive the TSC962 (such as paralleling) driving this pin directly will cause the internal oscillator to sync to the external clock.

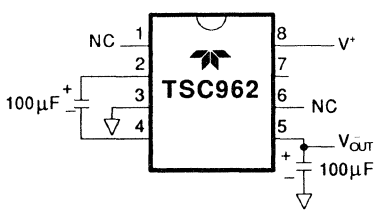
Features

- **Pin Compatible with TSC7662/ICL7662/SI7661**
- **High Output Current 80 mA**
- **No External Diodes Required**
- **Wide Operating Range 3.0 to 18 Volts**
- **Low Output Impedance 28Ω Typical**
- **No Low Voltage Terminal Required**
- **Application Zener On Chip**

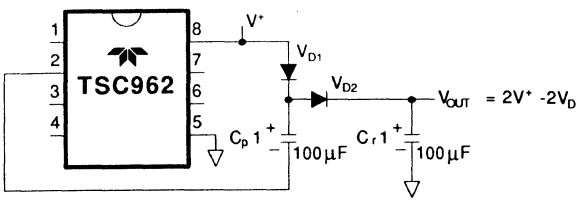
Ordering Information

Part No.	Package	Temp. Range
TSC962CPA	8-Pin Plastic DIP	0 to 70°C
TSC962IJA	8-Pin CerDIP	-40 to 85°C
TSC962MJA	8-Pin CerDIP	-55 to 125°C
TSC962COE	16-Pin SO	0 to 70°C
TSC962/Y	Chip	25°C Only

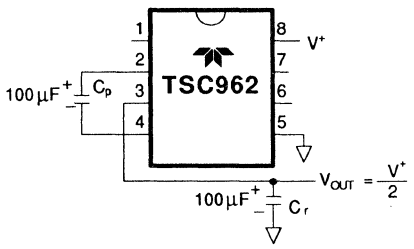
Typical Applications



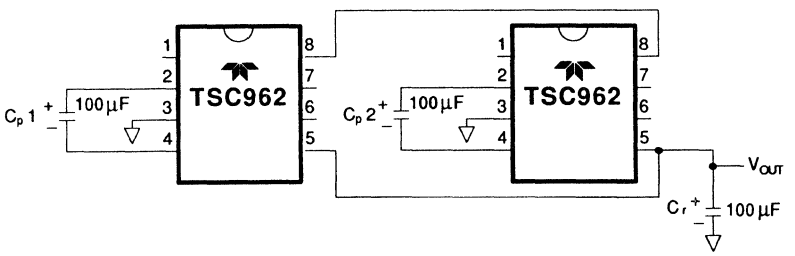
SIMPLE NEGATIVE CONVERTER



POSITIVE VOLTAGE MULTIPLIER



SPLIT V+ IN HALF



LOWERING OUTPUT RESISTANCE BY PARALLELING DEVICES

Teledyne Semiconductor

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TSC850

Fast 16-Bit Monolithic CMOS Analog-To-Digital Converter

General Description

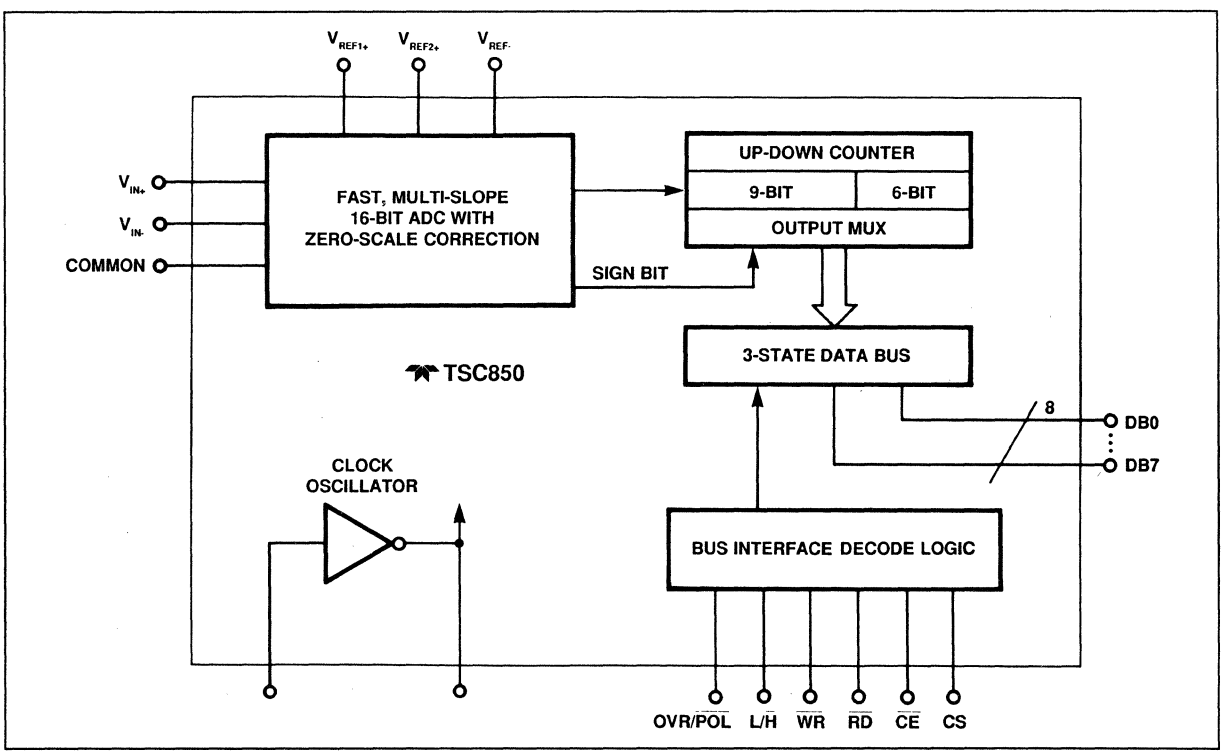
The TSC850 is a monolithic CMOS ADC with resolution of 15 bits plus sign. A novel multislope integration technique to increases conversion speed, resulting in a 16 times improvement in speed over previous 15 bit monolithic integrating ADCs.

The TSC850 incorporates an A-D converter, µP compatible digital interface, and crystal oscillator on-chip. Only a voltage reference, crystal, and a few noncritical passive components are required to form a complete 15-bit plus sign A-D conversion system.

Input sensitivity of 100 µV per LSB eliminates the need for precision external amplifiers. The internal amplifiers are auto-zeroed, which guarantees a zero digital output with 0 V analog input, making zero adjustment pots and calibrations unnecessary.

Features

- **15-bit Resolution Plus Sign Bit Integrating A/D Converter**
- **Up to 40 Conversions per Second**
- **Bus Compatible, 3-State Data Outputs**
  - **–8-bit Data Bus**
  - **–Continuous or On-Demand Conversions**
  - **–Data Valid Output**
  - **–Two Chip Enables**
  - **–Read A/D Converter Result Like Memory**
- **On-Chip Crystal Oscillator**
- **±5 V Power Supply Operation**
- **Low Power ..... 20 mW**



Block Diagram

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12 Bit μP-Compatible A/D Converter with Analog Mux

TSC804

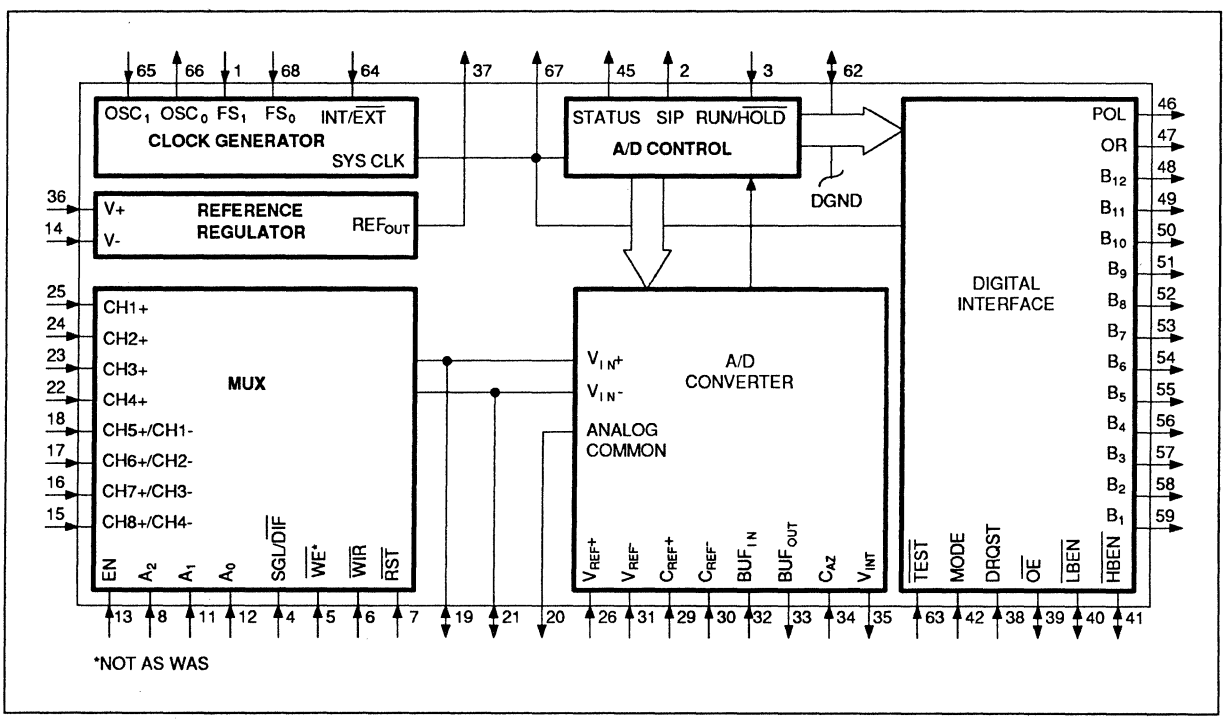
General Description

The TSC804 is a 12-bit plus sign and overrange analog to digital converter. The TSC804 is equivalent to the popular TSC7109 except that it incorporates an on-board analog multiplexer which may be configured for either 4 or 8 channel operation under software control. The TSC804 represents the latest technology in multi-slope, high noise immunity, integrating A/D conversion. The advanced CMOS design offers very low power consumption and high reliability.

The TSC804 provides two very flexible modes of digital interfacing to fit a variety of system configurations. The Handshake Mode supports either fast or slow UART interfacing with either triggered or continuous operation. The Direct Output Mode supports microprocessor systems that use a direct bus architecture with either an 8-bit or 16-bit data bus structure.

Features

- **12 Bit Plus Sign, High Accuracy A/D Converter**
- **On Board Analog Multiplexer**
- **Analog Mux Expansion Capability**
- **Programmable Conversion Rate– Up to 30 Conversions per Second**
- **Very Fast Overload Recovery**
- **High Impedance Differential Input**
- **Low Noise CMOS Design ..... 15 μVP-P**
- **Low Input Leakage Current ..... 10 pA (Max)**
- **Flexible Digital and μProcessor Interfacing**
- **Internal Reference Regulator ..... 50 ppm/ °C**
- **Power Up to Known State**
- **Crystal Controlled Clock Circuit**
- **Available in Compact Flat Package or PLCC**
- **Industrial Temperature Range Device Available**



Functional Block Diagram

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TSC901 TSC903 TSC904 Low Noise Auto-Zeroed Monolithic Single, Dual, Quad Operational Amplifiers

General Description

The TSC901, TSC903, and TSC904 are CMOS, single, dual and quad chopper stabilized op amps, respectively. This second generation design of the TSC911 series offers high voltage operation with on chip nulling capacitors. Industry standard pin-outs allow the TSC901,TSC903 and TSC904 to upgrade system performance by dropping into existing sockets. Fast recovery from saturation without an external clamp, low noise, and low parts count circuits are additional features of this unique family of amplifiers.

Features

- **High Voltage, ±15 V or 5 V to 32 V Supplies**
- **No External Capacitors Required**
- **7 Microvolts Offset Voltage**
- **5 Microvolts (@ 10 Hz Bandwidth) Noise**
- **450 µA Supply Current**
- **140 dB CMRR**
- **140 dB Open Loop Gain**
- **Pin Out Compatible with ICL7650(TSC901)**

TSC76HV52 High Voltage, Low Noise, Chopper-Stabilized Operational Amplifier

General Description

The TSC76HV52 is a chopper-stabilized CMOS op amp designed to provide low noise, low offset, and low bias current while operating from ±15 V supplies. Designed as a substitute for the 7652 in high voltage applications, the TSC76HV52 offers reduced power dissipation, wider common mode voltage and greater output current drive capability.

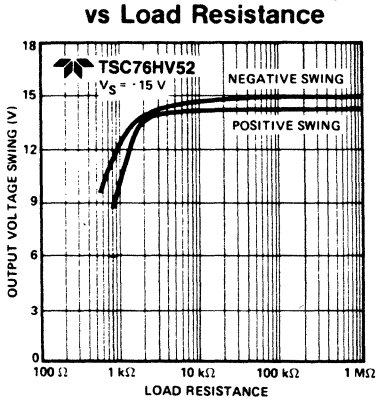
Features

- **High Voltage Operation ..... ±15 V**
- **Low Noise (0 to 1Hz) ..... 0.2 μV_{P-P}**
- **Low Supply Current ..... 1 mA**
- **Low Offset Voltage ..... 10 µV**
- **Single or Dual Supply Operation**
- **Pin Compatible to 7652**
- **Wide Common Mode Voltage ... V_S^- to V_S^+ -2 V**

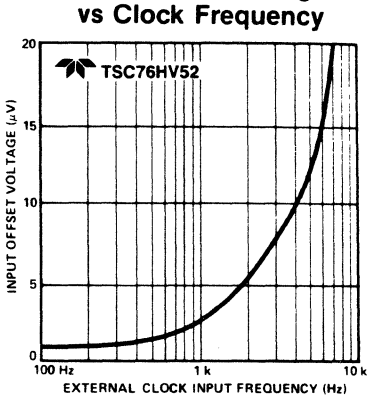
Comparison

Parameter	TSC76HV52	TSC7652CPD
Input noise	0.2 μV_{P-P}	0.2 μV_{P-P}
Operating voltage	7 to 32 V	5 to 16 V
Max supply current	1.5 mA	3.5 mA
Negative common mode voltage	V_S^-	V_S^- + 0.7V
Single supp operation	Yes	No
Operating temp	-25 to =85°C	0 to 70°C
Hermetic package	Yes	No

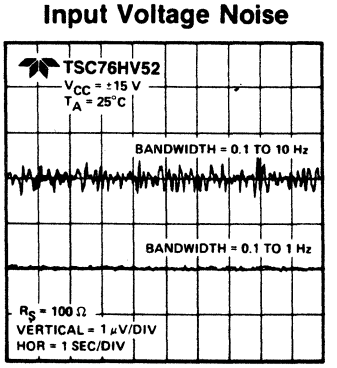
Output Voltage Swing vs Load Resistance



Input Offset Voltage vs Clock Frequency



Input Voltage Noise



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Processor Compatible CMOS Analog Switches

TSC441 TSC442 TSC443

General Description

The TSC441, TSC442 and TSC443 are CMOS quad SPST analog switches with data address latches. The switch family features single or dual logic supply operation with analog input range equal to the supply voltage. The CMOS design requires very low supply current. The pin-out matches the "201/221" configuration, and the address latch is transparent when WR is tied low.

Features

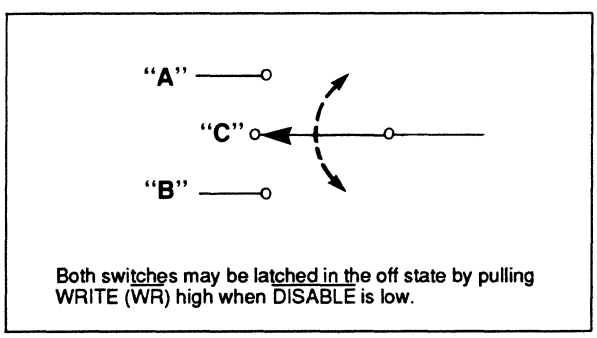
- **Data Address Latches On-Chip**
- **Dual ±5 V or Single +5 V to +15 V Supplies**
- **95 Ω on Resistance**
- **1 nA Leakage Current**
- **Rail to Rail Switching**
- **200 nS Switching Time**
- **Pin Compatible to DG221, DG201**
- **TTL/CMOS Compatible**

Processor Compatible CMOS 3 Position Analog Switch

TSC444

General Description

The TSC444 is configured as two single-pole, 3 position switches. Either switch can be independently selected (transparent or latched) for its own SPDT operation. Also, both switches are put in "everything open" condition by pulling the Disable input low. This switch is especially useful in multi-path operations that require complete isolation.



Switch Circuit

Features

- **2 Single Pole, 3 Position Switches**
- **Data Address Latch on Chip**
- **Dual ±5 V or Single +5 V to +15 V Supplies**
- **120 Ω on Resistance**
- **Low Power CMOS**
- **Rail to Rail Switching**
- **200 nS Switching Speeds**
- **TTL/CMOS Compatible**
- **Pin Compatible with AD 7592**

Teledyne Semiconductor

TSC445 TSC446 TSC447

Processor Compatible CMOS Analog Switches

General Description

The TSC445, TSC446, and TSC447 Series is a family of quad CMOS analog switches that offer superior performance at logic power supply voltages. Each provides for either transparent (non-latched) or latched address, making them ideal for µ processor applications. The switches operate from single or dual supplies and require low supply current.

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Features

- **Data Latches on Chip**
- **+5 V Only Operation**
- **120 Ω on Resistance**
- **Rail to Rail Analog Switching**
- **Mixed - 2 NO, 2 NC Switches (TSC447)**
- **Transparent Latch with WR = 0**
- **1 nA Leakage Current**
- **Pin Compatible AD7590/AD7591**

TSC4201 TSC4202 TSC4203

Low Cost Analog Switches

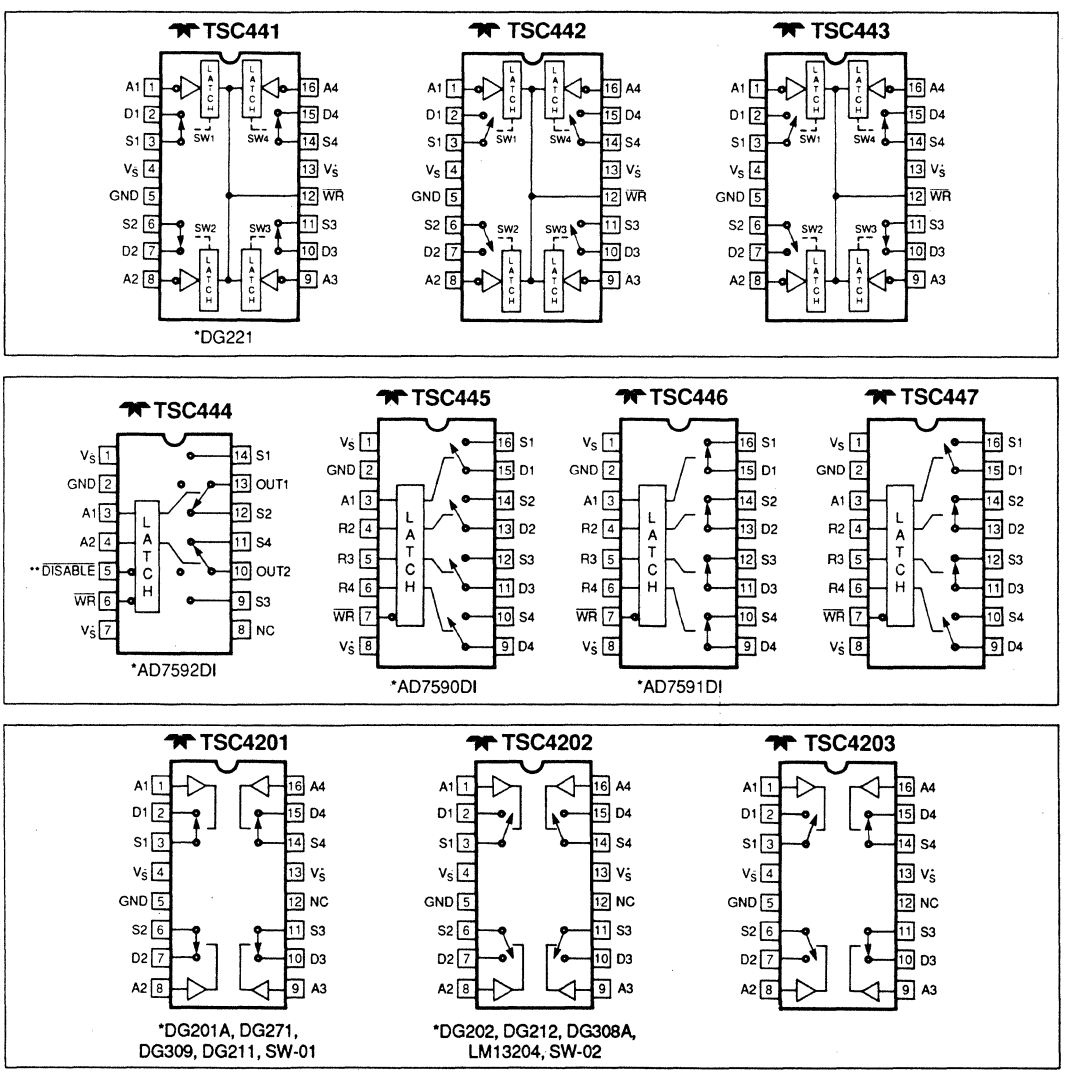
General Description

The TSC4201, TSC4202 and TSC4203 are quad CMOS analog switches identical with the TSC44X switch family but without the data latches. Switch configurations include quad normally open, quad normally closed and mixed, where two switches are normally open and two are normally closed providing convenient SPDT and DPST operation.

Features

- **Dual +5 V or Single +5 to +15 V Supplies**
- **Analog Signal Range Equal to Supply Voltage**
- **TTL/CMOS Compatible**
- **120 Ω on Resistance**
- **Pin Compatible to DG201 (TSC4201)**
- **Pin Compatible to DG202 (TSC4202)**
- **TSC4203 - 2 Normally Open , 2 Normally Closed**

Complete Switch Family



Notes:
All switches shown with A_N= 0.
* Pin compatible with part above. The parts may not be electrically compatible.
** Internally pulled high.

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3 3/4 Digit A/D Converter with Frequency Counter

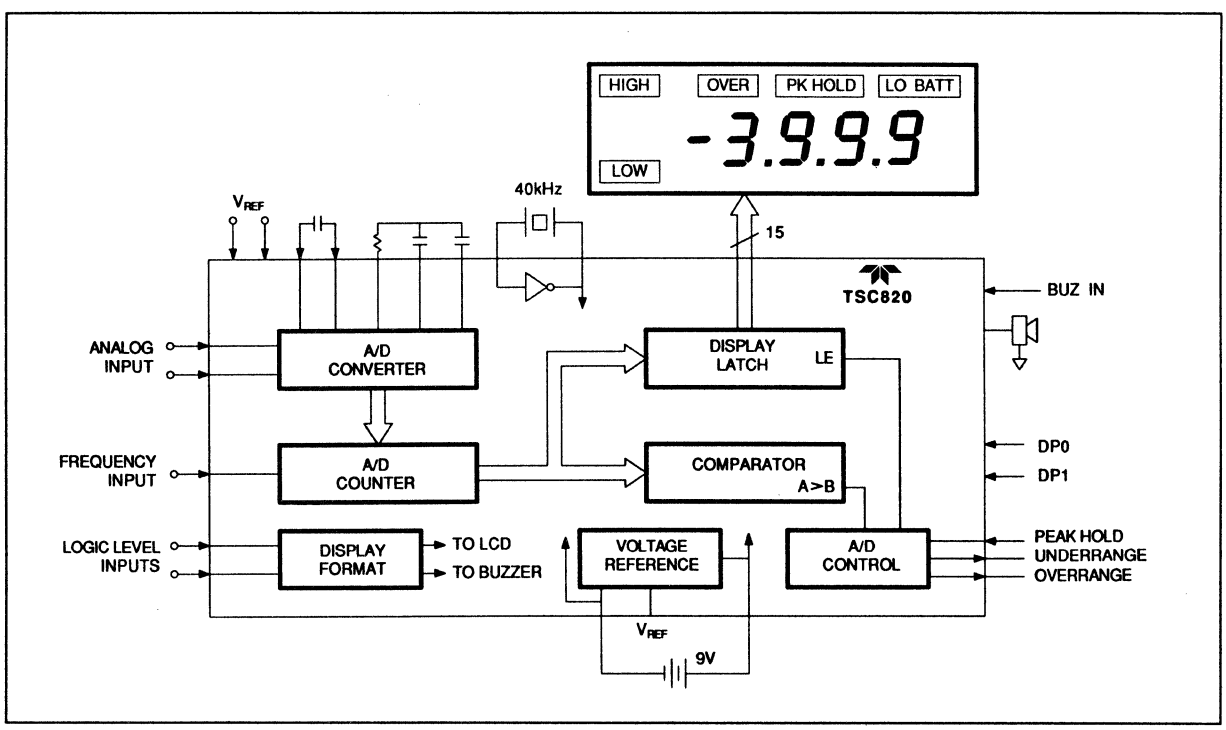
TSC820

General Description:

The TSC820 is a low power CMOS measurement system IC which includes both a 3 3/4 digit analog to digital converter and a frequency counter function. To further enhance functionally, two logic inputs are provided which drive LCD annunciators for high and low logic input levels. A peak hold input permits the highest A/D or frequency reading to be held and displayed automatically Other features include a piezoelectric transducer driver, decimal point select inputs, and a low-battery detection/LCD annunciator driver circuit. The TSC820 includes on-chip drivers for a triplexed LCD display, and operates from a single 9 V battery. Package options include 40-pin DIP and 44-lead PLCC and compact flat packages. The 44-pin packages also include a hold input and underrange/overrange outputs.

Features:

- **3 3/4 Digit (3999 maximum) Resolution**
- **Frequency Measurement Input, 2 MHz Max**
- **Low-Noise Analog to Digital Converter**
- **Differential Analog Signal Inputs**
- **Low Analog Input Leakage ..... 1 pA typ**
- **Differential Reference Inputs**
- **Low Temperature Drift Reference . . . 35 ppm/ °C**
- **Peak Reading Hold**
- **Two Logic Level Inputs with Annunciators**
- **LCD Display with Triplexed Drive**
- **On-chip Decimal Point Control Inputs**
- **Low Battery Detect with LCD Annunciator**
- **Piezo Buzzer Driver**
- **Single 9 V Battery Operation**
- **40-pin DIP or 44-lead PLCC and Flat Package**
- **44-pin Package Versions Also Include:**
  - **–Underrange and Overrange Outputs**
  - **–Display Hold Input to "Freeze" Reading**



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TSC827 1% ADC with LCD Bar-Graph Drive and Set Points

General Description

The TSC827 is a low power, integrating analog to digital converter with on-chip drivers for a 101 segment LCD display. Two user selected set points can be programmed and displayed. Logic outputs are also included for set points and overrange. A serial data output provides A/D data, at 0.1 % resolution, for a numeric display or µP interface. The TSC827 is packaged in a 60-pin flat package or 68-pin PLCC.

For numeric data and setpoint display, see also the TSC828.

Features

- **1 % LCD Bar-Graph Readout**
  - **–Triplex LCD Display**
  - **–101 Data Segments**
  - **–Overrange and Underrange Annunciators**
  - **–Two Set Point Annunciators**
- **Two Selectable Set Points**
  - **–Set with Simple Mechanical Switch or µP**
- **Differential Analog Input**
- **Differential Reference Input**
- **Low Drift On-Chip Reference .. 50 ppm/ °C, typ**
- **10-bit Serial Data Output**
- **9 V Battery or ±5 V Supply Operation**
- **Low Power Dissipation ..... 15 mW, typ**
- **60-pin Flat Package or 68-pin PLCC**

TSC828 Multiple-Digit LCD Display Driver

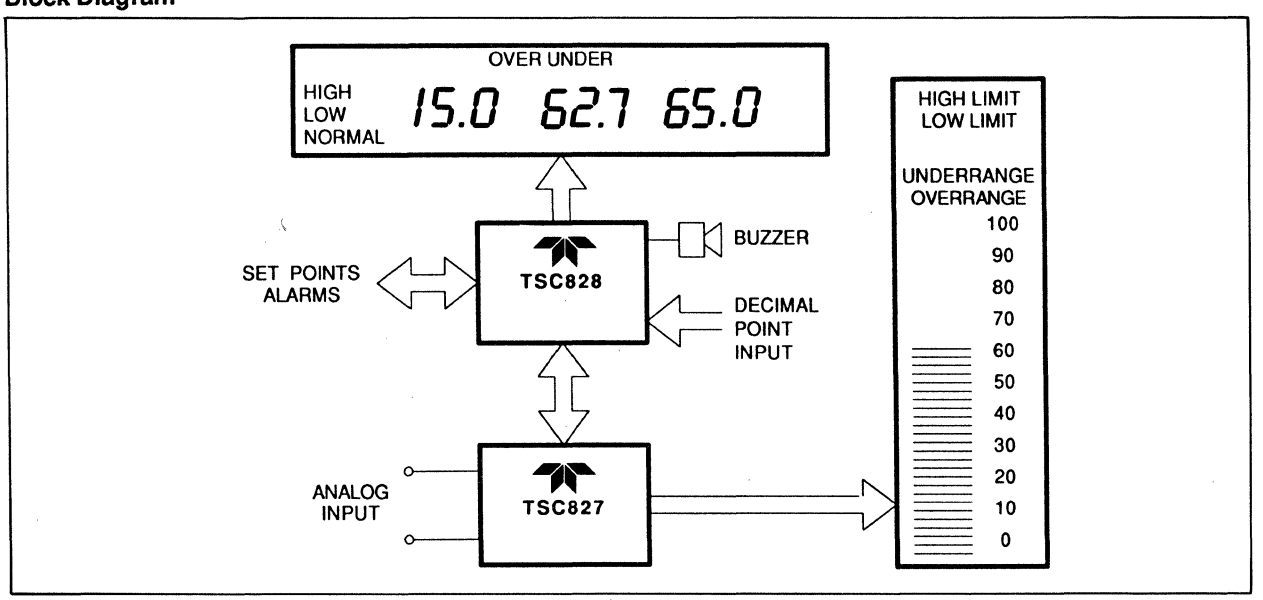
General Description

The TSC828 is a flexible multi-digit LCD display driver. The TSC828 directly connects to the TSC827 A/D converter, and simultaneously displays the A/D conversion result and high/low set point values. Five annunciator inputs , three alarm logic outputs and a piezoelectric buzzer driver are included. The TSC828 can also operate as a serial-input µP peripheral, providing three independent 3 1/2 digit displays.

Features

- **Drives three 3 1/2 Digit LCD Displays**
- **Direct Interface to TSC827 A/D Converter**
  - **–Displays A/D Result, High Limit, and Low Limit, Simultaneously**
  - **–Displays A/D Result to 0.1% Resolution**
  - **–Demultiplexes Set Point Inputs, Alarm Outputs**
- **All Display Decoders/Drivers On-Chip**
- **Five Decimal Point/Annunciator Inputs**
- **Piezoelectric Buzzer Driver**
- **Backplane Oscillator On-Chip**
- **Single 5 V Operation**
- **Low Power ..... 500 µA**

Block Diagram



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Low Power 3 1/2 Digit A/D with HOLD — TSC810

General Description:

The TSC810 is a low power, 3 1/2 digit, LCD display A/D converter with a display HOLD feature. The HOLD input will "freeze" the display indefinitely. The TSC810 is pin compatible with the TSC7116, requiring only a few changes in external component values to reduce power dissipation by 90%. The TSC810 also incorporates an "integrate to zero" conversion phase that ensures fast recovery from an input overrange.

Features:

- **Display Hold Function**
- **Pin Compatible with TSC7116**
  –Only External Component Changes Required
- **Low Power Dissipation ..... 1 mW Maximum**
- **Fast Overrange Recovery**
  –1st Reading Accurate After Overrange
- **Direct LCD Drive**
  –No External Components Required
- **Low Leakage Differential Inputs ..... 1 pA, typ.**
- **Low Noise ..... 15 μV p-p**
- **Low Drift Internal Reference ..... 35 ppm/ °C**
- **Guaranteed Zero Reading with Zero Input**
- **Convenient 9 V Battery Operation**
- **DIP, PLCC, and Flat Packages Available**

3 1/2 Digit A/D Converter with Hold and Differential Reference Inputs — TSC811

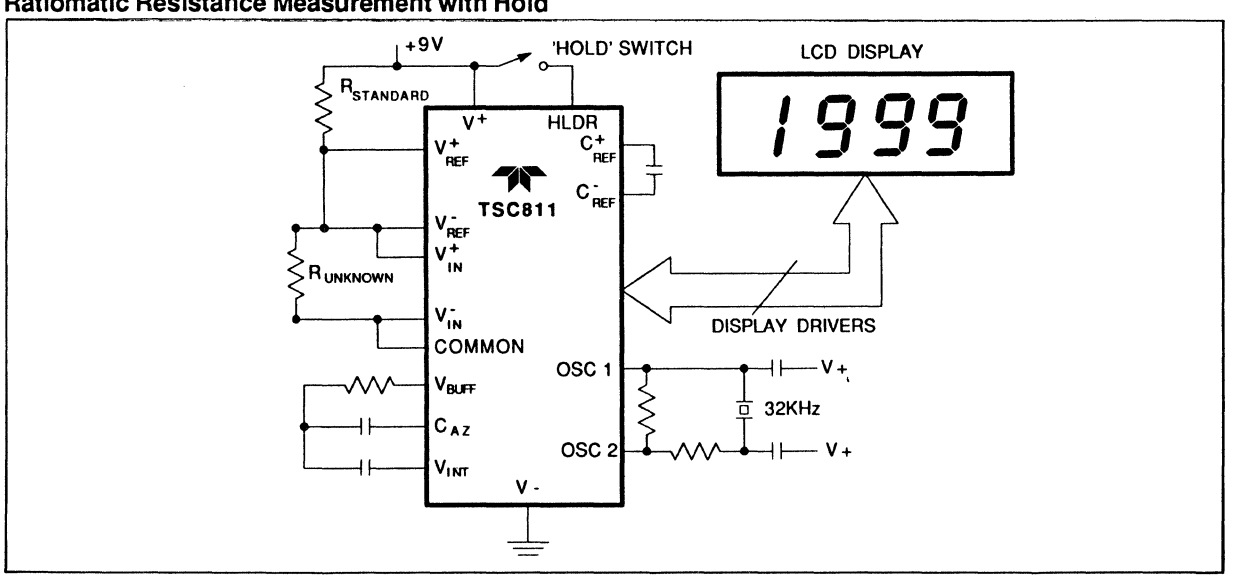
General Description:

The TSC811 is a low power, 3 1/2 digit, LCD display A/D converter with differential reference inputs and a display HOLD feature. The differential reference inputs permit accurate, inexpensive ratiometric resistance measurements to be made, while the HOLD feature will "freeze" the reading indefinitely. The TSC811 is ideal for panel meter and DMM applications which must measure Ohms as well as Volts, and which require the HOLD feature. Additional features include fast input overrange recovery and 100 μA supply current.

Features:

- **Display Hold Function**
- **Differential Reference Inputs**
- **Differential Signal Inputs**
- **Low Input Leakage Current ..... 1 pA**
- **Guaranteed Zero Reading with Zero Input**
- **Fast Input Overrange Recovery**
- **Direct LCD Drive**
- **Low Temperature Drift Internal Reference ..... 35 ppm/ °C Typical**
- **Crystal Clock Oscillator**
- **Available in DIP, PLCC, or Compact Flat Package.**
- **9 V Battery Operation, 100 μA Supply Current**

Ratiomatic Resistance Measurement with Hold



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Teledyne Semiconductor

TSC232 Dual RS-232 Transmitter/Receiver

General Description

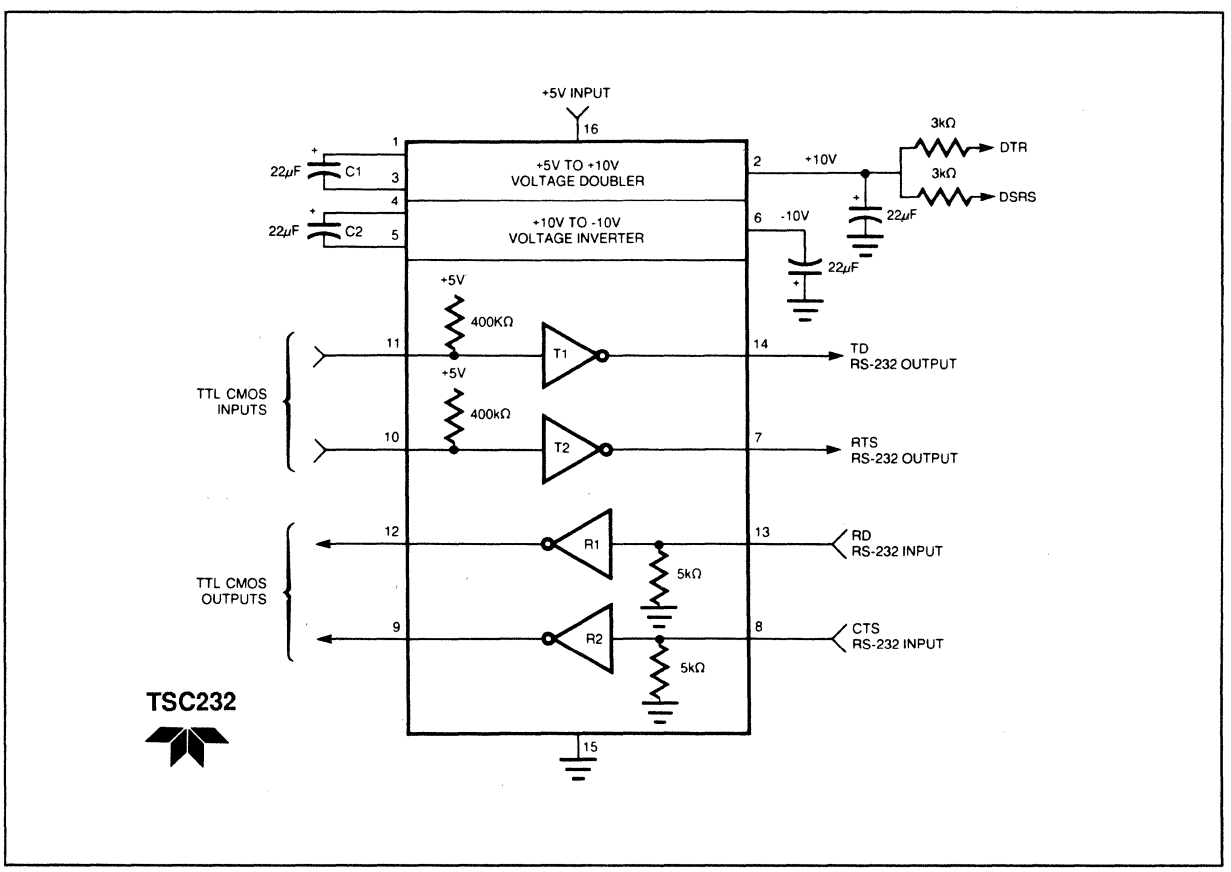
The TSC232 from Teledyne Semiconductor is a dual RS-232 transmitter/receiver that complies with EIA RS-232C guidelines and is ideal for all RS-232C communication links. This device has a 5 V power supply and two charge pump voltage converters that produce +10 V/-10 V power supplies.

The TSC232 has four level translators. Two are RS-232 transmitters that convert TTL/CMOS input levels to 9 V RS-232 outputs. The other two translators are RS-232 receivers that convert RS-232 inputs to 5 V TTL/CMOS output levels. The receivers have a nominal threshold of 1.3V, a typical hysteresis of 0.5 V, and can operate with up to ±30 V inputs.

Features

- **Meets all RS-232C Specifications**
- **Operates from Single 5 V Power Supply**
- **2 Drivers and 2 Receivers**
- **Onboard Voltage Quadrupler**
- **±30 V Input Levels**
- **±9 V Output Swing with +5 V Supply**
- **Low Power CMOS: 5 mA**

Functional Diagram



Teledyne Semiconductor

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3 1/2 Digit Direct Display Drive Analog-to-Digital Converters

TSC71XX

General Description:

The TSC71XX family of products are low power CMOS analog-to-digital converters which provide on-chip drivers for a 3 1/2 digit display. The TSC71X6 series drives an LCD display, while the TSC71X7 series provides 8 mA of drive current per segment to an LED display. The low power dissipation of the 71X6 devices makes them ideal for battery operated systems.

All of the active components required to construct a measurement system with 0.05% resolution are provided by the TSC71XX devices. Only a display, four resistors, and four capacitors are required to complete the system.

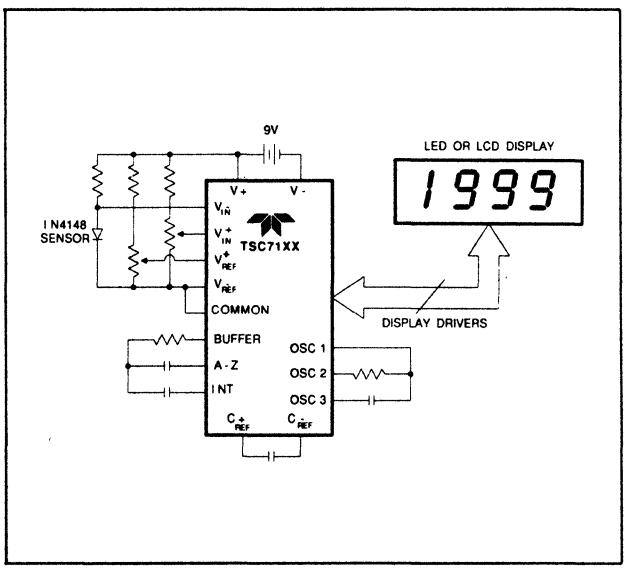
The TSC71XX family of converters reduces linearity errors to less than one count. High impedance inputs offer 1 pA bias current and 10^{12} Ω input impedance. An auto-zero cycle guarantees a zero display reading with a zero volt input. Some models include differential reference inputs which allows ratiometric measurements for ohms or bridge transducer measurements, while other models provide a HOLD input to "freeze" the display reading.

TSC71XX converters are available in a wide variety of packaging options, including 40-pin plastic and ceramic DIPs, 44-lead plastic leaded chip carrier (PLCC) and 44- and 60-pin flat packages.

For 3 1/2 digit converters with additional features, refer to the TSC810 and TSC811 data sheets.

Features:

- **Drives LCD or LED Displays Directly**
- **Guaranteed Zero Reading with Zero Input**
- **True Polarity at Zero for Precise Null Detection**
- **1 pA Input Current**
- **Linearity Error Less Than One Count**
- **"A" Versions Offer Low Drift Internal Voltage Reference . . . 50 ppm/°C to 75 ppm/°C Max Drift**
- **Low Power Operation . . . . . 1 mW to 10 mW**
- **DIP and Surface Mount Packages**



Temperature Sensor

Features at a Glance

Part No.	100 µV Resolution	Low Power I_S<100µA	Single Supply	Internal Reference	Differential Reference	Guaranteed Ref TC	Display "Hold" Feature	LCD Drive	LED Drive
TSC810	●	●	●	●		●	●	●	
TSC811	●	●	●	●	●	●	●	●	
TSC7106	●		●	●	●			●	
TSC7106A	●		●	●	●	●		●	
TSC7126	●	●	●	●	●			●	
TSC7126A	●	●	●	●	●	●		●	
TSC7136	●	●	●	●	●			●	
TSC7136A	●	●	●	●	●	●		●	
TSC7116	●		●	●			●	●	
TSC7116A	●		●	●		●	●	●	
TSC7107	●			●	●				●
TSC7107A	●			●	●	●			●
TSC7117	●			●			●		●
TSC7117A	●			●		●	●		●

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For further information call 415-968-9241 or 1-800-888-9966!

Overview

Texas Instruments Military program offers high reliability integrated circuits covering a complete product spectrum. The program is designed to meet and support Military processing requirements. Standard device offerings include JM38510, DESC Standard Military Drawing (SMD), Class B Processing, and the Military Temperature Range.

Product Line	Processing Flows	Types
Logic	SN, SNJ, JM38510	54TTL 54S 54LS 54AC 54ACT 54ALS 54AS 54BCT 54F 54HC 54HCT
	B, JM38510	PAL®
Linear	SN, SNJ, JM38510	Interface, Control, Display Drivers
MOS Memory	SM, SMJ	EPROM, DRAM, SRAM
Bipolar Memory	SNJ	FIFO
Microprocessor	SM, SMJ	320 DSP Family 340 GSP Family
	SN, SNJ	8 Bit Slice Family
	Class B	SBP9989, SBR9000

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Texas Instruments

Military Product Flows

Process Level	Order As	Description
JM38510 Class S	JM38510/XXXXXSXA	Qualified per MIL-M-38510 Class S. Produced in DESC certified production facilities.
JM38510 Class B	JM38510/XXXXXBXA	Qualified per MIL-M-38510 Class B. Produced in DESC certified production facilities.
DESC SMD	Drawing Number	Certified and symbolized to the DESC Standard Military Drawing where TI is an approved source.
Class B	SNJ, SMJ, B	Screened per requirements of MIL-Std-883 Class B Method 5004 & 5005. Conforms to the requirements of JEDEC Publication 101. (For detailed screening information, see Military Products Designers' Reference Guide.)
Military Extended Temperature Range	SN54, SN55, SM	Standard Commercial Processing

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Packages Available

Package Description	Package Type	Logic	Linear	Bipolar Memory	MOS Memory	µP
Ceramic DIP	J JG JT	ALL All except TTL, 54S	X X	X	X	
Side Braze Ceramic DIP	JD		X		X	X
Ceramic Flatpack	W WC, U HK	ALL	X X		 X	
Ceramic Chip Carrier (Square)	FK FD	ALL except TTL	X X	X		 X
Ceramic Chip Carrier (Rect)	FG, FV, FQ				X	
Ceramic SOJ	HJ				X	
Pin Grid Array	GB					X
Ceramic Chip Carrier (Leaded)	FJ		X			X

DESC Standard Military Drawings

The DESC Standard Military Drawing (SMD) program provides industry standard specifications in compliance with MIL-Std-883, Class B requirements for devices that are not JAN qualified. Texas Instruments fully supports the DESC SMD program. Contact the factory for 1989 DESC approval plans. The DESC SMD nomenclature is described below.

82005 or 5962-85155 — DRAWING NUMBER

01 — DEVICE TYPE

X — PACKAGE TYPE

C = 14 Pin DIP
D = 14 Pin Flatpack
E = 16 Pin DIP
F = 16 Pin Flatpack
L = 24 Pin DIP (300 MIL)
P = 8 Pin DIP
R = 20 Pin DIP
S = 20 Pin Flatpack
2 = 20 Pad LCCC
3 = 28 Pad LCCC
Z = 44 Pad LCCC

X — LEAD FINISH

A = Solder DIP (Standard)
B = Tin Plate
C = Gold Plate

Logic

Digital Logic Nomenclature

EXAMPLE: SNJ 54 LS00 J

PREFIX
Blank, SN = Standard Prefix
SNJ = Class B Processing

MIL TEMPERATURE (−55°C/125°C)

CIRCUIT DESIGNATOR
Blank = Standard TTL
LS = Low Power Schottky
S = Schottky
ALS = Advanced Low Power Schottky
F, AS = Advanced Schottky
HC = High-speed CMOS
HCT = TTL compatible HC
AC = Advanced CMOS
ACT = TTL compatible Advanced CMOS
BCT = BiCMOS

PACKAGE
J = CDIP
JT = 24 pin, 300 mil CDIP
W = Flatpack
FK = LCCC

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Advanced CMOS Logic (ACL)

ACL Nomenclature EXAMPLE: SNJ 54 AC 11 000 J

- PREFIX
  - SN = Standard Process
  - SNJ = Class B Process Option
- MILITARY TEMP RANGE
- PRODUCT FAMILY
  - AC = Advanced CMOS
  - ACT = TTL Compatible AC
- CENTER PIN VCC AND GND
- EQUIVALENT TTL FUNCTION
- PACKAGE TYPE
  - J = CDIP
  - FK = LCCC

Advanced Logic

EPIC Advanced CMOS Logic

TI's 1-micron EPIC Advanced CMOS Logic (ACL) family offers a 3X speed improvement over the High-Speed CMOS logic devices currently available and provides 24 mA of output drive. These products have a typical propagation delay of < 3 ns. Typical maximum operating frequency is 150 MHz. The advanced features of this family are made possible by a 1-micron, twin-well CMOS process which TI calls EPIC (Enhanced Performance Inplanted CMOS).

The ACL family provides superior latchup protection and electrostatic discharge protection on the inputs or outputs. At the same time, ACL offers all the traditional advantages of CMOS technology, such as low power consumption, high noise immunity and flexible power-supply requirements.

This advanced CMOS logic family is a joint development of Texas Instruments and Signetics/Philips. Each company has the responsibility to design specific functions in the 1-micron logic family product spectrum. The agreement involved the exchange of design data bases that allowed TI and Signetics/Philips to introduce a new alternately-sourced, identically specified product line into the marketplace.

Features:
PROP DELAY: < 3 NS
IOL, IOH: 24 mA
Vcc: 3V to 5.5V for AC
4.5V to 5.5V for ACT
- ZERO STANDBY POWER • ESD PROTECTION
- LATCH-UP PROTECTION • I μGATE LENGTH
- Center Pin Vcc and Ground

Packages: CERAMIC DIP: J, JT CHIP CARRIER: FK

54F Devices

Texas Instruments offers military versions of general-purpose SSI and MSI digital-logic functions in the 54F series of bipolar TTL integrated circuits.

TI currently supplies bipolar logic products from five families—TTL, Schottky (S), low-power Schottky (LS), advanced low-power Schottky (ALS), and advanced Schottky (AS). The addition of the 54F devices complements TI's existing family of standard products offered in military temperature range.

54F devices are offered in ceramic dual-in-line (DIP) packages as well as leadless chip carriers (LCCC) and ceramic flat packs.

Contact Texas Instruments Field Sales Offices for up to date 54F device product spectrum.

Texas Instruments

Advanced Logic Family Comparison

	54ALS	54AS	54F	54HC	54AC
Power/Gate-Static	1.2 mW	8 mW	4 mW	2.5 nW	2.5 nW
100 KHz	1.2 mW	8 mW	4 mW	0.17 mW	0.2 mW
Typical Prop Delay	4 nS	1.7 nS	3 nS	8 nS	3 nS
Speed-Power Product	4.8 pJ	13.6 pJ	12 pJ	1.4 pJ	0.6 pJ
FMAX-Typical	80 MHz	160 MHz	140 MHz	40 MHz	150 MHz
Output Current					
Standard	—.4/4 mA	—2/20 mA	—1/20 mA	—4/4 mA	—24/24 mA
Buffer/Drivers	—12/12 mA	—12/48 mA	—12/48 mA	—6/6 mA	—24/24 mA
Transceivers	—12/12 mA	—12/48 mA	—3/48 mA	—6/6 mA	—24/24 mA
Registers/Latches	—1/12 mA	—12/32 mA	—3/20 mA	—6/6 mA	—24/24 mA
(82X, 84X)	—	—24/32 mA	—3/20 mA	—	—
(10XX)	—1/12 mA	—40/40 mA		—	—
Product Features					
ESD Protection	Yes	Yes	Yes	Yes	Yes
Miller Killer CKTS	AC, DC	AC, DC	AC, DC	—	—
Inputs	PNP	PNP	PNP	PMOS/NMOS	PMOS/NMOS
DC & AC Guar Over Temp	Yes	Yes	Yes	Yes	Yes
Worst Case Limits	Yes	Yes	Yes	Yes	Yes
Functional Comparison-Defined Functions	40% LS 60% New	23% STTL 77% New 35% Fast, 65% New	21% STTL 79% New	72% TTL, 16% HCT 6% HC4000, 6% New	
Alternate Source	National	National	NSC, MOT, SIG	MOT, NSC, RCA	Philips/SIG

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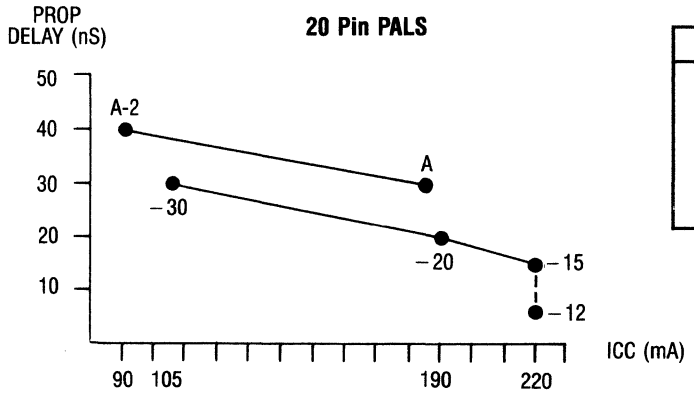
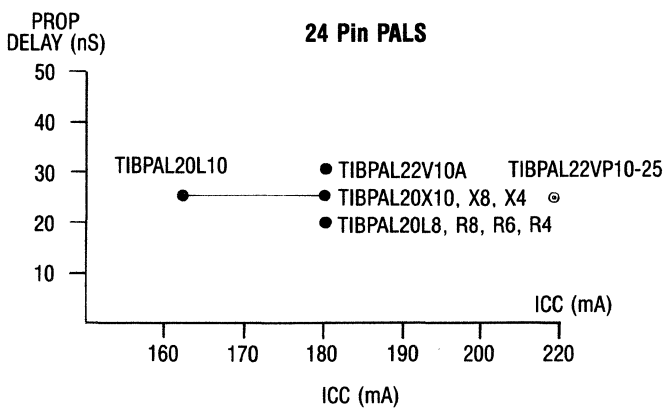
Bipolar Impact Technology

Fastest PALS

IMPACT™ (IMPlanted Advanced Composed Technology) is an advanced bipolar technology. IMPACT's 2 μM feature size and 1.05 mil^2 transistor area offers performance advantages in speed, power, and circuit density over preceding bipolar technologies, the IMPACT technology is in production today and is being applied PAL product families, and selected MSI/LSI ALS and AS devices.



DEVICE	MAX ICC	MAX tpd
16XXA	180 mA	30 nS
16XXA-2	90 mA	40 nS
16XX-12*	220 mA	12 nS
16XX-15	220 mA	15 nS
16XX-20	190 mA	20 nS
16XX-30	105 mA	30 nS



DEVICE	MAX ICC	MAX tpd
TIBPAL22V10A	180 mA	30 nS
TIBPAL22VP10-25	220 mA	25 nS
TIBPAL20L10-25	165 mA	25 nS
TIBPAL20X10-25	180 mA	25 nS
TIBPAL20X8-25	180 mA	25 nS
TIBPAL20X4-25	180 mA	25 nS
TIBPAL20L8-20	180 mA	20 nS
TIBPAL20R8-20	180 mA	20 nS
TIBPAL20R6-20	180 mA	20 nS
TIBPAL20R4-20	180 mA	20 nS

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PAL is a registered trademark of Monolithic Memories, Inc.
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Programmable Array Logic

PAL Nomenclature (Industry Leadership Part Types)

TIB PAL 16 R 8 –20 M J B

PREFIX
Blank = Industry Equivalent
TIB = TI Bipolar Leadership
TIC = TI CMOS Leadership

PAL = Product Family Designator

NUMBER OF ARRAY INPUTS

OUTPUT CONFIGURATION DESIGNATOR
L = Active Low
R = Registered
X = Exclusive OR

NUMBER OF OUTPUTS IN DESIGNATED CONFIGURATION

PERFORMANCE DESIGNATOR
–12
–15
–20
–25
–30
A
A-2

TEMPERATURE RANGE
M = –55°C to 125°C

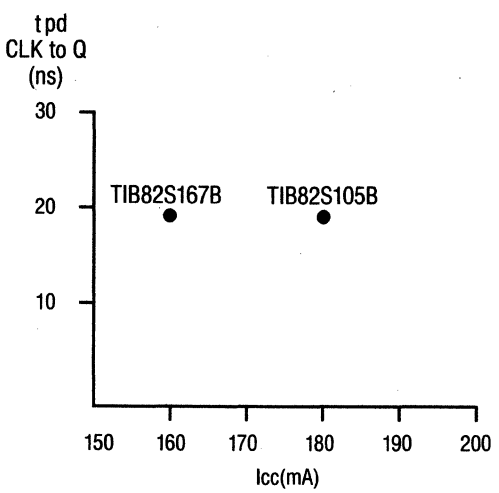
PACKAGE
J, JT = CDIP
FK = LCCC
W = Flatpack

CLASS B PROCESSING

Texas Instruments

FIELD PROGRAMMABLE LOGIC SEQUENCERS

The TIB82S105B and TIB82S167B are field programmable state machines of the Mealy type. TI's 40 MHz logic sequencers provide improved performance in both speed and power while offering a conventional preset function resulting in quick recovery times.



DEVICE	ORGANIZATION	ICC MAX	fMAX
TIB82S105B	16×48×8	180 mA	40 MHz
TIB82S167B	14×48×6	160 mA	40 MHz

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Linear

Linear Nomenclature

Orders for linear functions as described in Selection Guide should include complete Device Type Number as noted:
EXAMPLE: LinCMOS Dual, Low Bias Operational Amplifier. Device Type Number—TLC27L2BMJGB.

TLC 27 L 2 A M JG B

PREFIX
Must contain two or three letters
TL = TI Linear Products
TLC = TI LinCMOS Products

CIRCUIT DESIGNATION
Must contain two or three numbers

BIAS CURRENT
L = Low, M = Med
No Letter = High

DEVICE COMPLEXITY
1 = Single
2 = Dual
4 = Quad

INPUT OFFSET VOLTAGE
A = 5.0 mV
No Letter = 10.0 mV

OPERATING TEMPERATURE RANGE
M = Military (−55°C to 125°C)

PACKAGE
FK = LCC
J = 14 Pin C-DIP
JG = 8 Pin C-DIP
L = T099/T0100
KJ = 4 Pin T03
LA = T039
LD = T046
K = 2 Pin T03

Class B Processing

STANDARD SECOND SOURCE PREFIXES

ADC = National	OP = PMI	SG = Silicon General
LM = National	RM = Raytheon	μA = Fairchild
MC = Motorola	SE = Signetics	LT, LTC = Linear Technology

Interface functions as described in Selection Guide should include complete Device Type Number as noted:
EXAMPLE: Dual Line Driver with Class B Processing. Device Type Number—SNJ55109AJ

SNJ 55 109A J

PREFIX
SN = TI Interface Product
SNJ = TI Interface Product with Class B Processing

MIL TEMP RANGE
(−55°C to 125°C)

CIRCUIT DESIGNATION
May contain two, three or four numbers & letters

PACKAGE
FD, FK = Chip Carrier
J = 14/16/20Pin C-DIP
JD = Size Braze DIP
JG = 8 Pin C-DIP
W = Flat Pack

STANDARD SECOND SOURCE PREFIXES
AM = AMD
DS = National
μA = Fairchild

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MOS Memory

MOS Memory Nomenclature

EXAMPLE: SMJ 4164 –15 JD S

PREFIX
SM = Standard Prefix
SMJ = Class B Processing, JEDEC Publication 101

CIRCUIT DESIGNATOR
Must contain four characters

ACCESS TIME
Device types are available with various speeds

TEMPERATURE RANGE
Must contain one letter only
M = –55°C to 125°C
S = –55°C to 100°C (except 4164 & 4256 which are –55°C to 110°C)
L = 0°C to 70°C

PACKAGE TYPE
Must contain one or two letters

Military Memories

Texas Instruments offers a wide selection of MOS Memories. Three basic types are offered: DRAMs, EPROMs and SRAMs. Most are offered in both through hole style Ceramic Dual-in-line packages and surface mountable Leadless Ceramic Chip Carrier (LCCC) or Ceramic Small Outline "J" formed (CSOJ) packages.

DRAMs

There are an assortment of DRAM densities and organizations offered in the DRAM product line. Densities range from 64K through 1 Meg. Organizations offered include X1 and X4. A Specialized version of the DRAM is the Video RAM (VRAM) which includes an onboard shift register. The VRAM is also offered in a X1 and a X4 organization.

EPROMs

Texas Instruments' EPROM family features High Voltage CMOS technology. While these CMOS EPROMS are pin compatible with existing NMOS EPROMs they feature low standby and active power without sacrificing speed. Densities range from 128K to 512K with a 1 Meg planned for late 1989.

SRAMs

CMOS Static RAM's are new product offerings for TI. This product line features TI's exclusive EPIC™ technology and the six transistor (6T) memory cell design for improved speed, increased temperature stability and greater resistance to soft errors. Initial product offerings include 3 16K density parts. 1989 plans include 64K and 72K density parts with long range plans to include 256K density devices. Access times range from 25 to 70 ns.

Device	Type	Temp Range	Maximum Access Time (ns)	Organization	Package	
					Through Hole	Surface Mountable
4161	VRAM	S	150, 200	64K×1	20 Pin CDIP (JD)	
4164	DRAM	S, L	120, 150, 200	64K×1	16 Pin CDIP (JD)	18 Pad LCCC (FG)
4256	DRAM	S	120, 150, 200	256K×1	16 Pin CDIP (JD)	18 Pad LCCC (FV)
4416	DRAM	S, L	150, 200	16K×4	18 Pin CDIP (JD)	18 Pad LCCC (FG)
4461	VRAM	S	150, 200	64K×4	20 Pin CDIP (JD)	20/26 Pin CSOJ (HJ)*
4464	DRAM	S	120, 150, 200	64K×4	18 Pin CDIP (JD)	18 Pad LCCC (FV)*
44C256*	DRAM	M	100, 120, 150	256K×4	20 Pin CDIP (JD)	20/26 Pin CSOJ (HJ)*
4C1024	DRAM	M	100, 120, 150	1 Meg×1	18 Pin CDIP (JD)	20/26 Pin CSOJ (HJ)* 20/26 Pad LCCC (FQ)* 20 Pin Flatpack (HK)*
27C128	EPROM	M	150, 170, 200, 250, 300	16K×8	28 Pin CDIP (J)	32 Pad LCCC (FG)*
27C256	EPROM	M	150, 170, 200, 250, 300	32K×8	28 Pin CDIP (J)	32 Pad LCCC (FG)*
27C512	EPROM	M	200, 250, 300	64K×8	28 Pin CDIP (J)	32 Pad LCCC (FG)*
27C010*	EPROM	M	200, 250, 300	128K×8	28 Pin CDIP (J)	32 Pad LCCC (FG)*
27C210*	EPROM	M	200, 250, 300	64K×16	28 Pin CDIP (J)	32 Pad LCCC (FG)*
61CD16LA/SA	SRAM	M	25, 35, 45, 55, 70	16K×1	20 Pin CDIP (JD)	20 Pad LCCC (FG)*
64C16L/S	SRAM	M	25, 35, 45, 55, 70	4K×4	20 Pin CDIP (JD)	20 Pad LCCC (FG)*
68CE16L/S	SRAM	M	25, 35, 45,55, 70	2K×8	24 Pin CDIP (JD)	32 Pad LCCC (FG)*
68CE64L/S*	SRAM	M	25, 35, 45	8K×8	28 Pin CDIP (JD)	32 Pad LCCC (FG)
61CD64L/S*	SRAM	M	25, 35, 45	64K×1	22 Pin CDIP (JD)	22 Pad LCCC (FG)
64C64L/S*	SRAM	M	25, 35, 45	16K×4	22 Pin CDIP (JD)	22 Pad LCCC (FG)
69CE72L/S*	SRAM	M	25, 35, 45	8K×9	28 Pin CDIP (JD)	32 Pad LCCC (FG)

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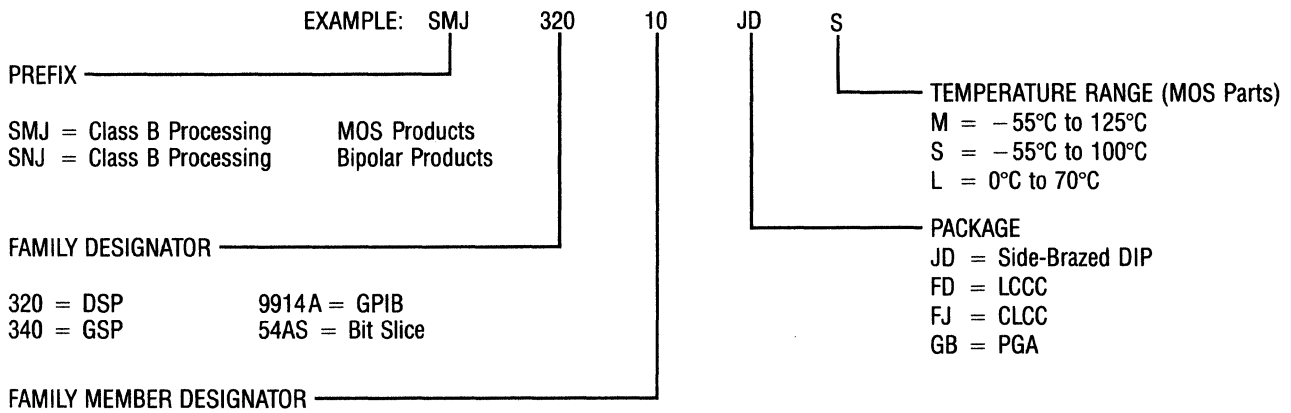
Application Processors

Part Number Nomenclature



Application Processors

Texas Instruments offers a variety of specialized processors that can be used in a number of military applications. Included are the 320 Digital Signal Processor (DSP) family, 340 Graphics System Processor (GSP) family, 8 Bit Slice family and the IEEE 488 General Purpose Interface Bus (GPIB) Controller. These state-of-the-art components can reduce component count up to 10X and improve system speed. System power can also be reduced by the component count reduction alone.

Graphics System Process

Texas Instruments has responded to the evolution within the Graphics industry with the development of a family of VLSI products to address their specific needs. Graphics system requirements have gone from static 2-dimensional (2D) wire frame with Sprite graphics to the present color filled 2D and 3D real-time systems with letter quality text. To meet those demands, a high-performance processor and controller are necessary to provide control of the VRAM and insure little overhead in managing the display memory. The SMJ34010 Graphics System Processor (GSP) and the SMJ34061 video system controller were developed by TI to address these needs.

The SMJ34010 combines the best features of general purpose processors and graphics controllers to create a powerful and flexible GSP. The on-chip processor executes both graphics instructions and general purpose instructions. The GSP is a true 32-bit processor with 32-bit internal data paths, a 32-bit ALU, a 128 megabyte address space, 32-bit general purpose registers, a 32-bit stack pointer and a 256 byte instruction cache to increase performance. Non-processor functions include CRT timing, screen refresh and DRAM refresh. Separate interfaces are provided for communicating with a Host processor to provide the video timing signals necessary to control a CRT monitor and for connecting directly to DRAMs and VRAMs.

The SMJ34061 Video System Controller (VSC) is a high-performance NMOS device that controls the video display and the dynamic memory of a bit-mapped graphics system. The principle role of the VSC is to provide an external processor with virtually unlimited access to video memory eliminating delays caused by conflicts with display update functions. Using the SMJ34061 relieves the system CPU of the burden of controlling system memory, refreshing video memory and reloading VRAM internal shift registers for bit-mapped displays.

SMJ9914A GPIB Controller

The SMJ9914A provides an interface between a Microprocessor System and the General Purpose interface bus specified in the IEEE-488 1975/1978 standards and the IEEE-488a 1980 supplement. It relieves the processor of the task of maintaining the IEEE protocol. By utilizing the interrupt capabilities of the device, the bus does not have to be continually polled, and fast responses to changes in the interface configuration can be achieved. This device can be complimented using the SNJ95160B and SNJ95161B tranceiver/drivers.

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Application Processors

Digital Signal Processors

Digital Signal Processors, which are essentially high speed microprocessors/microcomputers, are designed to execute computationally intensive signal processing algorithms. The 320 family of digital signal processors take advantage of powerful DSP instruction sets, advanced architecture, and parallel processing to make them ideal for DSP applications. As a result of this performance, the SMJ320 family is finding its way into military applications, such as missile guidance, smart munitions, control (Servo, Position and Rate, Reference), communications signal processing (Digital filtering, data encryption, companding), FFT's. Voice Processing, Radar, Sonar, ECM, ECCM, and many others.

The SMJ320 family contains three generations of compatible devices. Compatibility is provided at the pin-for-pin/object level within a given generation and at the software level between generations. The first and second generation are 16 bit fixed point processors with a 32 bit accumulator and the third generation supports 32 bit floating point arithmetic. All three generations enjoy the extensive support, both hardware and software, supplied by TI and third parties.

The first generation includes the SMJ32010, SMJ320C10, SMJ320C15*, and the SMJ320E15*. This generation offers 5 to 6.25 MIPS performance, 144 to 256 words on chip data memory, and 1.5 to 4K words on chip program memory (EPROM or Masked ROM).

The second generation is represented by the SMJ32020, SMJ320C25, SMJ320C25-50*, and the SMJ320E25*. Performance for the second generation ranges from 5 to 12.5 MIPS and is supported by features such as 544 words on chip data memory, 4K words on chip program memory (EPROM or Masked ROM), full duplex serial port, multiprocessor interface, and an auxiliary register ALU to name a few.

The third generation contains the SMJ320C30*. This device provides a 60 nanosecond cycle time allowing it to execute more than 33 million floating point operations per second (MFLOPS). This approaches the performance available on a supercomputer. This performance is further enhanced by large on chip memories (two 1KX32 blocks of dual access RAM, one block of 1KX32 ROM), instruction cashe, concurrent DMA controller, parallel floating point multiplier and ALU, serial ports, and timers, software support for the SMJ320C30 will include ADA.

*Planned

Bit-Slice Family

Texas Instruments' Bit-Slice product family compliments the other processor products by offering maximum flexibility at the fastest possible speed. While Bit-Slice solutions require typically higher component counts and power than some of the more dedicated processors there are certain high performance applications that need the features of a Bit-Slice design. TI's bit-slice family utilizes TI's oxide isolated 2-um IMPACT-S™ process. The combination of IMPACT™ technology and a low voltage internal circuit configuration called Schottky Transistor Logic (STL) offers high performance with low power dissipation.

The SNJ54AS888 is a registered 8-bit ALU slice that is the main component in TI's 8-bit slice product family. It can be cascaded to word widths up to 64 bits. The 8-bit ALU can perform seven arithmetic and six logical instructions, besides arithmetic, logical or circular shifts. other devices in the family include the SNJ54AS890 145-bit microsequencer and the SNJ54AS897 16-bit barrel shifter.

Hardware/Software Support

All of TI's microprocessor products are well supported with both hardware and software development tools. Contact the factory for details.

320 Digital Signal Processor Family Features

Characteristics	1st Gen	2nd Gen	3rd Gen
Technology	2.4μ NMOS/ 2.0μ CMOS	2.4μ NMOS/ 2.0μ CMOS	1.0μ CMOS 1.8μ CMOS
Clock Rate (MHz)	20.5/25.6	40.0/51.2	33.0
Cycle Time (ns)	200/160	100/80	60
Throughput	5–6.25 MIPS	5–12.5 MIPS	33 MFLOPS
Instructions	60	133	111
Temp Range	MIL Temp	MIL Temp	MI Temp
On Chip RAM	144/256 Words	544 Words	2K×32 Words
On Chip ROM/EPROM	1.5K/4K×16	4K×16	4K×32
Prog Mem Space (Ext)	4K×16	64K×16	16M×32
Data Mem Space (Ext)	—	64K×16	Shared

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Semicustom

Texas Instruments has actively participated in the military semicustom market for over 8 years. With a complete family of high performance, low power CMOS gate arrays and military qualified standard cells, the Military Custom/Semicustom Department of Texas Instruments continues to provide its customers with the state of the art military system solution. This complete military semicustom product line is backed by dedicated customer service network and by a comprehensive design and manufacturing support system that has placed TI at the forefront of the military semiconductor industry through the quality and reliability of its military products.

Standard Cell Technology

Texas Instruments Standard Cell products are custom design equivalents of standard products. Each cell layout is handcrafted by an IC designer, then thoroughly modeled and characterized. These logic building blocks are designed for interconnection on silicon, rather than on a printed circuit board, providing an efficient and economical path to the development of unique integrated circuits, customized for the user's application. Semicustom and custom circuits now incorporate major system functions such as processing, memory, and interface at the VLSI level.

Texas Instruments offers two standard cell families based on 1- and 2-μM twin-well CMOS technology. The 2-μM standard cell family is fabricated using an advanced double-level metal process, and the 1-μM product family is a natural geometric progression from TI's 2-μM EPIC I™ technology.

CMOS Standard Cell Software Library

Texas Instrument's design staff has carefully constructed the CMOS standard cell library to offer both functional variety and design flexibility. The library contains over 400 cells, encompassing a wide variety of elements ranging from simple inverters to complex LSI structures. Each cell is fully characterized over the military temperature range and contains a circuit simulation model, a logic simulation model, and a detailed data sheet.

In an effort to continually expand the variety and complexity of cells as well as ensure their accuracy, quarterly updates are performed. For further information on the software library contact your local TI Field Sales Office.

CMOS Gate Arrays

Texas Instruments also has available a high performance, low power CMOS gate array family. These arrays are designed utilizing the same proven 1-μM technology as previously noted for the standard cells. This family of arrays provides a high performance solution to random logic design needs with the benefit of fast turn around time and design cost effectiveness.

TI has participated in the gate array market for over eight years and this has provided the learning experience necessary for rapid availability of easily-routed low-risk arrays.

Gate Array Library

The CMOS gate array library provides a one-for-one mapping of all logic cells found in the TI standard cell library. This approach allows for a flexible design scenario wherein logic designs may be captured on a workstation regardless of final standard cell or gate array implementation. This approach also allows TI to readily convert an array or standard cell to the other technology without adding the unnecessary risk of re-generating the data base already in place.

Criteria for Semicustom Technology Selection

Both the CMOS gate arrays and CMOS standard cells offer the customer unique benefits in many potential applications. Each design would be evaluated for its specific semicustom requirements and target technology decisions should be made accordingly.

In general, a gate array is best suited for logic-only applications where there is an equitable balance between the number of gates and number of I/O cells utilized. This design would then need to fit into a given array with a reasonable number of available gates and I/O's utilized.

A random logic design which is dominated by the amount of core logic or by the number of I/O buffers must be evaluated for standard cell implementation. The potential dramatic reduction in final chip area could warrant the rejection for an inefficiently used gate array.

All designs requiring specialized on-chip functions, complex high performance macro cells, or extraordinary buffer requirements would immediately be targeted for a standard cell implementation.

Technology Roundup

Texas Instruments remains committed to supporting the semiconductor requirements of military systems. This commitment holds true for semicustom products. While supporting existing design commitments, TI will continue to improve technology for all semicustom products to offer state-of-the-art, high performance, reliable products. Our technology roadmap will encompass sub-micron CMOS which has already been proven feasible on TI's mega-bit DRAM.

Texas Instruments is well aware of the need for long term support of military programs. It is the intention of TI to support all semicustom products in their designed geometrics. Where this support is threatened by obsolescence of a given process or set of design rules, TI would be capable of upgrading existing designs to the mainstream. An example of this is TI's ability to utilize a 3 micron standard cell data set for equivalent logical definition in either 2 or 1 micron.

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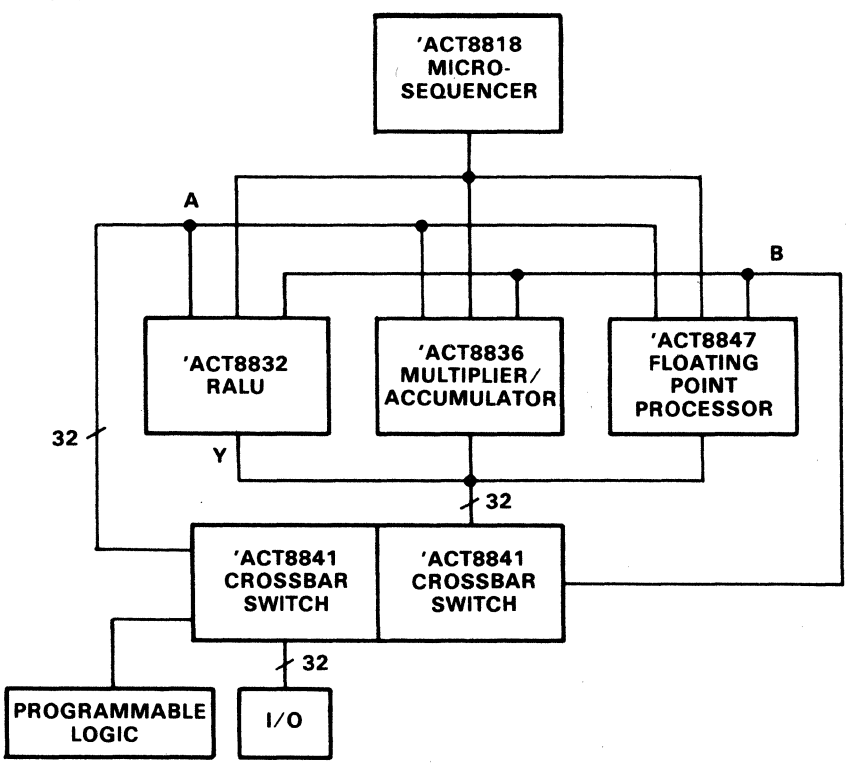
TEXAS INSTRUMENTS 32-BIT PROCESSOR FAMILY

Texas Instruments SN74ACT8800 family of 32-bit processor building blocks has been developed to allow the easy, custom design of functionally sophisticated, high-performance processor systems. The '8800 family is composed of single-chip, VLSI devices, each optimized for a specific processing function.

Geared for computationally intensive applications, the SN74ACT8800 family consists of the following high-performance ALUs, multipliers, microsequencers, and floating point processors:

- SN74ACT8818 16-bit microsequencer
- SN74ACT8832 32-bit registered ALU
- SN74ACT8836 32- x 32-bit parallel multiplier/accumulator
- SN74ACT8837 64-bit floating point processor
- SN74ACT8841 digital crossbar switch
- AN74ACT8847 64-bit floating point and integer processor
- Bipolar Support Chips
  - SN74AS8838 32-bit barrel shifter
  - SN74AS8839 32-bit shuffle/exchange network
  - SN74AS8840 16 x 4 crossbar switch

Each device represents a "building block" element of a CPU. These processor building blocks can be used singly or combined to create a vast array of functionally sophisticated, high-performance systems. You can use them to build a fully customized processing unit—or to accelerate and differentiate an off-the-shelf microprocessor.



32-BIT CMOS PROCESSOR BUILDING BLOCKS

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TEXAS INSTRUMENTS 32-BIT PROCESSOR FAMILY

20 MIPS and Low CMOS Power Consumption

With instruction cycle times of 50 ns or less and the low power consumption of TI's advanced, 1 μm EPIC™ CMOS technology, the 8800 chip set offers an unrivaled speed/power combination. Unlike traditional microprocessors, which require multiple cycles to perform an operation, the 'ACT8800 processors typically can complete instructions in a single cycle.

The 'ACT8832 registered ALU and 'ACT8818 microsequencer together create a powerful 20-MHz CPU. Because instructions can be performed in a single cycle, the '8832/'8818 combination is capable of executing over 20 million instructions per second (MIPS).

For math-intensive applications, the 'ACT8836 fixed-point multiplier/accumulator (MAC), 'ACT8837 64-bit floating point processor, and 'ACT8847 64-bit floating point and integer processor offer unprecedented computational power.

Features that make the '8800 family so adaptable include:

- Flexible building block approach

Function:	8800 Family Solution:
— high-speed CPU	'ACT8818, 'ACT8832
— high-speed integer multiplication	'ACT8836
— floating point precision	'ACT8837, 'ACT8847

- Three 32-bit data ports to eliminate I/O bottlenecks.
- Separate control bus eliminates the need for multiplexing instructions and data.
- Pipelined/flowthrough operation options
- Single- or double-precision accuracy

And, of course, all 'ACT8800 devices have the programmability to allow you to tailor instruction sets and data flows to fit your application.

The 8800 building blocks are the components to use whenever you find pre-defined hardware limiting your system's efficiency. The possibilities are virtually limitless.

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SN74ACT8818
16-BIT MICROSEQUENCER

Features

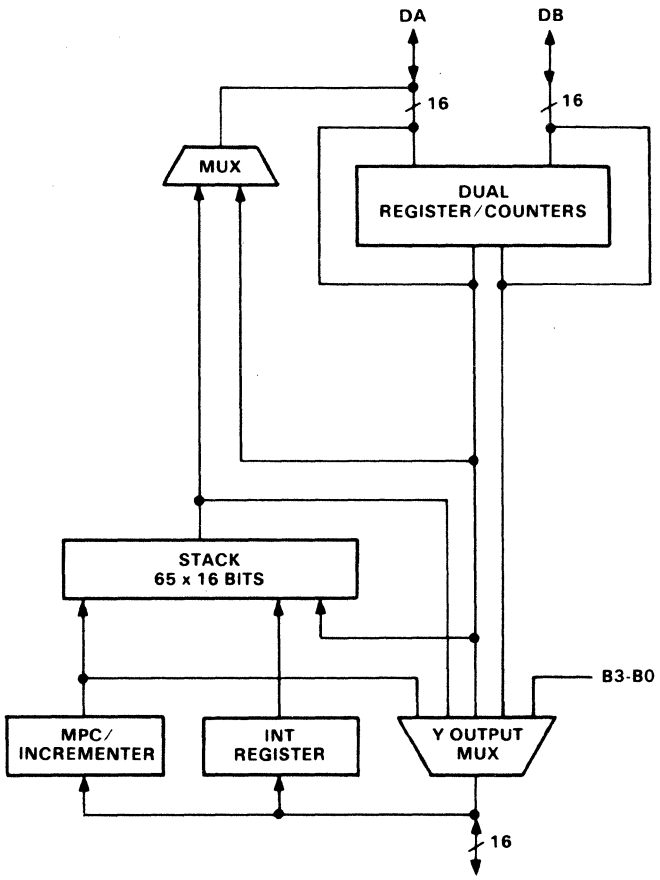
- Addresses Up to **64K** Locations of Microprogram Memory
- CLK-to-Y = 30 ns (t_{pd})
- Low-Power EPIC™ CMOS
- Addresses Selected from **Eight** Different Sources
- Performs Multiway Branching, Conditional Subroutine Calls, and Nested Loops
- Large **64-Word by 16-bit** Stack
- **Cascadable**

Description

The SN74ACT8818 is a high-speed, versatile 16-bit microsequencer capable of addressing 64K words of microcode memory. The 'ACT8818 can address the next instruction fast enough to support a 50-ns system cycle time.

The 'ACT8818 65-word-deep by 16-bit wide stack is useful for storing subroutine return addresses, top-of-loop addresses, and loop counts. For added flexibility, addresses can be selected from eight different sources: the three I/O ports, the two register/counters, the microprogram counter, the stack, and the 16-way branch input.

'ACT8818 FUNCTIONAL BLOCK DIAGRAM



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SN74ACT8832
CMOS 32-BIT REGISTERED ALU

Features

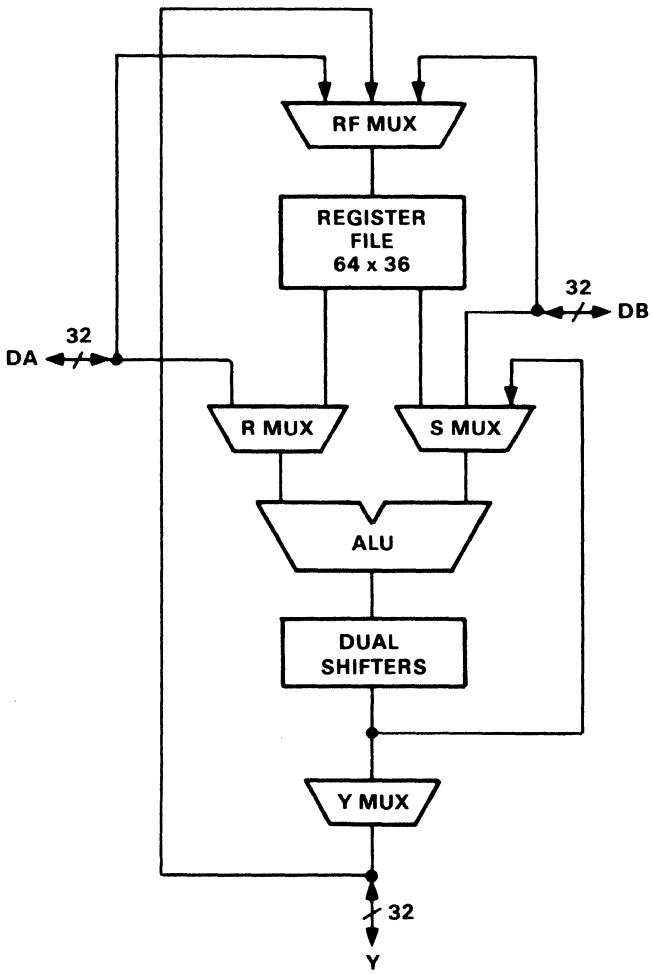
- **50-ns** Cycle Time
- **Low-Power EPIC™** CMOS
- **Three-Port I/O** Architecture
- **64-Word by 36-Bit** Register File
- Simultaneous ALU and Register **Operations**
- Configurable as Quad 8-Bit or Dual 16-Bit Single Instruction, Multiple Data Machine
- Parity Generation/Checking

Description

The SN74ACT8832 is a 32-bit registered ALU that can operate at 20 MHz and 20 MIPS (million instructions per second). Most instructions can be performed in a single cycle. The 'ACT8832 was designed for applications that require high-speed logical, arithmetic, and shift operations and bit/byte manipulations.

The 'ACT8832 can act as host CPU or can accelerate a host microprocessor. In high-performance graphics systems, the 'ACT8832 generates display-list memory addresses and controls the display buffer. In I/O controller applications, the 'ACT8832 performs high-speed comparisons to initalize and end data transfers.

'ACT8832 FUNCTIONAL BLOCK DIAGRAM



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SN74ACT8836
32-BIT X 32-BIT MULTIPLIER/ACCUMULATOR

Features

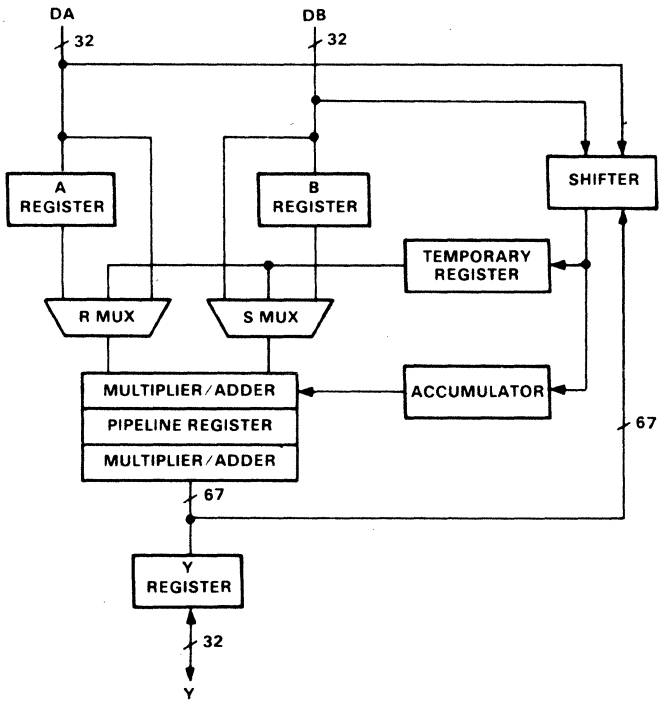
- Performs full 32- x 32-bit integer MAC in 60 ns flowthrough, 36 ns pipelined
- Can perform 64- x 64-bit operations
- Signed, unsigned, or mixed operands; integer or fractional operands
- Overflow status; three extended precision bits
- Supports division using Newton-Raphson algorithm
- Low-power EPIC™ CMOS

Description

The SN74ACT8836 is a 32-bit integer multiplier/accumulator (MAC) that accepts two 32-bit inputs and computes a 64-bit product. An on-board adder is provided to add or subtract the product or the complement of the product from the accumulator.

To speed-up calculations, many modern systems off-load frequently-performed multiply/accumulate operations to a dedicated single-cycle MAC. In such an arrangement, the 'ACT8836 MAC can accelerate 32-bit microprocessors, building block processors, or custom CPUs. The 'ACT8836 is well-suited for digital signal processing applications, including fast fourier transforms, digital filtering, power series expansion, and correlation.

'ACT8836 FUNCTIONAL BLOCK DIAGRAM



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SN74ACT8847
64-BIT FLOATING POINT UNIT

Features

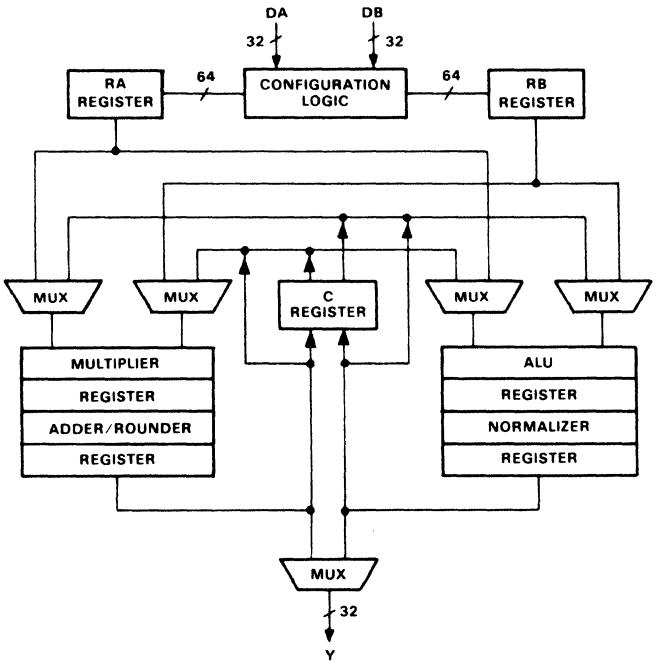
- Superset of TI's SN74ACT8837
- 30-ns, 40-ns and 60-ns Pipelined Performance
- Low-Power EPIC™ CMOS
- Meets **IEEE Standard** for Single- and Double- Precision Formats
- Performs **Floating Point** and **Integer** Add, Subtract, Multiply, Divide, Square Root, and Compare
- 64-Bit **IEEE Divide** in **11** Cycles, 64-Bit **Square Root** in **14** Cycles
- Performs Logical Operations and Logical Shifts

Description

The SN74ACT8847 is a high-speed, double-precision floating point and integer processor. It performs high-accuracy, scientific computations as part of a customized host processor or as a powerful stand-alone device. Its advanced math processing capabilities allow the chip to accelerate the performance of both CISC- and RISC-based systems.

High-end computer systems, such as graphics workstations, mini-computers and 32-bit personal computers, can utilize the single-chip 'ACT8847 for both floating point and integer functions.

'ACT8847 FUNCTIONAL BLOCK DIAGRAM



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SN74ACT8841
DIGITAL CROSSBAR SWITCH

Features

- High-Speed Programmable Switch for Parallel Processing Applications
- Dynamically Recongifurable for Fault-Tolerant Routing
- 64 Bidirectional Data I/Os in 16 Nibble (Four-Bit) Groups
- Data I/O Selection Programmable by Nibble
- Eight Banks of Control Flip-Flops for Storing Configuration Programs
- Two Selectable Hard-Wired Switching Configurations
- Selectable Stored-Data or Real-Time Inputs

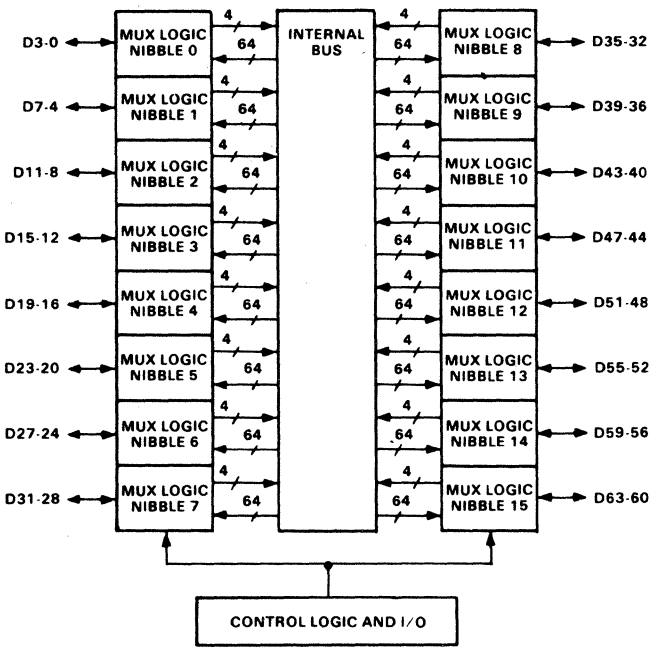
Description

The SN74ACT8841 is a single-chip digital crossbar switch that cost-effectively eliminates bottlenecks to speed data through complex bus architectures.

The 'ACT8841 has 16 four-bit bidirectional ports which can be connected in any conceivable combination. Total time for data transfer is 14-ns flowthrough.

The 'ACT8841 is ideal for multiprocessor application, where memory bottlenecks tend to occur. For example, four 32-bit buses can be easily connected by two 'ACT8841 devices. System architectures based on the 16-port 'ACT8841 can include up to 16 switching nodes (i.e., processors, memories, or bus interfaces). Larger processor arrays can be build with multistage interconnect schemes.

'ACT8841 FUNCTIONAL BLOCK DIAGRAM



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TEXAS INSTRUMENTS BUILDING BLOCK PROCESSORS

SELECTION GUIDE

8-BIT-SLICE PROCESSOR FAMILY

PINS/ PKG.	DEVICE TYPE	MAX POWER (W)	Tpd (ns) MAX	DESCRIPTION
68	SN74AS888	1.53	100§¶	8-BIT REGISTERED ALU
68	SN74AS888-1	1.53	87§¶	SPEED ENHANCED VERSION OF AS888
68	SN74AS887	1.53	75§	NON-CASCADABLE 8-BIT REGISTERED ALU
68	SN74AS890	1.82	76§	14-BIT MICROSEQUENCER
68	SN74AS890-1	1.82	69§	SPEED ENHANCED VERSION OF AS890
68	SN74AS895	1.53	87§	8-BIT MEMORY ADDRESS GENERATOR
68	SN74AS897A	0.85	33	16-BIT EXPANDABLE BARREL SHIFTER
24/28	SN74AS870/871	1.05	15	DUAL 16 X 4 REGISTER FILES

ECL 8 BIT-SLICE PROCESSOR FAMILY

84	TIET890	5	20§	AS890 TTL OUTPUTS

32 BIT PROCESSOR FAMILY

208	SN74ACT8832	<1	50§	32-BIT CMOS REGISTER ALU
156	SN74ACT8836	<1	35‡†	32 X 32 BIT CMOS MULTIPLIER/ACCUMULATOR
208	SN74ACT8837	<1	60‡	64-BIT CMOS FLOATING POINT PROCESSOR
84	SN74AS8838	<4	25	32-BIT BARREL SHIFTER
85	SN74AS8839	<4	25	32-BIT SHUFFEL EXCHANGE NETWORK
156	SN74AS8840	<4	25	16 PORT CROSSBAR SWITCH
156	SN74ACT8841	<1	20	16 PORT CMOS CROSSBAR SWITCH
208	SN74ACT8847	<1	30,40,60	64-BIT CMOS FLOATING POINT PROCESSOR
208	SN74ACT8867	<1	62	32-BIT VECTOR PROCESSOR

16-BIT CMOS PROCESSOR FAMILY

84	SN74ACT8818	<1	45	1μ EPIC™ 16-BIT CMOS MICROSEQUENCER
52	SN74ACT29116-1	145mW	85§	16-BIT MICROGRAMMABLE PROCESSOR

CMOS MULTIPLIERS

156	SN74ACT8836	<1	35†‡	32 X 32 BIT MULTIPLIER/ACCUMULATOR
208	SN74ACT8837	<1	60‡	64-BIT FLOATING POINT PROCESSOR
64	THCT1010-100	150mW	100†	16 X 16 BIT MULTIPLIER/ACCUMULATOR
64	TACT1010-65	150mW	65†	16 X 16 BIT MULTIPLIER/ACCUMULATOR
208	SN74ACT8847	<1	30,40,60‡	64-BIT FLOATING POINT PROCESSOR
208	SN74ACT8867	<1	62	32-BIT VECTOR PROCESSOR

† MULTIPLY/ACCUMULATE TIME
‡ INTERNAL PIPELINE MODE
§ MAXIMUM SYSTEM INSTRUCTION CYCLE TIME
¶ 16-BIT CONFIGURATION
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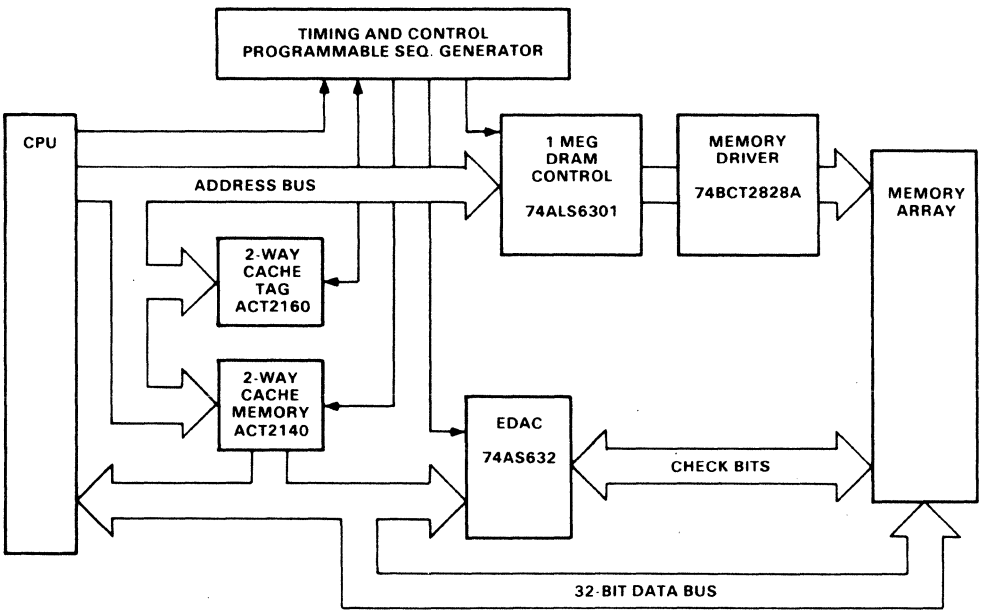
TEXAS INSTRUMENTS MEMORY MANAGEMENT PRODUCTS



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MEMORY MANAGEMENT SELECTION GUIDE

DRAM CONTROLLERS

PINS	DEVICE TYPE	Tpd (ns) MAX	DESCRIPTION
40	TMS4500A	250†	64K DRAMS, ON-CHIP REFRESH TIMING CONTROL
48	THCT4502	125†	256K DRAMS, ON-CHIP REFRESH TIMING CONTROL
48	THCT4502B	115†	256K DRAMS, ON-CHIP REFRESH TIMING CONTROL
52	SN74ACT4503	90†	1M-BIT DRAMS, ON-CHIP REFRESH TIMING CONTROL
48	SN74ALS2967	35†	256K DRAMS, >200 TO 60 NS DRAMS, RASI, CASI
48	SN74ALS2968	35†	256K DRAMS, >200 TO 60 NS DRAMS, RASI, CASI
16	SN74ALS6300	N/A	INPUT SELECTABLE REFRESH TIMER
52	SN74ALS6301	35†	1M-BIT DRAMS, >200 TO 60 NS DRAMS, RASI, CASI
52	SN74ALS6302	35†	1M-BIT DRAMS, >200 TO 60 NS DRAMS, RASI, CASI
20	SN74ALS6310	12	STATIC COLUMN DECODE, PAGE-MODE ACCESS
20	SN74ALS6311	12	STATIC COLUMN DECODE, PAGE-MODE ACCESS

CACHE COMPONENTS

52	SN74ACT2140	25/30†	8K x 18 OR 4K x 18 2-WAY SET ASSOCIATIVE CACHE DATA RAM
24	TMS2150	35‡	512 x 8 CACHE TAG RAM
24	TACT2150	30/20†	1μm EPIC™ FASTEST AVAILABLE, 512 x 8 RAM
28	SN74ACT2151	25/35‡	1K x 11 CACHE TAG RAM
28	SN74ACT2152	25/35‡	2K x 8 CACHE TAG RAM
28	SN74ACT2153	25/35‡	1K x 11 RAM WITH OPEN DRAIN MATCH PIN
28	SN74ACT2154	25/35‡	2K x 8 RAM WITH OPEN DRAIN MATCH PIN
48	SN74ACT2155	25/35‡	2K x 8 RAM 68030 CACHE TAG RAM
48	SN74ACT2158	25/35‡	8K x 9 CACHE TAG RAM
48	SN74ACT2159	25/35‡	8K x 9 RAM WITH OPEN DRAIN MATCH PIN
40	SN74ACT2160	20‡	8K x 4 2-WAY SET ASSOCIATIVE CACHE TAG RAM
28	SN74ACT2163	20‡	16K x 5 CACHE TAG RAM

† MEMORY ACCESS TIME
‡ ADDRESS MATCH TIME
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MEMORY MANAGEMENT SELECTION GUIDE

ERROR DETECTION AND CORRECTION DEVICES

PINS	DEVICE TYPE	Tpd (ns) MAX	DESCRIPTION
40	SN74ALS616	40§	16-BIT, 3-STATE
40	SN74AS616	25§	SPEED ENHANCED ALS616
28	SN74LS630	30§	16-BIT, NO BYTE-WRITE, 3-STATE
28	SN74LS631	30§	16-BIT, NO BYTE-WRITE, OPEN COLLECTOR
52	SN74ALS632A	40§	32-BIT, 3-STATE
52	SN74ALS632B	30§	SPEED ENHANCED ALS632A
52	SN74AS632	25§	FASTEST 32-BIT EDAC AVAILABLE
48	SN74ALS634A	40§	32-BIT, NO BYTE-WRITE, 3-STATE
48	SN74AS634	25§	SPEED ENHANCED ALS634

MEMORY MAPPERS PROVIDE PAGE MEMORY MAPPING

40	SN74LS610	85†	LATCHED, 3-STATE OUTPUTS
40	SN74LS611	90†	LATCHED, OPEN COLLECTOR OUTPUTS
40	SN74LS612	85†	3-STATE OUTPUTS
40	SN74LS613	90†	OPEN COLLECTOR

MOS MEMORY DRIVERS WITH SERIES DAMPING RESISTORS

20	SN74BCT2240	35‡	BiCMOS OCTAL BUFFER/DRIVERS INVERTING 3-STATE
20	SN74BCT2241	35‡	BiCMOS OCTAL LINE/MOS DRIVERS 3-STATE
20	SN74BCT2244	35‡	BiCMOS OCTAL LINE/MOS DRIVERS 3-STATE
20	SN74BCT2540	35‡	BiCMOS OCTAL BUFFER/DRIVERS INVERTING 3-STATE
20	SN74BCT2541	35‡	BiCMOS OCTAL LINE/MOS DRIVERS 3-STATE
24	SN74BCT2827A	12‡	BiCMOS 10-BIT BUFFER/DRIVER 3-STATE
24	SN74BCT2828A	12‡	BiCMOS 10-BIT BUFFER/DRIVER INVERTING 3-STATE
20	SN74ALS2240	15‡	OCTAL BUFFER/DRIVERS INVERTING 3-STATE
14	SN74ALS2242	30‡	QUAD BUS TRANSCEIVER/MOS DRIVER
20	SN74ALS2244	30‡	OCTAL BUFFER/DRIVERS INVERTING 3-STATE
20	SN74ALS2540	30‡	OCTAL LINE/MOS DRIVERS 3-STATE
20	SN74ALS2541	30‡	OCTAL LINE/MOS DRIVERS 3-STATE
20	SN74AS2620	30‡	OCTAL BUS TRANSCEIVER/MOS DRIVER
20	SN74AS2623	35‡	OCTAL BUS TRANSCEIVER/MOS DRIVER
20	SN74AS2640	35‡	OCTAL BUS TRANSCEIVER/MOS DRIVER
20	SN74AS2645	35‡	OCTAL BUS TRANSCEIVER/MOS DRIVER

§ SINGLE BIT DETECTION TIME
† ADDRESS MATCH TIME
‡ Iol (mA)

VLSI SUPPORT DOCUMENTATION

ITEM	LIT ID #
MEMORY MANAGEMENT INFORMATION PACKET	SDVP039A
MEMORY MANAGEMENT APPLICATIONS HANDBOOK	SDVA002A
LS610/631 APPLICATIONS REPORT	SDLA003
LS610 THRU 613 APPLICATIONS NOTE	SDLA004
MOS MEMORY/MEMORY MANAGEMENT DATA BOOK	SMYD008
ACT8800 FAMILY OVERVIEW	SCSB078
SN74ACT8800 FAMILY DATA BOOK	SCSS006A

ITEM	LIT ID #
SN74ACT8837/TMS34010 APPLICATION REPORT	SCAA003
SN74ACT8837 BINARY DIVISION AND SQUARE ROOT APPLICATION REPORT	SCAA002
BIT-SLICE PRODUCT BULLETIN	SDBT001
BIT-SLICE FAMILY PRODUCTS APPLICATIONS NOTE	SDBA001
AS888/890 USER'S GUIDE	SDBU001A
AS897 USER'S GUIDE	SDBU003
2 VOLT REGULATOR PRODUCT APPLICATIONS	SDBA002

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TEXAS INSTRUMENTS FIFO MEMORY PRODUCTS

HIGH-SPEED DATA TRANSFER WITHOUT THE HEADACHES

- TI's SN74ALS2238/9 40-MHz BIDIRECTIONAL FIFOs simplify bus coupling by offering two 32 X 9 FIFOs with programmable depths, transceiver circuitry, and control logic in a single package.
- The SN74ALS2232/3/4 (64 X 8/9) 40 MHz zero-fallthrough FIFOs are easily cascaded in width. The '2234 can also be cascaded in depth.
- TI's EPIC CMOS SN74ACT7201A/2A zero-fallthrough FIFOs offer an access time of 25 ns with <100 mA Icc at Fmax, and zero standby power.
- TI's SN74ALS234/5/6 toggle-through FIFOs can be cascaded to create larger buffers for continuous streams of data at rates up to 30 MHz. They are pin-compatible to the MMI '67400 series.
- Offering a 24-ns typical fallthrough time, TI's SN74ALS232A/233A/229A FIFOs provide a 50% improvement over other 16 X 4 and 16 X 5 FIFOs with this architecture.

FIFO SELECTION GUIDE

DEVICE TYPE	DENSITY	Fmax	FLAGS	ADDITIONAL FEATURES	PIN AND FUNCTIONALLY COMPATIBLE	
					DEVICE	Fmax
SN74ALS229A	16 x 5	30	Empty, Full, Full - 2, Empty + 2	3-State Outputs, 24-ns Typical Fallthrough	—	—
SN74ALS232A	16 x 4	30	Empty, Full	3-State Outputs, 24-ns Typical Fallthrough	—	—
SN74ALS233A	16 x 5	30	Full, Empty, Full - 1, Empty + 1	3-State Outputs, 24-ns Typical Fallthrough	—	—
SN74ALS234	64 x 4	30	Input Ready, Output Ready	3-State Outputs, Depth Expandable	—	—
SN74ALS235	64 x 5	25	Input Ready, Output Ready, Half-Full, Almost Full/Almost Empty	3-State Outputs, Depth Expandable	—	—
SN74ALS236	64 x 4	30	Input Ready, Output Ready	Depth Expandable	MMIC67401 'C67401A 'C67401B '67401 '67401A '67401B '67L401	10 15 16.5 10 15 16.5 5
SN74ALS2232	64 x 8	40	Empty, Full	3-State Outputs, 20-ns Typical Fallthrough	—	—
SN74ALS2233	64 x 9	40	Empty, Full, Half-Full, Almost Full/Almost Empty	3-State Outputs, 20-ns Typical Fallthrough	—	—
AVAILABLE SOON						
SN74ALS2234	64 x 9	40	Empty, Full	3-State Outputs, 20-ns Typical Fallthrough, Depth Expandable	—	—
SN74ALS2238	32 x 9 x 2	40	Empty, Full	Bidirectional, Programmable Depth, 'ALS652 Transceiver Control Logic	—	—
SN74ALS2239	32 x 9 x 2	40	Empty, Full	Bidirectional, Programmable Depth, 'ALS646 Transceiver Control Logic	—	—
SN74ACT7201A	512 x 9	28.5	Empty, Full, Half-Full	25-ns Access Time, Depth Expandable	IDT7201SA/LA	22
SN74ACT7202A	1K x 9	28.5	Empty, Full, Half-Full	25-ns Access Time, Depth Expandable	IDT7202SA/LA	22
SN74ACT7203	2K x 9	22	Empty, Full, Half-Full	35-ns Access Time, Depth Expandable	IDT7203S/L	15
SN74ACT7204	4K x 9	22	Empty, Full, Half-Full	35-ns Access Time, Depth Expandable	IDT7204S/L	15

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BUS INTERFACE PRODUCTS

SELECTION GUIDE

BIPOLAR BUS INTERFACE

DEVICE	PINCOUNT	DESCRIPTION
SN74ALS646	24	OCTAL BUS TRANSCEIVER
SN74ALS648	24	OCTAL BUS TRANSCEIVER, INVERTING
SN74ALS651	24	OCTAL BUS TRANSCEIVER/REGISTER, INVERTING
SN74ALS652	24	OCTAL BUS TRANSCEIVER/REGISTER
SN74ALS653	24	OCTAL BUS TRANSCEIVER/REGISTER, INVERTING
SN74ALS654	24	OCTAL BUS TRANSCEIVER/REGISTER
SN74ALS666	24	8 BIT D-TYPE READ-BACK LATCH
SN74ALS667	24	8 BIT D-TYPE READ-BACK LATCH, INVERTING
SN74ALS992	24	9 BIT D-TYPE READ-BACK LATCH
SN74ALS993	24	9 BIT D-TYPE READ-BACK LATCH, INVERTING
SN74ALS994	24	10 BIT D-TYPE READ-BACK LATCH
SN74ALS995	24	10 BIT D-TYPE READ-BACK LATCH, INVERTING
SN74ALS996	24	8 BIT EDGE-TRIGGER, READ-BACK LATCH

Am29800 BIPOLAR EQUIVALENTS WITH 20-60% LESS POWER

DEVICE	PINCOUNT	DESCRIPTION
SN74ALS29806	24	6 BIT COMPARATOR, 2 TO 6 DECODER
SN74ALS29809	24	9 BIT IDENTITY COMPARATOR
SN74ALS29818	24	8 BIT DIAGNOSTIC/PIPELINE REGISTER
SN74ALS29821	24	10 BIT REGISTER, NON-INVERTING
SN74ALS29822	24	10 BIT BUS INTERFACE FLIP-FLOP
SN74ALS29823	24	9 BIT REGISTER, NON-INVERTING
SN74ALS29824	24	9 BIT BUS INTERFACE FLIP-FLOP
SN74ALS29825	24	8 BIT BUS INTERFACE FLIP-FLOP
SN74ALS29826	24	8 BIT REGISTER, INVERTING
SN74ALS29827	24	10 BIT BUFFER
SN74ALS29828	24	10 BIT BUFFER, INVERTING
SN74ALS29833	24	8 TO 9 BIT PARITY TRANSCEIVER, REGISTER
SN74ALS29834	24	8 TO 9 BIT PARITY TRANSCEIVER, REGISTER, INVERTING
SN74ALS29841	24	10 BIT LATCH
SN74ALS29842	24	10 BIT LATCH, INVERTING
SN74ALS29843	24	9 BIT LATCH
SN74ALS29844	24	9 BIT LATCH, INVERTING
SN74ALS29845	24	8 BIT LATCH
SN74ALS29846	24	8 BIT LATCH, INVERTING
SN74ALS29853	24	8 TO 9 BIT PARITY TRANSCEIVER, LATCH
SN74ALS29854	24	8 TO 9 BIT PARITY TRANSCEIVER, LATCH, INVERTING
SN74ALS29861	24	10 BIT TRANSCEIVER
SN74ALS29862	24	10 BIT TRANSCEIVER, INVERTING
SN74ALS29863	24	9 BIT TRANSCEIVER
SN74ALS29864	24	9 BIT TRANSCEIVER, INVERTING

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TEXAS INSTRUMENTS BUS INTERFACE PRODUCTS

MetaFlops™

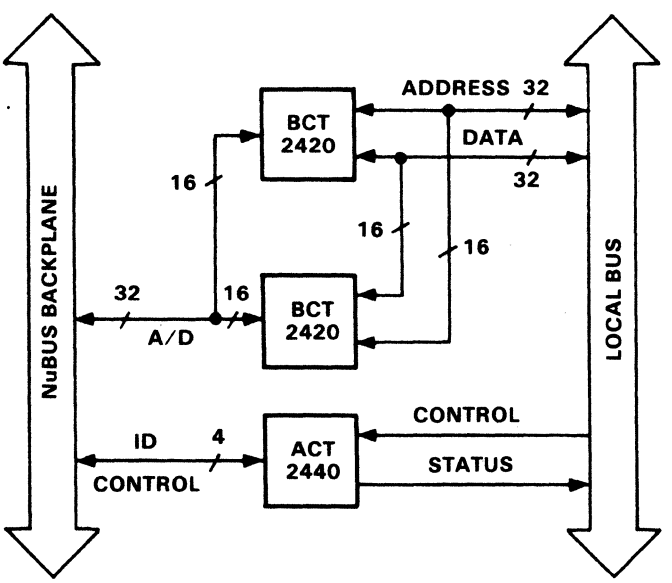
Improve data integrity and system reliability with TI's metastable resistant flip-flops - MetaFlops.

- Specifically designed for data synchronization applications
- Single-chip dual-ranked architecture dramatically improves metastable characteristics

DEVICE	PINCOUNT	DESCRIPTION
SN74AS3074	14	METASTABLE-RESISTANT DUAL, DUAL-RANKED FLIP-FLOPS
SN74AS3274	20	METASTABLE-RESISTANT OCTAL, DUAL-RANKED FLIP-FLOPS
SN74AS3374	20	METASTABLE-RESISTANT OCTAL, DUAL-RANKED FLIP-FLOPS, 3-STATE
SN74AS3474	24	METASTABLE-RESISTANT 9 BIT, DUAL-RANKED FLIP-FLOPS, 3-STATE
SN74AS3674	24	METASTABLE-RESISTANT OCTAL, DUAL-RANKED FLIP-FLOPS, 3-STATE
SN74AS4174	14	METASTABLE-RESISTANT DUAL, DUAL-RANKED FLIP-FLOPS
SN74AS4374	20	METASTABLE-RESISTANT OCTAL, DUAL-RANKED FLIP-FLOPS, 3-STATE

NuBus™ Interface Solutions

- SN74ACT2440
  32-bit Master/Slave NuBus Interface Controller
- SN74BCT2420
  16-bit NuBus Interface Transceivers and Registers
- SN74ACT2441
  16-bit NuBus Controller for Macintosh Coprocessor Platform™
- SN74BCT2425
  NuBus Transceivers for Macintosh Coprocessor Platform



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TEXAS INSTRUMENTS PROGRAMMABLE LOGIC DEVICES

STANDARD BIPOLAR PLDs

DESCRIPTION	DEVICE TYPE	PACKAGE	t_{pd} (nsec)		T_{su} (nsec)	t_{en} (nsec)		t_{dis} (nsec)		I_{CC} (mA)
			I TO O	CLK TO Q		OE TO Q	I TO O	OE TO Q	I TO O	
7 nsec, 20 pin IMPACT-X PLD	TIBPAL16L8-7 TIBPAL16R8-7 TIBPAL16R6-7 TIBPAL16R4-7	N, FN	7.5	6.5	7	7.5	7.5	7.5	7.5	210
10 nsec, 20 pin IMPACT-X PLD	TIBPAL16L8-10 TIBPAL16R8-10 TIBPAL16R6-10 TIBPAL16R4-10	N, FN	10	8	10	10	10	10	10	180
12 nsec, 20 pin IMPACT PLD	TIBPAL16L8-12 TIBPAL16R8-12 TIBPAL16R6-12 TIBPAL16R4-12	N, FN	12	10	10	10	12	10	12	200
15 nsec, 20 pin IMPACT PLD	TIBPAL16L8-15 TIBPAL16R8-15 TIBPAL16R6-15 TIBPAL16R4-15	N, FN	15	12	15	12	15	10	15	180
25 nsec, 20 pin IMPACT PLD	TIBPAL16L8-25 TIBPAL16R8-25 TIBPAL16R6-25 TIBPAL16R4-25	N, FN	25	15	20	20	25	20	25	100
15 nsec, 24 pin IMPACT PLD	TIBPAL20L8-15 TIBPAL20R8-15 TIBPAL20R6-15 TIBPAL20R4-15	NT, FN, NL	15	12	15	15	18	12	15	180
25 nsec, 24 pin IMPACT PLD	TIBPAL20L8-25 TIBPAL20R8-25 TIBPAL20R6-25 TIBPAL20R4-25	NT, FN, NL	25	15	25	15	25	15	25	105
20 nsec, Exclusive - OR	TIBPAL20L10-20 TIBPAL20X10-20 TIBPAL20X8-20 TIBPAL20X4-20	NT, FN	20	15	20	15	20	15	20	165/180
30 nsec, Exclusive - OR	TIBPAL20L10-30 TIBPAL20X10-30 TIBPAL20X8-30 TIBPAL20X4-30	NT, FN, NL	30	15	30	20	30	20	30	165/180
OUTPUT MACROCELL PLD	TIBPAL22V10	NT, FN	35	25	30	35	35	35	35	180
	TIBPAL22V10A	NT, FN	25	15	20	25	25	25	25	180
	TIBPAL22VP10-20	NT, FN	20	12	15	20	20	20	20	210
	TIBPAL22V10-15	NT, FN	15	12	12	15	15	15	15	180

PROGRAMMABLE ADDRESS DECODERS

DEVICE	DESCRIPTION	PACKAGE*	T_{pd} (nsec)	I_{cc} (mA)
TIBPAD16N8-7	7NS PROGRAMMABLE ADDRESS DECODER	N,FN	7	180
TIBPAD18N8-6	6NS PAD WITH INCREASED I/O FLEXIBILITY	N,FN	6	180

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TEXAS INSTRUMENTS PROGRAMMABLE LOGIC DEVICES

NEW PLD'S FROM TEXAS INSTRUMENTS

PROGRAMMABLE LOGIC SEQUENCERS

DEVICE	DESCRIPTION	PACKAGE*	f_{max} MHz	I_{CC} (mA)
TIBPSG507	PROGRAMMABLE SEQUENCE GENERATOR WITH 6-BIT BINARY COUNTER	FN, NT (24 PIN)	50	180
TIBPLS506	PROGRAMMABLE LOGIC SEQUENCER	FN, NT (24 PIN)	50	180
TIB82S105B	HIGH-SPEED LOGIC SEQUENCER	FN, N (28 PIN)	50	180
TIB82S167B	HIGH-SPEED LOGIC SEQUENCER	NT (24 PIN)	50	180

STANDARD BIPOLAR PLDs

DEVICE	DESCRIPTION	PACKAGE*	T_{pd} (nsec)	I_{CC} (mA)
TIBPAL16XXH-15	15 nsec 20 pin HALF-POWER IMPACT PLD	N, FN	15	90
TIBPAL20XX-10 (XX = L8, R8, R6, OR R4)	10 nsec 24 pin IMPACT PLD	N, FN	10	210

ECL PLDs

DEVICE	DESCRIPTION	PACKAGE*	T_{pd} (nsec)	I_{CC} (mA)
TIBPAL10H16P8-6	IMPACT-X 10KH ECL PAL	JT	6	240
TIBPAL10H16P8-3	IMPACT-X 10KH ECL PAL	JT	3	240
TIBPAL10H16P8-3	IMPACT-X 100K ECL PAL	JT	3	240

CMOS PLDs - COMMERICAL & INDUSTRIAL TEMPERATURE RANGE

DEVICE	DESCRIPTION	PACKAGE*	T_{pd} (nsec)	I_{CC} (mA)
TICPAL18V8-30	ERASABLE PLD; 0 STANDBY POWER	J, L, N, FN	30	0-70
TICPAL22V10Z-35	ERASABLE PLD; 0 STANDBY POWER, OR TURBO BIT OPTION	J, L, NT, FN	35	0-70

HIGH GATE COUNT EPLDs

DEVICE	DESCRIPTION	PACKAGE*	T_{pd} MHz	I_{CC} (mA)	EQUIV GATE COUNT
EP610	ZERO POWER, HIGH GATE COUNT, EPLD	D, P, J, L	25	0-70	600
EP910	ZERO POWER, HIGH GATE COUNT, EPLD	D, P, J, L	35	0-70	900
EP1810	ZERO POWER, HIGH GATE COUNT, EPLD	J, L, G	56	0-70	1800

*PACKAGE TYPES - PAL

SYMBOL	DESCRIPTION
N	20-PIN PLASTIC DIP
NL	28-PIN PLCC, NON-JEDEC PIN-OUT
NT	24-PIN, 300-MIL PLASTIC DIP
JT	24-PIN, 300-MIL CERAMIC DIP
FN	PLASTIC CHIP CARRIER

*PACKAGE TYPES - EPLD

SYMBOL	DESCRIPTION
D	CERAMIC DIP
P	PLASTIC DIP
J	J-LEAD CHIP CARRIER
L	PLASTIC J-LEAD CHIP CARRIER
G	PIN GRID ARRAY

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TEXAS INSTRUMENTS EPIC™ ACL

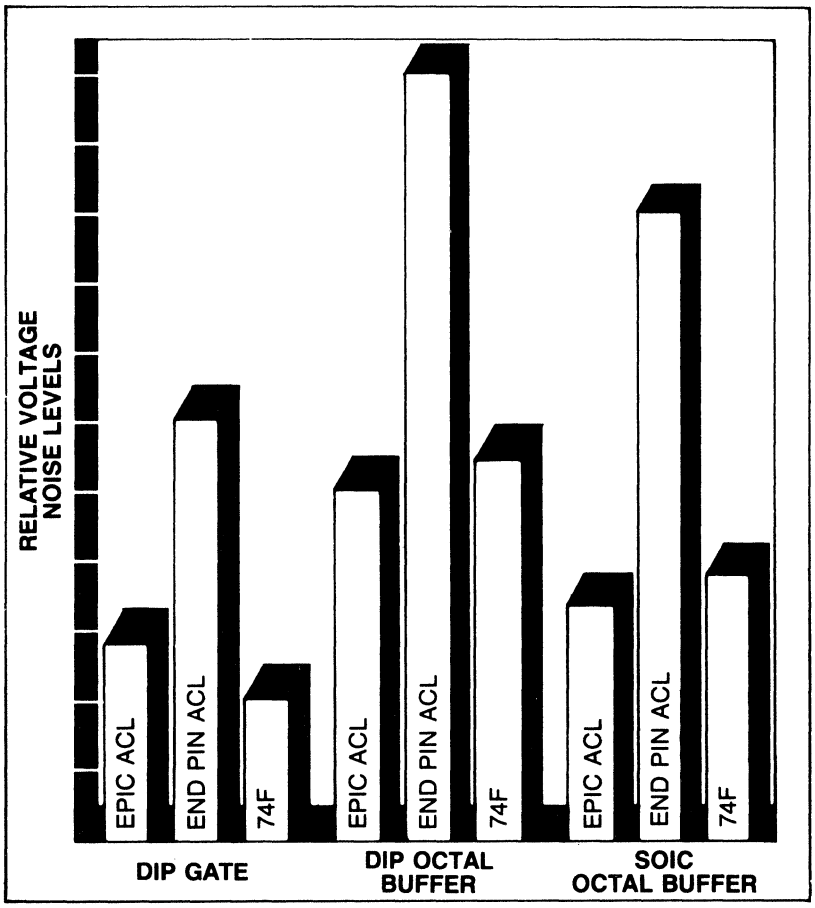
OVERVIEW

Texas Instruments offers the first advanced CMOS logic (ACL) family designed to improve system performance while reducing simultaneous switching noise. TI's EPIC™ ACL not only provides advanced speed, high drive, and low CMOS power consumption, but gives you reliable system-level operation as well.

Designated 54/74AC/ACT, components in the new EPIC ACL family have speeds comparable to advanced bipolar 74F. In addition, EPIC ACL provides 24 mA of sink/source current to drive 50-ohm transmission lines. Along with the traditional low power consumption of CMOS, TI's EPIC ACL devices feature flow-through architecture to simplify board layout.

Innovative packaging and design allow EPIC ACL to provide all this performance and still reduce noise levels by more than 50% over conventionally-packaged ACL. EPIC ACL noise levels are even less than those of advanced bipolar products.

A wide variety of traditionally bipolar logic applications will benefit from the more than 100 EPIC ACL functions. All functions are offered with both CMOS (74AC) and TTL (74ACT) level inputs, and alternate sourcing of the entire family is provided by co-developer Philips/Signetics. TI's EPIC ACL family will extend the applications of CMOS technology to such traditionally advanced bipolar markets as office automation systems, computer peripherals, mini-/personal computers, and telecommunications systems.



TI's EPIC ACL reduces simultaneous switching noise levels by more than 50% over conventional ACL and still provides advanced speed, high drive, and low CMOS power consumption. EPIC ACL noise levels are even 10% below those associated with bipolar devices.

FEATURES	BENEFITS
• OEC™ (Output Edge Control) and center-pin design	• Reduced simultaneous switching noise and a "flow through" pinout structure for easier design
• Performance comparable to advanced bipolar 74F	• Improved throughput without power penalty
• Low CMOS power consumption (essentially zero standby)	• Minimum system power required
• 24-mA sink/source currents	• High drive capability (50-ohm transmission line)
• 'AC and 'ACT options	• CMOS and TTL interface capability
• High-frequency operation (to 150 MHz)	• 3X improvement over HCMOS
• DIP and SOIC package offerings	• Flexibility of design across product family

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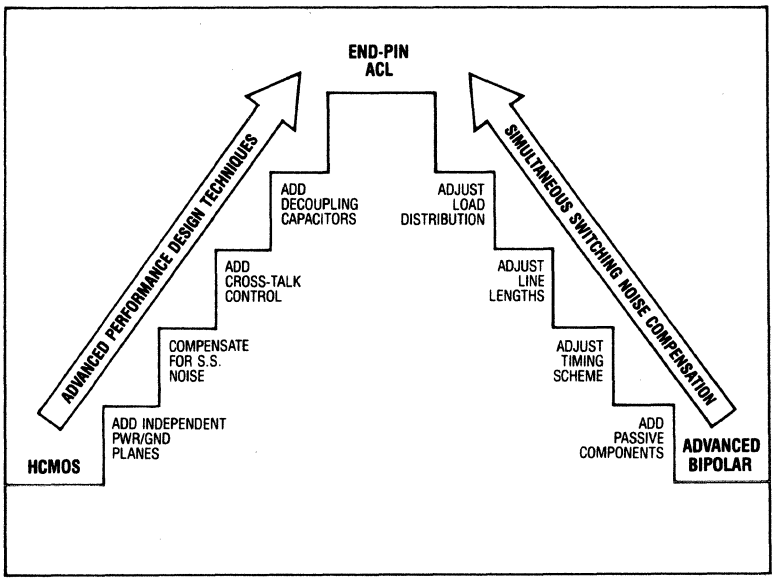
AND ABOUT DROP-IN REPLACEMENT...

Redesigning your current system to incorporate TI's EPIC ACL requires no more effort than that involved in changing to any type of ACL from some other technology. As the examples indicate, the idea of "drop-in" replacing HCMOS or advanced bipolar with end-pin ACL is unrealistic. Despite a common pinout, replacing one type of technology in a system with another type changes operating conditions and implies rethinking board layout. Changing to ACL from HCMOS means adapting your board to meet higher performance standards. Similarly, changing to conventional end-pin ACL from advanced bipolar means gearing your system to address a two-fold increase in simultaneous switching noise. The move to any type of ACL requires redesign of board layout. With EPIC ACL, you can be sure the results will be worth your efforts.



Upgrading to end-pin ACL design from HCMOS or advanced bipolar involves significantly more effort than simply dropping in the ACL devices. Several system issues must be addressed to ensure reliable operation.

THE TRUTH ABOUT DROP-IN REPLACEMENT FOR CONVENTIONAL ACL

Replacing one device in a system with a device of a different technology requires considering a great deal more than pinout compatibility, as the following examples indicate.

HCMOS TO CONVENTIONAL ACL

To change from an HCMOS design, you must introduce techniques to meet the stringent design rules associated with advanced performance products. Such board changes include:

- Adding passive components to compensate for simultaneous switching noise
- Adding independent power and ground planes
- Adding cross-talk control
- Adding decoupling capacitors
- Adjusting and recalculating termination schemes
- Re-evaluating clocks and timing to correct race conditions

ADVANCED BIPOLAR TO CONVENTIONAL ACL

Although advanced bipolar systems have been designed to handle advanced performance products, they can not handle the two-fold increase in simultaneous switching noise that a change to conventional ACL implies. The advanced bipolar system must be adapted to control the noise. The most common technique is the addition of passive components such as series resistors. The addition of passive components increases space requirements and system component cost and alters the electrical characteristics of the system.

Board layout changes include:

- Adding passive components
- Recalculating and adjusting termination schemes
- Adjusting timing schemes
- Changing trace lengths
- Correcting loading distributions

In short, conventional ACL, despite the pinout, is not drop-in replaceable to HCMOS or advanced bipolar sockets. Rather, on a broad scale, end-pin ACL demands almost an entire redesign effort.

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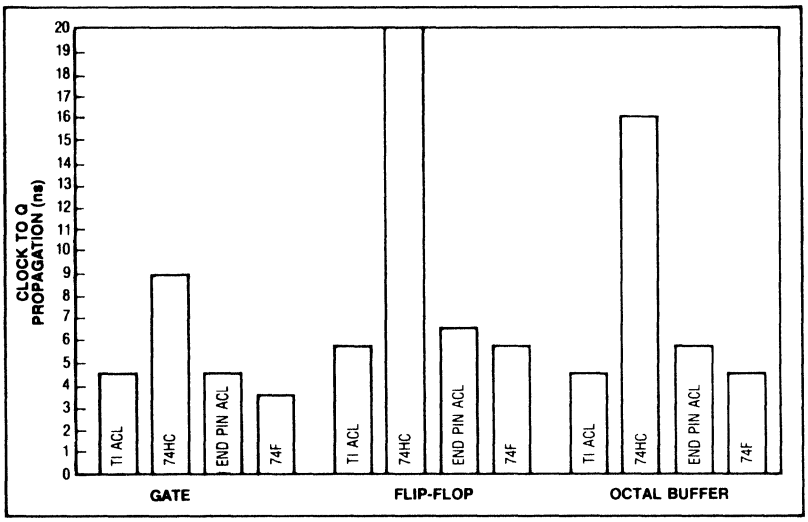
ADVANTAGES OF EPIC ACL TECHNOLOGY

TI's EPIC CMOS process combines twin-well structures for increased density with 1-micron gate lengths for increased speed. As indicated in the graph, EPIC ACL speed performance is comparable to 74F speeds. TI's EPIC process achieves advanced bipolar external propagation delay times in low-power CMOS functions with 24-mA output drive. This 24-mA drive is the standard for addressing CMOS loading, TTL loading, and low impedance line effects.



EPIC ACL speed performance is comparable to that of advanced bipolar devices, surpassing both HCMOS and end-pin ACL speeds.

CENTER PIN DESIGN REDUCES NOISE SPIKE WITHOUT SACRIFICING PERFORMANCE

System-level noise is generated in all high-performance logic chips during simultaneous switching of multiple outputs, due to package inductance and the rapid change in current levels. The wide, rail-to-rail (0 to 5 V) voltage swings of CMOS transistors cause ACL devices to generate greater levels of this noise than comparable advanced bipolar products, despite similar switching speeds. (Bipolar swings are only 0.5 to 3.5 V.)

Because the customary end-pin location of power and ground maximize package inductance, conventionally packaged ACL creates noise spikes that are unacceptably high, leading to system noise, output glitching, loss of stored data, and performance degradation. End-pin ACL forces the system designer to compensate for the noise at the system level with such techniques as limiting the number of outputs that can switch at one time; introducing "wait states" to allow outputs to settle; or, most commonly, utilizing passive components, such as series resistors, on outputs to limit current surge. Such makeshift remedies degrade system performance, defeating the purpose that led the designer to Advanced CMOS Logic in the first place.

Power and ground pins have been assigned in EPIC ACL devices to the center of dual-in-line and small-outline packages, reducing overall package inductance. An allocation scheme of one ground per two outputs allows control of switching noise throughout the family of functions. Combined with a new design technique called OEC™ (Output Edge Control), center-pin packaging significantly reduces system noise levels, enhancing system reliability.

OEC: Part Two of TI's Switching Noise Solution

OEC is the second part of EPIC ACL's dual solution for reducing system noise. OEC rounds, or smooths, the edges of the output waveform, softening the otherwise sharp, square transitions. The instantaneous current changes represented by such sharp edges contribute heavily to simultaneous switching noise. The beauty of OEC is that although output edges are smoothed, overall device speed is uncompromised and remains comparable to advanced bipolar.

TI's EPIC ACL typically achieves 50% noise level reduction over conventional end-pin ACL and 10% reduction over advanced bipolar devices in both DIP and SOIC packaging. In fact, even in SOIC packaging, conventional ACL produces noise levels still well above acceptable levels. SOIC EPIC ACL, on the other hand, keeps noise levels typically below 0.8 volts.

	DIP Gate	DIP Octal Buffer	SOIC Octal Buffer
Noise Margin Over End-Pin ACL	>50%	>50%	>60%
Noise Margin Over 74F	—	>10%	>10%

Noise Spike Summary T = 25°C, V = 5.0 V

EPIC ACL achieves substantial noise level reduction over end-pin ACL and advanced bipolar devices.

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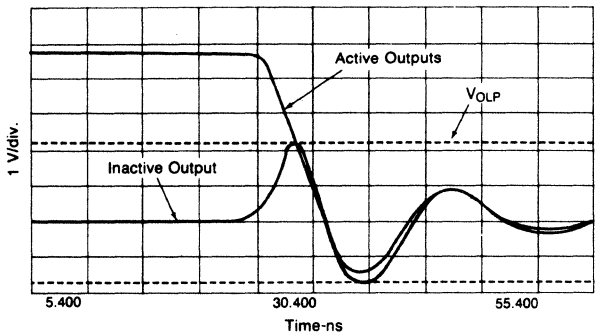
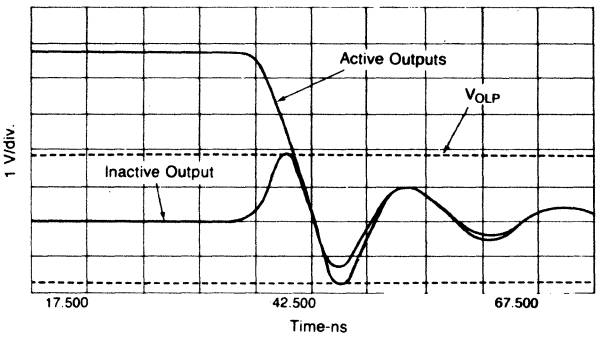
SWITCHING NOISE TEST RESULTS: EPIC VS. END-PIN

End-pin ACL DIP octal voltage spike.



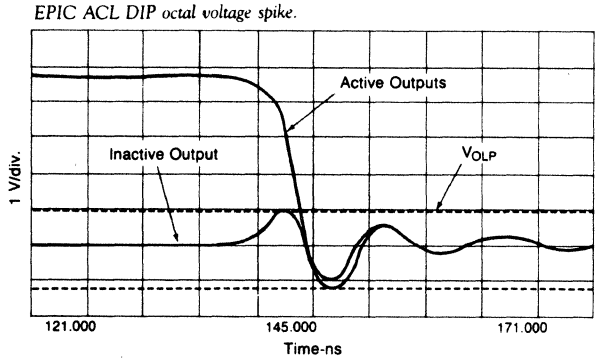
End-pin ACL SOIC octal voltage spike.



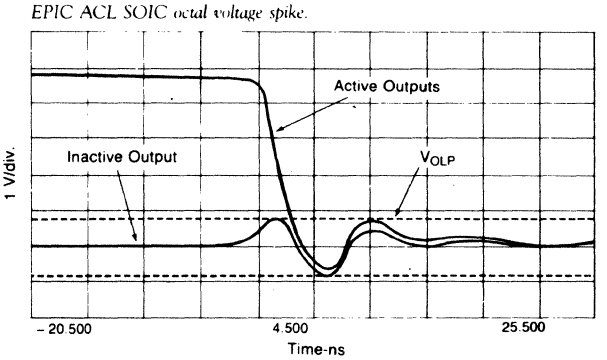
T_A 25°C, V_{CC}=5V

Seven outputs switching H-L, one output quiescent.

EPIC ACL DIP octal voltage spike.



EPIC ACL SOIC octal voltage spike.



Switching noise waveforms produced by octal devices illustrate that the voltage spike generated by EPIC ACL devices is significantly less than that produced by end-pin ACL devices in both DIP and SOIC packages.

TI UTILIZES A PRECISE TESTING STANDARD

To make ACL simultaneous switching noise comparisons, TI utilizes a testing method verified by customers, which isolates device noise from environment noise under real system conditions. Discrete leads are used as close as possible to the device output with the device noise level referenced to the ground plane of the test board. In this manner, the noise level is obtained looking at the input of the receiving device, as in a real system, rather than on-chip of the driving device.

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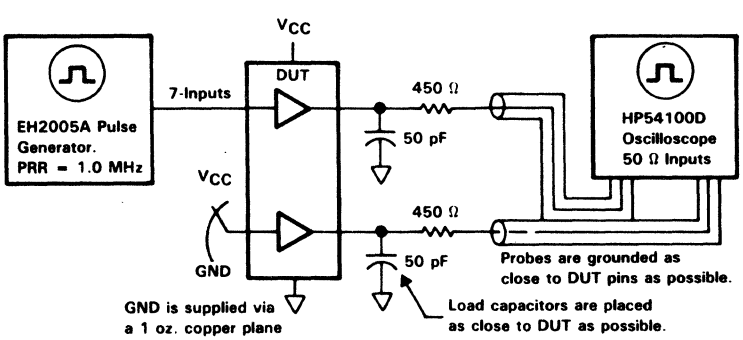

TI uses this set-up for accurately measuring simultaneous switching events. This test method yields results that have been shown to correlate with the level of switching noise produced by a circuit in a system environment.

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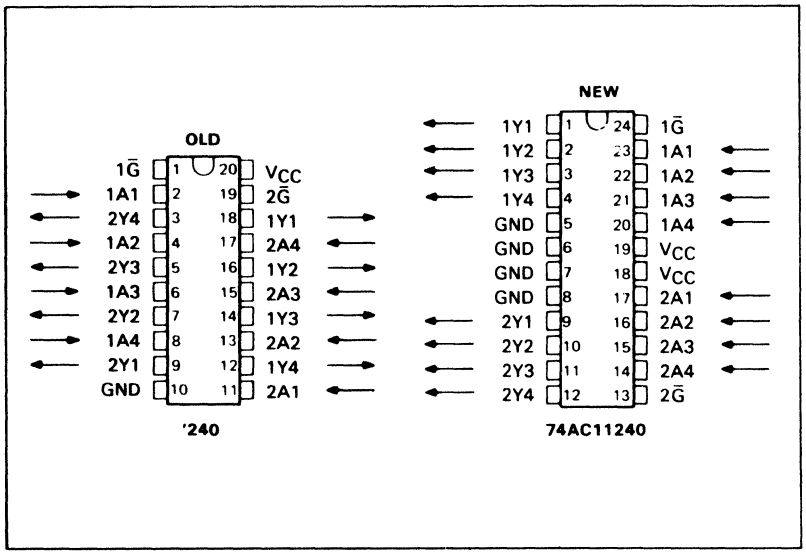
EPIC ACL OFFERS UNIQUE DESIGN ADVANTAGES

As illustrated in the adjacent figure, the EPIC ACL pinouts also simplify system design. Inputs surround power pins on one side, outputs surround ground pins on the other side, and control pins are strategically located at the package ends. This "flow-through architecture" simplifies printed circuit board design, layout, and troubleshooting.

Additionally, from a system perspective, EPIC ACL offers the lowest cost of design when compared to conventional end-pin ACL alternatives. Conventional designs sacrifice board space to passive components. Even with additional pins for reduced noise, EPIC ACL requires less system board space than end-pin ACL. The saving in component and PCB area expense makes EPIC ACL the most cost-effective design choice.



The new EPIC ACL pinout arrangement creates a "flow-through" architecture that simplifies design.

PACKAGING AND SYMBOLIZATION

EPIC ACL is available in both DIP and SOIC packages. The 103 identified device functions are offered in both AC (CMOS-compatible inputs) and ACT (TTL-compatible inputs) versions, as future additions to the family will be. EPIC ACL symbolization is summarized below. The familiar function nomenclature "XXX" is preceded by "11" to indicate a noise-reducing center-pin package.

	74	AC	11	XXX	N
1	2	3	4	5	6

1. PREFIX
BLANK = STANDARD PRODUCT
SNJ = MIL-STD-883 PROCESSED
JANB = MIL-M-38510 PROCESSED

2. TEMPERATURE RANGE
74 = COMMERCIAL/INDUSTRIAL
54 = MILITARY

3. FAMILY CODE
AC = ADVANCED CMOS
ACT = TTL COMPATIBLE ADVANCED CMOS

4. PIN DESIGNATOR
11 = CENTER PIN V_{CC}/GND

5. DEVICE TYPE
NOTE: THIS IS A THREE CHARACTER CODE, 00 NOW = 000

6. PACKAGE CODE
N = PLASTIC DIP
NT = PLASTIC DIP SLIM LINE
J = CERAMIC DIP
JT = CERAMIC SLIM LINE DIP
D = PLASTIC SMALL OUTLINE
DW = PLASTIC WIDE BODY SMALL OUTLINE
FK = LEADLESS CERAMIC CHIP CARRIER
FN = PLASTIC LEADED CHIP CARRIER

Pin Count	Package	Designator	Width (mils)
14	SOIC	D	150
16	SOIC	D	150
20	SOIC	DW	300
24	SOIC	DW	300
28	SOIC	DW	300
14	P-DIP	N	300
16	P-DIP	N	300
20	P-DIP	N	300
24	P-DIP	NT	300
28	P-DIP	NT	300
14*	C-DIP	J	300
16*	C-DIP	J	300
20*	C-DIP	J	300
24*	C-DIP	JT	300
28*	C-DIP	JT	300
20*	LCCC	FK	350
28*	LCCC	FK	450

*Military Versions

EPIC ACL is offered in a variety of DIP and SOIC packages.

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GATES AND INVERTERS WITH TWO-STATE OUTPUTS

POSITIVE-NAND GATES AND INVERTERS

74AC/ACT11004	HEX INVERTER
74AC/ACT11034	HEX NONINVERTER
74AC/ACT11010	TRIPLE 3-INPUT NAND GATE
74AC/ACT11020	DUAL 4-INPUT NAND GATE
74AC/ACT11030	8-INPUT NAND GATE
74AC/ACT11000	QUAD 2-INPUT NAND GATE

POSITIVE-AND GATES

74AC/ACT11008	QUAD 2-INPUT AND GATE
74AC/ACT11011	TRIPLE 3-INPUT AND GATE
74AC/ACT11021	DUAL 4-INPUT AND GATE

POSITIVE-NOR GATES

74AC/ACT11002	QUAD 2-INPUT NOR GATE
74AC/ACT11027	TRIPLE 3-INPUT NOR GATE

POSITIVE-OR GATES

74AC/ACT11032	QUAD 2-INPUT OR GATE

SCHMITT-TRIGGER GATES

74AC/ACT11014	HEX SCHMITT-TRIGGER INVERTER
74AC/ACT11013	DUAL 4-INPUT NAND SCHMITT-TRIGGER
74AC/ACT11132	QUAD 2-INPUT NAND SCHMITT-TRIGGER

POSITIVE AND-OR, EXCLUSIVE-OR GATES

74AC/ACT11051	DUAL 2-INPUT AND-OR GATE
74AC/ACT11064	QUAD 4-2-3-2-INPUT AND-OR GATE
74AC/ACT11086	QUAD 2-INPUT EXCLUSIVE-OR GATE
74AC/ACT11810	QUAD 2-INPUT EXCLUSIVE-NOR GATE

BUFFERS, DRIVERS AND TRANSCEIVERS WITH 3-STATE OUTPUTS

BUFFERS, DRIVERS, AND TRANSCEIVERS

74AC/ACT11827	10-BIT NONINVERTING BUFFER/DRIVER
74AC/ACT11241	8-BIT NONINVERTING BUFFER/DRIVER
74AC/ACT11244	8-BIT NONINVERTING BUFFER/DRIVER
74AC/ACT11828	10-BIT INVERTING BUFFER/DRIVER
74AC/ACT11240	8-BIT INVERTING BUFFER/DRIVER
74AC/ACT11861	10-BIT NONINVERTING TRANSCEIVER
74AC/ACT11863	9-BIT NONINVERTING TRANSCEIVER
74AC/ACT11862	10-BIT INVERTING TRANSCEIVER
74AC/ACT11864	9-BIT INVERTING TRANSCEIVER

8-BIT BIDRIECTIONAL BUS TRANSCEIVERS

74AC/ACT245	8-BIT NONINVERTING BUS TRANSCEIVERS
74AC/ACT11623	8-BIT NONINVERTING BUS TRANSCEIVERS
74AC/ACT11652	8-BIT NONINVERTING BUS TRANSCEIVERS
74AC/ACT11620	8-BIT INVERTING BUS TRANSCEIVERS
74AC/ACT11651	8-BIT INVERTING BUS TRANSCEIVERS
74AC/ACT11640	8-BIT INVERTING BUS TRANSCEIVERS
74AC/ACT11643	8-BIT INVERTING AND NONINVERTING BUS TRANSCEIVERS
74AC/ACT11646	8-BIT NONINVERTING REGISTERED BUS TRANSCEIVERS
74AC/ACT11648	8-BIT INVERTING REGISTERED BUS TRANSCEIVER
74AC/ACT11657	8-BIT NONINVERTING WITH PARITY BUS TRANSCIEVER
74AC/ACT11833	8-BIT NONINVERTING REGISTERED BUS TRANSCEIVER
74AC/ACT11834	8-BIT INVERTING REGISTERED BUS TRANSCEIVER
74AC/ACT11853	8-BIT NONINVERTING LATCHED BUS TRANSCEIVER
74AC/ACT11854	8-BIT INVERTING LATCHED BUS TRANSCEIVER

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FLIP-FLOPS

DUAL AND SINGLE FLIP-FLOPS WITH ASYNCHRONOUS CLEAR AND PRESET

74AC/ACT11109	DUAL J-K EDGE TRIGGERED FLIP-FLOP
74AC/ACT11112	DUAL J-K EDGE-TRIGGERED FLIP FLOP
74AC/ACT11074	DUAL D-TYPE FLIP-FLOP

QUAD AND HEX FLIP-FLOPS WITH POSITIVE CLOCK EDGE

74AC/ACT11174	HEX D-TYPE FLIP-FLOP
74AC/ACT11378	HEX D-TYPE FLIP-FLOP
74AC/ACT11175	QUAD D-TYPE FLIP-FLOP
74AC/ACT11379	QUAD D-TYPE FLIP-FLOP

8-, 9-, AND 10-BIT D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

74AC/ACT11374	8-BIT D-TYPE NONINVERTING FLIP-FLOP
74AC/ACT11874	8-BIT D-TYPE NONINVERTING FLIP-FLOP
74AC/ACT11534	8-BIT INVERTING D-TYPE FLIP-FLOP
74AC/ACT11825	8-BIT NONINVERTING D-TYPE FLIP-FLOP
74AC/ACT11826	8-BIT INVERTING D-TYPE FLIP-FLOP
74AC/ACT11823	9-BIT NONINVERTING D-TYPE FLIP-FLOP
74AC/ACT11822	9-BIT INVERTING D-TYPE FLIP-FLOP
74AC/ACT11821	10-BIT NONINVERTING D-TYPE FLIP-FLOP
74AC/ACT11822	10-BIT INVERTING D-TYPE FLIP-FLOP
74AC/ACT11273	8-BIT D-TYPE FLIP-FLOP
74AC/ACT11377	8-BIT D-TYPE FLIP-FLOP

META-FLOPS

74AC/ACT11476	8-BIT METASTABLE-RESISTANT FLIP-FLOP
74AC/ACT11477	8-BIT METASTABLE-RESISTANT FLIP-FLOP
74AC/ACT11478	8-BIT METASTABLE-RESISTANT FLIP-FLOP

COUNTERS AND LATCHES

SYNCHRONOUS COUNTERS WITH POSITIVE-EDGE CLOCK

74AC/ACT11160	4-BIT SYNCHRONOUS DECADE COUNTER
74AC/ACT11162	4-BIT SYNCHRONOUS DECADE COUNTER
74AC/ACT11168	4-BIT SYNCHRONOUS DECADE UP/DOWN COUNTER
74AC/ACT11190	4-BIT SYNCHRONOUS DECADE UP/DOWN COUNTER
74AC/ACT11192	4-BIT SYNCHRONOUS DECADE UP/DOWN COUNTER
74AC/ACT11568	4-BIT SYNCHRONOUS DECADE UP/DOWN COUNTER
74AC/ACT11161	4-BIT SYNCHRONOUS BINARY COUNTER
74AC/ACT11163	4-BIT SYNCHRONOUS BINARY COUNTER
74AC/ACT11169	4-BIT SYNCHRONOUS BINARY UP/DOWN COUNTER
74AC/ACT11191	4-BIT SYNCHRONOUS BINARY UP/DOWN COUNTER
74AC/ACT11193	4-BIT SYNCHRONOUS BINARY UP/DOWN COUNTER
74AC/ACT11569	4-BIT SYNCHRONOUS BINARY UP/DOWN COUNTER
74AC/ACT11269	8-BIT BIDIRECTIONAL BINARY COUNTER
74AC/ACT11579	8-BIT SYNCHRONOUS BIDIRECTIONAL BINARY COUNTER
74AC/ACT11461	8-BIT SYNCHRONOUS BINARY COUNTER
74AC/ACT11463	8-BIT SYNCHRONOUS BINARY COUNTER
74AC/ACT11469	8-BIT SYNCHRONOUS UP/DOWN COUNTER
74AC/ACT11590	8-BIT REGISTERED BINARY COUNTER
74AC/ACT11592	8-BIT REGISTERED BINARY COUNTER
74AC/ACT11593	8-BIT REGISTERED BINARY COUNTER
74AC/ACT11867	8-BIT SYNCHRONOUS UP/DOWN COUNTER
74AC/ACT11869	8-BIT SYNCHRONOUS UP/DOWN COUNTER

8-, 9-, AND 10-BIT LATCHES WITH 3-STATE OUTPUTS

74AC/ACT11373	8-BIT TRANSPARENT D-TYPE LATCH
74AC/ACT11873	8-BIT NONINVERTING DUAL 4-BIT LATCH
74AC/ACT11533	8-BIT INVERTING D-TYPE LATCH
74AC/ACT11845	8-BIT NONINVERTING LATCH
74AC/ACT11846	8-BIT INVERTING LATCH
74AC/ACT11843	9-BIT NONINVERTING LATCH
74AC/ACT11844	9-BIT INVERTING LATCH

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COUNTERS AND LATCHES

8-, 9-, AND 10-BIT LATCHES WITH 3-STATE OUTPUTS

74AC/ACT11841	10-BIT NONINVERTING D-TYPE LATCH
74AC/ACT11842	10-BIT INVERTING D-TYPE LATCH

DATA SELECTORS/MULTIPLEXERS AND DECODERS/DEMULTIPLEXERS

DATA SELECTORS/MULTIPLEXERS

74AC/ACT11151	8-TO-1 MULTIPLEXER
74AC/ACT11251	8-TO-1 MULTIPLEXER
74AC/ACT11153	DUAL 4-TO-1 MULTIPLEXER
74AC/ACT11253	DUAL 4-TO-1 MULTIPLEXER
74AC/ACT11352	DUAL 4-TO-1 MULTIPLEXER
74AC/ACT11353	DUAL 4-TO-1 MULTIPLEXER
74AC/ACT11157	QUAD 2-TO-1 MULTIPLEXER
74AC/ACT11158	QUAD 2-TO-1 MULTIPLEXER
74AC/ACT11257	QUAD 2-TO-1 MULTIPLEXER
74AC/ACT11258	QUAD 2-TO-1 MULTIPLEXER
74AC/ACT11150	1-OF-16 DATA GENERATOR/MULTIPLEXER

DECODERS/DEMULTIPLEXERS WITH TWO-STATE OUTPUTS

74AC/ACT11138	3-TO-8 DECODER/DEMULTIPLEXER
74AC/ACT11139	DUAL 2-TO-4 DECODER/DEMULTIPLEXER
74AC/ACT11238	3-TO-8 DECODER/DEMULTIPLEXER
74AC/ACT11239	DUAL 2-TO-4 DECODER/DEMULTIPLEXER
74AC/ACT11154	4-TO-16 LINE DECODER/DEMULTIPLEXER

REGISTERS WITH POSITIVE-CLOCK EDGE

SHIFT REGISTERS

74AC/ACT11299	8-BIT PARALLEL-IN SHIFT REGISTER
74AC/ACT11323	8-BIT PARALLEL-OUT SHIFT REGISTER
74AC/ACT11194	4-BIT BIDIRECTIONAL SHIFT REGISTER
74AC/ACT11823	9-BIT REGISTER
74AC/ACT11824	9-BIT REGISTER
74AC/ACT11825	8-BIT REGISTER
74AC/ACT11826	8-BIT REGISTER
74AC/ACT11898	10-BIT SHIFT REGISTER

OTHER REGISTERS

74AC/ACT11299	8-BIT UNIVERSAL REGISTER
74AC/ACT11323	8-BIT UNIVERSAL REGISTER
74AC/ACT11818	8-BIT DIAGNOSTIC/PIPELINE REGISTER
74AC/ACT11819	8-BIT DIAGNOSTIC WITH PARITY PIPELINE REGISTER
74AC/ACT11858	DUAL PORT 16 X 5 REGISTER FILE
74AC/ACT11859	DUAL PORT 32 X 4 REGISTER FILE
74AC/ACT11870	DUAL PORT 16 X 4 REGISTER FILE
74AC/ACT11979	8-BIT MULTIPLEXED I/O READ-BACK REGISTER
74AC/ACT11980	16 X 8 MULTIPLEXED I/O READ-BACK REGISTER
74AC/ACT11981	16 X 8 MULTIPLEXED I/O READ-BACK REGISTER
74AC/ACT11987	8 X 9 MULTIPLEXED I/O READ-BACK REGISTER
74AC/ACT11988	8 X 9 MULTIPLEXED I/O READ-BACK REGISTER
74AC/ACT11378	PARALLEL D-TYPE REGISTER
74AC/ACT11379	QUAD PARALLEL REGISTER

ARITHMETIC LOGIC UNITS, COMPARATORS, AND PARITY GENERATORS/CHECKERS

ARITHMETIC LOGIC UNITS AND LOOK-AHEAD CARRY GENERATORS

74AC/ACT11181	4-BIT ARITHMETIC LOGIC UNIT FUNCTION GENERATORS
74AC/ACT11881	4-BIT ARITHMETIC LOGIC UNIT FUNCTION GENERATORS
74AC/ACT11882	32-BIT LOOK-AHEAD CARRY GENERATOR

COMPARATORS WITH TWO-STATE OUTPUTS

74AC/ACT11520	8-BIT 20-Ω PULL-UP IDENTITY COMPARATOR
74AC/ACT11521	8-BIT STANDARD IDENTITY COMPARATOR

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9-BIT PARITY GENERATORS/CHECKERS WITH TWO-STATE OUTPUTS

74AC/ACT11280	9-BIT ODD/EVEN PARITY GENERATOR/CHECKER
74AC/ACT11286	9-BIT PARITY GENERATOR/CHECKER
74AC/ACT11250	1-OF-16 DATA GENERATOR/MULTIPLEXER
74AC/ACT11882	32-BIT FAST CARRY LOOK-AHEAD GENERATORS
74AC/ACT11677	16-BIT ADDRESS COMPARATOR
74AC/ACT11678	16-BIT LATCHED ADDRESS COMPARATOR
74AC/ACT11860	8-BIT MAGNITUDE COMPARATOR
74AC/ACT11865	8-BIT MAGNITUDE COMPARATOR
74AC/ACT11885	8-BIT MAGNITUDE COMPARATOR

DRIVERS

74AC/ACT11208	DUAL 1-TO-4 CLOCK DRIVER
74AC/ACT11800	TRIPLE 4-INPUT AND/NAND DRIVER
74AC/ACT11802	TRIPLE 4-INPUT OR/NOR DRIVER
74AC/ACT11655	8-BIT BUS DRIVER WITH PARITY
74AC/ACT11656	8-BIT BUS DRIVER WITH PARITY

TRANSCEIVERS

74AC/ACT11245	8-BIT BUS TRANSCEIVER
74AC/ACT11470	8-BIT BUS TRANSCEIVER
74AC/ACT11471	8-BIT BUS TRANSCEIVER
74AC/ACT11472	9-BIT BUS TRANSCEIVER
74AC/ACT11473	9-BIT BUS TRANSCEIVER
74AC/ACT11474	9-BIT BUS TRANSCEIVER
74AC/ACT11475	9-BIT BUS TRANSCEIVER
74AC/ACT11543	8-BIT REGISTERED TRANSCEIVER
74AC/ACT11544	8-BIT REGISTERED TRANSCEIVER

CONTROLLERS

74AC/ACT11852	8-BIT UNIVERSAL PORT CONTROLLER
74AC/ACT11856	8-BIT UNIVERSAL PORT CONTROLLER
74AC/ACT11877	8-BIT UNIVERSAL PORT CONTROLLER

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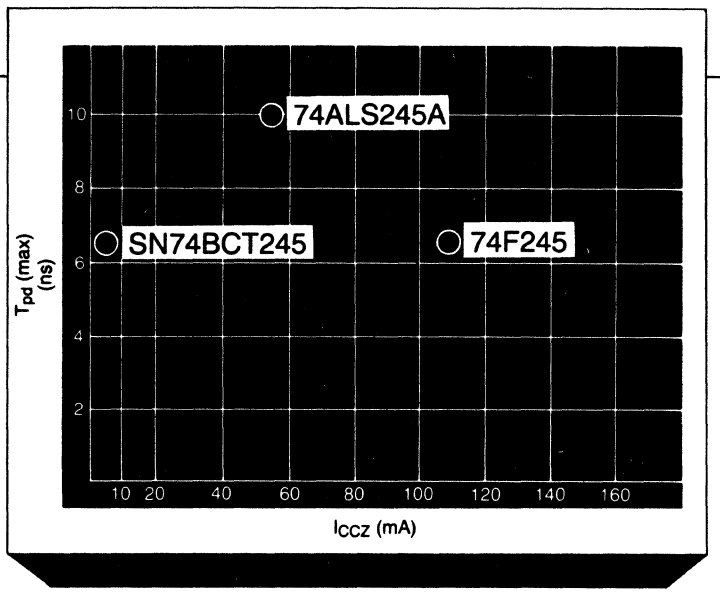
TEXAS INSTRUMENTS BiCMOS BUS INTERFACE

OVERVIEW

Texas Instruments new BiCMOS bus interface family is now available to reduce your system's power consumption up to 25% while maintaining advanced speed and output drive.

Fabricated in TI's BiCMOS process, which combines the best of bipolar and CMOS technologies, TI's new bus interface devices have switching speeds comparable to advanced bipolar products and provide the 48/64 mA drive current needed for high capacitive loads and backplanes. In addition, TI's BiCMOS devices can reduce disable supply currents by 95%, and typically reduce active currents by 50-80% over their bipolar equivalents. The comparison below of TI's new BiCMOS devices with existing technologies demonstrates the potential savings. The result can be a total system IC power savings of more than 25%.

Designated SN74BCT, TI's BiCMOS bus interface family comprises 44 popular bus interface functions, including 8-, 9-, and 10-bit latches, buffers, drivers, and transceivers, allowing for easy plug-in upgrades. These devices give you a simple means to rid your system of power waste without compromising advanced performance.



BiCMOS provides advanced bipolar speed with low CMOS power.

BiCMOS FEATURES AND BENEFITS

FEATURE	BENEFIT
• Advanced bipolar performance	• Supports 25-30 MHz bus cycle times
• 48/64 mA output drive current	• Drives high capacitive loads and backplanes
• Low power consumption	• Up to 95% power savings over advanced bipolar devices
• Offered with popular industry-standard functions	• Easy to implement for plug-in upgrades

'863 9-bit Transceiver

	I_{CC} max (mA)	
	Enabled	Disabled
SN74BCT29863	30	7
AM29863*	160	160
74F863†	145	155
Current Reduction	71-81%	95-96%

'827 10-bit Buffer/Driver

	I_{CC} max (mA)	
	Enabled	Disabled
SN74BCT29827	40	5
AM29827*	80	80
74F827†	90	90
Current Reduction	50-56%	94%

*1985 Advanced Micro Devices Bipolar Microprocessor Logic and Interface Databook
†1986 Signetics FAST Data Manual

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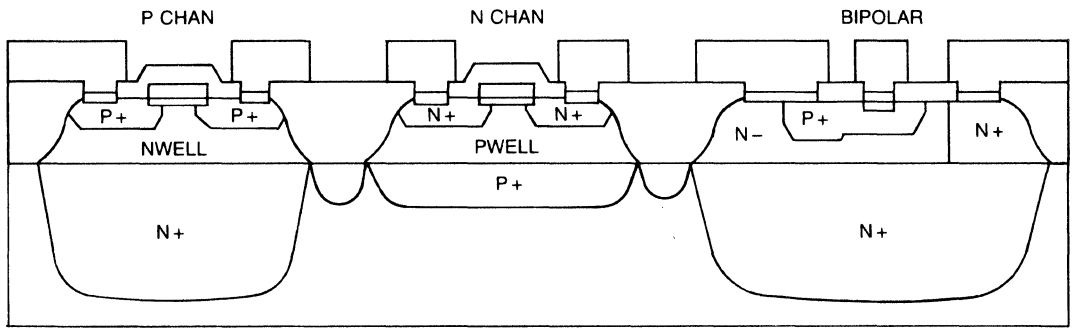


BiCMOS combines bipolar and CMOS technology on the same chip to provide advanced performance characteristics.

BiCMOS COMBINES BIPOLAR PERFORMANCE WITH CMOS EFFICIENCY

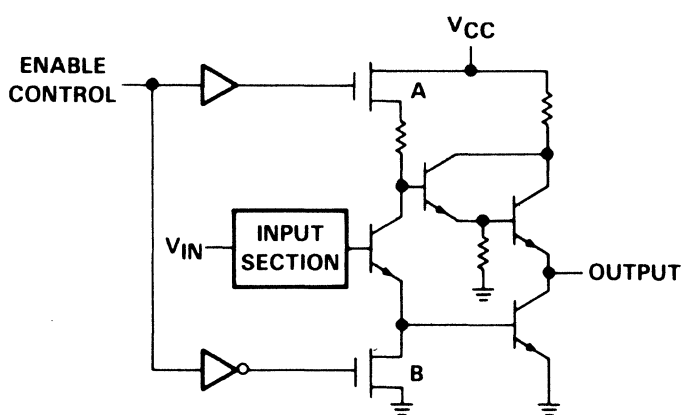
BiCMOS bus interface logic is a TTL-to-TTL interface product that surpasses traditional technology by combining TI's 2-micron bipolar IMPACT™ (Implanted Advanced Composed Technology) process with a 1.5-micron CMOS process. The combination provides advanced speed performance, enhanced output drive, and low power consumption.

Bipolar output transistors supply the 48/64 mA drive current. Hence, TI's BiCMOS products can replace advanced bipolar devices in backplane interface applications and high capacitive load lines. In particular, devices meet the drive requirements of industry-standard buses, including Multibus II® and VMEbus®.

In addition, the bipolar TTL outputs utilize the typical 0.5 V-to-3.5 V voltage swings, smaller than the GND-to-V_{CC} swings of CMOS output transistors. Smaller voltage swings reduce the overall effects of transient voltage noise produced during simultaneous switching of multiple outputs.

The CMOS process, plus an innovative circuit design, provides reduced supply current demand. TI's BiCMOS devices feature a disable characteristic that consumes about 95% less current than a pure bipolar circuit. The CMOS components combine with the bipolar to interrupt the flow of I_{CC} during the disable, or 3-state mode. Because each device spends 80-90% of its time disabled, reducing disable currents substantially lowers overall power consumption. Remaining internal components further reduce power consumption.

BiCMOS CIRCUITRY OFFERS 95% POWER REDUCTION



BiCMOS 3-state circuitry consumes 95% less disable current than pure bipolar circuitry. In this 3-state BiCMOS gate, during operation, A is shorted and B is open. During the disable, or 3-state mode, A is open and B is shorted to interrupt the flow of I_{CC}.

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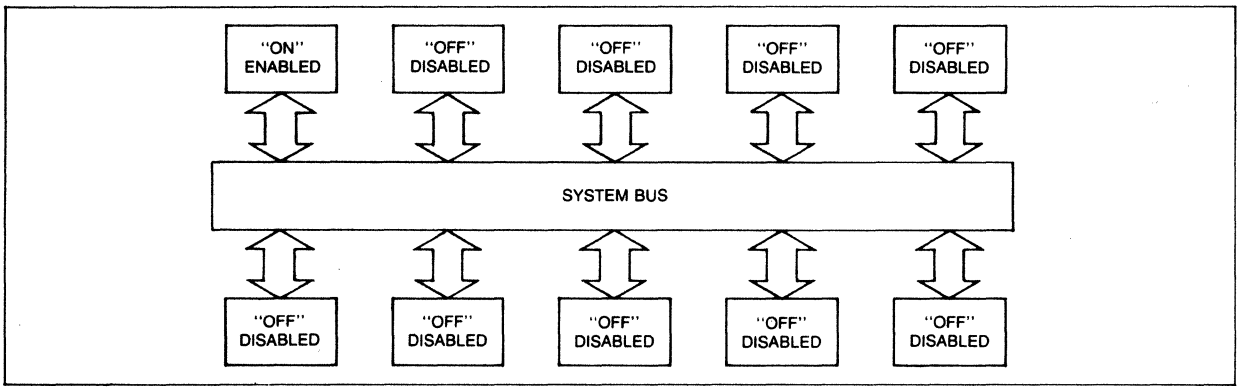

In a typical bus network only one device will be enabled at any one time. Therefore, lowering the disable current is key to overall power savings.

SUBSTANTIAL SYSTEM POWER SAVINGS MADE POSSIBLE WITH BiCMOS

TI's BiCMOS products reduction in interface logic current translates into substantial system power savings. As an example, in a typical bus interface application with 10 devices attached to a system bus, 90% of the interface logic is disabled, while one device drives the bus.

Using advanced bipolar in this example, total I_{CC} is 1600 mA:

Am29863:

I_{CC} (Enabled): 1×160 mA = 160 mA
I_{CC} (Disabled): 9×160 mA = 1440 mA
I_{CC} (Total): = 1600 mA

Using TI BiCMOS, the total current is much less, at 93 mA:

SN74BCT29863:

I_{CC} (Enabled): 1× 30 mA = 30 mA
I_{CC} (Disabled): 9× 7 mA = 63 mA
I_{CC} (Total): = 93 mA

The result is a bus interface power savings of 94%.

Because bus interface logic typically consumes 30% of the total IC power of a system, TI's BiCMOS bus interface products can reduce total system power by more than 25%. Achieving such power savings without compromising output drive or speed is a feat unmatched by traditional technologies.

OFFERING INDUSTRY STANDARD LOGIC FUNCTIONS

TI's BiCMOS family's 44 bus interface functions include 8-, 9-, and 10-bit latches, buffers, drivers, and transceivers. Listed below are the series of functional options in the BiCMOS family.

Function	Description
SN74BCT240 Series	Octal Buffer/Drivers
'245 Series	Octal Transceivers
'373 Series	Octal Latches
'543 Series	Octal Registered Transceivers
'646 Series	Octal Registered Transceivers
'29818/819	Pipeline Registers
'29820 Series	9-10 Bit Buffers and Registers
'29830 Series	Bi-Directional Parity Transceivers
'29840 Series	9-10 Bit Latches and D-Latches
'29850 Series	Bi-Directional Parity Transceivers
'29860 Series	9-10 Bit Transceivers

All these devices will be offered in both DIP and SOIC packaging. In addition, the '298XX Series devices will be offered in PLCC packaging.

The variety of functional options, combined with the choice of pinout configurations and packaging, will allow the designer to select BiCMOS devices tailored to individual system needs.

FOR MORE INFORMATION

For more information on Texas Instruments BiCMOS bus interface products, just complete and return the attached reply card. Or call your local TI field sales office, authorized distributor, or TI's Customer Response Center at 1-800-232-3200.

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BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

74BCT245	8-BIT NONINVERTING BUS TRANSCEIVER
74BCT620	8-BIT INVERTING BUS TRANSCEIVERS
74BCT623	8-BIT NONINVERTING BUS TRANSCEIVER
74BCT640	8-BIT INVERTING BUS TRANSCEIVERS
74BCT543	8-BIT NONINVERTING BUS TRANSCEIVER WITH REGISTERS
74BCT544	8-BIT INVERTING BUS TRANSCEIVER WITH REGISTERS
74BCT646	8-BIT NONINVERTING BUS TRANSCEIVER WITH REGISTERS
74BCT648	8-BIT INVERTING BUS TRANSCEIVER WITH REGISTERS
74BCT651	8-BIT INVERTING BUS TRANSCEIVER WITH REGISTERS
74BCT652	8-BIT NONINVERTING BUS TRANSCEIVER WITH REGISTERS
74BCT29833	8-9 BIT NONINVERTING BUS TRANSCEIVERS WITH PARITY CHECKER/GENERATOR
74BCT29834	8-9 BIT INVERTING BUS TRANSCEIVERS WITH PARITY CHECKER/GENERATOR
74BCT29853	8-9 BIT NONINVERTING BUS TRANSCEIVERS WITH PARITY CHECKER/GENERATOR
74BCT29854	8-9 BIT INVERTING BUS TRANSCEIVERS WITH PARITY CHECKER/GENERATOR
74BCT29863	9-BIT NONINVERTING TRANSCEIVERS
74BCT29864	9-BIT INVERTING TRANSCEIVERS
74BCT29861	10-BIT NONINVERTING TRANSCEIVERS
74BCT29862	10-BIT INVERTING TRANSCEIVERS
74BCT956	8-BIT LATCHED BUS TRANSCEIVER
74BCT957	8-BIT LATCHED BUS TRANSCEIVER
74BCT958	8-BIT LATCHED BUS TRANSCEIVER
74BCT959	8-BIT LATCHED BUS TRANSCEIVER

25-Ω BUS TRANSCEIVERS

74BCT25245	25Ω 8-BIT NONINVERTING BUS TRANSCEIVER
74BCT25620	25Ω 8-BIT INVERTING BUS TRANSCEIVER
74BCT25621	25Ω 8-BIT NONINVERTING BUS TRANSCEIVER
74BCT25622	25Ω 8-BIT INVERTING BUS TRANSCEIVER
74BCT25623	25Ω 8-BIT NONINVERTING BUS TRANSCEIVER
74BCT25640	25Ω 8-BIT INVERTING BUS TRANSCEIVER
74BCT25641	25Ω 8-BIT NONINVERTING BUS TRANSCEIVER
74BCT25642	25Ω 8-BIT INVERTING BUS TRANSCEIVER
74BCT25756	25Ω OCTAL BUS TRANSCEIVER

BUFFERS AND LINE DRIVERS/MOS MEMORY DRIVERS

74BCT2240	8-BIT BUS DRIVER (SERIES RESISTOR)
74BCT2241	8-BIT BUS DRIVER (SERIES RESISTOR)
74BCT2244	8-BIT BUS DRIVER (SERIES RESISTOR)
74BCT2410	11-BIT BUFFER (SERIES RESISTOR)
74BCT2411	11-BIT BUFFER (SERIES RESISTOR)

FLIP-FLOPS

FLIP-FLOPS WITH 3-STATE OUTPUTS

74BCT374	8-BIT NONINVERTING FLIP-FLOP D-TYPE EDGE-TRIGGERED
74BCT534	8-BIT INVERTING FLIP-FLOP D-TYPE EDGE-TRIGGERED
74BCT564	8-BIT INVERTING FLIP-FLOP D-TYPE EDGE-TRIGGERED
74BCT574	8-BIT NONINVERTING FLIP-FLOP D-TYPE EDGE-TRIGGERED
74BCT29821	10-BIT D-TYPE REGISTER, NONINVERTING
74BCT29822	10-BIT D-TYPE REGISTER, INVERTING

LATCHES AND REGISTERS

LATCHES WITH 3-STATE OUTPUTS

74BCT373	8-BIT NONINVERTING D-TYPE LATCH
74BCT533	8-BIT TRANSP. LATCH
74BCT563	8-BIT D-TYPE LATCH
74BCT573	8-BIT D-TYPE LATCH
74BCT29841	10-BIT LATCH, NONINVERTING
74BCT29842	10-BIT LATCH, INVERTING
74BCT29843	9-BIT LATCH, NONINVERTING
74BCT29844	9-BIT LATCH, INVERTING
74BCT29845	8-BIT LATCH, INVERTING
74BCT29846	8-BIT LATCH, INVERTING

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BUFFERS AND DRIVERS WITH 3-STATE OUTPUTS

74BCT125	4-BIT BUFFER WITH INDEPENDENT OUTPUT CONTROLS
74BCT126	4-BIT BUFFER WITH INDEPENDENT OUTPUT CONTROLS
74BCT241	8-BIT NONINVERTING BUS DRIVER WITH SYMMETRICAL $\overline{G}$ INPUTS
74BCT244	8-BIT NONINVERTING BUS DRIVER WITH SYMMETRICAL $\overline{G}$ INPUTS
74BCT541	8-BIT NONINVERTING BUS DRIVER WITH SYMMETRICAL $\overline{G}$ INPUTS
74BCT240	8-BIT INVERTING BUS DRIVER
74BCT540	8-BIT INVERTING BUS DRIVER
74BCT2827	10-BIT BUS DRIVERS, NONINVERTING
74BCT29827	10-BIT BUS DRIVERS, NONINVERTING
74BCT2828	10-BIT BUS DRIVERS, INVERTING
74BCT29828	10-BIT BUS DRIVERS, INVERTING

BUFFERS AND DRIVERS WITH OPEN-COLLECTOR OUTPUTS

74BCT757	8-BIT NONINVERTING BUS DRIVER
74BCT760	8-BIT NONINVERTING BUS DRIVER
74BCT756	8-BIT INVERTING BUS DRIVER

25-Ω DRIVERS WITH OPEN-COLLECTOR OUTPUTS

74BCT25757	25-Ω 8-BIT NONINVERTING BUS DRIVER
74BCT25760	25-Ω 8-BIT NONINVERTING BUS DRIVER
74BCT25756	25-Ω 8-BIT INVERTING BUS DRIVER

25-Ω LINE DRIVERS WITH 3-STATE OUTPUTS

74BCT25241	25-Ω 8-BIT BUS DRIVER
74BCT25244	25-Ω 8-BIT WITH SYMMETRICAL $\overline{G}$ INPUTS BUS DRIVER
74BCT25240	25-Ω 8-BIT INVERTING BUS DRIVER

SPECIAL BUFFERS/DRIVERS

74BCT455	8-BIT BUFFER PARITY GENERATOR/CHECKER
74BCT456	8-BIT BUFFER PARITY GENERATOR/CHECKER

OCTAL BUS TRANSCEIVERS

74BCT657	OCTAL BUS TRANSCEIVER
74BCT29861	10-BIT TRANSCEIVER, NONINVERTING
74BCT29862	10-BIT TRANSCEIVER, NONINVERTING
74BCT29863	9-BIT TRANSCEIVER, NONINVERTING
74BCT29864	9-BIT TRANSCEIVER, NONINVERTING
74BCT29833	PARITY BUS TRANSCEIVER, NONINVERTING
74BCT29834	PARITY BUS TRANSCEIVER, INVERTING

REGISTERS

74BCT819	PIPELINE REGISTER
74BCT29818	SSR DIAGNOSTIC/WCS PIPELINE REGISTER
74BCT29823	9-BIT REGISTER, NONINVERTING
74BCT29824	9-BIT REGISTER, INVERTING
74BCT29825	8-BIT REGISTER, NONINVERTING
74BCT29826	8-BIT REGISTER, INVERTING
74BCT299	8-BIT UNIVERSAL SHIFT/STRORAGE REGISTER
74BCT323	8-BIT UNIVERSAL SHIFT/STRORAGE REGISTER

BUFFERS

74BCT2827	10-BIT BUFFER (SERIES RESISTOR)
74BCT2828	10-BIT BUFFER (SERIES RESISTOR)

MEMORY DRIVERS

74BCT2827A	10-BIT MEMORY DRIVERS
74BCT2828A	10-BIT MEMORY DRIVERS

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TEXAS INSTRUMENTS OCTAL ECL TRANSLATOR FAMILY

OVERVIEW

As system complexity increases, it is often necessary to translate from one logic level to another. The need for translating usually occurs at the bus interface level, where there is an abundance of data being transmitted. Texas Instruments now offers an Octal ECL Translator family for translating from ECL to TTL or TTL to ECL logic levels. TI's IMPACT™ (Implanted Advanced Composed Technology) process is utilized to provide advanced speed, drive and low power. TI's Octal ECL Translator family uses an innovative control logic arrangement allowing the control signal to originate from either ECL or TTL environments.

The TI Octal ECL Translator family utilizes a flow through architecture and center power and ground pins. This architecture simplifies board layout while the center power and ground pins minimize high speed switching noise.

Functions in the Octal ECL Translator family include the most popular bus interface functions associated with advanced TTL logic families. All devices in the Octal ECL Translator family are 10KH or 100K compatible, offering maximum power supply flexibility.

To ensure sufficient drive and compatibility with existing TTL Bus standards, all TTL outputs on the Octal ECL Translator family provide −15mA/48mA Source/Sink capability. ECL outputs are designed to drive a 50 ohm line to −2 volts ensuring compatibility to ECL designs.

TI's ECL Translator family can fill the need for TTL to ECL and ECL to TTL translation.

OCTAL ECL TRANSLATOR FEATURES AND BENEFITS

FEATURE	BENEFIT
• 10KH or 100K ECL compatible	• Flexible power supply
• 24 pin 300 mil DIP package 24 pin SOIC package	• Reduced board area
• Octal functionality	• Reduced component count
• ECL or TTL control	• Greater control signal flexibility
• Low speed/power product rating	• Optimal system performance
• Center pin power/ground	• Minimizes high speed switching noise
• Flow through architecture	• Simplifies board layout
• TTL: −15mA/48mA source/sink ECL: 50 ohm line to −2 volts	• Bus interface capability

APPLICATIONS

ECL Translator end equipment applications include:

- Mainframe, super-mini, and mini-computer systems
- High-end workstations
- Telecommunications
- Graphics/image processing
- Office automation
- Hard disk drives
- Automatic test equipment
- Instrumentation

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INPUT AND OUTPUT CHARACTERISTICS

TI's Octal ECL Translator family includes both ECL and TTL input circuits (Fig. 1). The TTL input circuit is the PNP input structure. The PNP input structure provides reduced input current and capacitive loading to the bus. The ECL input circuit is made up of one side of an ECL differential amplifier. A 50k ohm pull down resistor to V_{EE} is provided on the ECL input circuit, which allows unused inputs to be left floating.

Output structures for TI's Octal ECL Translator family are designed to provide the drive capability required for today's advanced systems. TTL outputs provide −15/48mA source/sink output drive which allows for efficient TTL bus interfacing. The ECL outputs of TI's Octal ECL Translator family are designed to drive a 50 ohm line to −2 volts.

SYSTEM APPLICATIONS

Customers and end users expect electronic systems to become smaller, faster, and more powerful. In response to this demand, ECL is being utilized. The use of ECL brings along with it the need to be able to communicate with a TTL environment. TI's Octal ECL Translator family provides a solution for crossing the ECL and TTL boundaries efficiently. An example of a system application for TI's Octal ECL Translator family can be seen in Figure 2.

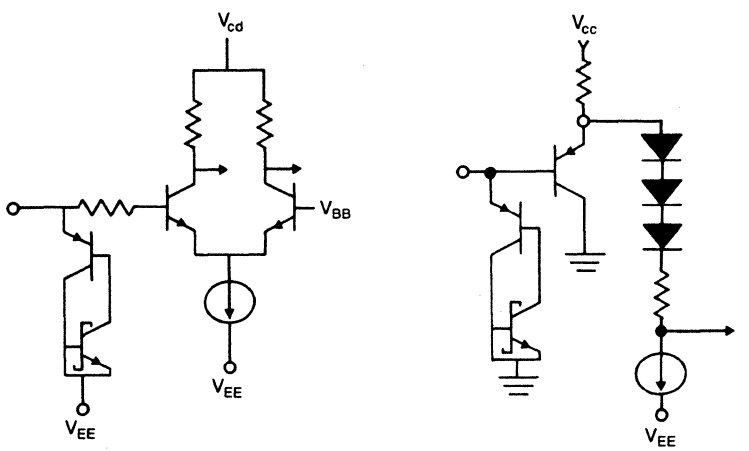

Figure 1: PNP input structure provides reduced input current and capacitive loading to the bus.

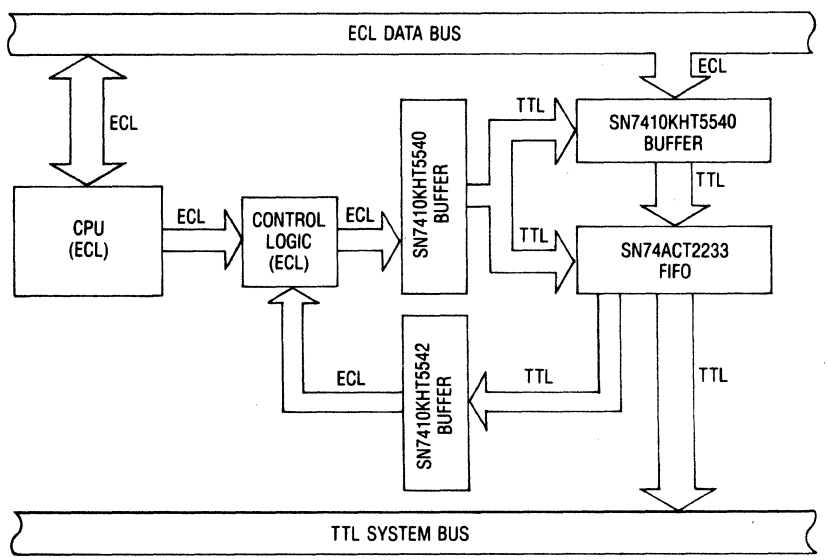

Figure 2: System application for TI's Octal ECL Translator family.

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DEVICES

TI's Octal ECL Translator family currently has over 20 devices identified—and each device is offered with a 10KH and 100K option. For every function offered, there is an ECL-to-TTL option, or a TTL-to-ECL option.

To receive the ECL Data Sheet Packet, call TI's Customer Response Center at 1-800-232-3200.

Functions currently identified are:

		ECL-to-TTL		TTL-to-ECL
Function	**Output**	**Three-State**	**O.C.**	**Output Enable**
Octal Buffers/Drivers	True Inverting	5541 5540	5539 5538	5542 —
Octal D-type Flip-Flops	True Inverting	5574 5576	— —	5578 5580
Octal D-type Latches	True Inverting	5573 5575	— —	5577 5579

		ECL-to-TTL
Function	**Output**	**Output Enable**
Octal Bidirectional Bus Transceivers A port ECL, B port TTL	True Inverting	5562 5563
Octal Bidirectional Latched Bus Transceiver A port ECL, B port TTL	True Inverting	5590 5591
Octal D-type Bidirectional Flip-Flop Bus Transceiver A port ECL, B port TTL	True Inverting	5592 5593
Octal Bidirectional Registered Bus Transceiver A port ECL, B port TTL	True Inverting	5646 5648

SYMBOLIZATION

TI's Octal ECL Translator family are available in both DIP and SOIC packages for commercial product. Translator family symbolization is summarized below:

SN	10KH	T	5542	NT
1	2	3	4	5

1. Prefix
   - SN = Standard product
   - SNJ = Mil-Std-883-processed
   - JANB = Mil-M-38510 processed
2. Family Characteristics
   - 10KH = Voltage Compensated
   - 100K = Temperature and Voltage Compensated
3. Family Code
   - T = ECL-to-TTL or TTL-to-ECL Translation
4. Device Type
   - Note: This is a four character code
5. Package Code
   - NT = 24/28 pin 300 mil DIP
   - J = ceramic DIP
   - JT = 24/28 pin 300 mil DIP
   - DW = plastic wide body SOIC
   - FK = leadless ceramic chip carrier

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Power Management?

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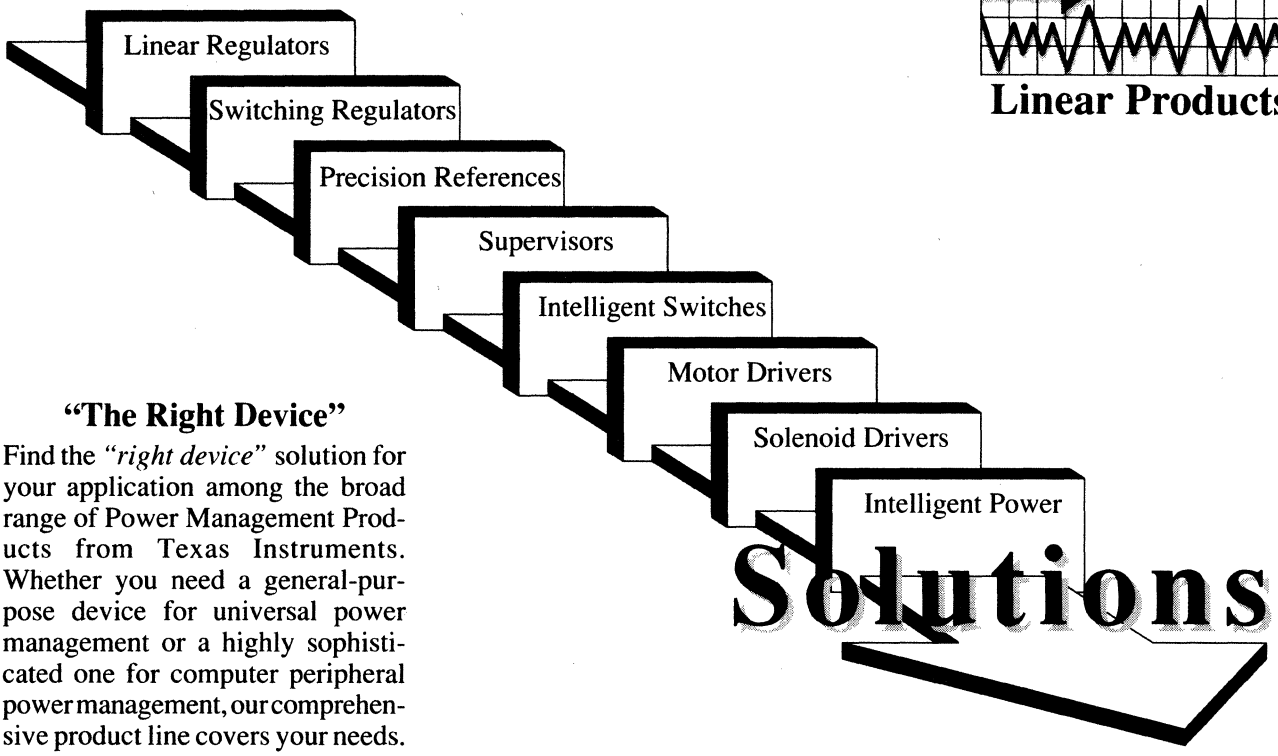
Linear Products



"The Right Device"

Find the *"right device"* solution for your application among the broad range of Power Management Products from Texas Instruments. Whether you need a general-purpose device for universal power management or a highly sophisticated one for computer peripheral power management, our comprehensive product line covers your needs. From low-dropout voltage regulators to switching power-supply controllers to advanced motor drivers to intelligent-power actuators, we have your *"right device."*

Encompassing a diverse range of devices, TI power management products are characterized by:

- Precision
- Efficiency
- Reliability
- Variety of Packages

Because of a tradition of processing expertise, you can be assured of the quality of power management products from TI. Proven quality, service, volume availability, and applications support make our devices the *"right device."*

Texas Instruments

Voltage Regulators

DEVICE	FUNCTION	PACKAGE
TL750L	Low-Dropout Voltage Regulator Series	TO92, SO, DIP
LT1009	0.2% Tolerance Voltage Regulator	TO92, SO
MC34060	PWM Controller	DIP, SO
TL1451A	Dual PWM Controller	DIP, SO
LT1054	Switched-Capacitor DC to DC Converter	DIP
TL431A	Adjustable Precision Reference	TO92, SO
LT1004	Micro-power Voltage Reference	TO92, SO
LM385-2.5	Micro-power Voltage Reference	TO92, SO

Power Integrated Circuits

DEVICE	FUNCTION	PACKAGE
L293	Quad Half-H Driver	DIP
L293D	Quad Half-H Driver	DIP
SN754410	Quad Half-H Driver	DIP
SN754411	Quad Half-H Driver	DIP
SN75439	Quad Peripheral Driver	DIP
L298	Dual Full-H Driver	SIP
TLP298	Dual Full-H Driver	SIP
TLP609	Dual Flux-Regulating Driver	SIP

For more information, contact our
Customer Response Center
1-800-232-3200
Ask for Inquiry #3406

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Linear Products

Enhanced JFETs

Precision Op Amps

for the long run . . .

TI Linear's new Enhanced JFET process solves the dilemma of extreme offset voltage drift and adds precision linear to our tradition of technology innovation and high volume manufacturing. Breaking through barriers of standard JFET technology, TI's new Enhanced JFET amplifiers provide:

- Low Initial Offset Voltage
- Virtually No Offset Voltage Drift
- Traditional JFET AC Performance
- Volume Availability
- Plastic Packaging including SO

The broad family of Enhanced JFET amplifiers includes:

High Speed TL05X

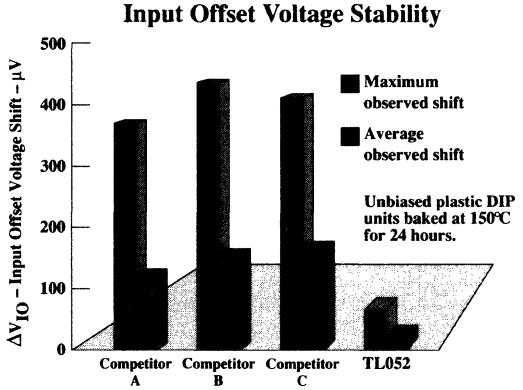
	Single	Dual	Quad	
Input Offset Voltage	1.5 mV	1.5 mV	4.0 mV	Max.
"A" Grade	0.8 mV	0.8 mV	1.5 mV	Max.
Offset Voltage Drift	8 µV/°C	6 µV/°C	23 µV/°C	Typ.
Slew Rate	23.7 V/µs	20.7 V/µs	17.8 V/µs	Typ.
Unity-Gain Bandwidth	3.1 MHz	3 MHz	3 MHz	Typ.

Low Power TL03X

	Single	Dual	Quad	
Input Offset Voltage	1.5 mV	1.5 mV	4.0 mV	Max.
"A" Grade	0.8 mV	0.8 mV	1.5 mV	Max.
Offset Voltage Drift	5.0 µV/°C	10.8 µV/°C	12 µV/°C	Typ.
Slew Rate	2.9 V/µs	2.9 V/µs	2.9 V/µs	Typ.
Unity-Gain Bandwidth	1.1 MHz	1.1 MHz	1.1 MHz	Typ.

Texas Instruments

Input Offset Voltage Stability



TI's new Enhanced JFET op amps maintain extremely stable input offset voltage even after high temperature testing.

As indicated by the adjacent graph, traditional JFET op amps are susceptible to extreme offset voltage drift due to temperature stress. The new Enhanced JFET process allows fabrication of devices with lower initial offset voltage and higher offset voltage stability than previously possible using zener trim techniques. As a result, stable, precision JFET op amps covering all performance options are now available to you in volume. Thus, TI Linear's new Enhanced JFET op amps offer you *precision for the long run.*

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For more information, contact our

Customer Response Center

1-800-232-3200

Ask for Inquiry #3403

The *"one-chip"* Analog Interface for your DSP system

Texas Instruments
Linear Products

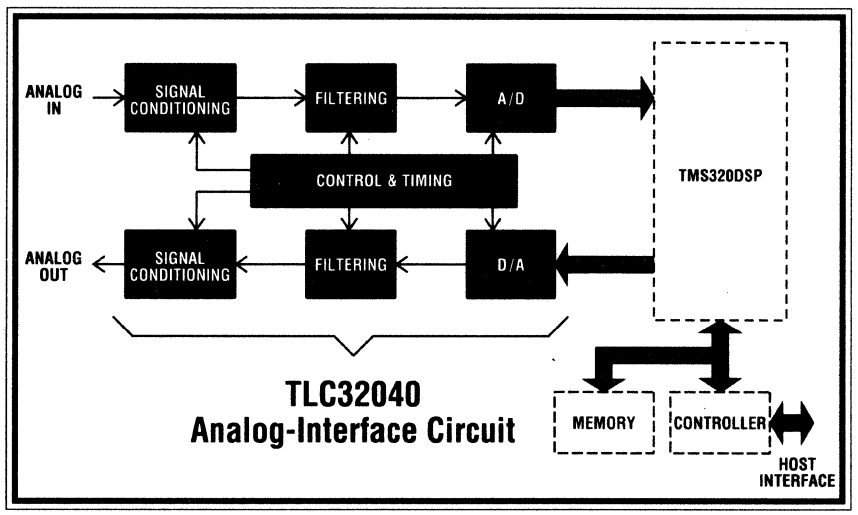
With "one-chip" convenience, TI's TLC32040 family of Analog-Interface Circuits (AICs) simplifies the task of interfacing your digital signal processing (DSP) systems with the analog world. Each AIC is a complete, flexible analog-to-digital and digital-to-analog input/output system that integrates 10-15 MSI/LSI packages. Fabrication using Advanced LinCMOS™ technology enables dense, high-performance combinations of extensive digital and analog circuitry. The result– each highly-integrated TLC32040 AIC provides these key functions:

- Input Multiplexer
- Switched-Capacitor Filters
  – antialiasing input bandpass filter
  – low-pass ouput-reconstruction filter
- High Resolution (14-bit accuracy) A/D & D/A Converters
- Four-mode Serial Port
- Control & Timing Logic

Designed as a universal DSP peripheral, each TLC32040 AIC offers flexibility. Filter characteristics, sampling rates, gain selection, and phase adjustment are all software programmable. The 14-bit dynamic range of the A/D and D/A converters enables accurate processing of both large and small signals. For flexibility and convenience, a four-mode serial port allows easy interface with most DSPs and provides direct interface with serial-input devices including the popular TMS320 DSP family.

Since the on-board filters are designed for applications in the audio band, these AICs are well suited for high speed modems, secure telephony, and high-definition speech applications, in addition to general purpose data acquisiton uses.

For more information, contact our
Customer Response Center
1-800-232-3200
Ask for Inquiry #3404



A universal DSP peripheral, the high-performance TLC32040 AIC is a complete analog interface that virtually eliminates the need for analog-design expertise in the development of DSP systems.

TLC32040 AIC Highlights

- Single-clock operation
- Signal-to-distortion ratio: 60 dB minimum
- Synchronous or asynchronous A/D & D/A operation
- Flexible, real-time software control
- Single-ended or differential mode inputs
- Auxiliary analog inputs
- 14-bit A/D & D/A Converters
- Programmable gain input buffer with 16-bit dynamic range
- Built-in loopback feature for system tests
- Fabricated in Advanced LinCMOS™ technology
- Interfaces directly with TMS320-family DSPs

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LinCMOS™ Technologies offer you Low-Power Alternatives

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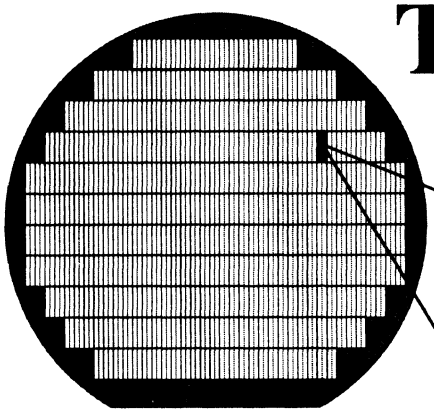

LinCMOS™

Specifically developed for Linear ICs, Texas Instruments proprietary LinCMOS™ process technology allows the development of a complete family of low-power, high-performance analog components. Designed to operate from low-voltage, single supplies at minimal power dissipation with optimum performance, LinCMOS™ devices are your low-power alternatives.

With the introduction of TI's LinCMOS™ technology, the same system advantages offered by CMOS digital circuits became available with linear devices. Low-power, low-voltage, single-supply LinCMOS™ circuits, with their reduced operating temperature and enhanced reliability, allow for smaller equipment sizes and can reduce your total system cost.

Advanced LinCMOS™

Advanced LinCMOS™ features a scaled down version of the first generation LinCMOS™ process. In addition to 5μm, Advanced LinCMOS™ has 3μm capability which is so important for integrated circuits containing both analog and digital circuits. TI's Advanced LinCMOS™ achieves the density needed for complex data-acquisition and telecommunication chips in addition to other high-performance circuits requiring the use of combined analog and digital circuitry.

For more information, contact our
Customer Response Center
1-800-232-3200
Ask for Inquiry #3405

Data Converters

TLC540/1	8-bit, 12-channel A/D Converters
TLC548/9	8-bit, single-channel A/D Converters
TLC1540/1	10-bit, 12-channel A/D Converters
TLC0820	1 MHz, 8-bit, A/D Converter
TLC7524/8	5 MHz, 8-bit D/A Converters

Switched-Capacitor Filters (SCF)

TLC10/20-MF10	Universal Dual SCF

Telecommunications & Analog Interface Circuits

TCM29C13-19	Combo (Codec & Filter) Family
TLC32040	Analog Interface Circuits for DSPs

Operational Amplifiers

TLC277/9	Precision Op Amps
TLC1078/79	Precision Micro-Power Op Amps
TLC2201	Precision Low-Noise Op Amp
TLC2652/4	Chopper-Stabilized Op Amps

Comparators

TLC339/393	Open-Drain Output Comparators
TLC372/4	High-Speed Comparators
TLC3702/4	Ultra-Low-Power Comparators

Timers

TLC551	1-Volt Timer
TLC555	5-Volt Timer

Data Transmission

SN75C188/9	RS232 Drivers/Receivers

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DRAM/VRAM/FRAM SELECTION GUIDE

DENSITY	ORGANIZATION (WORDS × BITS)	DEVICE NUMBER	MAX ACCESS TIME (ns)	POWER SUPPLY (V)	MAX POWER DISSIPATION		PINS	PACKAGE†	COMMENTS	DOCUMENT
					ACTIVE (mW)	STANDBY (mW)				
256K	256K × 1	TMS4256-8	80	5±5%	368	24	16,18	N,FM, SD	Page Mode	SMQS256C
		TMS4256-10	100	5±10%	385	25				
		TMS4256-12	120	5±10%	358	25	16			
		TMS4256-15	150	5±10%	330	25				
		TMS4257-10	100	5±10%	385	25	16,18	N,FM, SD	Nibble Mode	SMQS256C
		TMS4257-12	120		358		16			
		TMS4257-15	150		330					
	64K × 4	TMS4461-12	120	5±10%	853	110	24,24	N,SD	Multiport Video RAM	SMVS011B
		TMS4461-15	150		770					
		TMS4464-10	100	5±10%	385	25	18,18	N,FM	Page Mode	SMS464B
		TMS4464-12	120		358					
		TMS4464-15	150		330					

†N Plastic Dual In-line Package (DIP)
FM Plastic Chip Carrier (PLCC)
SD Plastic Zig-zag In-line Package (ZIP)

For a complete product specification, please call 1-800-232-3200 and request the appropriate document listed in the table above.

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DRAM/VRAM/FRAM SELECTION GUIDE (CONCLUDED)

DENSITY	ORGANIZATION (WORDS × BITS)	DEVICE NUMBER	MAX ACCESS TIME (ns)	POWER SUPPLY (V)	MAX POWER DISSIPATION		PINS	PACKAGE†	COMMENTS	DOCUMENT
					ACTIVE (mW)	STANDBY (mW)				
1024K	1024K × 1	TMS4C1024-10	100	5 ± 10%	385	17	18, 20/26	N,DJ	CMOS Enhanced Page Mode	SMGS024B
		TMS4C1024-12	120		330					
		TMS4C1024-15	150		303					
		TMS4C1025-10	100	5 ± 10%	385	17	18, 20/26	N,DJ	CMOS Nibble Mode	SMGS024B
		TMS4C1025-12	120		330					
		TMS4C1025-15	150		303					
		TMS4C1027-10	100	5 ± 10%	385	17	18, 20/26	N,DJ	CMOS Static Column Decode Mode	SMGS024B
		TMS4C1027-12	120		330					
		TMS4C1027-15	150		303					
	256K × 4	TMS44C251-10‡	100	5 ± 10%	605	28	28,28	DJ,SD	CMOS Multiport Video RAM	SMVS251
		TMS44C251-12‡	120		523					
		TMS44C251-15‡	150		468					
		TMS44C256-10	100	5 ± 10%	385	17	20, 20/26	N,DJ	CMOS Enhanced Page Mode	SMGS256A
		TMS44C256-12	120		330					
		TMS44C256-15	150		303					
		TMS44C257-10	100	5 ± 10%	385	17	20, 20/26	N,DJ	CMOS Static Column Decode Mode	SMGS256A
		TMS44C257-12	120		330					
		TMS44C257-15	150		303					
		TMS4C1050-3‡	25	5 ± 10%	275	39	16,20,26	N,SD,DJ	CMOS FRAM	SMGS050A
		TMS4C1050-4‡	30		248					
		TMS4C1050-6‡	50		193					

†N Plastic Dual In-line Package (DIP)
DJ Plastic Small Outline J-lead (SOJ)
SD Plastic Zig-zag In-line Package (ZIP)
‡Advance information for product under development by TI.

For a complete product specification, please call 1-800-232-3200 and request the appropriate document listed in the table above.

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DYNAMIC RAM MODULE SELECTION GUIDE

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					ACTIVE (mW)	STANDBY (mW)				
1024K	1024K × 1	TM4256FC1-10	100	5 ± 10%	440	99	22	Leaded	Page Mode	SMMS561B
		TM4256FC1-12	120		413					
		TM4256FC1-15	150		385					
	256K × 4	TM4256EC4-10	100	5 ± 10%	1540	99	22	Leaded	Page Mode	SMMS564C
		TM4256EC4-12	120		1430					
		TM4256EC4-15	150		1320					
2048K	256K × 8	TM4256FL8-10	100	5 ± 10%	3080	198	30	Leaded	Page Mode	SMMS568B
		TM4256FL8-12	120		2860					
		TM4256FL8-15	150		2640					
		TM4256GU8-10	100	5 ± 10%	3080	198	30	Socketable with Presence Detect	Page Mode	SMMS568B
		TM4256GU8-12	120		2860					
		TM4256GU8-15	150		2640					
2304K	256K × 9	TM4256EL9-10	100	5 ± 10%	3465	226	30	Leaded	Page Mode	SMMS569B
		TM4256EL9-12	120		3218					
		TM4256EL9-15	150		2970					
		TM4256GU9-10	100	5 ± 10%	3465	226	30	Socketable with Presence Detect	Page Mode	SMMS569B
		TM4256GU9-12	120		3218					
		TM4256GU9-15	150		2970					
4096K	1024K × 4	TM024HAC4-10	100	5 ± 10%	1540	66	24	Leaded	CMOS Enhanced Page Mode	SMMS104A
		TM024HAC4-12	120		1320					
		TM024HAC4-15	150		1210					
8192K	1024K × 8	TM024GAD8-10	100	5 ± 10%	3080	132	30	Socketable	CMOS Enhanced Page Mode	SMMS102C
		TM024GAD8-12	120		2540					
		TM024GAD8-15	150		2420					
9216K	1024K × 9	TM024EAD9-10	100	5 ± 10%	3465	149	30	Socketable	CMOS Enhanced Page Mode	SMMS102C
		TM024EAD9-12	120		2970					
		TM024EAD9-15	150		2723					

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DENSITY	ORGANIZATION (WORDS × BITS)	DEVICE NUMBER	MAX ACCESS TIME (ns)	POWER SUPPLY (V)	MAX POWER DISSIPATION		PINS	PACKAGE†	COMMENTS	DOCUMENT
					ACTIVE (mW)	STANDBY (mW)				
16K	2K × 8	TMS27C291-3	35	5±5%	394	N/A	24	J	High-Speed CMOS	SMLS291B
		TMS27C291-35	35	5±10%	413					
		TMS27C291	45	5±5%	315					
		TMS27C291-45	45	5±10%	330					
		TMS27C291-5	50	5±5%	289					
		TMS27C291-50	50	5±10%	303					
		TMS27C292-3	35	5±5%	394	N/A	24	J	High-Speed CMOS	SMLS291B
		TMS27C292-35	35	5±10%	413					
		TMS27C292	45	5±5%	315					
		TMS27C292-45	45	5±10%	330					
		TMS27C292-5	50	5±5%	289					
		TMS27C292-50	50	5±10%	303					
32K	4K × 8	TMS27C32-100‡	100	5±5%	132	1.4	24	J	CMOS	SMLS032
		TMS27C32-10‡	100	5±10%	138					
		TMS27C32-120‡	120	5±5%	132					
		TMS27C32-12‡	120	5±10%	138					
		TMS27C32-150‡	150	5±5%	132					
		TMS27C32-15‡	150	5±10%	138					
		TMS27C32-2‡	200	5±5%	132					
		TMS27C32-20‡	200	5±10%	138					
		TMS27C32‡	250	5±5%	132					
		TMS27C32-25‡	250	5±10%	138					
		TMS2732A-17	170	5±5%	657	158	24	J	NMOS	SMES732E
		TMS2732A-20	200							
		TMS2732A-25	250							
		TMS2732A-45	450							
64K	8K × 8	TMS27C49-4‡	45	5±5%	473	N/A	24	J,JT	High-Speed CMOS	SMLS049
		TMS27C49-45‡	45	5±10%	495					
		TMS27C49-5‡	55	5±5%	473					
		TMS27C49-55‡	55	5±10%	495					
		TMS27C64-100	100	5±5%	158	1.4	28	J	CMOS	SMLS064A
		TMS27C64-120	120	5±5%	158					
		TMS27C64-12	120	5±10%	165					
		TMS27C64-1	150	5±5%	158					
		TMS27C64-15	150	5±10%	165					
		TMS27C64-2	200	5±5%	158					
		TMS27C64-20	200	5±10%	165					
		TMS27C64	250	5±5%	158					
		TMS27C64-25	250	5±10%	165					
		TMS2764-17	170	5±5%	788	184	28	J	NMOS	SMES764C
		TMS2764-20	200							
		TMS2764-25	250							
		TMS2764-45	450							
		TMS28C64-25‡	250	5±10%	110	17	28	J, N	CMOS EEPROM	SMIS064
		TMS28C64-35‡	350							

†J Ceramic DIP
JT 300-mil Ceramic DIP (TMS27C49 only)
N Plastic DIP
‡Advance Information for product under development by TI.

For a complete product specification, please call 1-800-232-3200 and request the appropriate document listed in the table above.

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DENSITY	ORGANIZATION (WORDS × BITS)	DEVICE NUMBER	MAX ACCESS TIME (ns)	POWER SUPPLY (V)	MAX POWER DISSIPATION		PINS	PACKAGE†	COMMENTS	DOCUMENT
					ACTIVE (mW)	STANDBY (mW)				
128K	16K × 8	TMS27C128-100	100	5±5%	158	1.4	28	J	CMOS	SMLS128B
		TMS27C128-120	120	5±5%	158					
		TMS27C128-12	120	5±10%	165					
		TMS27C128-1	150	5±5%	158					
		TMS27C128-15	150	5±10%	165					
		TMS27C128-2	200	5±5%	158					
		TMS27C128-20	200	5±10%	165					
		TMS27C128	250	5±5%	158					
		TMS27C128-25	250	5±10%	165					
256K	32K × 8	TMS27C256-120	120	5±5%	158	1.4	28	J	CMOS	SMLS256C
		TMS27C256-12	120	5±10%	165					
		TMS27C256-150	150	5±5%	158					
		TMS27C256-15	150	5±10%	165					
		TMS27C256-1	170	5±5%	158					
		TMS27C256-17	170	5±10%	165					
		TMS27C256-2	200	5±5%	158					
		TMS27C256-20	200	5±10%	165					
		TMS27C256	250	5±5%	158					
		TMS27C256-25	250	5±10%	165					
512K	64K × 8	TMS27C512-1	170	5±5%	158	1.4	28	J	CMOS	SMLS512B
		TMS27C512-17	170	5±10%	165					
		TMS27C512-2	200	5±5%	158					
		TMS27C512-20	200	5±10%	165					
		TMS27C512	250	5±5%	158					
		TMS27C512-25	250	5±10%	165					
		TMS27C512-3	300	5±5%	158					
		TMS27C512-30	300	5±10%	165					

†J Ceramic DIP
JT 300-mil Ceramic DIP (TMS27C49 only)

For a complete product specification, please call 1-800-232-3200 and request the appropriate document listed in the table above.

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DENSITY	ORGANIZATION (WORDS × BITS)	DEVICE NUMBER	MAX ACCESS TIME (ns)	POWER SUPPLY (V)	MAX POWER DISSIPATION		PINS	PACKAGE†	COMMENTS	DOCUMENT
					ACTIVE (mW)	STANDBY (mW)				
1024K	128K × 8	TMS27C010-170‡	170	5±5%	210	1.4	32	J	CMOS	SMLS010
		TMS27C010-200‡	200	5±5%	210					
		TMS27C010-20‡	200	5±10%	220					
		TMS27C010-250‡	250	5±5%	210					
		TMS27C010-25‡	250	5±10%	220					
		TMS27C010-300‡	300	5±5%	210					
		TMS27C010-30‡	300	5±10%	220					
	64K × 16	TMS27C210-170	170	5±5%	210	1.4	40	J	CMOS	SMLS210A
		TMS27C210-200	200	5±5%	210					
		TMS27C210-20	200	5±10%	220					
		TMS27C210-250	250	5±5%	210					
		TMS27C210-25	250	5±10%	220					
		TMS27C210-300	300	5±5%	210					
		TMS27C210-30	300	5±10%	220					

†J Ceramic DIP
JT 300-mil Ceramic DIP (TMS27C49 only)
‡Advance Information for product under development by TI.

For a complete product specification, please call 1-800-232-3200 and request the appropriate document listed in the table above.

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ONE-TIME PROGRAMMABLE PROM SELECTION GUIDE

DENSITY	ORGANIZATION (WORDS × BITS)	DEVICE NUMBER	MAX ACCESS TIME (ns)	POWER SUPPLY (V)	MAX POWER DISSIPATION		PINS	PACKAGE†	COMMENTS	DOCUMENT
					ACTIVE (mW)	STANDBY (mW)				
16K	2K × 8	TMS27PC291-3	35	5±5%	394	N/A	24,28	N, FN	High-Speed CMOS	SMLS291B
		TMS27PC291-35	35	5±10%	413					
		TMS27PC291	45	5±5%	315					
		TMS27PC291-45	45	5±10%	330					
		TMS27PC291-5	50	5±5%	289					
		TMS27PC291-50	50	5±10%	303					
32K	4K × 8	TMS27PC32-120‡	120	5±5%	132	1.4	24	N	CMOS	SMLS032
		TMS27PC32-12‡	120	5±10%	138					
		TMS27PC32-150‡	150	5±5%	132					
		TMS27PC32-15‡	150	5±10%	138					
		TMS27PC32-2‡	200	5±5%	132					
		TMS27PC32-20	200	5±10%	138					
		TMS27PC32‡	250	5±5%	132					
		TMS27PC32-25‡	250	5±10%	138					
64K	8K × 8	TMS27PC49-4‡	45	5±5%	473	N/A	24,24, 28	N,NT, FN	CMOS	SMLS049
		TMS27PC49-45‡	45	5±10%	495					
		TMS27PC49-5‡	55	5±5%	473					
		TMS27PC49-55‡	55	5±10%	495					
		TMS27PC64-120	120	5±5%	158	1.4	28	N	CMOS	SMLS064A
		TMS27PC64-12	120	5±10%	165					
		TMS27PC64-1	150	5±5%	158					
		TMS27PC64-15	150	5±10%	165					
		TMS27PC64-2	200	5±5%	158					
		TMS27PC64-20	200	5±10%	165					
		TMS27PC64	250	5±5%	158					
		TMS27PC64-25	250	5±10%	165					
128K	16K × 8	TMS27PC128-1	150	5±5%	158	1.4	28,32	N,FM	CMOS	SMLS128B
		TMS27PC128-15	150	5±10%	165					
		TMS27PC128-2	200	5±5%	158					
		TMS27PC128-20	200	5±10%	165					
		TMS27PC128	250	5±5%	158					
		TMS27PC128-25	250	5±10%	165					
256K	32K × 8	TMS27PC256-150	150	5±5%	158	1.4	28,32	N, FM	CMOS	SMLS256C
		TMS27PC256-15	150	5±10%	165					
		TMS27PC256-1	170	5±5%	158					
		TMS27PC256-17	170	5±10%	165					
		TMS27PC256-2	200	5±5%	158					
		TMS27PC256-20	200	5±10%	165					
		TMS27PC256	250	5±5%	158					
		TMS27PC256-25	250	5±10%	165					

†N Plastic DIP
NT 300-mil Plastic DIP (TMS27PC49 only)
FM Plastic Chip Carrier
FN Plastic Chip Carrier

‡Advance Information for product under development by TI.

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ONE-TIME PROGRAMMABLE PROM SELECTION GUIDE (CONCLUDED)

DENSITY	ORGANIZATION (WORDS × BITS)	DEVICE NUMBER	MAX ACCESS TIME (ns)	POWER SUPPLY (V)	MAX POWER DISSIPATION		PINS	PACKAGE†	COMMENTS	DOCUMENT
					ACTIVE (mW)	STANDBY (mW)				
512K	64K × 8	TMS27PC512-2	200	5 ± 5%	158	1.4	28,32	N,FM	CMOS	SMLS512B
		TMS27PC512-20	200	5 ± 10%	165					
		TMS27PC512	250	5 ± 5%	158					
		TMS27PC512-25	250	5 ± 10%	165					
		TMS27PC512-3	300	5 ± 5%	158					
		TMS27PC512-30	300	5 ± 10%	165					
1024K	128K × 8	TMX27PC010-200§	200	5 ± 5%	210	1.4	32	N	CMOS	N/A
		TMX27PC010-20§	200	5 ± 10%	220					
		TMX27PC010-250§	250	5 ± 5%	210					
		TMX27PC010-25§	250	5 ± 10%	220					
		TMX27PC010-300§	300	5 ± 5%	210					
		TMX27PC010-30§	300	5 ± 10%	220					
	64K × 16	TMX27PC210-200§	200	5 ± 5%	210	1.4	40	N	CMOS	N/A
		TMX27PC210-20§	200	5 ± 10%	220					
		TMX27PC210-250§	250	5 ± 5%	210					
		TMX27PC210-25§	250	5 ± 10%	220					
		TMX27PC210-300§	300	5 ± 5%	210					
		TMX27PC210-30§	300	5 ± 10%	220					

†N Plastic DIP
NT 300-mil Plastic DIP (TMS27PC49 only)
FM Plastic Chip Carrier
FN Plastic Chip Carrier
§Preliminary Target Specification for product under development by TI.

For a complete product specification, please call 1-800-232-3200 and request the appropriate document listed in the table above.

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Toshiba continues to lead the world in high density memory devices. We are now the first to be in full production of 256K x 4 (1 Mbit) Multiport RAMs. These devices are offered with and without Raster operation features in DIP, SOJ and ZIP packages.

262,144 WORDS × 4 BITS MULTIPORT DYNAMIC RAM — **TC524256P/Z/J-10**
SILICON GATE CMOS — **TC524256P/Z/J-12**

The TC524256P/Z/J is a CMOS Multiport memory equipped with a 262,144-word × 4 bit dynamic random access memory (RAM) port and a 512-word × 4 bit static serial access memory (SAM) port. In addition to the conventional DRAM operation modes, the TC524256P/Z/J features a write-per-bit function on the RAM port; Bi-directional transfer capability between the DRAM memory array and the SAM data register and a high-speed serial read/write capability on the SAM port. The RAM port and the SAM port can be accessed independently except when data is being transferred between them internally. The TC524256P/Z/J is fabricated using TOSHIBA's CMOS silicon gate process technology as well as advanced circuitry to provide low power dissipation and wide operating margin. Multiplexed address inputs and a common input/output organization allow the TC524256P/Z/J to be housed in a standard 28-pin, 400-mil wide plastic DIP and 400-mil height ZIP and in a standard 32-pin 400-mil wide plastic SOJ. System oriented features include a single 5V±10% power supply operation and compatibility with high performance schottky TTL logic.

ITEM		TC524256P/Z/J -10	TC524256P/Z/J -12
t_{RAC}	$\overline{RAS}$ Access Time (Max.)	100ns	120ns
t_{CAC}	$\overline{CAS}$ Access Time (Max.)	50ns	60ns
t_{RC}	Cycle Time (Min.)	190ns	220ns
t_{PC}	Page Mode Cycle Time (Min.)	90ns	105ns
t_{SCA}	Serial Access Time (Max.)	25ns	35ns
t_{SCC}	Serial Cycle Time (Min.)	30ns	40ns
I_{CC1}	RAM Operating Current (SAM: Standby)	70mA	60mA
I_{CC2A}	SAM Operating Current (RAM: Standby)	50mA	45mA
I_{CC2}	RAM/SAM Standby Current	10mA	

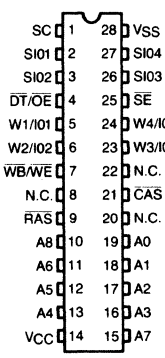
- Organization
  RAM port: 262,144 words × 4 bits
  SAM port: 512 words × 4 bits
- Single Power Supply of 5V±10% with a Built-in V_{BB} generator
- Read-Modify-Write, $\overline{CAS}$ before $\overline{RAS}$ Refresh, Hidden Refresh, Page Mode, Write-Per-Bit, Read Transfer, Write Transfer, Serial Read, Serial Write Capability
- All Inputs and Outputs TTL Compatible
- 512 refresh cycle/8ms
- Package
  TC524256P: 0.4 inches 28 pins standard Plastic DIP
  TC524256Z: 0.4 inches 28 pins standard Plastic ZIP
  TC524256J: 0.4 inches 32 pins standard Plastic SOJ

PIN NAMES

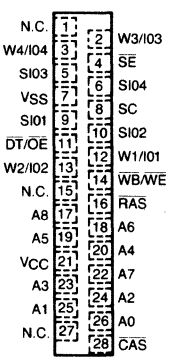
A0~A8	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{DT/OE}$	Data Transfer/Output Enable
$\overline{WB/WE}$	Write Per Bit/Write Enable
W1/I01~W4/I04	Write Mask/Data IN, OUT
SC	Serial Clock
$\overline{SE}$	Serial Enable
SI01~SI04	Serial Input Output
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

PIN CONNECTION (TOP VIEW)

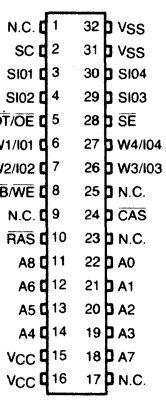
- Plastic DIP



- Plastic ZIP



- Plastic SOJ



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World Leader in High Speed SRAMs.

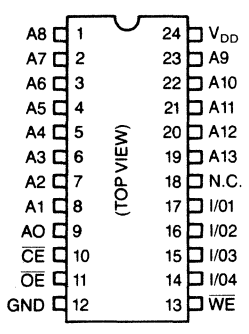
16,384 WORD × 4 BIT CMOS STATIC RAM — **TC55417P/J-15H**
SILICON GATE CMOS — **TC55417P/J-20H**

The TC55417P/J is a 65,536 bit high speed static random access memory organized as 16,384 words by 4 bits using CMOS technology, and operated from a single 5-volt supply. Toshiba's high performance device technology provides both high speed and low power features with a maximum access time of 15ns/20ns and maximum operating current of 120mA/100mA at minimum cycle time. The TC55417P/J also features an automatic stand-by mode. When deselected by Chip Enable ($\overline{CE}$), the operating current is reduced to 1mA. The TC55417P/J is suitable for use in cache memory and high speed storage, where high speed/high density are required. The TC55417P/J is molded in a 24 pin standard plastic DIP and a 24 pin plastic SOJ, with 0.3 inch width for high density assembly. The TC55417P/J is fabricated with ion implanted CMOS silicon gate MOS technology for high performance and high reliability.

- Fast access time:
  TC55417P/J-15H 15ns (MAX.)
  TC55417P/J-20H 20ns (MAX.)
- Low power dissipation:
  Operation TC55417P/J-15H 120mA (MAX.)
  TC55417P/J-20H 100mA (MAX.)
  Standby 1mA (MAX.)
- 5V single power supply: 5V ± 10%
- Fully static operation
- Directly TTL compatible:
  All Input and Output
- Output buffer control: $\overline{OE}$
- Package:
  24 Pin plastic 300 mil DIP (TC55417P)
  24 Pin plastic 300 mil SOJ (TC55417J)

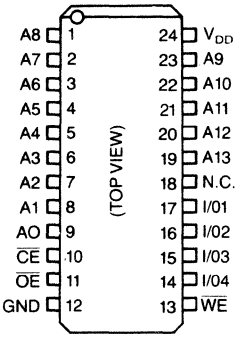
PIN CONNECTION

(TC55417P)



(DIP)

(TC55417J)

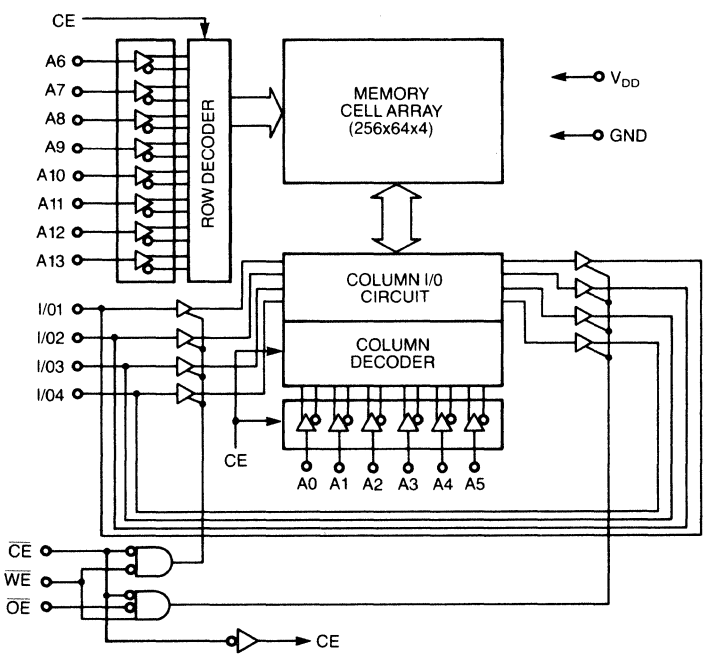


(SOJ)

PIN NAMES

A_0~A_{13}	Address Inputs
I/O_1~I/O_4	Data Input/Output
$\overline{CE}$	Chip Enable Input
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
V_{DD}	Power (+5V)
GND	Ground
N.C.	No Connection

BLOCK DIAGRAM



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256K CMOS High Speed EPROM

32,768 WORD × 8 BIT CMOS UV ERASABLE AND ELECTRICALLY PROGRAMMABLE READ ONLY MEMORY
SILICON STACKED GATE MOS

TC57H256D-70
TC57H256D-85

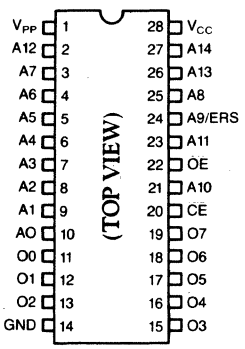
The TC57H256D is a 32,768 word × 8 bit CMOS ultraviolet light erasable and electrically programmable read only memory. For read operation, the TC57H256D's access time is 70ns, and the TC57H256D operates from a single 5-volt power supply and has low power standby mode is achieved by applying a TTL-high level signal to the $\overline{CE}$ input. Advanced CMOS technology reduces the maximum active current to 40mA/14.2MHz and standby current to 100μA. For program operation, the programming is achieved by using the high speed programming mode. TC57H256D is fabricated with the CMOS technology and the N-channel silicon double layer gate MOS technology.

- Peripheral Circuit: CMOS
  Memory Cell: N-MOS

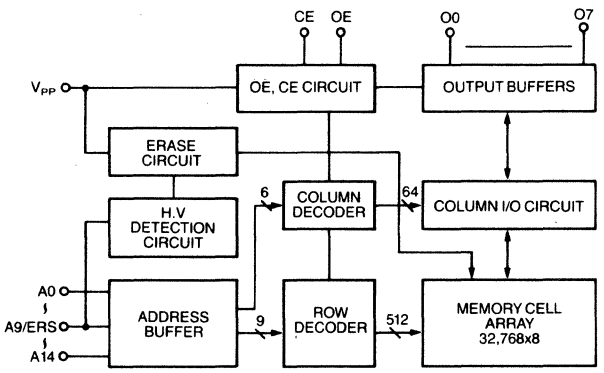
	-70	-85
V_{CC}	5V ± 5%	5V ± 10%
t_{ACC}	70ns	85ns

- Single 5V Power Supply
- Full Static Operation
- High Speed Programming Mode
- Inputs and Outputs TTL Compatible
- Pin Compatible with ROM TC53257P, TMM23256P, TMM27256AD and TC57256AD
- Standard 28 Pin DIP Cerdip Package

PIN CONNECTION



BLOCK DIAGRAM



PIN NAMES

$A_0 \sim A_{14}$	Address Inputs
$O_0 \sim O_7$	Outputs (Inputs)
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
V_{PP}	Program Supply Voltage
V_{CC}	V_{CC} Supply Voltage (+5V)
GND	Ground

MODE SELECTION

MODE \ PIN	$\overline{CE}$ (20)	$\overline{OE}$ (22)	V_{PP} (1)	V_{CC} (28)	$O_0 \sim O_7$ (11~13, 15~19)	POWER
Read	L	L	5V	5V	Data Out	Active
Output Deselect	*	H			High Impedence	
Standby	H	*			High Impedence	Standby
Program	L	H	12.5V1)	6V1)	Data In	Active
Program Inhibit	H	H	12.75V2)	6.25V2)	High Impedence	
Program Verify	*	L			Data Out	

*: H or L
1): HIGH SPEED PROGRAM MODE I
2): HIGH SPEED PROGRAM MODE II

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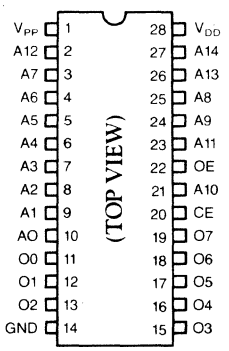
256K CMOS Flash EEPROM

TC58257AP/AF 32,768 WORD × 8 BIT ELECTRICALLY CHIP ERASABLE AND PROGRAMMABLE READ ONLY MEMORY SILICON STACKED GATE MOS	TC58257AP/AF-17 TC58257AP/AF-20 TC58257AP/AF-25

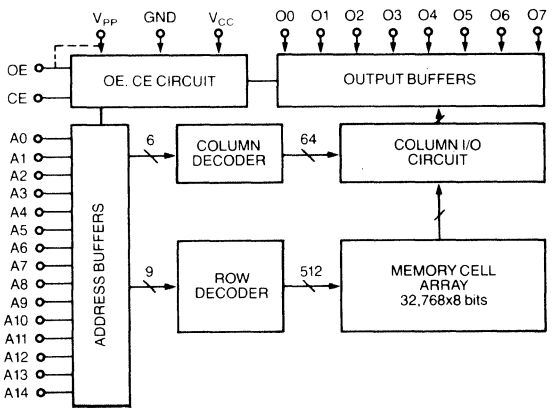
TC58257AP/AF is a 32,768 word × 8 bit electrically chip erasable and programmable read only memory, and molded in a 28 pin plastic package. The TC58257AP/AF's access time is 170ns/200ns/250ns, and has low power standby mode which reduces the power dissipation without increasing access time. The electrical characteristics are the same as U.V. EPROM TC57256AD's. For program operation, the programming is achieved by using the high speed programming mode. The TC58257AP/AF has an electrically chip erasing mode which can erase whole bits at the same time.

- Peripheral Circuit: CMOS
  Memory Cell: NMOS
- Fast Access Time:
  TC58257AP/AF-17 170ns
  TC58257AP/AF-20 200ns
  TC58257AP/AF-25 250ns
- Low Power Dissipation
  Active: 30mA/5.9MHz
  Standby: 100μA
- Full Static Operation
- High Speed Programming Mode
- Electrically Chip Erasing Mode
- Inputs and Outputs TTL Compatibility
- Pin Compatible with MASK ROM TC53257P, TMM23256P, EPROM TMM27256D/AD, and TC57256D/AD, one time PROM TMM24256P/AP/AF and TC54256P/AP/AF
- Standard 28 Pin DIP Plastic Package: TC58257A
- Plastic Flat Package: TC58257A

PIN CONNECTION



BLOCK DIAGRAM



MODE SELECTION

MODE \ PIN	$\overline{CE}$	$\overline{OE}$	A_9	V_{PP}	V_{CC}	A_0~A_8 (10~14)	O_0~O_7	POWER
Read	L	L	*	5V	5V	*	Data Output	Active
Output Deselect	*	H	*			*	High Impedence	
Standby	H	*	*			*	High Impedence	Standby
Program	L	H	*	12.75V	6.25V	*	Data Input	Active
Program Inhibit	H	*	*			*	High Impedence	
Program Verify	L	L	*			*	Data Output	
Chip Erase	L	H	12V	12.75V	5V	*	Data FF (H) Input	Active
Chip Erase Inhibit	H	*				*	High Impedence	

*: V_{IH} or V_{IL}

PIN NAMES

A_0 ~ A_{14}	Address Inputs
O_0 ~ O_7	Output (Input)
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
A_9/ERS	Address And Erase Control Input
V_{PP}	Program And Erase Power Supply Voltage
V_{CC}	V_{CC} Power Supply Voltage
GND	Ground

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512K CMOS EPROM

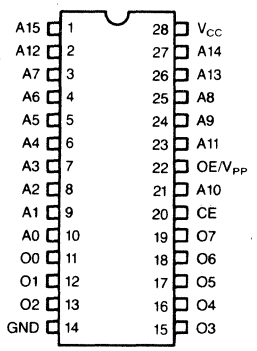
65,536 WORDS × 8 BITS CMOS UV ERASABLE AND ELECTRICALLY PROGRAMMABLE READ ONLY MEMORY
SILICON STACKED GATE MOS

TC57512AD-15
TC57512AD-20

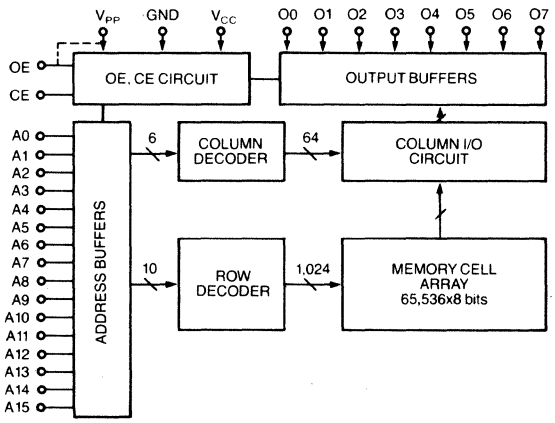
The TC57512AD is a 65,536 word × 8 bit CMOS ultraviolet light erasable and electrically programmable read only memory. For read operation, the TC57512AD's access time is 150ns/200ns, and the TC57512AD operates from a single 5-volt power supply and has low power standby mode which reduces the power dissipation without increasing access time. The standby mode is achieved by applying a TTL-high level signal to the $\overline{CE}$ input. Advanced CMOS technology reduces the maximum active current to 30mA/6.7MHz and standby current to 100μA. For program operation, the programming is achieved by using the high speed programming mode. For program operation, the programming is achieved by using high speed programming mode. TC57512AD is fabricated with the CMOS technology and the N-channel silicon double layer gate MOS technology.

- Peripheral Circuit: CMOS
  Memory Cell: N-MOS
- Fast Access Time:
  TC57512AD-15 150ns
  TC57512AD-20 200ns
- Low Power Dissipation
  Active: 30mA/6.7MHz
  Standby: 100μA
- Full Static Operation
- High Speed Programming Mode I, II
- Inputs and Outputs TTL Compatible
- Standard 28 Pin DIP Cerdip Package

PIN CONNECTION (TOP VIEW)



BLOCK DIAGRAM (2MB)



PIN NAMES

$A_0 \sim A_{15}$	Address Inputs
$O_0 \sim O_7$	Outputs (Inputs)
$\overline{CE}$	Chip Enable Input
$\overline{OE}/V_{PP}$	Output Enable Input / Program Supply Voltage
V_{CC}	Power Supply Voltage (+5V)
GND	Ground

MODE SELECTION

MODE \ PIN	$\overline{CE}$ (20)	$\overline{OE}/V_{PP}$ (22)	V_{CC} (28)	$O_0 \sim O_7$ (11 ~ 13, 15 ~ 19)	POWER
Read	L	L	5V	Data Out	Active
Output Deselect	*	H		High Impedence	
Standby	H	*		High Impedence	Standby
Program	L	V_{PP}	6V[1] / 6.25V[2]	Data In	Active
Program Inhibit	H	V_{PP}		High Impedence	
Program Verify	L	L		Data Out	

*: H or L

1): HIGH SPEED PROGRAMMING MODE I
2): HIGH SPEED PROGRAMMING MODE II

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MICROCONTROLLER 8048/8049

DEVICE	PKG	DESCRIPTION
TMP8049A	P,T	8 BIT MCU, RAM, ROM, I/O - 11 MHz
TMP8048A	P,T	8 BIT MCU, RAM, ROM, I/O - 11 MHz
TMP80C50A	P,F,T	8 BIT CMOS MCU, RAM, ROM, I/O - 6MHz, 11 MHz
TMP80C49A	P,F,T	8 BIT CMOS MCU, RAM, ROM, I/O - 6MHz, 11 MHz
TMP80C48A	P,F,T	8 BIT CMOS MCU, RAM, ROM, I/O - 11 MHz

Clock Rates and Package Type of the TLCS-68000 Family (Advance information)

DEVICE	DEVICE NAME	PROC.	SPEEDS (MHz)	DIP		CER. PGA W/&W/O* Standoffs*	PLAS. LCC
				PLAS.	CER.		
TMP68000	MPU	N	8, 10, 12.5	64 †	64	68 †	68
TMP68008	MPU	N	8, 10	48 †	48	–	52
TMP68010	VMPU	N	8, 10,12.5	64 †	64	68	68
TMP68230	PI/T	N	8, 10	48 †	48	–	–
TMP68450	DMAC	N	8, 10	–	64 †	68	–
TMP68681	DUART	N	1 Mbit/s	40	40	–	–
TMP68901	MFP	N	4	48 †	48	–	–
TMP68153	BIM	B	16	40	40	–	–
TMP68440	DDMA	N	8, 10	64 †	64	68	–
TMP68442	EDDMA	N	8, 10	–	–	68 *	–
TMP68452	BAM	B	50ns (Arbitration time)	28	28	–	–
TMP68652	MPCC	N	2 Mbit/s	40	–	–	–
TMP68661	EPCI	N	1 Mbit/s	28	–	–	–

Note. † denotes the device which will be available 2Q '88. (Others will be available 3Q '88 or later)

OTHER PERIPHERALS

TYPE NUMBER		DESCRIPTION
TC8250AP	RTC	REAL TIME CLOCK/CALENDAR
TC8505AP/AF	CRTC	CRT DISPLAY CONTROLLER
TMPZ80C47C	HDC	HARD DISK CONTROLLER
TC8565AP/AF	FDC	FLOPPY DISK CONTROLLER INCLUDES VFO
TC8566AF		
TC8570P/F	UART	UART FOR PC
TC8576AF	CPC	CENTRONICS I/O - RS232C
TC8577AP		CENTRONICS OUTPUT - RS232C
TC8578AP		CENTRONICS INPUT - RS232C
TC8600F	FDMC	5.25" FD MECHANISM CONTR'L
TC8601F		3.5" FD MECHANISM CONTR'L
TC8602F		3.5" FD MECHANISM CONTR'L
T7779*	LCD/CRTC	LCD/CRTC CONTROLLER 640 x 400 DOT MATRIX
BAC84110	MULTIBUS II BUS ARBITER CONTROLLER	
MIC84120	MULTIBUS II MESSAGE INTERRUPT CONTROLLER	

*OTHER LCD DISPLAY CONTROLLERS ARE ALSO AVAILABLE

ASSP PRODUCTS (Z80 MPU + Peripheral Integrated Devices)

TYPE NUMBER	PKG	DESCRIPTION
TMPZ84C011A	F	Z80 MPU (4MHz) + CGC + CTC + I/O (8×5)
TMPZ84C011A-6	F	Z80 MPU (6MHz) + CGC + CTC + I/O (8×5)
TMPZ84C015A	F	Z80 MPU (4MHz) + CGC + CTC + PIO + SIO
TMPZ84C015A-6	F	Z80 MPU (6MHz) + CGC + CTC + PIO + SIO
TMPZ84C013A	T	Z80 MPU (4MHz) + CGC + CTC + SIO
TMPZ84C013A-6	T	Z80 MPU (6MHz) + CGC + CTC + SIO

MICROPROCESSOR AND PERIPHERALS 8085

DEVICE	PKG	DESCRIPTION
TMP8085A/A-2/AH/AH-2	P	8 BIT MICROPROCESSOR 3/5MHz
TMP8155/-2	P	256 BYTE RAM WITH I/O AND TIMER 3/5MHz
TMP8156/-2	P	256 BYTE RAM WITH I/O AND TIMER 3/5MHz
TMP8237A/A-5	P	PROG. DMA CONTROLLER 3/5MHz
TMP8251A	P	PROG. COMMUNICATION INTERFACE 3MHz
TMP8253-5	P	PROG. INTERVAL TIMER 2.5MHz
TMP8255A-5	P	PROG. PERIPHERAL INTERFACE 3MHz
TMP8259A	P	PROG. INTERRUPT CONTROLLER 3MHz
TMP8279-5	P	PROG. KEYBOARD/DISPLAY CONTROLLER 3MHz
TMP8355	P	2 BYTE ROM, I/O PORTS 3MHz
TMP82C79-2	P,F	PROG. KEYBOARD/DISPLAY CONTROLLER 5MHz, CMOS
TMP82C59A-2	P	PROG. INTERRUPT CONTROLLER 8MHz, CMOS
TMP82C55A-5/2/10	P,F	PROG. PERIPHERAL INTERFACE 3/5/10MHz, CMOS
TMP82C54/-2	P	PROG. INTERVAL TIMER 8/10MHz, CMOS
TMP82C53-2	P	PROG. INTERVAL TIMER 5MHz, CMOS
TMP82C51A-2/-8	P,F	PROG. COMMUNICATION INTERFACE 5/8MHz, CMOS
TMP82C37A-5	P,F	DMA CONTROLLER 5MHz, CMOS

CMOS Z80 FAMILY

DEVICE	PKG	FREQ.	DESCRIPTION
TMPZ84C00A	P,T,F	4MHZ	MICROPROCESSOR-Z80A
TMPZ84C00A-6	P,T,F	6MHZ	MICROPROCESSOR-Z80B
TMPZ84C00A-8	P,T	8MHZ	MICROPROCESSOR-Z80H
TMPZ84C10A	P,T,F	4MHZ	DIRECT MEMORY ACCESS CONTROLLER
TMPZ84C10A-6	P,T,F	6MHZ	DIRECT MEMORY ACCESS CONTROLLER
TMPZ84C20A	P,T,F	4MHZ	PARALLEL I/O CONTROLLER
TMPZ84C20A-6	P,T,F	6MHZ	PARALLEL I/O CONTROLLER
TMPZ84C30A	P,T,F	4MHZ	COUNTER TIMER CIRCUIT
TMPZ84C30A-6	P,T,F	6MHZ	COUNTER TIMER CIRCUIT
TMPZ84C40A	P	4MHZ	SERIAL I/O CONTROLLER
TMPZ84C40A-6	P	6MHZ	SERIAL I/O CONTROLLER
TMPZ84C41A	P	4MHZ	SERIAL I/O CONTROLLER
TMPZ84C41A-6	P	6MHZ	SERIAL I/O CONTROLLER
TMPZ84C42A	P	4MHZ	SERIAL I/O CONTROLLER
TMPZ84C42A-6	P	6MHZ	SERIAL I/O CONTROLLER
TMPZ84C43A	F	4MHZ	SERIAL I/O CONTROLLER
TMPZ84C43A-6	F	6MHZ	SERIAL I/O CONTROLLER
TMPZ84C44A	T	4MHZ	SERIAL I/O CONTROLLER
TMPZ84C44A-6	T	6MHZ	SERIAL I/O CONTROLLER
TMPZ84C60	P	4MHZ	CLOCK GENERATOR CONTROLLER
TMPZ84C61A	P	6/8MHZ	CLOCK GENERATOR CONTROLLER
TMPZ84C01	F	4MHZ	MICROPROCESSOR + CGC
TMPZ84C02A-6	F	6MHZ	MICROPROCESSOR + CGC

SPEECH PRODUCTS

ADM – SPEECH RECORDING & REPRODUCTION

PART NUMBER	FUNCTION
T6668	RECORDING/REPRODUCTION, DRAM TYPE
TC8831F	RECORDING/REPRODUCTION 1 MEG DRAM TYPE
TC8830F	RECORDING/REPRODUCTION, SRAM/EPROM
T6667	REPRODUCTION ONLY, BUILT-IN MROM

VOICE RECOGNITION

T6658A	SPEAKER DEPENDENT WORK RECOGNITION

PARCOR – SPEECH SYNTHESIS

T6803	SPEECH SYNTHESIS, BUILT IN 64K MROM
T6721	SPEECH SYNTHESIS

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TOSHIBA HIGH SPEED (HC) AND ADVANCED HIGH SPEED (AC) CMOS FUNCTION SELECTION GUIDE

FUNCTION			HIGH SPEED (P/N TC74HC-)	ADVANCED HIGH SPEED (P/N TC74AC-)
GATE	NAND NOR AND OR INVERTER		00A, T00A, 03A, 10A, 20A, 133A 02A, T02A, 27A, 4002A, 4078A 08A, T08A, 09A, 11A, 21A 32A, T32A, 4072A, 4078A 04A, U04A, T04A, 05A, 07A	00, T00, 10, 20 02 08, 11 32 04, T04
	SCHMITT TRIGGER		14A, 132A	
	MULTIFUNCTION		51A, 86A, T86A, 266A, 386A, 7266A	86
BUFFER			4049A, 4050A, T7007A	
	3-STATE		125A, 126A, 240A, T240A, 241A, T241A, 244A, T244A, 365A, 366A, 367A, 368A, 540A, T540A, 541A, T541A, 7240A, 7241A, 7244A	240, T240, 241, 244, T244, 367, 368, 540, 541
	BIDIRECTIONAL		242A, 243A, 245A, T245A, 620A, 623A, 640A, T640A, 643A, T643A, 7640A, 7643A, 7645A	245, T245, 620, 623, 640, T640, 643, T643
FLIP-FLOP	J-K TYPE		73A, 76A, 107A, 109A, 112A, 113A	109, 112
	D TYPE		74A, T74A, 174A, T174A, 273A, T273A, 377A	74, T74, 174, 175, 273
		3-STATE	374A, T374A, 534A, T534A, 564A, T564A, 574A, T574A, 646A, T646A, 648A, T648A, 651A, T651A, 652A, T652A	374, T374, 534, T534, 564, 574
LATCH			75A, 77A, 259A, 279A, 375A	259
		3-STATE	373A, T373A, 533A, T533A, 563A, T563A, 573A, T573A	373, T373, 533, T533, 563, 573
MULTIVIBRATOR			123, 123A, 221, 221A, 423, 423A, 4538A	
DECODER			42A, 131A, 137A, T137A, 138A, T138A, 139A, T139A, 154A, 155A, 237A, 238A, 4028A, 4514A, 4515A	138, T138, 139
		7-SEGMENT	4511A, 4543A	
ENCODER			147A, 148A	
REGISTER			164A, T164A, 165A, 166A, 173A, 194A, 195A, 299A, 323A, 595A, 597A, 670A, 4094A, 40105A	164, 166, 299, 323, 670
COUNTER		BINARY	161A, 163A, 191A, 193A, 393A, 590A, 592A, 593A, 691A, 693A, 697A, 699A, 4520A	161, 163, 393
		DECADE	160A, 162A, 190A, 192A, 390A, 690A, 692A, 696A, 698A, 4518A	160, 162, 390
		DIVIDER	4017A, 4020A, 4022A, 4024A, 4040A, 4060A, 40102A, 40103A, 7292A, 7294A	
MULTIPLEXER		ANALOG	4016A, 4051A, 4052A, 4053A, 4066A, 4316A, 4351A, 4352A, 4353A	
		DIGITAL	151A, 153A, 157A, T157A, 158A, T158A, 251A, 253A, 257A, T257A, 258A, T258A, 298A, 352A, 353A, 354A, 356A	151, 153, 157, 158, 251, 253, 257, 258
OTHER	COMPARATOR		85A, 688A, T688A	
	ADDER		283A	
	ALU		181A, 182A	
	PARITY TREE		280A	

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TOSHIBA STANDARD C²MOS FUNCTION SELECTION GUIDE

FUNCTION			TYPE NUMBER
GATE BUFFERS	NAND		TC4011BP/BF, TC4011UBP, TC4012BP/BF, TC4023BP/BF, TC4068BP/BF, TC7400BP
	NOR		TC4000BP, TC4001BP/BF, TC4001UBP, TC4002BP/BF, TC4025BF/BP, TC4078BP/BF
	AND		TC4068BP/BF, TC4073BP/BF, TC4081BP/BF, TC4082BP
	OR		TC4071BP/BF, TC4072BP/BF, TC4075BP/BF, 4078BP/BF
	INVERTER		TC4007UBP/UBF, TC4009UBP, TC4049BP/BF, TC4069UBP/UBF, TC7404UBP
	BUFFERS		TC4009UBP, TC4010BP, TC4049BP/BF, TC4050BP/BF
		3-STATE	TC4502BP, TC5012BP/BF, TC5024BP, TC5025BP
		OPEN DRAIN	TC40107BP, TC5029BP, TC5064BP, TC5065BP, TC5066BP, TC5067BP
	MULTIFUNCTION		TC4019BP/BF, TC4030BP/BF, TC4077BP/BF, TC4085BP, TC4086BP, TC4501BP, TC4519BP, TC4530BP, TC4572BP/BF
	SCHMITT TRIGGER		TC4093BP/BF, TC4583BP, TC4584BP/BF
	LEVEL SHIFTER		TC4009UBP, TC4010BP, TC4049BP/BF, TC4050BP/BF, TC5020BP
FLIP-FLOP			TC4013BP/BF, TC4027BP/BF, TC40174BP/BF, TC40175BP/BF, TC7476BP
LATCHES			TC4042BP/BF, TC4043BP, TC4044BP/BF, TC4099BP/BF, TC4508BP
MULTIVIBRATORS			TC4047BP, TC4528BP/BF, TC4538BP/BF
DECODERS			TC4028BP/BF, TC4514BP, TC4515BP, TC4555BP, TC4556BP/BF
DISPLAY DRIVER	LED		TC4511BP/BF, TC5002BP, TC5022BP
	LCD		TC4054BP/BF, TC4055BP, TC4056BP/BF, TC4543BP/BF
	DIGITRON		TC5068BP, TC5069BP
ENCODER			TC4532BP
REGISTERS	SHIFT		TC4006BP, TC4014BP, TC4015BP/BF, TC4021BP, TC4034BP, TC4035BP, TC4094BP/BF, TC40104BP, TC40194BP, TC5050P
	STORAGE		TC4076BP
COUNTERS	BINARY		TC4029BP/BF, TC40161BP, TC40163BP, TC40193BP, TC4516BP/BF, TC4520BP/BF, TC5018BP, TC5027BP
	DECADE		TC4029BP/BF, TC40160BP, TC40162BP, TC40192BP, TC4510BP/BF, TC4518BP/BF, TC5026BP
	DIVIDER		TC4020BP/BF, TC4024BP/BF, TC4040BP/BF, TC4521BP, TC5036P, TC5048P
	DIVIDE-BY-"N"		TC4018BP, TC40102BP, TC40103BP, TC4522BP, TC4526BP/BF
	N-DIGIT DECADE		TC5001P, TC5032P, TC5037P, TC5051P, TC5052P, TC5053P, TC5054P, TC5070P
	OTHER		TC4017BP/BF, TC4022BP
TIMERS			TC5043P, TC5071P, TC5072P
MULTI-PLEXERS	ANALOG		TC4051BP/BF, TC4052BP/BF, TC4053BP/BF
	DIGITAL		TC4512BP/BF, TC4539BP/BF, TC5023BP
ARITHMETIC CIRCUITS	ADDER		TC4008BP, TC4032BP, TC4038BP, TC4560BP
	COMPARATOR		TC4063BP/BF, TC4585BP
	PARITYTREE		TC4531BP
	RATE MULTIPLIER		TC4527BP
	9's COMPLEMENTER		TC4561BP
MEMORIES (RAM)			TC4036BP, TC4039BP
A/D CONVERTERS			TC5090AP, TC5091AP, TC5092AP, TC5093AP
ANALOG SWITCH			TC4016BP/BF, TC4066BP/BF
OTHER			TC40117BP

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PACKAGE AND PIN-COMPATIBLE

AMD	VLSI	Device Description
AM9122-25PC	VT7C122-25PC	25 ns 256 x 4 SRAM 22-Lead
AM9122-35PC	VT7C122-35PC	35 ns 256 x 4 SRAM 22-Lead
AM9150-20PC	VT20C50-20PC	20 ns 1,024 x 4 SRAM 24-Lead with Reset
AM9150-25PC	VT20C50-25PC	25 ns 1,024 x 4 SRAM 24-Lead with Reset

Cypress	VLSI	Device Description
CY7C122-15PC	VT7C122-15PC	15 ns 256 x 4 SRAM 22-Lead
CY7C122-25PC	VT7C122-25PC	25 ns 256 x 4 SRAM 22-Lead
CY7C122-35PC	VT7C122-35PC	35 ns 256 x 4 SRAM 22-Lead
CY7C128-25PC	VT20C18-25PC	25 ns 2,048 x 8 SRAM 24-Lead
CY7C128-25SC	VT20C18-25SC	25 ns 2,048 x 8 SRAM 24-Lead SOG
CY7C128-35PC	VT20C18-35PC	35 ns 2,048 x 8 SRAM 24-Lead
CY7C128-35SC	VT20C18-35SC	35 ns 2,048 x 8 SRAM 24-Lead SOG
CY7C132-55PC	VT7132-55PC	55 ns 2,048 x 8 Dual-Port RAM
CY7C142-55PC	VT7142-55PC	55 ns 2,048 x 8 Dual-Port RAM
CY7C150-15PC	VT20C50-15PC	15 ns 1,024 x 4 SRAM 24-Lead with Reset
CY7C150-15SC	VT20C50-15SC	15 ns 1,024 x 4 SRAM 24-Lead SOG with Reset
CY7C150-25PC	VT20C50-25PC	25 ns 1,024 x 4 SRAM 24-Lead with Reset
CY7C150-25SC	VT20C50-25SC	25 ns 1,024 x 4 SRAM 24-Lead SOG with Reset
CY7C168-25PC	VT20C68-25PC	25 ns 4,096 x 4 SRAM 20-Lead
CY7C168-35PC	VT20C68-35PC	35 ns 4,096 x 4 SRAM 20-Lead
CY7C169-25PC	VT20C69-25PC	25 ns 4,096 x 4 SRAM 20-Lead
CY7C169-35PC	VT20C69-35PC	35 ns 4,096 x 4 SRAM 20-Lead
CY7C170-25PC	VT20C79-25PC	25 ns 4,096 x 4 SRAM 22-Lead
CY7C170-35PC	VT20C79-35PC	35 ns 4,096 x 4 SRAM 22-Lead
CY7C171-25PC	VT20C71-25PC	25 ns 4,096 x 4 SRAM 24-Lead Separate I/O
CY7C171-35PC	VT20C71-35PC	35 ns 4,096 x 4 SRAM 24-Lead Separate I/O
CY7C172-25PC	VT20C72-25PC	25 ns 4,096 x 4 SRAM 24-Lead Separate I/O
CY7C172-35PC	VT20C72-35PC	35 ns 4,096 x 4 SRAM 24-Lead Separate I/O

Goldstar	VLSI	Device Description
GM76C422-15	VT7C122-15PC	15 ns 256 x 4 SRAM 22-Lead
GM76C422-25	VT7C122-25PC	25 ns 256 x 4 SRAM 22-Lead
GM76C422-35	VT7C122-35PC	35 ns 256 x 4 SRAM 22-Lead
GM76C28-35	VT20C18-35PC	35 ns 2,048 x 8 SRAM 24-Lead

Hitachi	VLSI	Device Description
HM6268P-25DP	VT20C68-25PC	25 ns 4,096 x 4 SRAM 20-Lead
HM6268P-35DP	VT20C68-35PC	35 ns 4,096 x 4 SRAM 20-Lead
HM6716-25DG (Note 1)	VT20C18-25PC	25 ns 2,048 x 8 SRAM 24-Lead

Note:
1. This ceramic package is size and pin-compatible with VLSI's plastic package.

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PACKAGE AND PIN-COMPATIBLE

Hyundai	VLSI	Device Description
HY61C16AS25	VT20C18-25PC	25 ns 2,048 x 8 SRAM 24-Lead
HY61C16AS35	VT20C18-35PC	35 ns 2,048 x 8 SRAM 24-Lead
HY61C68S25	VT20C68-25PC	25 ns 4,096 x 4 SRAM 20-Lead
HY61C68S35	VT20C68-35PC	35 ns 4,096 x 4 SRAM 20-Lead

IDT	VLSI	Device Description
IDT6116SA20SO	VT20C18-20SC	20 ns 2,048 x 8 SRAM 24-Lead SOG
IDT6116SA20TP	VT20C18-20PC	20 ns 2,048 x 8 SRAM 24-Lead
IDT6116SA25SO	VT20C18-25SC	25 ns 2,048 x 8 SRAM 24-Lead SOG
IDT6116SA25TP	VT20C18-25PC	25 ns 2,048 x 8 SRAM 24-Lead
IDT6116SA35SO	VT20C18-35SC	35 ns 2,048 x 8 SRAM 24-Lead SOG
IDT6116SA35TP	VT20C18-35PC	35 ns 2,048 x 8 SRAM 24-Lead
IDT6168SA20TP	VT20C68-20PC	20 ns 4,096 x 4 SRAM 20-Lead
IDT6168SA25TP	VT20C68-25PC	25 ns 4,096 x 4 SRAM 20-Lead
IDT6168SA35TP	VT20C68-35PC	35 ns 4,096 x 4 SRAM 20-Lead
IDT7132SA55J	VT7132-55QC	55 ns 2,048 x 8 Dual-Port RAM PLCC
IDT7132SA55P	VT7132-55PC	55 ns 2,048 x 8 Dual-Port RAM
IDT7132SA70J	VT7132-70QC	70 ns 2,048 x 8 Dual-Port RAM PLCC
IDT7132SA70P	VT7132-70PC	70 ns 2,048 x 8 Dual-Port RAM
IDT7132SA90J	VT7132-90QC	90 ns 2,048 x 8 Dual-Port RAM PLCC
IDT7132SA90P	VT7132-90PC	90 ns 2,048 x 8 Dual-Port RAM
IDT7142SA55J	VT7142-55QC	55 ns 2,048 x 8 Dual-Port RAM PLCC
IDT7142SA55P	VT7142-55PC	55 ns 2,048 x 8 Dual-Port RAM
IDT7142SA70J	VT7142-70QC	70 ns 2,048 x 8 Dual-Port RAM PLCC
IDT7142SA70P	VT7142-70PC	70 ns 2,048 x 8 Dual-Port RAM
IDT7142SA90J	VT7142-90QC	90 ns 2,048 x 8 Dual-Port RAM PLCC
IDT7142SA90P	VT7142-90PC	90 ns 2,048 x 8 Dual-Port RAM
IDT71681SA25P	VT20C71-25PC	25 ns 4,096 x 4 SRAM 24-Lead Separate I/O
IDT71681SA25SO	VT20C71-25SC	25 ns 4,096 x 4 SRAM 24-Lead Separate I/O SOG
IDT71681SA35P	VT20C71-35PC	35 ns 4,096 x 4 SRAM 24-Lead Separate I/O
IDT71681SA35SO	VT20C71-35SC	35 ns 4,096 x 4 SRAM 24-Lead Separate I/O SOG
IDT71682SA25P	VT20C72-25PC	25 ns 4,096 x 4 SRAM 24-Lead Separate I/O
IDT71682SA25SO	VT20C72-25SC	25 ns 4,096 x 4 SRAM 24-Lead Separate I/O SOG
IDT71682SA35P	VT20C72-35PC	35 ns 4,096 x 4 SRAM 24-Lead Separate I/O
IDT71682SA35SO	VT20C72-35SC	35 ns 4,096 x 4 SRAM 24-Lead Separate I/O SOG

Inmos	VLSI	Device Description
IMS1423P-25	VT20C68-25PC	25 ns 4,096 x 4 SRAM 20-Lead
IMS1423P-35	VT20C68-35PC	35 ns 4,096 x 4 SRAM 20-Lead
IMS1433S-35 (Note 1)	VT20C18-20PC	20 ns 2,048 x 8 SRAM 24-Lead

Mitsubishi	VLSI	Device Description
M5M2168P-35	VT20C68-35PC	35 ns 4,096 x 4 SRAM 20-Lead

Note:
1. This ceramic package is size and pin-compatible with VLSI's plastic package.

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PACKAGE AND PIN-COMPATIBLE

Fujitsu	VLSI	Device Description
MB81C68A-25P	VT20C68-25PC	25 ns 4,096 x 4 SRAM 20-Lead
MB81C68A-35P	VT20C68-35PC	35 ns 4,096 x 4 SRAM 20-Lead
MB81C69A-25P	VT20C69-25PC	25 ns 4,096 x 4 SRAM 20-Lead
MB81C69A-35P	VT20C69-35PC	35 ns 4,096 x 4 SRAM 20-Lead

Motorola	VLSI	Device Description
MCM2018N35	VT20C18-35PC	35 ns 2,048 x 8 SRAM 24-Lead
MCM6268P35	VT20C68-35PC	35 ns 4,096 x 4 SRAM 20-Lead
MCM93422AP35	VT7C122-35PC	35 ns 256 x 4 SRAM 22-Lead

Mostek	VLSI	Device Description
MK41H68N25	VT20C68-25PC	25 ns 4,096 x 4 SRAM 20-Lead
MK41H68N35	VT20C68-35PC	35 ns 4,096 x 4 SRAM 20-Lead
MK41H69N25	VT20C69-25PC	25 ns 4,096 x 4 SRAM 20-Lead
MK41H69N35	VT20C69-35PC	35 ns 4,096 x 4 SRAM 20-Lead
MK41H78N25	VT20C78-25PC	25 ns 4,096 x 4 SRAM 22-Lead
MK41H78N35	VT20C78-35PC	35 ns 4,096 x 4 SRAM 22-Lead

Performance	VLSI	Device Description
P4C116-20PC	VT20C18-20PC	20 ns 2,048 x 8 SRAM 24-Lead
P4C116-25PC	VT20C18-25PC	25 ns 2,048 x 8 SRAM 24-Lead
P4C116-35PC	VT20C18-35PC	35 ns 2,048 x 8 SRAM 24-Lead
P4C150-15PC	VT20C50-15PC	15 ns 1,024 x 4 SRAM 24-Lead with Reset
P4C150-20PC	VT20C50-20PC	20 ns 1,024 x 4 SRAM 24-Lead with Reset
P4C150-25PC	VT20C50-25PC	25 ns 1,024 x 4 SRAM 24-Lead with Reset
P4C168-20PC	VT20C68-20PC	20 ns 4,096 x 4 SRAM 20-Lead
P4C168-25PC	VT20C68-25PC	25 ns 4,096 x 4 SRAM 20-Lead
P4C168-35PC	VT20C68-35PC	35 ns 4,096 x 4 SRAM 20-Lead
P4C1681-25PC	VT20C71-25PC	25 ns 4,096 x 4 SRAM 24-Lead Separate I/O
P4C1681-35PC	VT20C71-35PC	35 ns 4,096 x 4 SRAM 24-Lead Separate I/O
P4C1682-25PC	VT20C72-25PC	25 ns 4,096 x 4 SRAM 24-Lead Separate I/O
P4C1682-35PC	VT20C72-35PC	35 ns 4,096 x 4 SRAM 24-Lead Separate I/O
P4C169-20PC	VT20C69-20PC	20 ns 4,096 x 4 SRAM 20-Lead
P4C169-25PC	VT20C69-25PC	25 ns 4,096 x 4 SRAM 20-Lead
P4C169-35PC	VT20C69-35PC	35 ns 4,096 x 4 SRAM 20-Lead
P4C170-20PC	VT20C78-20PC	20 ns 4,096 x 4 SRAM 22-Lead
P4C170-25PC	VT20C78-25PC	25 ns 4,096 x 4 SRAM 22-Lead
P4C170-35PC	VT20C78-35PC	35 ns 4,096 x 4 SRAM 22-Lead
P4C22-12PC	VT7C122-12PC	12 ns 256 x 4 SRAM 22-Lead
P4C22-15PC	VT7C122-15PC	15 ns 256 x 4 SRAM 22-Lead
P4C22-25PC	VT7C122-25PC	25 ns 256 x 4 SRAM 22-Lead
P93U422-35PC	VT7C122-35PC	35 ns 256 x 4 SRAM 22-Lead

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PACKAGE AND PIN-COMPATIBLE

Saratoga	VLSI	Device Description
SSM6116-20PC	VT20C18-20PC	20 ns 2,048 x 8 SRAM 24-Lead
SSM6116-25PC	VT20C18-25PC	25 ns 2,048 x 8 SRAM 24-Lead
SSM6116-35PC	VT20C18-35PC	35 ns 2,048 x 8 SRAM 24-Lead
SSM6168-20PC	VT20C68-20PC	20 ns 4,096 x 4 SRAM 20-Lead
SSM6168-25PC	VT20C68-25PC	25 ns 4,096 x 4 SRAM 20-Lead
SSM6168-35PC	VT20C68-35PC	35 ns 4,096 x 4 SRAM 20-Lead
SSM6170-20PC	VT20C78-20PC	20 ns 4,096 x 4 SRAM 22-Lead
SSM6170-25PC	VT20C78-25PC	25 ns 4,096 x 4 SRAM 22-Lead
SSM6170-35PC	VT20C78-35PC	35 ns 4,096 x 4 SRAM 22-Lead
SSM6171-25PC	VT20C71-25PC	25 ns 4,096 x 4 SRAM 24-Lead Separate I/O
SSM6171-35PC	VT20C71-35PC	35 ns 4,096 x 4 SRAM 24-Lead Separate I/O
SSM6172-25PC	VT20C72-25PC	25 ns 4,096 x 4 SRAM 24-Lead Separate I/O
SSM6172-35PC	VT20C72-35PC	35 ns 4,096 x 4 SRAM 24-Lead Separate I/O

T.I.	VLSI	Device Description
SMJ64C16 (Note 1)	VT20C68-20PC	20 ns 4,096 x 4 SRAM 20-Lead
TACT2150-20NT	VT7150-20PC	20 ns 512K x 8 Cache-Tag
TACT2150-20DW	VT7150-20SC	20 ns 512K x 8 Cache-Tag
TACT2150-30NT	VT7150-30PC	30 ns 512K x 8 Cache-Tag
TACT2150-30DW	VT7150-30SC	30 ns 512K x 8 Cache-Tag

Toshiba	VLSI	Device Description
TMM2018AP-25	VT20C18-25PC	25 ns 2,048 x 8 SRAM 24-Lead
TMM2018AP-35	VT20C18-35PC	35 ns 2,048 x 8 SRAM 24-Lead
TMM2068AP-25	VT20C68-25PC	25 ns 4,096 x 4 SRAM 20-Lead
TMM2068AP-35	VT20C68-35PC	35 ns 4,096 x 4 SRAM 20-Lead
TMM2978AD-25 (Note 1)	VT20C78-25PC	25 ns 4,096 x 4 SRAM 22-Lead
TMM2978AD-35 (Note 1)	VT20C78-35PC	35 ns 4,096 x 4 SRAM 22-Lead

Vitelic	VLSI	Device Description
V61C16P25	VT20C18-25PC	25 ns 2,048 x 8 SRAM 24-Lead
V61C16P35	VT20C18-35PC	35 ns 2,048 x 8 SRAM 24-Lead
V61C16S25	VT20C18-25SC	25 ns 2,048 x 8 SRAM 24-Lead SOG
V61C16S35	VT20C18-35SC	35 ns 2,048 x 8 SRAM 24-Lead SOG
V61C68P25	VT20C68-25PC	25 ns 4,096 x 4 SRAM 20-Lead
V61C68P35	VT20C68-35PC	35 ns 4,096 x 4 SRAM 20-Lead

Note:
1. This ceramic package is size and pin-compatible with VLSI's plastic package.

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VT7C122

256 × 4 STATIC RAM

FEATURES

- High-speed access and cycle times: 12 ns
- CMOS process for low power: 330 mW (typical)
- Separate, TTL-compatible inputs and outputs
- All pins capable of withstanding electrostatic discharge greater than 2000 V.
- 22-lead, 400 mil plastic DIP
- 24-lead, 300 mil SOG and SOJ packages

DESCRIPTION

The VT7C122 is a high-speed static RAM (SRAM) that is organized as 256 words by 4 bits. If offers very high performance and reliability, as well as low power, making it ideally suited for use in high-performance cache memory, writeable control store and high-speed data buffer applications.

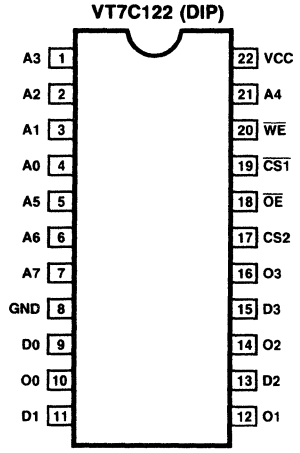
For easy memory expansion, the VT7C122 has an active-LOW chip select one ($\overline{CS1}$) input, an active-HIGH chip select two (CS2) input, and three-state outputs.

The read and write operations of the VT7C122 are controlled by an active-LOW write enable ($\overline{WE}$) input. When $\overline{WE}$ and chip select 1 ($\overline{CS1}$) are LOW and the chip select two (CS2) input is HIGH, information on the data input lines (D0 through D3) is written into the memory word addressed by the A0 through A7 inputs. Simultaneously, the output circuitry is preconditioned so that the correct data is available at the non-inverting output lines (O0 through O3) when the write cycle is complete. Preconditioning minimizes write recovery time by eliminating the "write recovery glitch."

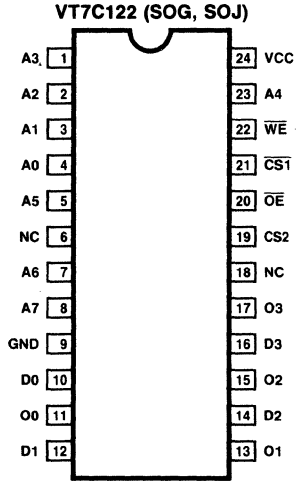
To read data from the VT7C122, the $\overline{CS1}$ and output enable ($\overline{OE}$) inputs must be LOW while CS2 and $\overline{WE}$ are HIGH. The data stored in the addressed memory word is then read out on O0 through O3.

PIN DIAGRAMS

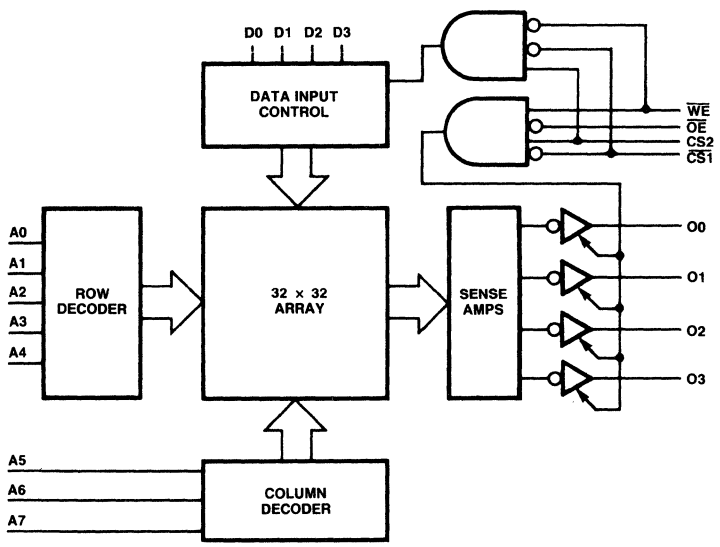
VT7C122 (DIP)



VT7C122 (SOG, SOJ)



BLOCK DIAGRAM



PIN NAMES

A0–A7	Address Inputs
$\overline{CS1}$	Chip Select 1
CS2	Chip Select 2
D0–D3	Data Inputs
GND	Ground (0 V)
O0–O3	Data Outputs
$\overline{OE}$	Output Enable
VCC	Power (5 V)
$\overline{WE}$	Write Enable

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VT20C50

1,024 x 4 CLEARABLE SRAM

FEATURES

- High speed: 15 ns maximum access time
- 1K x 4 organization
- Memory reset (clear) function
- Separate data input/output
- Three-state output buffers
- High-reliability six-transistor memory cell
- Capable of withstanding greater than 2,000 V ESD
- Single 5 V ± 10% power supply
- 24-lead, 300 mil plastic DIP, SOG and SOJ packages

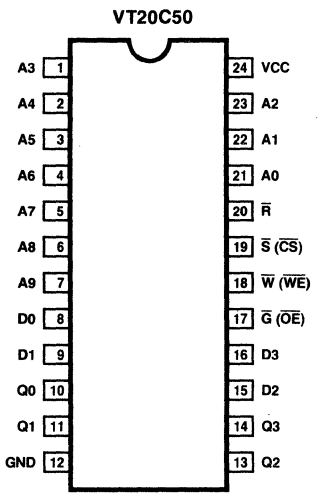
DESCRIPTION

The VT20C50 Clearable SRAM is a high-performance static RAM with a 1,024 x 4 organization. It offers TTL-compatible input and output levels, and features separate input and output pins that enhance system performance and adaptability.

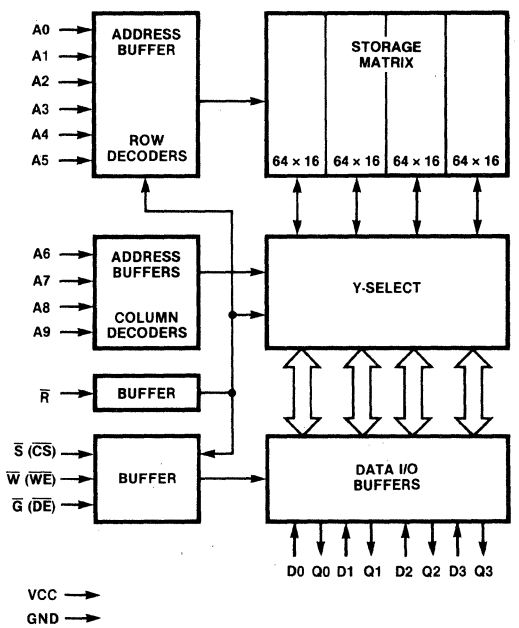
The contents of the VT20C50 can be cleared (all memory cells set to logic 0) within two cycles. To accomplish this, the user regulates the Reset ($\overline{R}$), Chip Select ($\overline{S}$) and Write Enable ($\overline{W}$) inputs.

The VT20C50 features 15 ns access time and a maximum operating current of only 130 mA. It is fabricated using VLSI Technology's CMOS process, and is available in a 24-lead 300 mil plastic dip, as well as 24-lead SOG and SOJ packages.

PIN DIAGRAM



BLOCK DIAGRAM



PIN NAMES

A0 - A9	Address Inputs
D0 - D3	Data Input
Q0 - Q3	Data Output
$\overline{S}$ ($\overline{CS}$)	Chip Select
$\overline{G}$ ($\overline{OE}$)	Output Enable
$\overline{W}$ ($\overline{WE}$)	Write Enable
$\overline{R}$	Reset
VCC	Power (5 V)
GND	Ground (0 V)

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VT20C18 • VT20C19

2,048 × 8 SRAM

FEATURES

- High-speed access and cycle times: 20, 25, and 35 ns
- Fast output enable control
- Fast chip select option (VT20C19)
- Automatic power-down when deselected (VT20C18)
- CMOS process for low power:
  - 600 mW (typical) active
  - 35 mW (typical) standby (VT20C18)
  - 100 μW (typical) CMOS standby (VT20C18)
- Highly reliable six-transistor memory cell
- All pins capable of withstanding electrostatic discharge greater than 2,000 V
- 24-lead, 300 mil plastic DIP, SOG and SOJ packages

DESCRIPTION

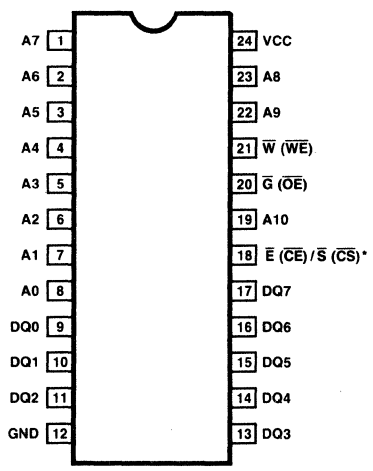
The VT20C18 and VT20C19 are high-speed static RAMs (SRAMs) that are organized as 2,048 words by 8 bits. They were developed in conjunction with VISIC Inc., and are fabricated using an advanced 1.5 micron CMOS process. These devices offer very high performance and reliability, as well as low power, making them suitable for use in high-performance cache memory, writeable control store and high-speed data buffer applications.

The VT20C18, with automatic power-down, offers standby current of only 7 mA (typical) when deselected. The VT20C19 offers a fast chip select option that provides data access in only 10 ns.

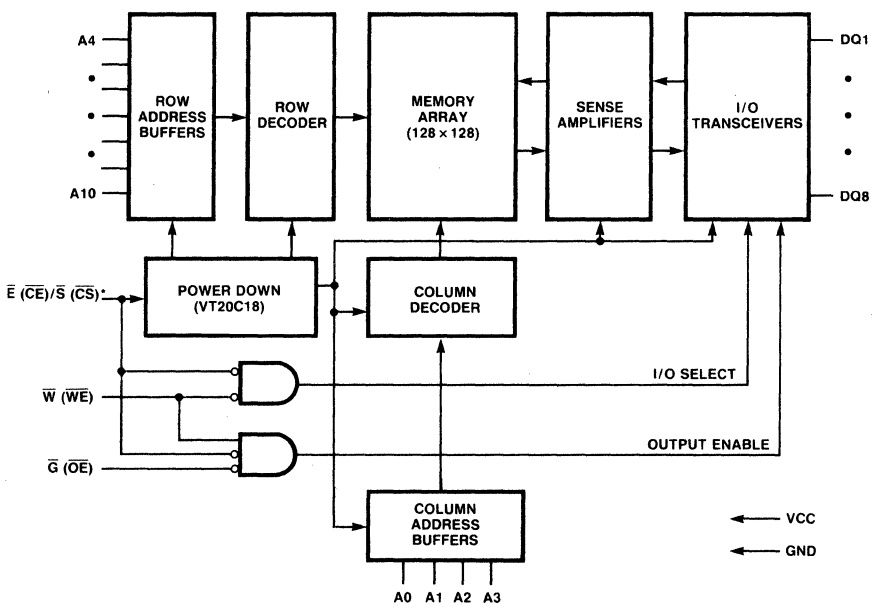
For easy memory expansion, both devices have active-LOW chip enable ($\overline{E}$), output enable ($\overline{G}$) and write enable ($\overline{W}$) signals, as well as three-state outputs. The VT20C18 and VT20C19 are packaged in 300-mil DIPs with industry-standard pinouts, but offer higher speeds for increased system performance.

PIN DIAGRAM

VT20C18 • VT20C19



BLOCK DIAGRAM



PIN NAMES

A0–A10	Address Inputs
DQ0–DQ7	Data Inputs/Outputs
$\overline{E}$ ($\overline{CE}$)/$\overline{S}$ ($\overline{CS}$)*	Chip Enable/Chip Select*
$\overline{W}$ ($\overline{WE}$)	Write Enable
$\overline{G}$ ($\overline{OE}$)	Output Enable
VCC	Power (5 V)
GND	Ground (0 V)

*VT20C19 only.

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VT20C68 • VT20C69

4,096 × 4 SRAM

FEATURES

- High-speed access and cycle times: 20, 25, and 35 ns
- Fast chip select option (VT20C69)
- Automatic power-down when deselected (VT20C68)
- CMOS process for low power:
  - 600 mW (typical) active
  - 35 mW (typical) standby (VT20C68)
  - 100 μW (typical) CMOS standby
- Highly reliable six-transistor memory cell
- Capable of withstanding electrostatic discharge greater than 2,000 V
- 20-lead, 300 mil plastic DIP package
- Pin-compatible with standard 4K × 4 SRAMs

DESCRIPTION

The VT20C68 and VT20C69 are high-speed static RAMs (SRAMs) that are organized as 4,096 words by 4 bits. They were developed in conjunction with VISIC Inc., and are fabricated using an advanced 1.5 micron CMOS process. These devices offer very high performance and reliability, as well as low power. This makes them suitable for use in high-performance cache memory, writeable control store and high-speed data buffer applications.

The VT20C68, with automatic power-down, offers standby current of only 7 mA (typical) when deselected. The VT20C69 offers a fast chip select option that provides data access in only 10 ns.

For easy memory expansion, both devices have active-LOW chip enable ($\overline{E}$) and write enable ($\overline{W}$) signals as well as three-state outputs. The VT20C68 and VT20C69 are packaged in 300 mil DIPs with industry-standard pinouts that are compatible with other static RAMs, but offer higher speeds for increased system performance.

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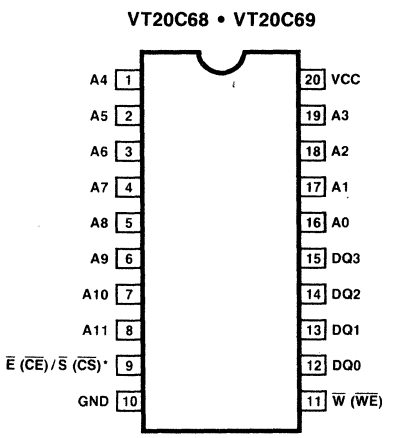
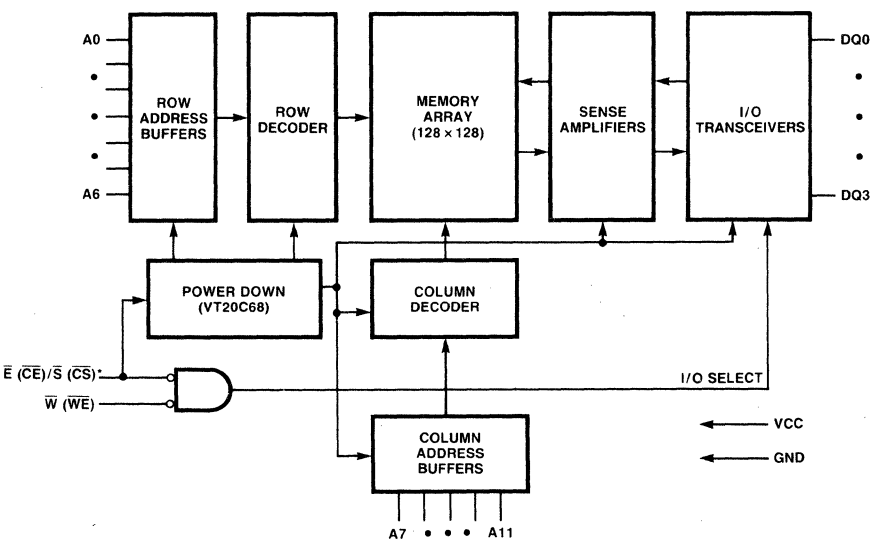
PIN DIAGRAM



BLOCK DIAGRAM



PIN NAMES

A0–A11	Address Inputs
DQ0–DQ3	Data Inputs/Outputs
$\overline{E}$ ($\overline{CE}$) /$\overline{S}$ ($\overline{CS}$)*	Chip Enable/Chip Select*
$\overline{W}$ ($\overline{WE}$)	Write Enable
VCC	Power (5 V)
GND	Ground (0 V)

*VT20C69 only.

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VT20C71 • VT20C72

4,096 × 4 SEPARATE I/O SRAM

FEATURES

- High-speed access and cycle times: 25, 35 ns
- Automatic power-down at deselect
- Pin-compatible with standard 4K × 4 separate I/O SRAMs
- Low-power CMOS process: 600 mW active (typical) 35 mW standby (typical)
- High-reliability six-transistor memory cell
- Capable of withstanding greater than 2000 V ESD
- 24-lead, 300 mil plastic DIP, SOG and SOJ packages

DESCRIPTION

The VT20C71 and VT20C72 are high-speed static RAMs organized as 4,096 words by 4 bits. They were developed in conjunction with VISIC Inc., and are fabricated using an advanced 1.5 micron CMOS process. These devices offer very high performance and reliability as well as low power, making them suitable for use in high-performance cache memory, writeable control store, and high-speed data buffer applications.

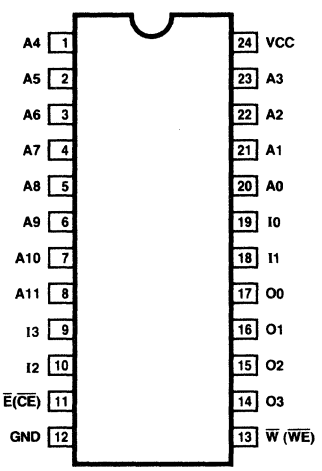
The VT20C71 and VT20C72 feature an automatic power-down that offers a standby current of only 7 mA (typical) when deselected.

For easy memory expansion, both devices have active-LOW Chip Enable ($\overline{E}$) and Write Enable ($\overline{W}$) signals, as well as three-state outputs. The outputs may be placed in the high-impedance state with the Write Enable signal LOW (VT20C72 only) or with the Chip Enable HIGH.

The VT20C71 and VT20C72 are packaged in 300 mil dual in-line packages with industry-standard pinouts, and in 24-lead small-outline packages. They are compatible with other static RAMs, yet offer higher speeds for increased system performance.

PIN DIAGRAM

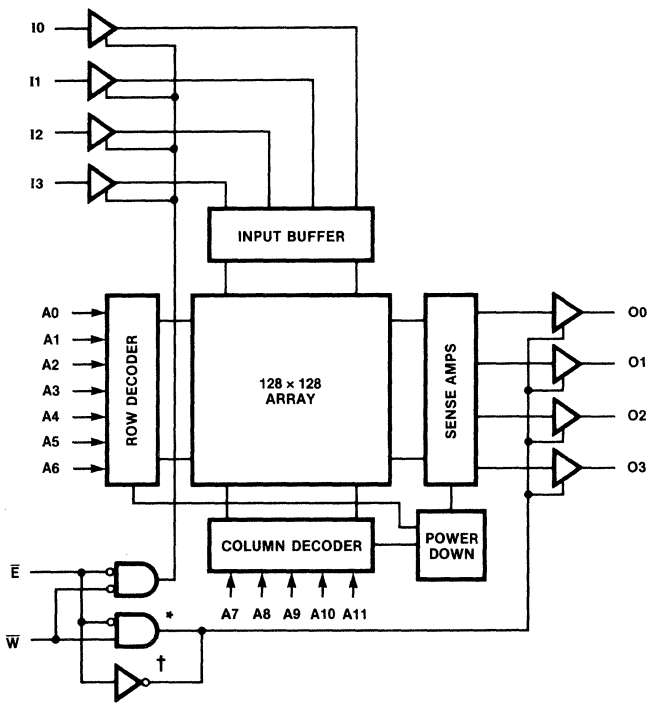
VT20C71 • VT20C72



PIN NAMES

A0 – A11	Address Inputs
I0 – I3	Data Input
O0 – O3	Data Output
E ($\overline{CE}$)	Chip Enable
W ($\overline{WE}$)	Write Enable
VCC	Power (5 V)
GND	Ground (0 V)

BLOCK DIAGRAM



* VT20C72 ONLY
† VT20C71 ONLY

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VT20C78 • VT20C79

4,096 × 4 SRAM

FEATURES

- High-speed access and cycle times: 20, 25, and 35 ns
- Fast output enable control
- Fast chip select option (VT20C79)
- Automatic power-down when deselected (VT20C78)
- CMOS process for low power:
  - — 600 mW (typical) active
  - — 35 mW (typical) standby (VT20C78)
  - — 100 μW (typical) CMOS standby
- Highly reliable six-transistor memory cell
- Capable of withstanding electrostatic discharge greater than 2,000 V
- 22-lead, 300 mil plastic DIP
- 24-lead, 300 mil SOG and SOJ packages
- Pin-compatible with standard 4K × 4 SRAMs

DESCRIPTION

The VT20C78 and VT20C79 are high-speed static RAMs (SRAMs) that are organized as 4,096 words by 4 bits. They were developed in conjunction with VISIC Inc., and are fabricated using an advanced 1.5 micron CMOS process. These devices offer very high performance and reliability, as well as low power. This makes them suitable for use in high-performance cache memory, writeable control store and high-speed data buffer applications.

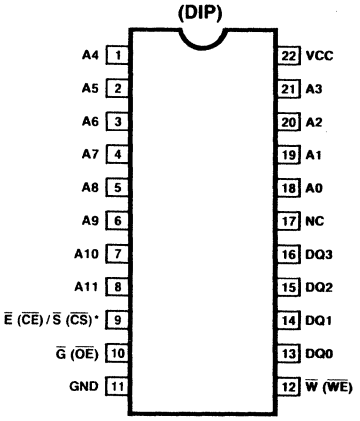
The VT20C78, with automatic power-down, offers standby current of only 7 mA (typical) when deselected. The VT20C79 offers a fast chip select option that provides data access in only 10 ns.

For easy memory expansion, both devices have active-LOW chip enable ($\overline{E}$), output enable ($\overline{G}$), and write enable ($\overline{W}$) signals, as well as three-state outputs. The VT20C78 and VT20C79 are packaged in 300-mil DIPs with industry-standard pinouts that are compatible with other static RAMs, but offer higher speeds for increased system performance.

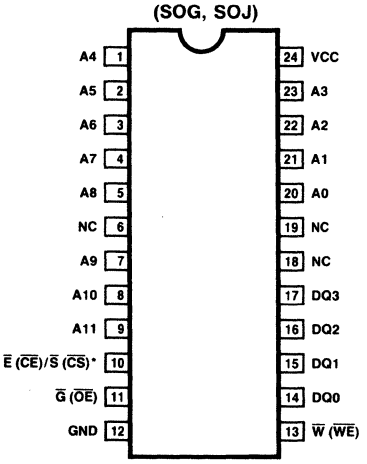
PIN DIAGRAM

VT20C78 • VT20C79

(DIP)

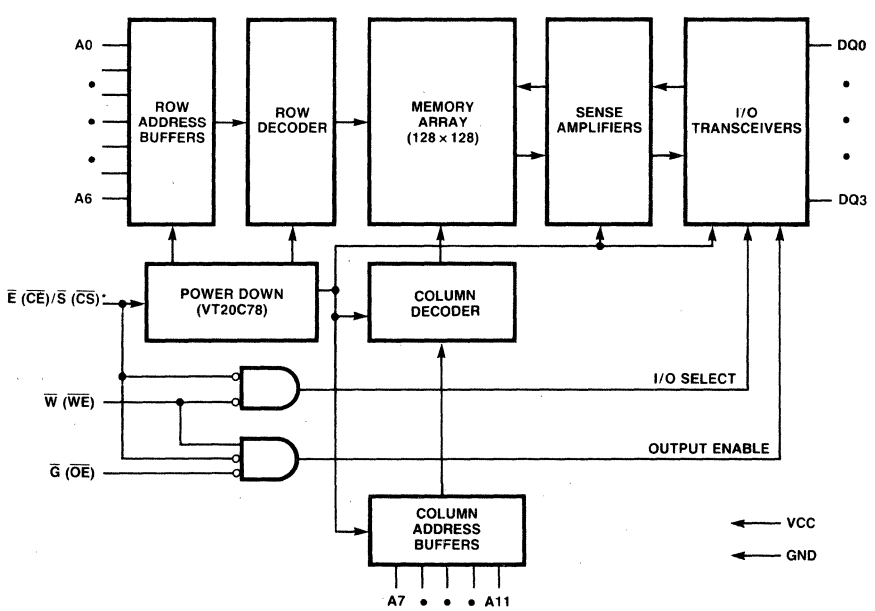


(SOG, SOJ)



*VT20C79 only.

BLOCK DIAGRAM



PIN NAMES

A0–A11	Address Inputs
DQ0–DQ3	Data Inputs/Outputs
$\overline{E}$ ($\overline{CE}$)/$\overline{S}$ ($\overline{CS}$)*	Chip Enable/Chip Select*
$\overline{W}$ ($\overline{WE}$)	Write Enable
$\overline{G}$ ($\overline{OE}$)	Output Enable
VCC	Power (5 V)
GND	Ground (0 V)

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ADVANCED INFORMATION **VT6288**

16,384 x 4 HIGH-SPEED 64K SRAM

FEATURES

- 16,384 x 4-bit organization
- High-speed access time
  — 25 ns max
- Low current
  — Operating: 60 mA (typ)
  — Standby: .02 mA (typ)
- Total static operation
- Single 5 V supply
- Complete TTL compatibility
- 3-state I/O
- 22-lead, 300 mil plastic DIP

DESCRIPTION

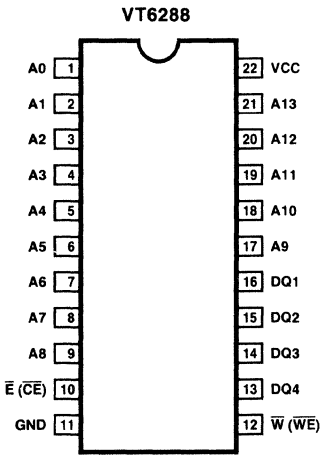
The VT6288 is a 64K high-speed static random access memory that is organized as 16,384 words by four bits.

The device is fabricated in CMOS technology and achieves access times of 25 ns with a maximum power consumption of 600 mW. The high speed of the VT6288 enables it to replace bipolar and fast NMOS memories in many applications.

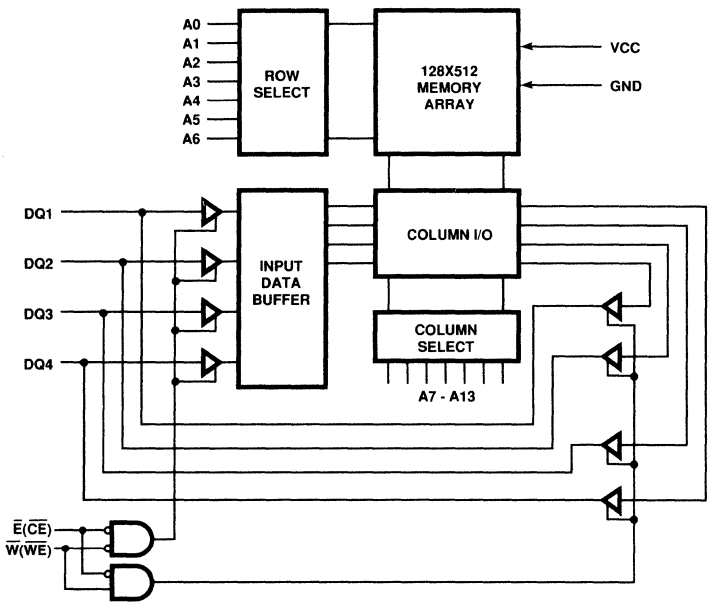
The fully static circuit requires no clocks or refreshing for operation. The VT6288 provides equal access and cycle times for ease of use.

The device operates from a single 5 V power supply and is completely TTL compatible.

PIN DIAGRAM



BLOCK DIAGRAM



PIN NAMES

A0–A13	Address
DQ1–DQ4	Data Input/Output
Ē (C̄Ē)	Chip Enable
W̄ (W̄Ē)	Write Enable
VCC	Power (5 V)
GND	Ground (0 V)

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ADVANCED INFORMATION **VT62832**

32,768 x 8 SRAM

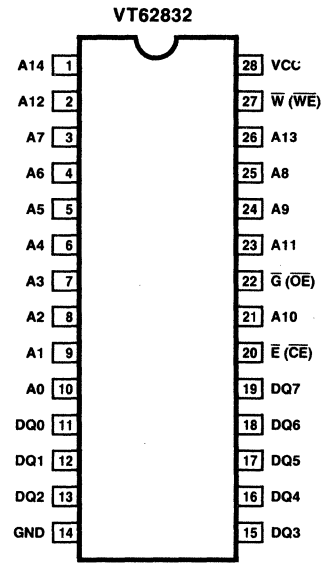
FEATURES

- High-speed access and cycle times: 35, 45 ns
- Low-power CMOS process:
  - 300 mW active (typical)
  - 100 μW standby (typical)
  - 15 μW CMOS standby (typical)
- Total static operation
- Single 5 V supply
- Full TTL compatibility
- 28-lead, 300 mil plastic DIP and SOJ packages

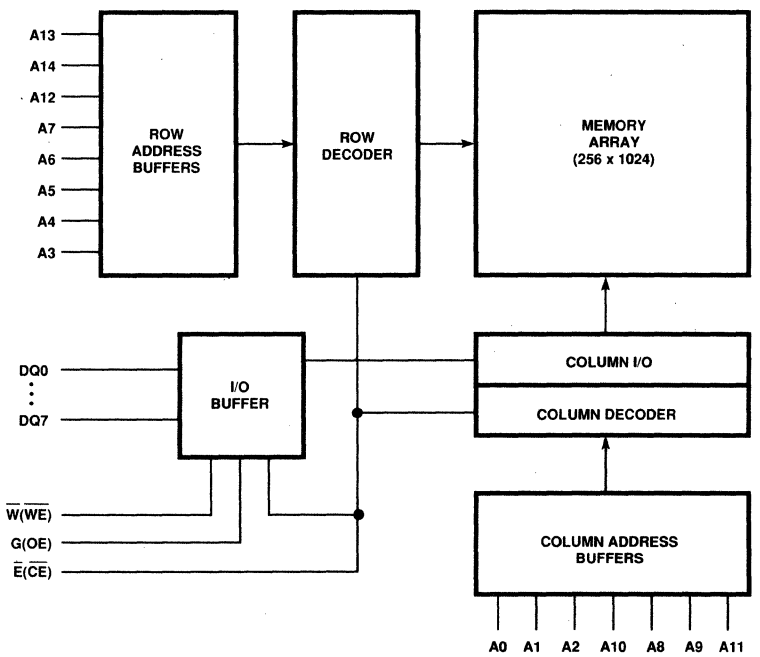
DESCRIPTION

The VT62832 is a high-speed static RAM organized as 32,768 words by 8 bits. This device offers very high performance and reliability as well as low power, making it suitable for use in high-performance cache memory, writeable control store, and high-speed data buffer applications.

PIN DIAGRAM



BLOCK DIAGRAM



PIN NAMES

A0–A14	Address Inputs
DQ0–DQ7	Data Input/Output
E (CE)	Chip Enable
W (WE)	Write Enable
G (OE)	Output Enable
VCC	Power (5 V)
GND	Ground (0 V)

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PRELIMINARY **VT6208 • VT6208L**

65,536 x 4 SRAM

FEATURES

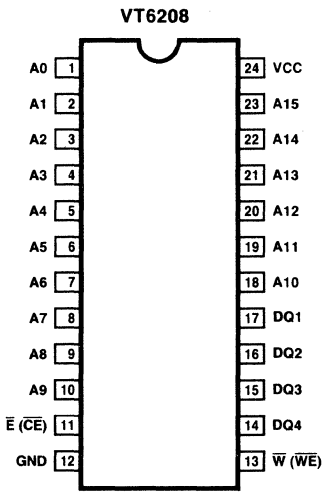
- High-speed access and cycle times: 35 and 45 ns (max)
- 1.2 μ CMOS process
- Fully static operation
- Chip enable input, automatic power-down when disabled
- CMOS process for low power
  - 300 mW (typical) active
  - 100 μW (typical) standby
  - 10 μW (typical) CMOS standby
- Single 5 V $\pm$ 10% power supply
- Fully TTL compatible
- Battery back-up operation (VT6208L)
- 24-lead, 300 mil plastic DIP

DESCRIPTION

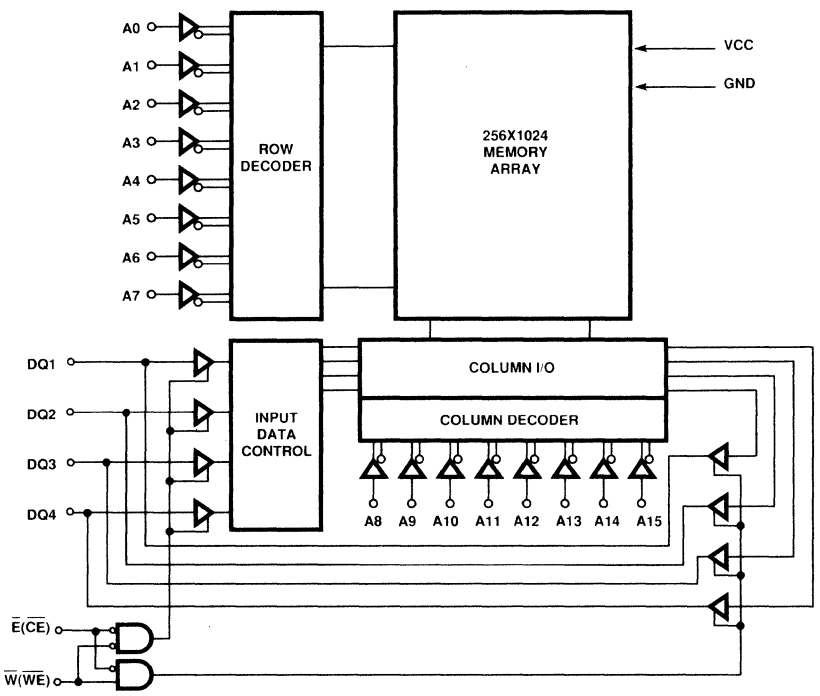
The VT6208 and VT6208L are high-speed static RAMs (SRAMs) organized as 65,536 words by four bits. These devices are fabricated using an advanced 1.2 μ CMOS process. They offer high performance 35 and 45 ns access times as well as high reliability and low power.

The VT6208L offers typical standby current of 10 μW, and is ideal in systems where power dissipation is a major consideration. This includes battery-operated systems and systems employing battery back-up. Both the VT6208 and the VT6208L are offered in 300 mil plastic DIP.

PIN DIAGRAM



BLOCK DIAGRAM



PIN NAMES

A0–A15	Address Inputs
DQ1–DQ4	Data Inputs/Outputs
$\overline{E}$ ($\overline{CE}$)	Chip Enable
$\overline{W}$ ($\overline{WE}$)	Write Enable
VCC	Power (5 V)
GND	Ground (0 V)

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PRELIMINARY **VT16DP8**

1,024 x 16, 2,048 x 8 DUAL-PORT RAM

FEATURES

- Organization:
  - — Left port: 1,024 x 16
  - — Right port: 2,048 x 8
- High speed:
  - — 70 ns access (max)
- Fully static operation
- Full contention arbitration
- Simple microprocessor interface
- Output enable function
- Separate port power-down
- Advanced CMOS technology
- Two interrupt flags
- Low power:
  - — 90 mA (max) operating
- 68-lead PLCC

DESCRIPTION

The VT16DP8 is a 16,384-bit dual-port static random access memory. Its left port is organized as 1,024 16-bit words and its right port as 2,048 8-bit words. It is designed to facilitate the transfer of data between 16- and 8-bit microprocessors.

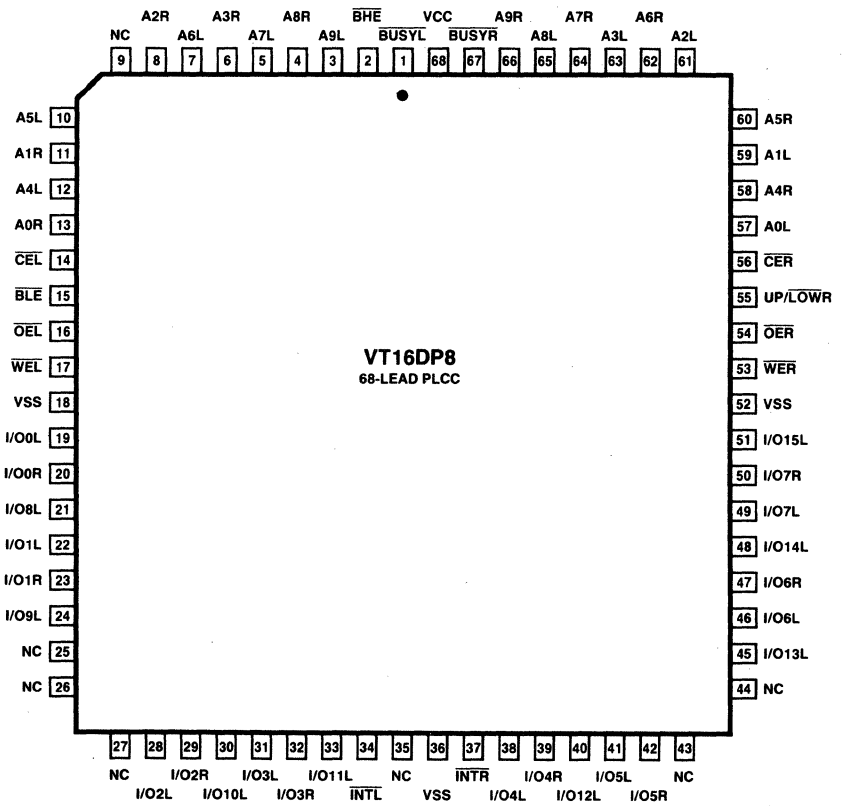
The VT16DP8 features two separate I/O ports that each allow independent access for read or write to any location in the memory. The memory is designed to enable simultaneous read and/or write from either the 16-bit or the 8-bit port. Contention arbitration logic is provided to eliminate overlapping operations to the same memory location. Two modes of operation are provided. One mode allows contention to be ignored and both operations to proceed. In the other mode, the on-chip contention logic arbitrates and delays one port until the other port's operation is completed. When this occurs, a Busy flag is sent to the side delayed. This flag stays set until the first operation is complete. When both sides request at exactly the same time, the 16-bit port takes priority.

The 16-bit port is designed to allow easy interface to all 16-bit microprocessors by the inclusion of the ability to read and write in either a word or a byte mode. The $\overline{BHE}$ and $\overline{BLE}$ control lines enable the upper byte or the lower byte, respectively. When both lines are active, the VT16DP8 is in word mode.

PIN NAMES

I/O0L–I/O15L	Left Port Data Input/Output
A0L–A9L	Left Port Address
$\overline{CEL}$	Left Port Chip Enable
$\overline{OEL}$	Left Port Output Enable
$\overline{WEL}$	Left Port Write Enable
$\overline{BUSYL}$	Left Port Busy Flag Output
$\overline{INTL}$	Left Port Interrupt Output
$\overline{BHE}$	Byte High Enable
$\overline{BLE}$	Byte Low Enable
I/O0R–I/O7R	Right Port Data Input/Output
UP/$\overline{LOW}$R	Right Port Upper or Lower Byte Select
A0R–A9R	Right Port Address
$\overline{CER}$	Right Port Chip Enable
$\overline{OER}$	Right Port Output Enable
$\overline{WER}$	Right Port Write Enable
$\overline{BUSYR}$	Right Port Busy Flag Output
$\overline{INTR}$	Right Port Interrupt Output
VCC	Power (5 V)
VSS	Ground (0 V)
NC	No Connect (7 leads)

PIN DIAGRAM



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ADVANCED INFORMATION **VT7202**

1,024 x 9 FIFO MEMORY

FEATURES

- First-in, first-out dual-port memory
- Low-power CMOS process
- Fully asynchronous operation
- Simultaneous read and write
- Fully expandable in depth and width
- Access time: 20 ns
- Dependable empty, half-full, and full warning flags
- Rate buffer applications
- Multi-processing master/slave applications
- 28-lead, 600 mil plastic DIP
- 32-lead PLCC

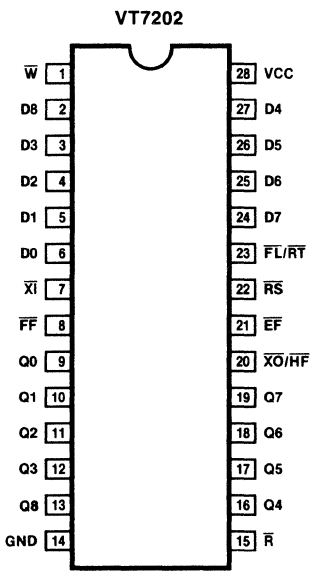
DESCRIPTION

The VT7202 is a first-in, first-out (FIFO) memory that uses a high-performance static RAM array with internal logic to ensure totally asynchronous operation. Full, half-full, and empty flags are provided to allow the device to operate without external logic. The VT7202 also contains logic that allows for unlimited expansion in both word size and depth.

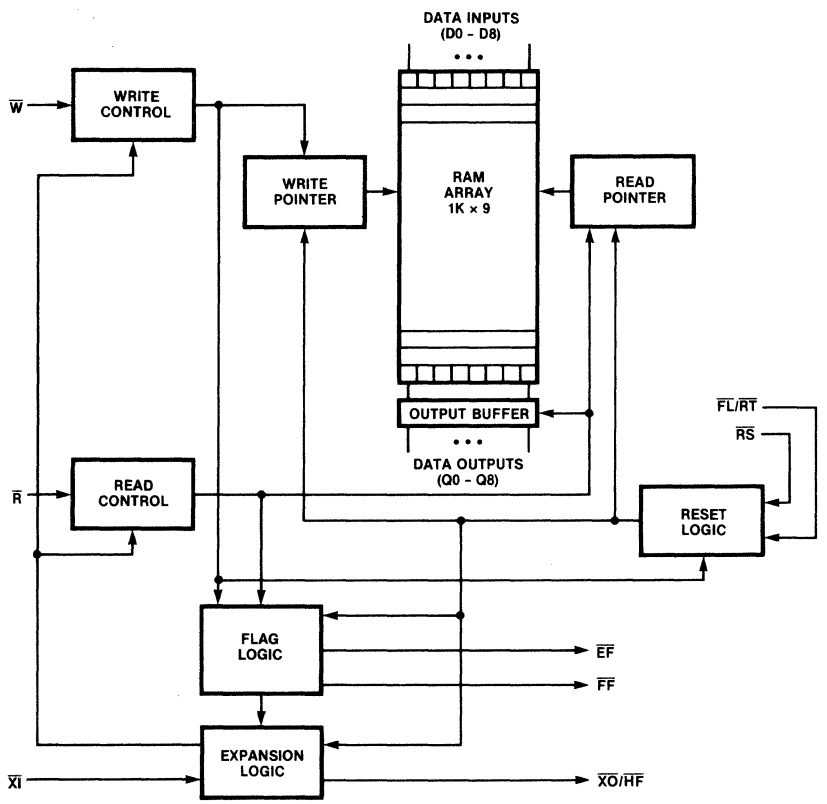
Although the VT7202 uses a static RAM array as its memory element, a system of read and write pointers has been included to sequence through the array. Data is toggled in and out of the device by means of the Write Enable ($\overline{W}$) and Read Enable ($\overline{R}$) signals. The VT7202 has an access time of 20 ns and a read/write cycle time of 30 ns (33 MHz). Its 1,024 x 9 organization permits the use of control or parity bits at the option of the user, and also allows a 1,024-deep word structure without the need for expansion.

The VT7202 is fabricated using VLSI Technology's high-performance CMOS process. Its design is ideally suited to asynchronous and simultaneous reading and writing in multi-processing and rate buffer applications. The FIFO is available in both plastic dual in-line and plastic leaded chip carrier packages.

PIN DIAGRAM



BLOCK DIAGRAM



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ADVANCED INFORMATION **VT7203**

2,048 x 9 FIFO MEMORY

FEATURES

- First-in, first-out dual-port memory
- Low-power CMOS process
- Fully asynchronous operation
- Simultaneous read and write
- Fully expandable in depth and width
- Access time: 20 ns
- Dependable empty, half-full, and full warning flags
- Rate buffer applications
- Multi-processing master/slave applications
- 28-lead, 600 mil plastic DIP
- 32-lead PLCC

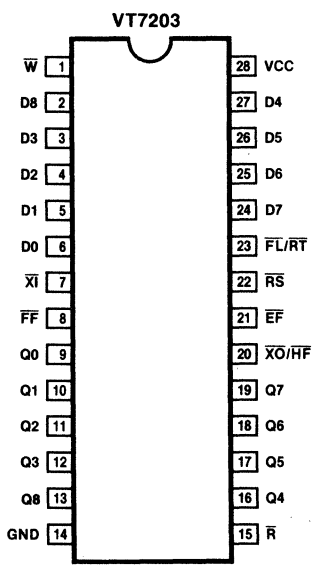
DESCRIPTION

The VT7203 is a first-in, first-out (FIFO) memory that uses a high-performance static RAM array with internal logic to ensure totally asynchronous operation. Full, half-full, and empty flags are provided to allow the device to operate without external logic. The VT7203 also contains logic that allows for unlimited expansion in both word size and depth.

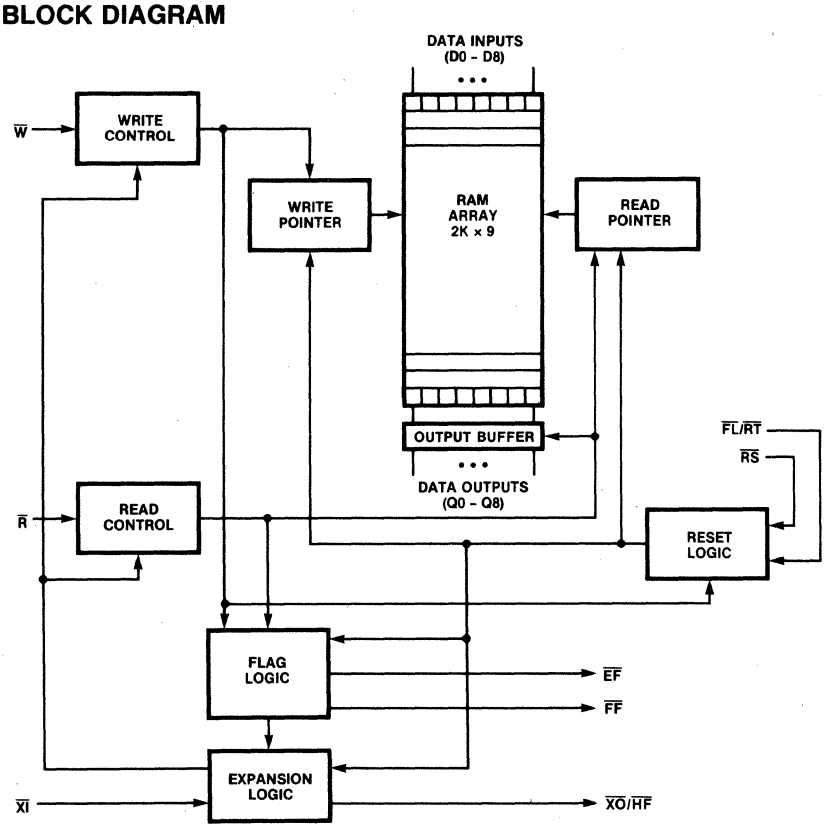
Although the VT7203 uses a static RAM array as its memory element, a system of read and write pointers has been included to sequence through the array. Data is toggled in and out of the device by means of the Write Enable ($\overline{W}$) and Read Enable ($\overline{R}$) signals. The VT7203 has an access time of 20 ns and a read/write cycle time of 30 ns (33 MHz). Its 2,048 x 9 organization permits the use of control or parity bits at the option of the user, and also allows a 2,048-deep word structure without the need for expansion.

The VT7203 is fabricated using VLSI Technology's high-performance CMOS process. Its design is ideally suited to asynchronous and simultaneous reading and writing in multi-processing and rate buffer applications. The FIFO is available in both plastic dual in-line and plastic leaded chip carrier packages.

PIN DIAGRAM



BLOCK DIAGRAM



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PRELIMINARY **VT7132 • VT7142**

2,048 x 8 CMOS DUAL-PORT RAM

FEATURES

- High speed:
  — 55, 70, and 90 ns access
- Fully static operation
- Full contention arbitration (VT7132)
- VT7142 slave for bus expansion
- Output enable function
- Separate port power-down
- Advanced CMOS technology
- Low power: 150 mA (max) operating
- 48-lead, 600 mil plastic DIP
- 52-lead PLCC

DESCRIPTION

The VT7132 and VT7142 are 16,384-bit dual-port static random access memories that are organized as 2,048 8-bit words. The VT7132 is designed to be used as a stand-alone "master" dual-port RAM with the VT7142 "slave" dual-port RAM in a system application larger than 8 bits. The master/slave approach in large bus systems requires no external contention logic.

The VT7132/VT7142 feature two separate I/O ports that each allow independent access to read or write to any location in the memory. The memory is designed to permit read and/or write operations to be performed at both ports at the same time. Contention arbitration logic is provided to eliminate overlapping operations to the same memory location.

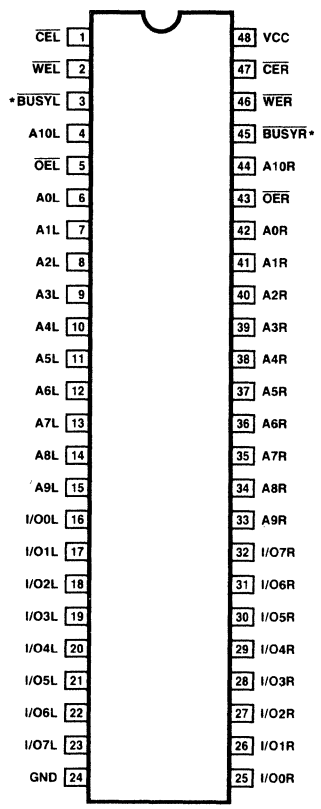
The on-chip contention logic arbitrates and delays one port until the other port's operation is completed. When this occurs, a Busy flag is sent to the side delayed. This flag stays set until the first operation is complete. When both sides request access at exactly the same time, the left port takes priority.

Automatic power down for each port is controlled independently by its Chip Enable input.

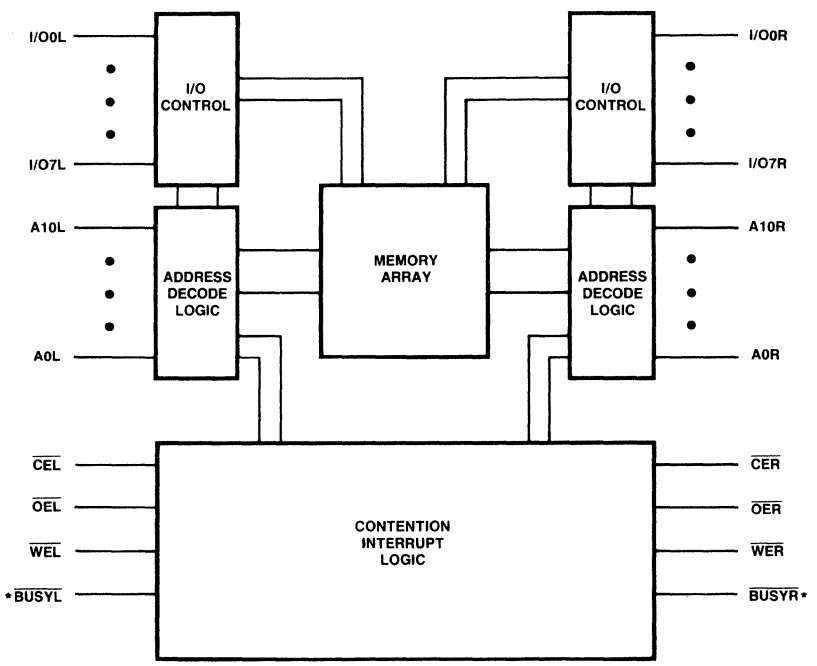
Interfacing to the VT7132/VT7142 is further simplified by the incorporation of an Output Enable control for each port.

PIN DIAGRAM

VT7132/VT7142



BLOCK DIAGRAM



* OPEN-DRAIN OUTPUTS FOR VT7132. INPUTS FOR VT7142.

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PRELIMINARY **VT7132A • VT7142A**

HIGH-SPEED 2,048 x 8 CMOS DUAL-PORT RAM

FEATURES

- High speed:
  — 30, 35, and 45 ns access
- Fully static operation
- Full contention arbitration
- VT7142A slave for bus expansion
- Output enable function
- Separate port power-down
- Advanced CMOS technology
- Dual interrupt flags in PLCC
- Low power: 150 mA (max) operating
- 48-lead, 600 mil plastic DIP
- 52-lead PLCC

DESCRIPTION

The VT7132A and VT7142A are 16,384-bit dual-port static random access memories that are organized as 2,048 8-bit words. The VT7132A is designed to be used as a stand-"master" dual-port RAM with the VT7142A "slave" dual-port RAM in a system application larger than 8 bits. The master/slave approach in large bus systems requires no external contention logic.

The VT7132A/VT7142A feature two separate I/O ports that each allow independent access for read or write to any location in the memory. The memory is designed to permit read and/or write operations to be performed at both ports at the same time. Contention arbitration logic is provided to eliminate overlapping operations to the same memory location.

The on-chip contention logic arbitrates and delays one port until the other port's operation is completed. When this occurs, a Busy flag is sent to the side delayed. This flag stays set until the first operation is complete. When both sides request at exactly the same time, the left port takes priority.

When used in the 52-pin PLCC package, a dual-level interrupt function is available. The interrupt function acts like writable flags and is provided to allow communication between systems. When the flag's location is written from one side, the other side's $\overline{INT}$ pin goes LOW until the flag location is read by that side.

One flag is set during a write operation to any location and the other flag is set during a write to location 7FF/7FE.

Both Interrupt and Busy flags are open drain for simple wired OR operation.

Automatic power down for each port is controlled independently by its Chip Enable input.

Interfacing to the VT7132A/VT7142A is further simplified by the incorporation of an Output Enable control for each port.

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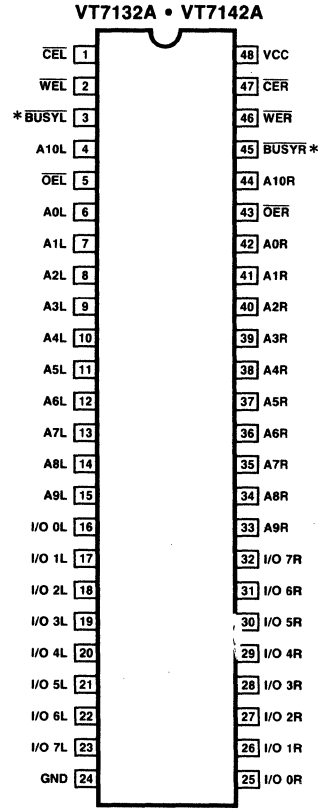
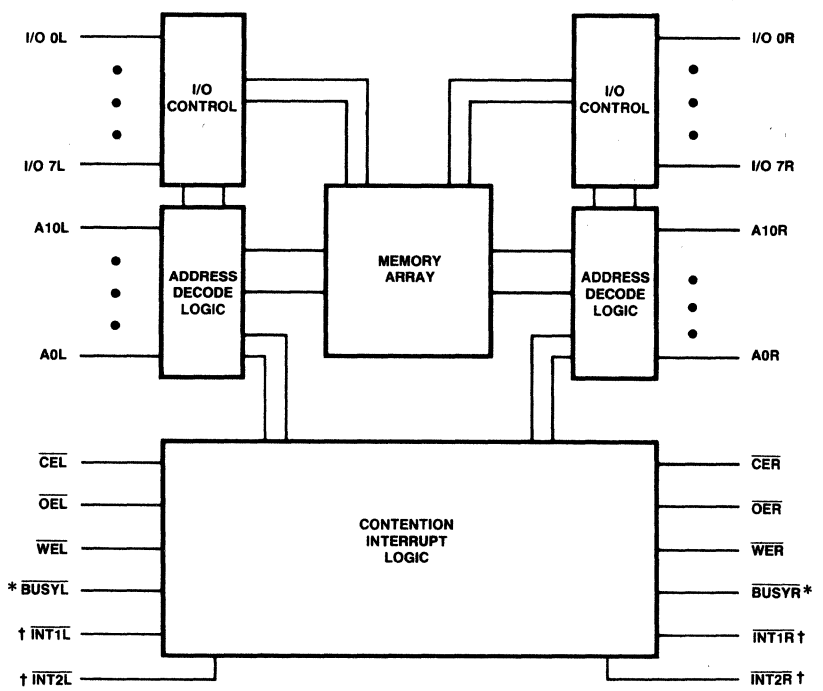
PIN DIAGRAM

VT7132A • VT7142A



BLOCK DIAGRAM



* OPEN-DRAIN OUTPUTS FOR VT7132A. INPUTS FOR VT7142A.
† AVAILABLE ONLY WITH 52-LEAD PLCC.

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PRELIMINARY **VT7150**

512 x 8 CACHE TAG RAM

FEATURES

- Fast address to match valid delay — three speed ranges: 20 ns, 25 ns, 30 ns and 35 ns
- 512 x 9 internal RAM
- On-chip parity generation and checking
- Parity error output/force parity error input
- On-chip address/data comparator
- Asynchronous, single-cycle reset
- Easily expandable
- Fully static
- Reliable CMOS technology
- TTL- and CMOS-compatible inputs and outputs
- 750 mW maximum power dissipation
- 24-lead, 300 mil plastic DIP, SOG and SOJ packages

DESCRIPTION

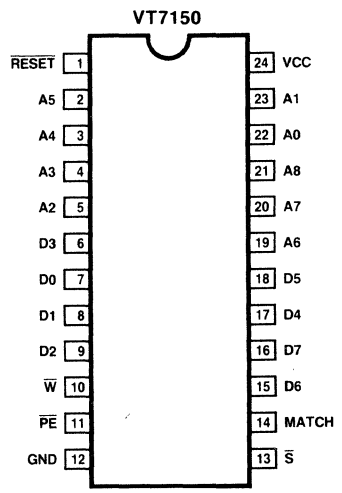
The VT7150 Cache Tag RAM contains a high-speed CMOS static RAM array that uses a full CMOS six-transistor cell for reliable high-speed and low-power operation. Also included on the chip are a parity generator, parity checker, and high-speed 9-bit comparator for comparing input tag data with stored tag data. The device is easily cascadable for wider addresses or deeper tag memories, and interfaces easily with TTL, MOS, and CMOS circuits.

In a compare cycle, the comparator compares the contents of the currently addressed RAM location, including the stored parity bit, with the data present at the data inputs together with the generated parity bit. When all 9 bits of each word match, the MATCH output is asserted. The parity checker checks the parity of the stored byte being accessed, 8 data bits plus 1 parity bit. A parity error is indicated when the number of 1's in the stored byte plus the stored parity bit add up to an odd number. A parity error on the stored tag data is indicated when $\overline{PE}$ and MATCH are both low. The parity generator generates the parity bit from the 8-bit data word at the data inputs.

In a write cycle, the data at the data inputs, plus the generated parity, is written into the memory location addressed by the address inputs.

When the $\overline{RESET}$ input goes LOW, all RAM bits are cleared to zero, and the MATCH output is forced HIGH.

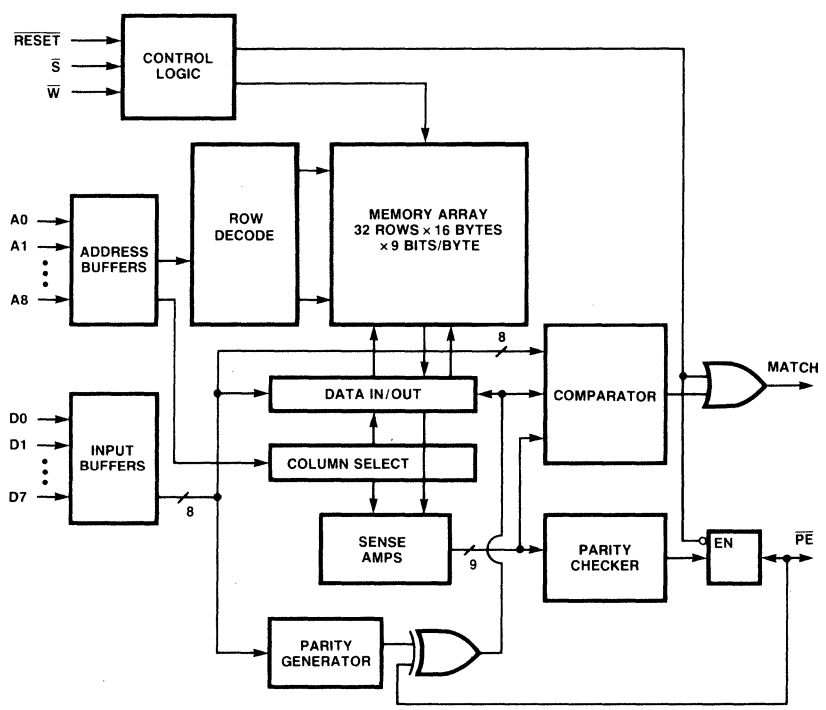
PIN DIAGRAM



PIN NAMES

$\overline{RESET}$	Reset Input
A0–A8	Address Inputs
D0–D7	Data Inputs
$\overline{W}$	Write Control Input
$\overline{PE}$	Parity Error I/O
$\overline{S}$	Chip Select Input
MATCH	Comparator Output
VCC	Power (5 V)
GND	Ground (0 V)

BLOCK DIAGRAM



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ADVANCED INFORMATION **VT7152 • VT7154**

2,048 x 8 CACHE TAG RAM

FEATURES

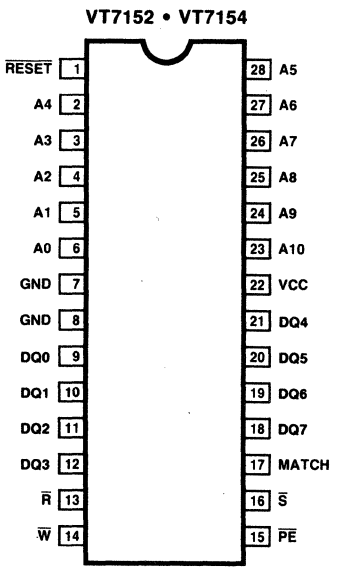
- Fast address to MATCH — 25 ns, 35 ns
- 2K x 9 internal RAM array
- On-chip parity generation and checking
- Parity error output/force parity error input
- On-chip tag comparator
- Common input/output with read feature
- Parity error output
  — Open-drain
- MATCH output
  — Totem-pole on VT7152
  — Open-drain on VT7154
- Easily expandable
- Single-pulse asynchronous reset
- Pin and function compatible with the TI2152/54
- TTL-compatible inputs and outputs
- 28-lead, 600 mil plastic DIP, and 28-lead PLCC

DESCRIPTION

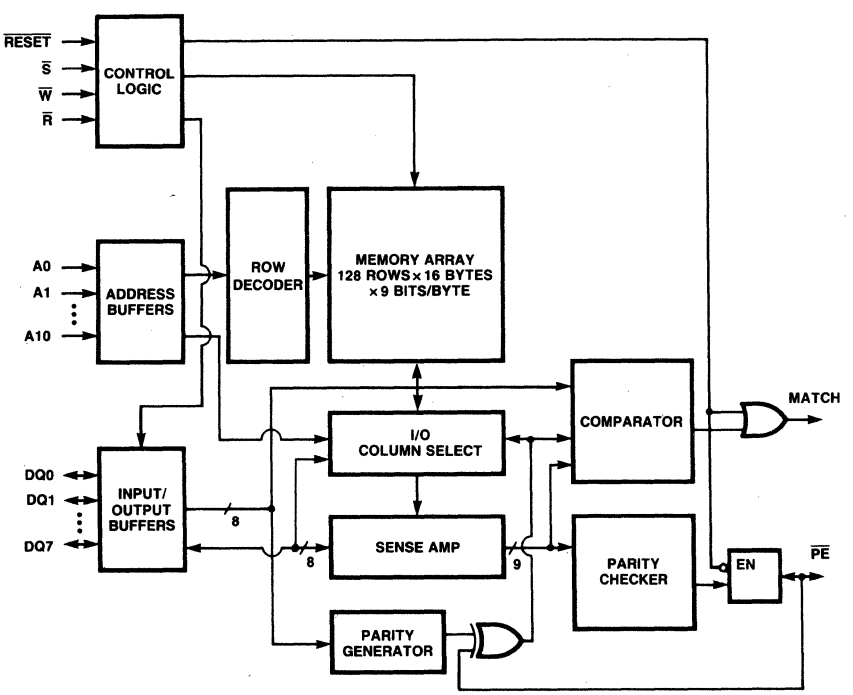
The VT7152 and VT7154 cache tag RAMs consist of a high-speed 2K x 9 static RAM array, parity generator and checker, and a 9-bit high-speed comparator. These cache tag RAMs are easily cascadable to achieve wider tag addresses or deeper tag memories. They offer significant reductions in cache memory component count, power dissipation, and board area.

The VT7152 and VT7154 are fabricated using CMOS technology for high speed and simple interface to MOS and bipolar TTL circuits. They operate from a single 5 V supply, over a temperature range of 0°C to 70°C, and are available in a 600 mil, 28-lead plastic dual in-line package, and in a 28-lead plastic leaded chip carrier (PLCC).

PIN DIAGRAM



BLOCK DIAGRAM



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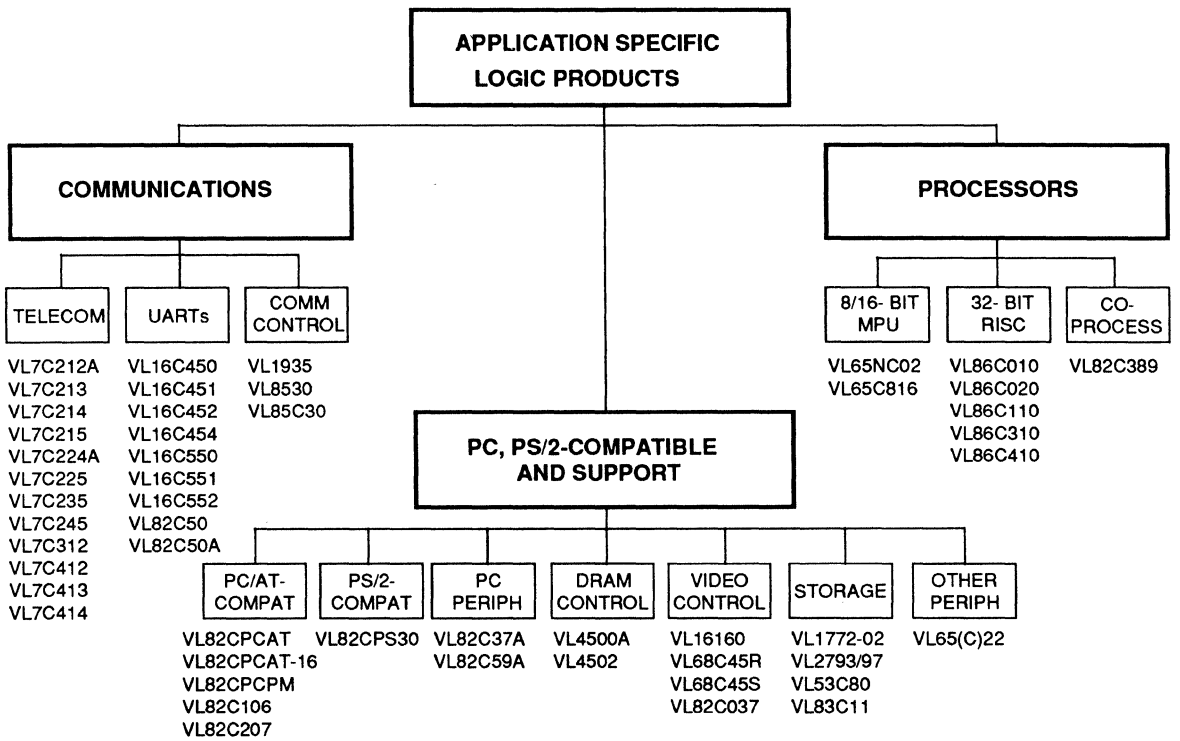
APPLICATION SPECIFIC LOGIC PRODUCTS

LINE CARD



DEVICE	DESCRIPTION	DEVICE	DESCRIPTION
VL16160	Raster Operation Graphics/Boolean ALU	**VL7C245**	CMOS 2400 bps MAC, Serial Interface
VL16C450	CMOS High Speed UART (IBM-AT)	**VL7C312**	CMOS 1200 bps Modem with Gain Select
VL16C451	CMOS UART & Centronics Printer Port	**VL7C412**	CMOS 1200 bps Modem (+5 Volts only Supply)
VL16C452	CMOS Dual UART & Centronics Printer Port	**VL7C413**	CMOS Modem Cont., Para. Bus, with Pwr-down Cont.
VL16C454	CMOS Quad UART	**VL7C414**	CMOS Modem Cont., Ser. Bus, with Pwr-down Cont.
VL16C550	CMOS UART (IBM PS/2-Compatible Rev.)	**VL82CPS30**	CMOS IBM PS/2 Mod.30-Compatible 2 Chip Set
VL16C551	CMOS UART (IBM PS/2-Comp. & Cent.Printer Pt.)	**VL82C037**	CMOS IBM PS/2-Compat. Video Graphics Cont. (VGA)
VL16C552	CMOS Dual UART (IBM PS/2 Compatible Rev.)	**VL82C37A**	CMOS Direct Memory Access (DMA) Controller
VL1772-02	Floppy Disk Controller (Digital Data Separator)	**VL82C50**	CMOS UART (IBM-PC/XT)
VL1935	Sync, Data Link Controller (SDLC/HDLC)	**VL82C50A**	CMOS Enhanced UART (Improved 82C50)
VL2793/97	Floppy Disk Controller (Analog Data Separator)	**VL82C59A**	CMOS Programmable Interrupt Controller
VL4500A	64K DRAM Controller	**VL82C389**	CMOS Multibus II Message Passing Coproc. (MPC)
VL4502	CMOS 256K DRAM Controller	**VL82CPCAT**	CMOS IBM PC/AT-Compatible 5 Chip Set (12 MHz)
VL53C80	CMOS SCSI Interface Controller	**VL82CPCAT-16**	CMOS IBM PC/AT-Compatible 5 Chip Set (16 MHz)
VL65NC02	8-bit CMOS MPU (NMOS 6502 Compatible)	**VL82CPCPM**	CMOS IBM PC/AT-Comp.(6 Chips)(16MHz),Page Md.
VL65(C)22	Para. Interface/Timr. (VL65C22 - CMOS Vers.)	**VL82C106**	CMOS Dual UART, R.T.C., KBD Controller
VL65C816	16-bit CMOS 65C02 Soft. Compat. MPU	**VL82C207**	CMOS UART with Parallel Port, R.T.C. & KBD Cont.
VL68C45R/S	CMOS CRT Cont. (/R - Moto., /S - Hit. Equivalent)	**VL83C11**	CMOS SCSI Interface Buffer
VL7C212A	CMOS 1200 bit-per-second Modem	**VL8530**	Serial Communications Controller (SCC)
VL7C213	CMOS Modem Controller - Parallel Bus Interface	**VL85C30**	CMOS Enhanced SCC (ESCC)
VL7C214	CMOS Modem Controller - Serial Interface	**VL86C010**	CMOS 32-bit RISC Processor
VL7C215	Turbo CMOS Modem Cont. - Para. Bus Interface	**VL86C020**	CMOS Enhanced 32-bit RISC Microprocessor
VL7C224A	CMOS 2400 bps Analog Modem Processor	**VL86C110**	CMOS RISC Processor Memory Controller (MEMC)
VL7C225	CMOS 2400 bps Modem Advanced Coprocessor	**VL86C310**	CMOS RISC Processor Video Controller (VIDC)
VL7C235	CMOS 2400 bps MAC, Parallel Interface	**VL86C410**	CMOS RISC Processor I/O Controller (IOC)

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VL16C451

PARALLEL/ASYNCHRONOUS COMMUNICATIONS ELEMENT

FEATURES

- IBM PC/AT-compatible
- VL16C450 with on-board Centronix printer interface
- Completely pin- and upward-compatible with the dual serial channel VL16C452
- Independent control of transmit, receive, line status and data set interrupts
- Individual modem control signals
- Programmable serial interface characteristics:
  - 5-, 6-, 7- or 8-bit characters
  - Even-, odd- or no-parity bit generation and detection
  - 1, 1 1/2 or 2 stop bit generation
- Three-state TTL drive for the data and control bus

DESCRIPTION

The VL16C451 is an enhanced version of the popular VL16C450 asynchronous communications element (ACE). The serial channel performs serial-to-parallel conversion on data characters received from peripheral devices or modems, and parallel-to-serial conversion on data characters transmitted by the CPU. The complete status of the Parallel/Asynchronous Communications Element (P/ACE) can be read at any time during functional operation by the CPU. The information obtained includes the type and condition of the transfer operation being performed, and error conditions. It is fully pin- and upward-compatible with the dual serial channel VL16C452. The second serial channel of the VL16C452 occupies pins that are VCC, GND, or NC (not connected) on the VL16C451.

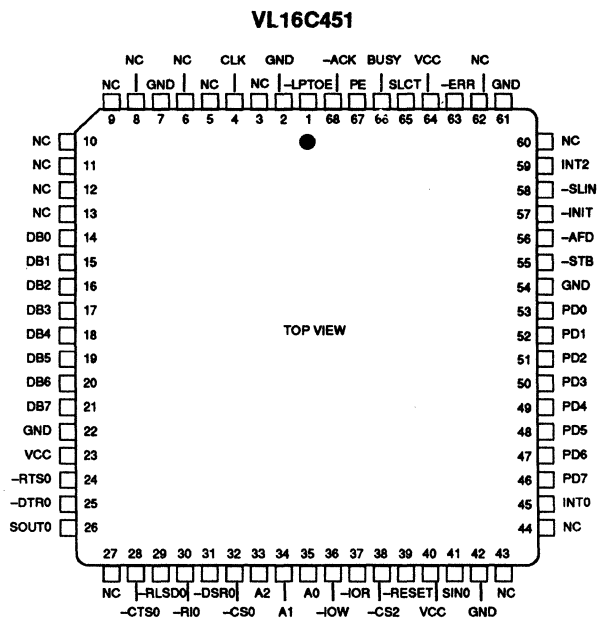
The VL16C451 also provides the user with a fully bidirectional parallel data port that fully supports the parallel Centronics type printer. The parallel port, together with the serial port, provide IBM PC/AT-compatible computers with a single device to serve the two system ports.

A programmable baud rate generator is included that can divide the timing reference clock input by a divisor between 1 and (2^{16}–1).

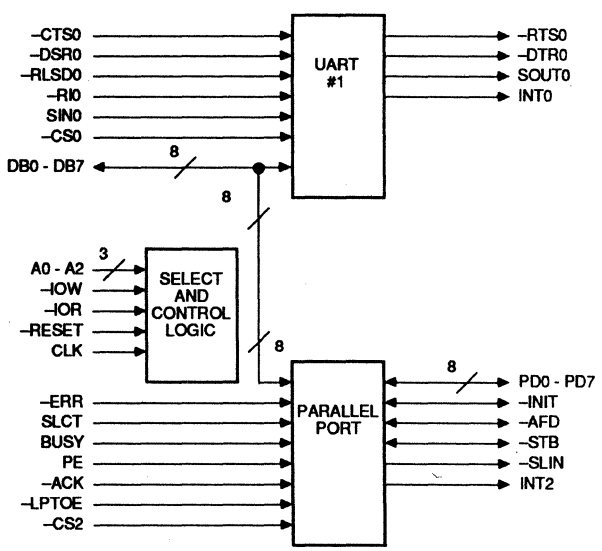
The VL16C451 is housed in a 68-pin plastic leaded chip carrier.

VLSI Technology

PIN DIAGRAM



BLOCK DIAGRAM



ORDER INFORMATION

Part Number	Maximum Clock Frequency	Package
VL16C451-QC	3.1 MHz	Plastic Leaded Chip Carrier (PLCC)

Note: Operating temperature range is 0°C to +70°C.

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VL16C452

DUAL ASYNCHRONOUS COMMUNICATIONS ELEMENT

FEATURES

- IBM PC/AT-compatible
- Dual-channel version of VL16C450
- Centronix printer interface
- Independent control of transmit, receive, line status and data set interrupts on each channel
- Individual modem control signals for each channel
- Programmable serial interface characteristics for each channel:
  - 5-, 6-, 7- or 8-bit characters
  - Even-, odd- or no-parity bit generation and detection
  - 1, 1 1/2 or 2 stop bit generation
- Three-state TTL drive for the data and control bus on each channel

DESCRIPTION

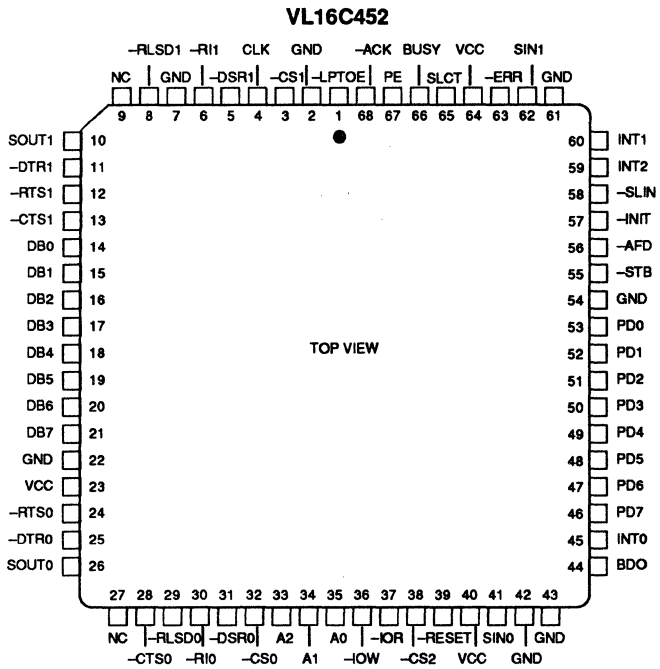
The VL16C452 is an enhanced dual-channel version of the popular VL16C450 asynchronous communications element (ACE). The device serves two serial input/output interfaces simultaneously in microcomputer- or microprocessor-based systems. Each channel performs serial-to-parallel conversion on data characters received from peripheral devices or modems, and parallel-to-serial conversion on data characters transmitted by the CPU. The complete status of each channel of the dual ACE can be read at any time during functional operation by the CPU. The information obtained includes the type and condition of the transfer operations being performed, and error conditions.

In addition to its dual communications interface capabilities, the VL16C452 provides the user with a fully bidirectional parallel data port that fully supports the parallel Centronics type printer. The parallel port, together with the two serial ports, provide IBM PC/AT-compatible computers with a single device to serve the three system ports.

A programmable baud rate generator is included that can divide the timing reference clock input by a divisor between 1 and (2^{16} –1).

The VL16C452 is housed in a 68-pin plastic leaded chip carrier.

PIN DIAGRAM



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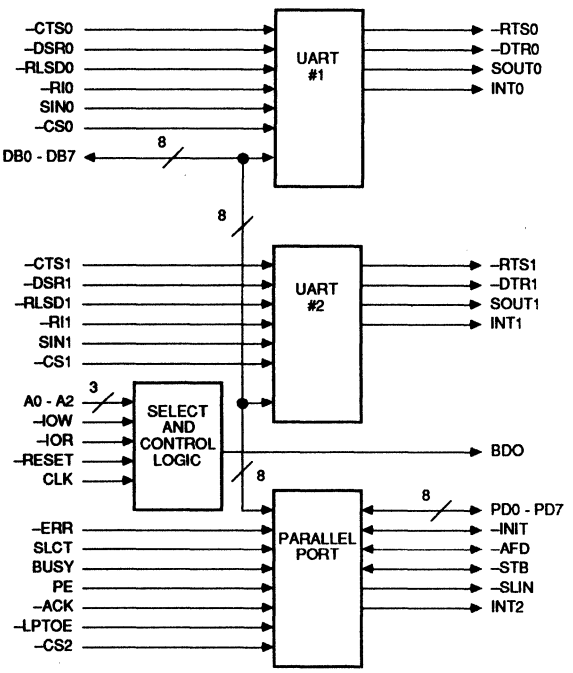

ORDER INFORMATION

Part Number	Maximum Clock Frequency	Package
VL16C452-QC	3.1 MHz	Plastic Leaded Chip Carrier (PLCC)

Note: Operating temperature range is 0°C to +70°C.

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VL16C454

QUAD ASYNCHRONOUS COMMUNICATIONS ELEMENT

FEATURES

- IBM PC/AT-compatible
- Quad-channel version of VL16C450
- Independent control of transmit, receive, line status and data set interrupts on each channel
- Individual modem control signals for each channel
- Programmable serial interface characteristics for each channel:
  - 5-,6-,7- or 8-bit characters
  - Even-, odd- or no-parity bit generation and detection
  - 1, 1 1/2 or 2 stop bit generation
- Three-state TTL drive capabilities for bidirectional data bus and control bus on each channel

DESCRIPTION

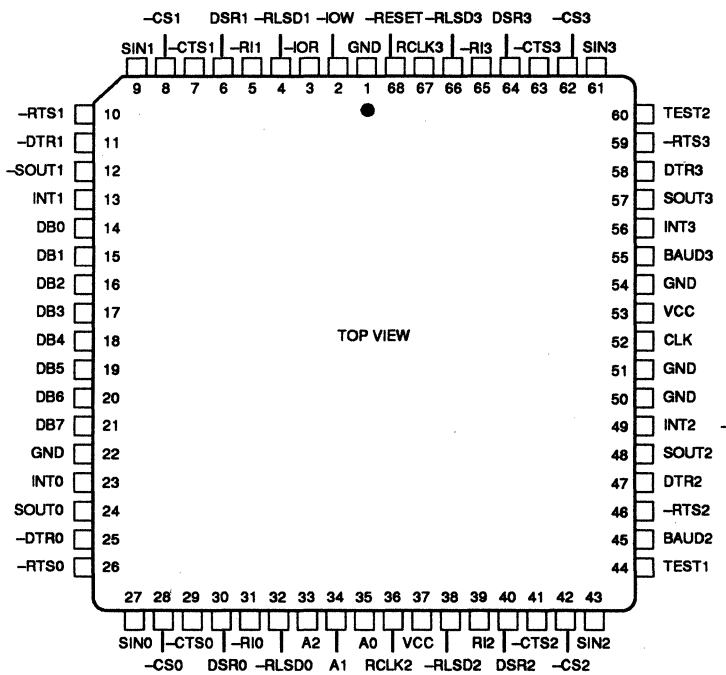
The VL16C454 is an enhanced quad-channel version of the popular VL16C450 asynchronous communications element (ACE). The device serves four serial input/output interfaces simultaneously in microcomputer- or microprocessor-based systems. Each channel performs serial-to-parallel conversion on data characters received from peripheral devices or modems, and parallel-to-serial conversion on data characters transmitted by the CPU. The complete status of each channel of the quad ACE can be read at any time during functional operation by the CPU. The information obtained includes the type and condition of the transfer operations being performed, and error conditions.

A programmable baud rate generator is included that can divide the timing reference clock input by a divisor between 1 and (2^{16} –1).

The VL16C454 is housed in a 68-pin plastic leaded chip carrier.

PIN DIAGRAM

VL16C454



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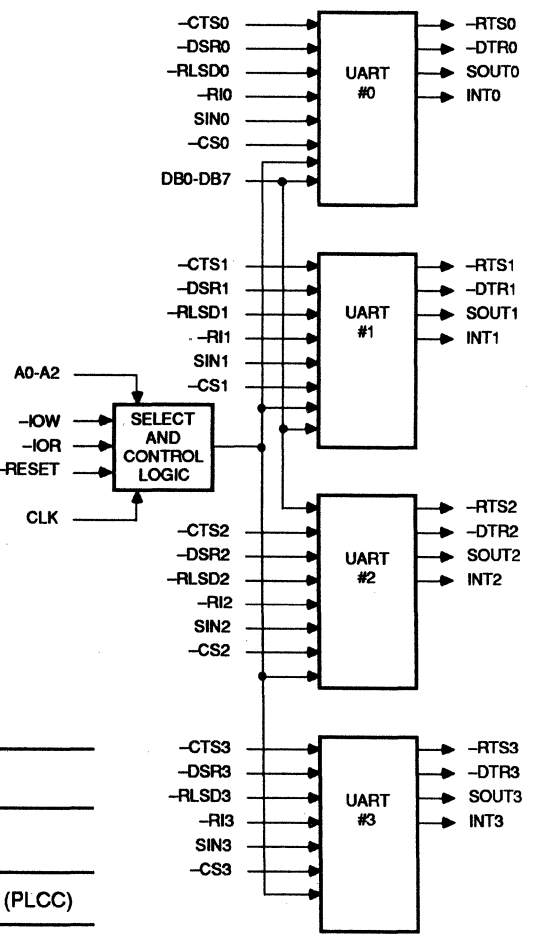

ORDER INFORMATION

Part Number	Maximum Clock Frequency	Package
VL16C454-QC	3.1 MHz	Plastic Leaded Chip Carrier (PLCC)

Note: Operating temperature range is 0°C to +70°C.

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VL16C550

ASYNCHRONOUS COMMUNICATIONS ELEMENT WITH FIFOs

FEATURES

- Fully compatible with VL16C450 ACE
- 16 byte FIFO reduces CPU interrupts
- Full double buffering
- Modem control signals include –CTS, –RTS, –DSR, –DTR, –RI and –DCD
- Programmable serial characteristics:
  - 5-, 6-, 7- or 8-bit characters
  - Even-, odd-, or no-parity bit generation and detection
  - 1, 1 1/2 or 2 stop bit generation
  - Baud rate generation (DC to 56K baud)
- Independent control of transmit, receive, line status, data set interrupts, FIFOs
- Full status reporting capabilities
- Three-state, TTL drive capabilities for bidirectional data bus and control bus

DESCRIPTIONS

The VL16C550 is an asynchronous communications element (ACE) that is functionally equivalent to the VL16C450, and additionally incorporates a 16 byte FIFO. The FIFOs are available on both the transmitter and receiver, and can be activated by placing the device in the FIFO mode. After a reset, the registers of the VL16C550 are identical to those of the VL16C450.

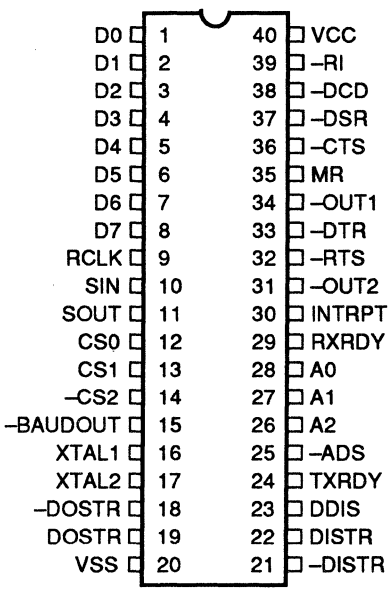
Improved VL16C550 specifications provide compatibility with most newer state-of-the-art CPUs. The VL16C550 serves as a serial data input/output interface in microcomputer systems. It performs serial-to-parallel conversion on data characters received from peripheral devices or modems, and parallel-to-serial conversion on data characters transmitted by the CPU. In the FIFO mode, FIFOs are enabled permitting 16 bytes to be stored in both transmit and receive mode. The FIFOs also provide three bits per byte of error data in the receiver FIFO. The complete status of the VL16C550 can be read at any time during functional operation by the CPU. The information obtained includes the type and condition of the transfer operations being performed, and error conditions involving parity, overrun, framing, or break interrupt.

A programmable baud rate generator is included that can divide the timing reference clock input by a divisor between 1 and $(2^{16}-1)$.

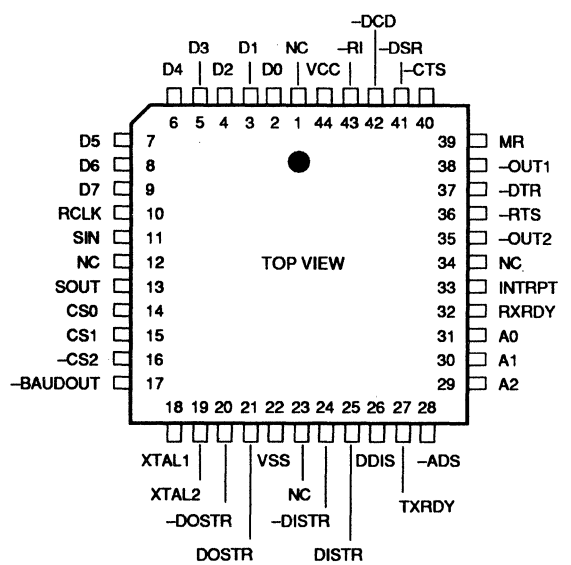
The VL16C550 ACE with FIFOs is available in plastic DIP as well as a PLCC.

PIN DIAGRAMS

VL16C550



VL16C550



ORDER INFORMATION

Part Number	External Clock Frequency	Package
VL16C550-PC VL16C550-QC	3.1 MHz	Plastic DIP Plastic Leaded Chip Carrier (PLCC)

Note: Operating temperature range is 0°C to +70°C.

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VL53C80

SMALL COMPUTER SYSTEM INTERFACE (SCSI)

FEATURES

SCSI INTERFACE

- Interface to 1.5M bps (asynchronous)
- Supports initiator and target roles
- Parity generation with optional checking
- Arbitration support
- Direct control of all bus signals
- High current outputs drive SCSI bus

MPU INTERFACE

- Memory or I/O mapped interface
- DMA of programmed I/O
- Normal or block mode DMA
- Optional MPU interrupts

DESCRIPTION

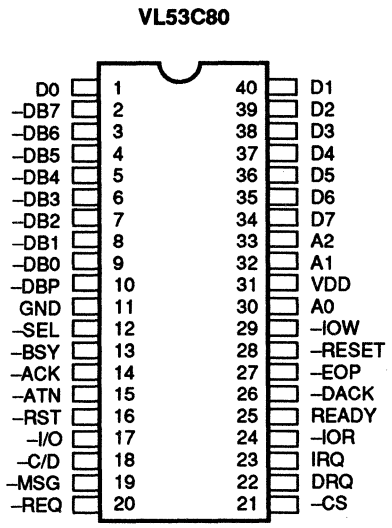
The VLSI Technology VL53C80 SCSI device is a 40-pin CMOS device designed to accommodate the Small Computer Systems Interface (SCSI) as defined by the ANSI X3T9.2 committee. The VL53C80 operates as both the initiator and the target and can therefore be used in host adapter, host port, and formatter designs. This device supports arbitration, including reselection. Special high-current open-collector output drivers, capable of sinking 48 mA at 0.5 V, connect directly to the SCSI bus.

The VL53C80 interfaces with the system microprocessor as a peripheral.

The device is controlled by reading and writing several internal registers which are addressed as standard or memory mapped I/O. DMA transfers require little CPU support because the VL53C80 controls the necessary handshake signals. The VL53C80 interrupts the MPU when it detects a bus condition requiring service. Normal and block mode DMA is also available to match several popular DMA controllers.

The VL53C80 is available in a 40-pin plastic DIP as well as a 44-pin plastic leaded chip carrier.

PIN DIAGRAM



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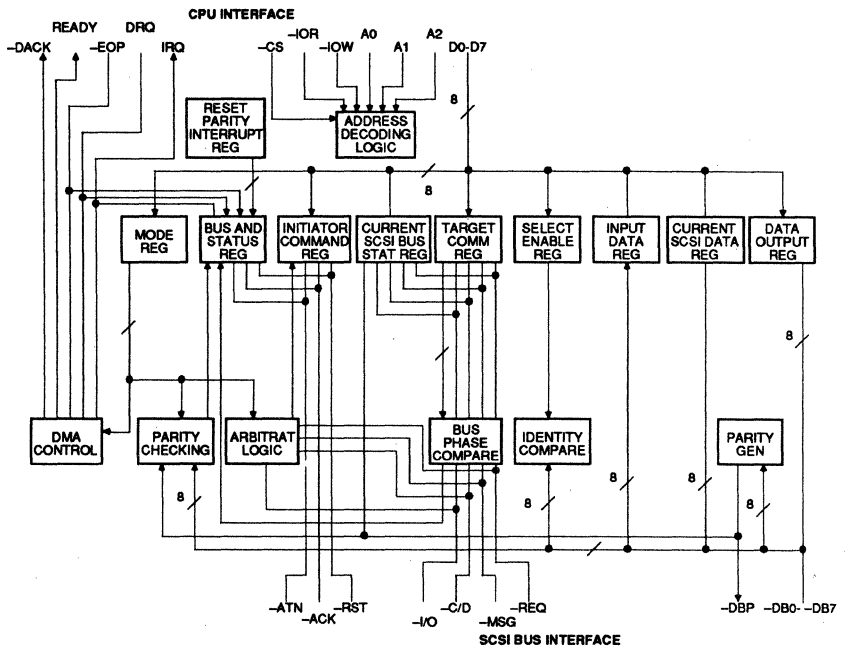

ORDER INFORMATION

Part Number	Package
VL53C80-PC	Plastic DIP
VL53C80-QC	Plastic Leaded Chip Carrier (PLCC)

Note: Operating temperature range is 0°C to +70°C.

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VL7C212A • VL7C312 •VL7C412

300/1200 BIT-PER-SECOND MODEM (VL7C312, VL7C412 WITH PIN-PROGRAMMABLE RECEIVER GAIN) (VL7C412 WITH SINGLE 5-VOLT POWER SUPPLY)

FEATURES

- FSK and PSK modulators and demodulators, high-band and low-band filters with compromise amplitude and group delay equalizers
- Built-in call progress mode and tone generators for DTMF V.21 and V.22 guard tones
- Bell 212A and CCITT V.21 and V.22 compatible; V.22 notch filters included
- Serial control interface
- Programmable audio output port
- Analog, digital, and remote digital loopback capabilities
- 24-pin DIP and 28-pin plastic leaded chip carrier available
- High level of integration provides a highly cost effective 300/1200 bit-per-second modems
- Eliminates external components, easing design of intelligent modems
- Usable in North American and European modem designs
- Simple board layout
- Simple speaker interface for monitoring phone line
- Testable signal path
- Reduced board area
- VL7C412 is a direct replacement for Sierra SC11016
- VL7C312 is a direct replacement for Sierra SC11015
- VL7C212A is a direct replacement for Sierra SC11004 and SC11014
- VL7C312 and VL7C412 pin programmable receiver gain
- VL7C412 has single 5 V power supply with power down by pin or code

DESCRIPTION

The VL7C212A, VL7C312 and VL7C412 are complete 300/1200 bit-per-second modems. All of the signal processing functions needed for a full duplex, 300/1200 bit-per-second 212A (V.21 or V.22) modem, including both FSK and PSK modulators and demodulators and the high-band and low-band filters, are integrated on a single chip. They are built using a three-micron CMOS double-polysilicon process that allows analog and digital functions to be combined on the same chip. This design includes capabilities for progress monitoring and for generating DTMF as well as V.21 or V.22 guard tones. The two-to-four wire hybrid is also included, simplifying the interface to a DAA. Each also includes analog loopback and remote digital loopback functions for self-testing.

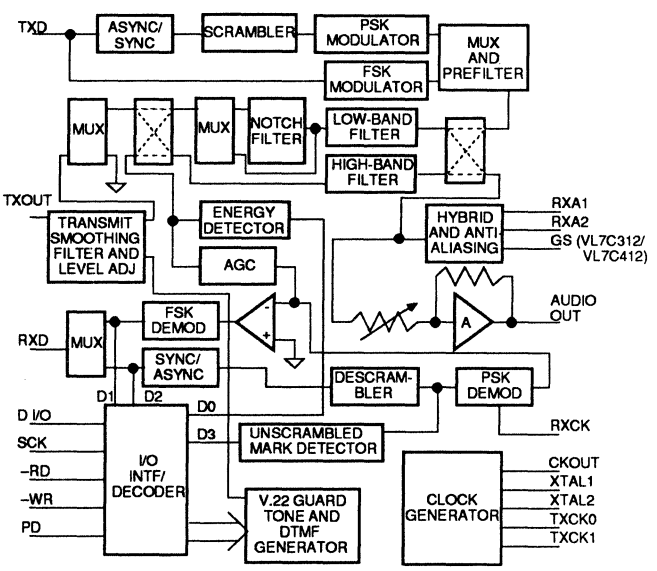
VLSI Technology

ORDER INFORMATION

Part Number	Package
VL7C212A-PC	Plastic DIP
VL7C212A-QC	Plastic Leaded Chip Carrier (PLCC)
VL7C312-PC	Plastic DIP
VL7C312-QC	Plastic Leaded Chip Carrier (PLCC)
VL7C412-PC	Plastic DIP
VL7C412-QC	Plastic Leaded Chip Carrier (PLCC)

Note: Operating temperature range is 0°C to +70°C.

BLOCK DIAGRAM



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VLSI TECHNOLOGY, INC.

VL7C213 • VL7C215 • VL7C413

PARALLEL BUS MODEM CONTROLLERS

FEATURES

- Direct interface to single-chip, single-supply modems
- Complete Hayes AT command set in firmware
- Built-in UART
- Direct IBM PC bus interface
- IORDY pin for use on high-speed buses on VL7C215, VL7C413
- Complete intelligent modem in two ICs
- Compatible with industry-standard software
- Automatic power up/down control of VL7C412 (VL7C413 only)
- VL7C413 replaces Sierra SC11037
- VL7C215 replaces Sierra SC11017
- VL7C213 replaces Sierra SC11007

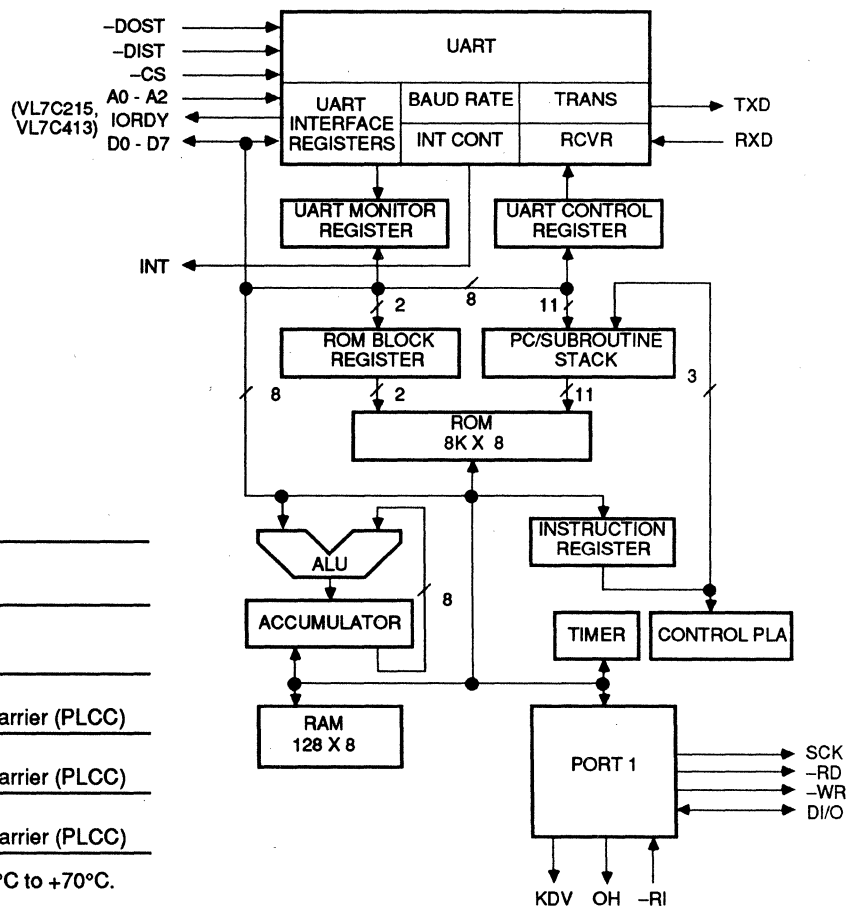
DESCRIPTION

The VL7C413 Parallel Bus Modem Controller is specifically designed to control the VL7C412 single-chip, 300/1200 bit-per-second modem. The VL7C213 and VL7C215 control the VL7C212A 300/1200 bit-per-second modem. Built with an advanced two-micron CMOS process, each provides a highly cost effective solution for interfacing a modem IC to a system bus. When connected to its modem, with the addition of a data access arrangement (DAA), each controller implements a Hayes-type smart modem for board-level, integral-modem applications. Because each controller fully emulates the functionality of the VL82C50 UART and includes data bus transceivers, they can be directly interfaced to a computer's parallel data bus (in particular to the bus of the IBM PC, XT or AT). All of the popular communications software written for the PC will work with each chip set. In addition to including the functionality of the VL82C50 UART, the VL7C413 contains an 8-bit microprocessor, 8K by 8 bits of ROM and 128 by 8 bits of RAM.

The VL7C413 automatically controls the power up/down feature of the VL7C412 to maintain lowest possible system power consumption.

For specific high-volume applications, the control program can be modified by VLSI to include additional command functions.

BLOCK DIAGRAM



ORDER INFORMATION

Part Number	Package
VL7C213-PC	Plastic DIP
VL7C213-QC	Plastic Leaded Chip Carrier (PLCC)
VL7C215-PC	Plastic DIP
VL7C215-QC	Plastic Leaded Chip Carrier (PLCC)
VL7C413-PC	Plastic DIP
VL7C413-QC	Plastic Leaded Chip Carrier (PLCC)

Note: Operating temperature range is 0°C to +70°C.

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VLSI TECHNOLOGY, INC.

VL7C214 • VL7C414

STAND-ALONE MODEM INTERFACE CONTROLLERS (VL7C414 WITH AUTOMATIC MODEM POWER DOWN CONTROL)

FEATURES

- Direct interface to single chip modems
- Complete Hayes AT command set in firmware
- Built-in UART for RS232C interface
- Two-micron CMOS process
- 28-pin DIP or PLCC package
- Complete intelligent modem in two ICs
- Compatible with industry-standard software
- Low power consumption
- VL7C214 replaces Sierra SC11008
- VL7C414 replaces Sierra SC11028

DESCRIPTION

The VL7C214/VL7C414 Stand-Alone Modem Interface Controllers are specifically designed to control the VL7C212A/VL7C412A single-chip, 300/1200 bit-per-second modems. Built with an advanced two-micron CMOS process, they provide a highly cost effective solution for interfacing a modem IC to a computer's RS232C port. When connected to the modem, with the addition of a data access arrangement (DAA), they implement a Hayes-type smart modem for stand-alone modem applications. All of the popular communications software written for the IBM PC will work with the two chip set. Each contains an 8-bit microprocessor, 8K by 8 bits of ROM and 128 by 8 bits of RAM. In order to support the stand-alone functionality of the device, an 8-bit switch input port allows immediate user access and manual control of the system. Either Bell 103 or CCITT V.22 may be selected in this manner.

The VL7C414 automatically controls the power up/down feature of the VL7C412 to maintain lowest possible system power consumption.

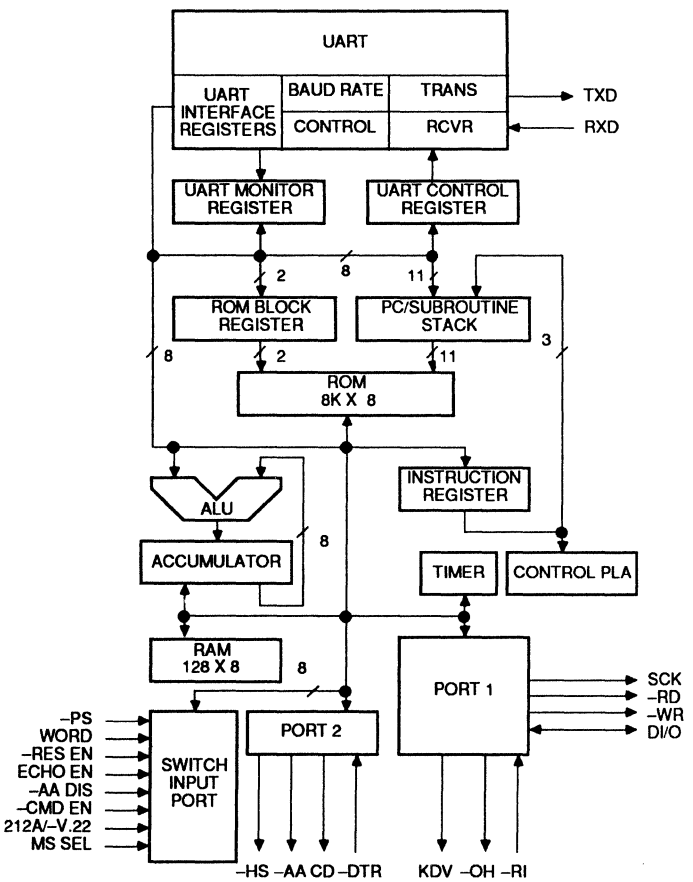
For specific high volume applications, the control program can be modified by VLSI Technology, Inc. to include additional commands and functions.

ORDER INFORMATION

Part Number	Package
VL7C214-PC	Plastic DIP
VL7C214-QC	Plastic Leaded Chip Carrier (PLCC)
VL7C414-PC	Plastic DIP
VL7C414-QC	Plastic Leaded Chip Carrier (PLCC)

Note: Operating temperature range is 0°C to +70°C.

BLOCK DIAGRAM



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VL7C224A

2400 BIT-PER-SECOND MODEM

FEATURES

- Complete 2400 bit-per-second modem conforming to V.22 bis specifications
- Compatible with CCITT V.22 bis, V.22, V.21 and BELL 212A and 103 standards
- Integrated DTMF/Guard Tone Generator, call progress monitor and contains an on-chip hybrid
- Analog, digital and remote digital loopback
- Programmable audio output port
- Three-micron CMOS technology
- DIP or PLCC package
- Audio interface for phone line monitoring
- High-level of integration provides for economical 2400 bit-per-second modem solution
- Broadly adaptable to established worldwide standards at 2400, 1200 and 300 bits-per-second
- Minimizes need for external components simplifying design of intelligent modems
- Testable signal path diagnostics
- Low power consumption

DESCRIPTION

The VL7C224A is a complete 2400 bit-per-second modem IC containing all modem functions except the adaptive equalizer. It is used in conjunction with an external controller such as the VL7C235 (for parallel bus applications), the VL7C245 (for RS232 applications) or a general purpose microcontroller such as 8096, to implement a 2400 bps full duplex modem, compatible with the CCITT V.22 bis recommendation. The controller performs all modem control and handshaking functions as well as the adaptive equalization.

The VL7C224A operates in 2400 bps QPSK/QAM and 1200 bps PSK as well as 0 to 300 baud FSK modes, compatible with Bell 103 and 212A as well as CCITT V.21, V.22 and V.22 bis standards. When used with the VL7C225, VL7C235, or VL7C245 controllers, the VL7C224A becomes an intelligent modem controlled by the industry standard "AT" command set. The interface between the VL7C224A modem and the controller (either the 8096 or the VL7C225/235/245) is a standard microcontroller interface that easily connects to an EEPROM for permanent storage of configuration settings and phone numbers.

ORDER INFORMATION

Part Number	Package
VL7C224A-PC	Plastic DIP
VL7C224A-QC	Plastic Leaded Chip Carrier (PLCC)

Note: Operating temperature range is 0°C to +70°C.

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VL7C225 • VL7C235 • VL7C245

2400 BIT-PER-SECOND MODEM ADVANCED COPROCESSOR FAMILY

FEATURES

- Direct interface to the VL7C224A single-chip modem
- Complete "AT" command set in firmware
- Built-in 82C50B UART equivalent
- Direct IBM PC bus interface
- External ROM/RAM addressable
- 2400 bps intelligent modem using just two chips
- Compatible with industry standard software
- Two-micron CMOS technology
- No external buffers required

DESCRIPTION

The VL7C225 family are specialized controllers that interface directly to the VL7C224A Modem to form a 2400 bps full duplex intelligent modem. The two-chip set performs all the modem functions as well as automatic control features compatible to the Hayes "AT" Command Set. The chip set is compatible to the CCITT V.22 bis with V.22 fallback, Bell 212A with 103 fallback, as well as the V.21 standard.

The VL7C235 interfaces to a parallel system bus, such as the bus in the IBM PC, while the VL7C245 interfaces to an RS232 port.

The controller receives 8-bit signal samples from the VL7C224A and performs adaptive equalization, carrier phase recovery, data decode, and descrambling.

The VL7C225, VL7C235, and VL7C245 have identical hardware. However, they can be configured as a parallel (VL7C235), or serial (VL7C245) device by programming the internal ROM. The VL7C225 is the ROM-less version and is available in a 68-pin PLCC package. It is intended for use with external memory to accommodate customized firmware.

These controllers use a bit slice core processor to perform digital signal processing (DSP) and the control function. Its instruction set is a fast subset of the 8096 instruction set.

ORDER INFORMATION

Part Number	Package
VL7C225-QC	Plastic Leaded Chip Carrier (PLCC)
VL7C235-PC	Plastic DIP
VL7C235-QC	Plastic Leaded Chip Carrier (PLCC)
VL7C245-PC	Plastic DIP
VL7C245-QC	Plastic Leaded Chip Carrier (PLCC)

Note: Operating temperature range is 0°C to +70°C.

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VLSI TECHNOLOGY, INC.

VL82CPCAT

12 MHz PC/AT-COMPATIBLE CHIP SET

FEATURES

- Fully compatible with IBM PC/AT-type designs
- High-integration five-chip set
- Reduces non-memory system device count from 88 to 17
- Supports 12 MHz processor clock
- Devices are available as "cores" for user-specific designs
- All devices designed in CMOS for low power consumption

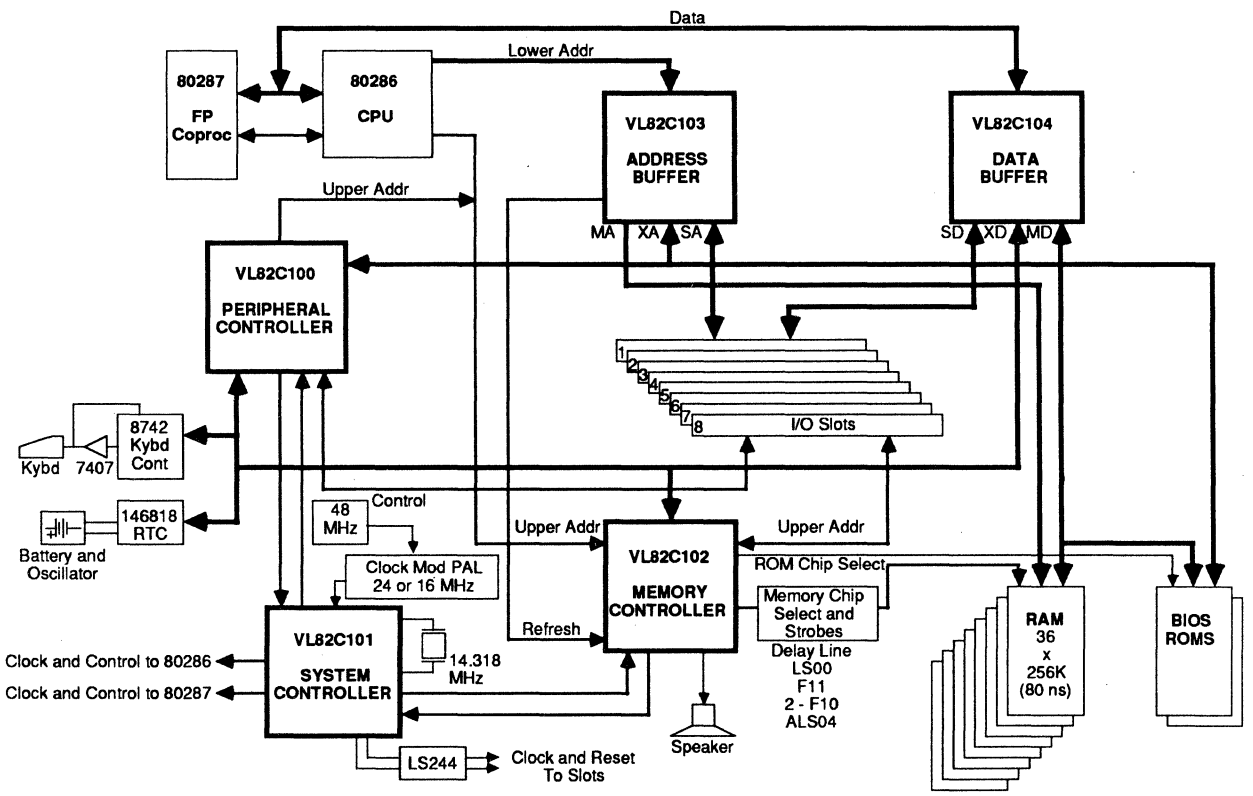
DESCRIPTION

The IBM PC/AT-compatible chip set from VLSI Technology, Inc. supports 256K and 1-Megabit dynamic RAMs, and is utilized in systems with clock speeds up to 12 MHz. The chip set provides the IBM PC/AT-compatible low-cost board design solution. Further, since the devices were designed using VLSI's design tools, the devices can be quickly modified for use as cores in user-specific designs.

The five-device chip set has been designed using the hightest integration consistent with economic and reliable system design. The VL82C103 Address Buffer and VL82C104 Data Buffer are offered in separate packages, although their circuitry is relatively small. If they were offered as a single device, the pin count would be extremely high, or some performance degradation would occur.

The devices are manufactured with VLSI's advanced high-performance CMOS process and all five are available in a JEDEC-standard 84-pin plastic leaded chip carrier (PLCC) package.

BLOCK DIAGRAM



ORDER INFORMATION

Part Number	Package
VL82CPCAT-QC	12 MHz, 0 Wait State, Five Device Chip Set

Note: Operating temperature range is 0°C to +70°C.

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VLSI TECHNOLOGY, INC.

VL82CPCAT-16

16 MHz PC/AT-COMPATIBLE CHIP SET

VLSI Technology

FEATURES

- Up to 16 MHz system operation
- Zero wait state DRAM accesses
- Norton SI '87 benchmark rating of 18.7
- Allows 8M byte RAM on mother-board
- Built-in clock modulation for maximum slot compatibility with expansion boards
- Shadow RAM for zero wait state BIOS® accesses
- "Hot Reset" support for 80286 allows maximum performance under new OS/2®
- LIM EMS 4.0® implementation available in software
- All devices implemented in CMOS
- Available as cores for user-specific designs

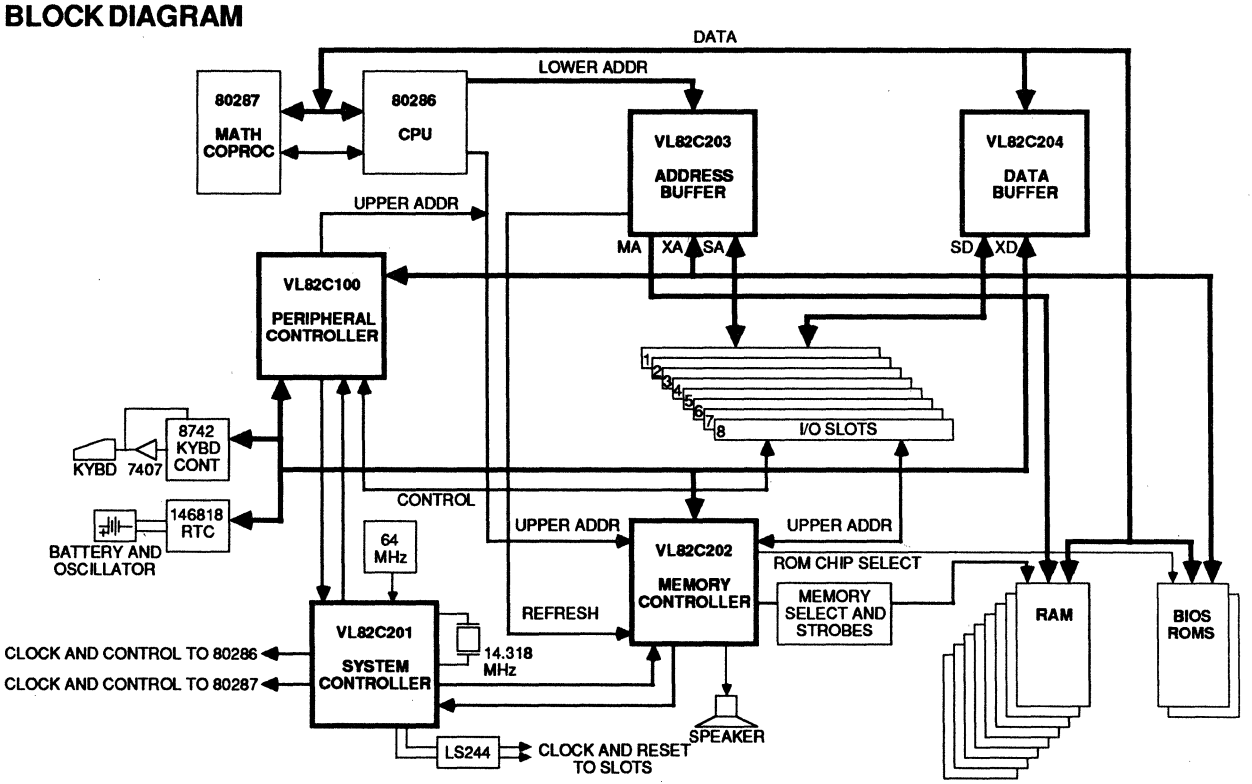
DESCRIPTION

The VLSI VL82CPCAT-16 five device 16 MHz zero wait state chip set is a fully PC/AT-compatible solution that offers significant cost and performance advantages over discrete and other implementations. The VL82CPCAT-16 can operate at 16 MHz zero wait states with 60 ns DRAMs. Other performance options with the VL82PCAT-16 include operation at 16 MHz one wait state with 100 ns DRAMs and 12 MHz zero wait states with 80 ns DRAMs.

15 non-memory ICs implement a PC/AT-compatible system versus the 88 non-memory ICs required for discrete solutions.

New features include clock modulation function to allow dynamic system speed to half system speed on any I/O or slot access, and "Shadow RAM" which duplicates the ROM space in upper RAM space and provides fast zero or one wait state BIOS accesses. The "Hot Reset" feature provides streamlined operation of the new OS/2 operating system and allows the software implementation of LIM EMS 4.0 which improves the performance of applications under DOS with large DRAM subsystems.

BLOCK DIAGRAM



ORDER INFORMATION

Part Number	Package
VL82CPCAT-16QC	16 MHz, 0 Wait State, Five Device Chip Set

Note: Operating temperature is 0°C to +70°C.

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VLSI TECHNOLOGY, INC.

VL82C031 • VL82C032 • VL82C037

IBM PS/2® MODEL 30-COMPATIBLE CHIP SET AND VGA

FEATURES

- Supports 8086 or V30 CPU speed at 8 MHz or 10 MHz with zero wait state using 150 ns DRAMs
- Generates programmable fast and normal timing for PC memory
- Provides either DRAM or SRAM control
- Supports up to 8M bytes of expanded memory
- Supports 256K or 1M bit DRAMs on LIM EMS 4.0® memory
- Arbitrates the system bus among the CPU, DMA, math coprocessor, and DRAM memory refresh cycle
- Provides four channels of 8 MHz DMA as well as burst mode
- RAM pin available to select static of dynamic memory interface
- Power down mode

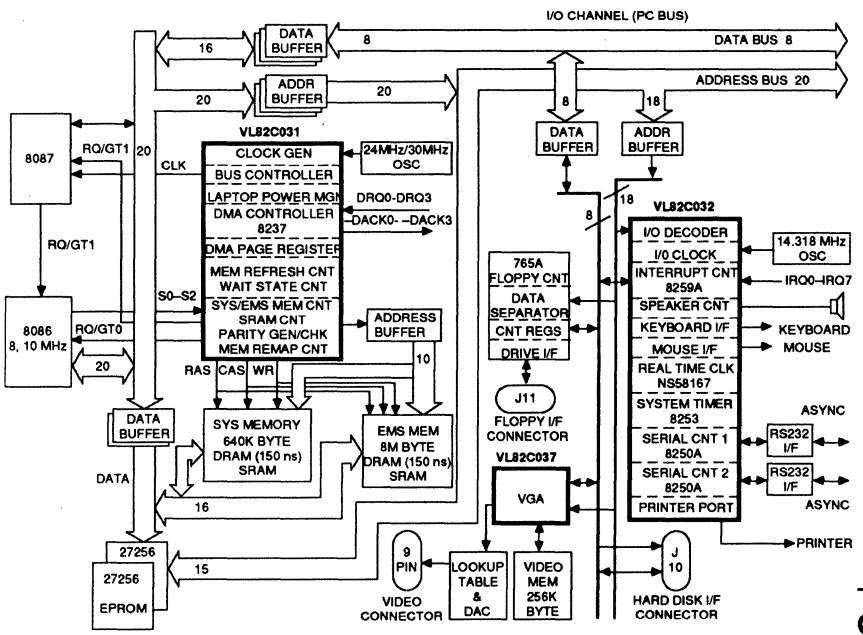
DESCRIPTION

The CMOS VL82C031 is the System Controller device in the two-chip VLSI PS/2 Model 30-compatible chip set. The other device is the VL82C032 I/O Controller.

The chip set integrates logic and functions on PS/2 Model 30-compatible systems to the point of reducing the printed circuit board device count by half, when memories are excluded. Further, while offering complete compatibility with the PS/2 Model 30-compatible system, the VLSI chip set improves system performance by allowing 10 MHz operation with no "wait states" (using 150 ns DRAMS), supports an additional 8M bytes of memory using LIM EMS (Expanded Memory Specification) 4.0, and controls system speed as necessary for optimum performance.

A third device, the VL82C037 VGA, Video Graphics Controller, is also used in the PS/2 Model 30-compatible system and provides high resolution graphics of 800 x 600 elements with 16 colors. Graphic capabilities of this resolution are usually found only on more expensive systems.

SYSTEM DIAGRAM



Notes: Operating temperature range is 0°C to +70°C.
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LIM EMS 4.0® is a registered trademark of Lotus Development Corp., Intel Corp., and Microsoft Corp.

ORDER INFORMATION

Part Number	Package
VL82CPS30-FC	Plastic Flatpack
VL82C037-FC	Plastic Flatpack

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VL82C205

PAGE-MODE ACCESS CONTROLLER

FEATURES

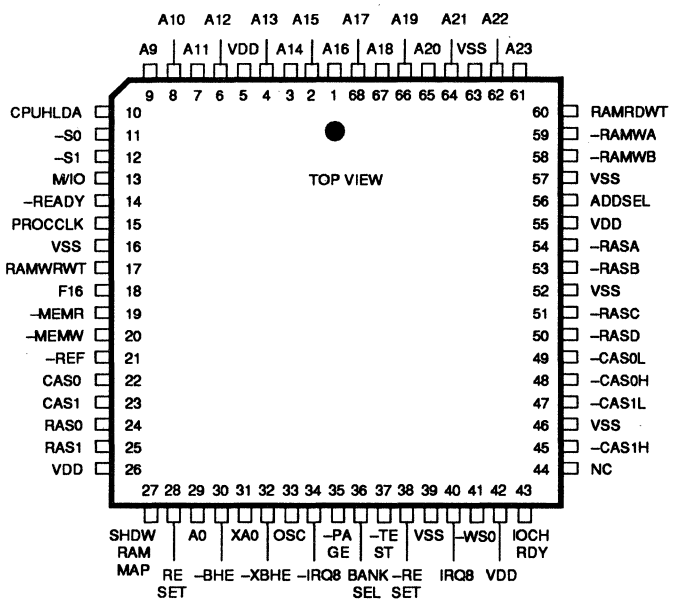
- Supports 16 MHz 80286 operation with 100 ns DRAMs
- Supports page-mode DRAM access for PC/AT-compatible systems
- Speed upgrades to 20 MHz in the future
- Companion to VL82CPCAT-16, 16 MHz PC/AT-compatible chip set
- 11 chip PC/AT implementation (non-memory chips)
- 0.6 wait state operation
- Low power CMOS technology
- 68-pin PLCC package

DESCRIPTION

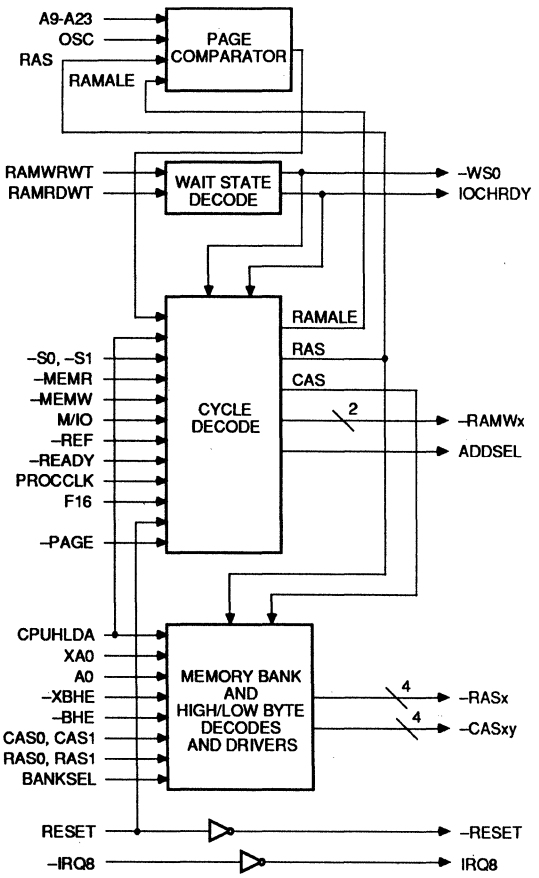
The VL82C205 is a page-mode memory controller for the VLSI, VL82CPCAT-16, 16 MHz PC/AT-compatible chip set. This chip, in addition to the other five chips from the VLSI chip set, allows page-mode memory cycles to be run, permitting a 16 MHz processor to use standard 100 ns DRAMs and still have only 0.6 wait states.

When using page-mode, accesses that are within 512 words of the last access are performed with zero wait states, accesses that are outside that range are performed in one to two wait states.

PIN DIAGRAM



BLOCK DIAGRAM



ORDER INFORMATION

Part Number	Clock Freq.	Package
VL82C205-16QC	16 MHz	Plastic Leaded Chip Carrier (PLCC)

Note: Operating temperature is 0°C to +70°C.

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VLSI TECHNOLOGY, INC.

VL82C389

MESSAGE-PASSING COPROCESSOR MULTIBUS® II

FEATURES

- Full-function, single-chip interface to Parallel System Bus (iPSB)
- Implements full message-passing protocol on iPSB bus
- Offloads managing iPSB bus arbitration, transfer and exception cycles from local CPU
- Maximizes performance on iPSB bus and local on-board bus
- Simplifies highly function interconnect space implementations for both local and iPSB buses
- Processor-independent interface to iPSB bus
- Supports co-existence of dual-port and message-passing architectures
- Supports limited Central Services Module (CSM) functions

DESCRIPTION

The VL82C389 Message-Passing Coprocessor (MPC) provides a high-integration interface solution for the Parallel System Bus (iPSB) of the Multibus II architecture. The device integrates the logic necessary to implement a full bus interface solution, including support for message passing and interconnect spaces, as well as memory and I/O references on the iPSB bus. In addition, the MPC is designed to simplify implementation of dual-port memory functions for those designs that must co-exist with message passing, maintaining existing software bases.

The message address space in the Multibus II architecture has been defined to provide a high-performance interprocessor communication mechanism for multiprocessor systems. By performing the message space interface, the VL82C389 MPC offloads the interprocessor communication tasks from the local on-board CPU, which decouples the local bus activities from the iPSB bus activities. Decoupling these two functions eliminates an interface bottleneck present in traditional dual-port architectures. The bottleneck is a result of having a dual-port architecture that requires a tight coupling between a processor and some shared memory resource of limited size. Unfortunately, as the number of processors increases, the dual-port structure degrades system performance even more dramatically.

Using the MPC component to decouple these resources yields several enhancements to system performance. For example, resources on the local processor bus and Parallel System Bus are not held in wait states while arbitration for other resources is performed. In addition, each transfer can occur at the full bandwidth of the associated bus. The benefit of this is the increased overall system performance that results from processors being able to process other tasks in parallel, with message transfers being handled by the MPC component.

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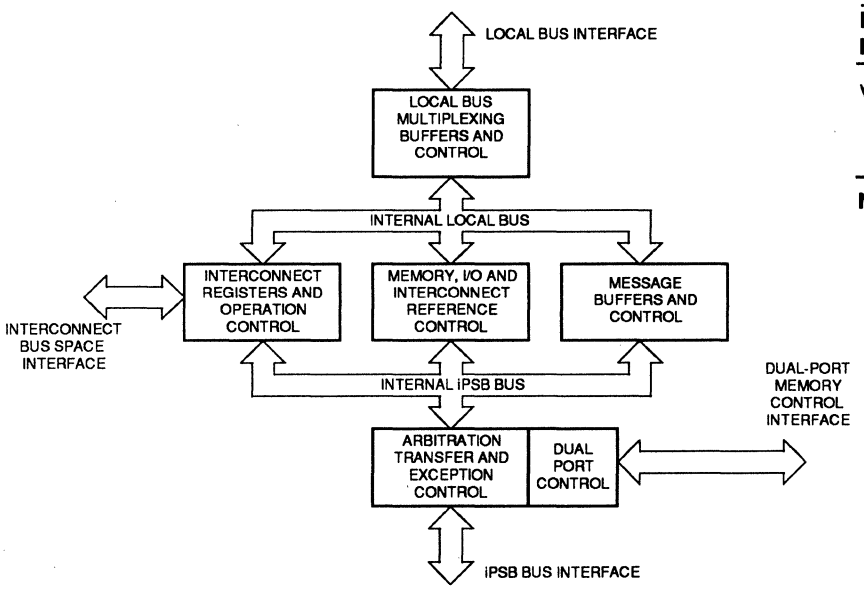
BLOCK DIAGRAM



ORDER INFORMATION

Part Number	Package
VL82C389-GC	Ceramic Pin Grid Array (PGA)

Note: Operating temperature range is 0°C to +70°C.

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VL83C11

GENERAL PURPOSE (SCSI) BUS TRANSCEIVER

FEATURES

- Meets full Small Computer Systems Interface (SCSI) specifications for system cables up to six meters long
- Fully buffered, bidirectional data and control buses
- Interfaces directly to NCR 5386 family
- Can be used with other interfaces requiring a 48 mA drive
- Low cost
- Two-micron CMOS technology
- Housed in a standard 52-pin PLCC

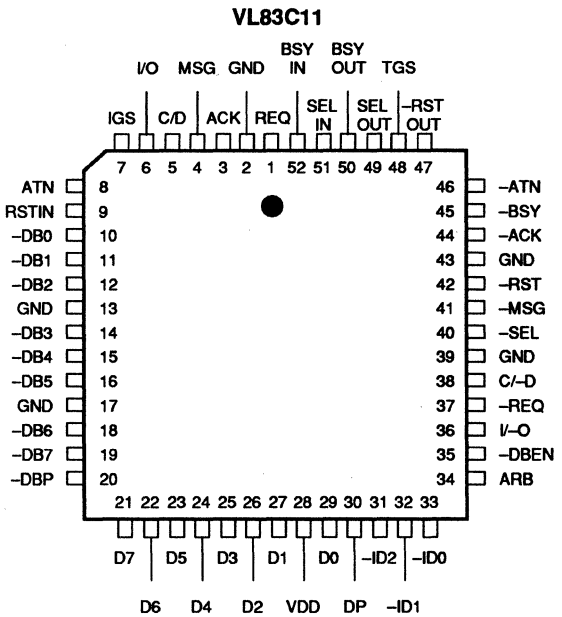
DESCRIPTION

The VL83C11 General Purpose Bus Transceiver Chip, is a two-micron CMOS device designed as a 48 mA bus transceiver chip for all of the Small Computer System Interface (SCSI) bus signals. It incorporates high current single-ended drivers for the SCSI bus. The VL83C11 is specifically intended to be used with the NCR 53C86 SCSI Protocol Controller family. It interfaces directly to those devices, with no additional circuits required. It can be used with other interfaces where a general purpose 48 mA bus transceiver is required. Logical and electrical flexibility also allow its use as a general purpose interface driver/receiver chip.

The VL83C11 is functionally equivalent to the NMOS NCR 8310, but has been designed in CMOS technology. It meets the full electrical specifications of Small Computer Systems Interface (SCSI) for system cable lengths up to six meters long. Further, it has been optimized for connection to the standard SCSI connector.

The VL83C11 General Purpose Tranceiver Chip is packaged in a 52-pin plastic leaded chip carrier (PLCC).

PIN DIAGRAM



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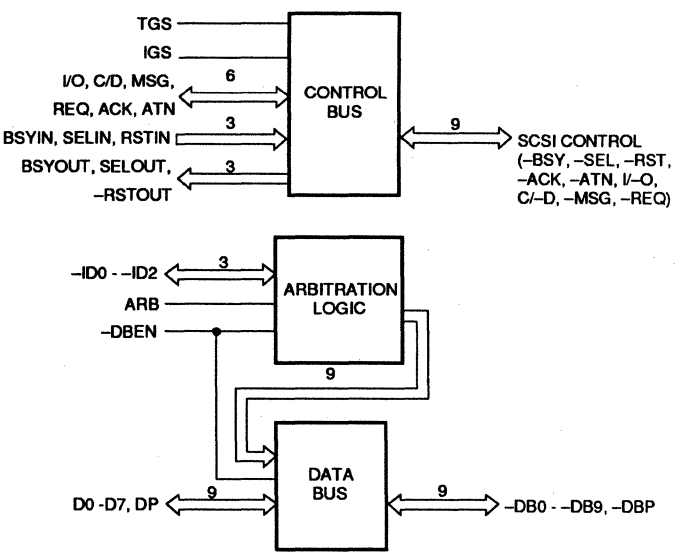

ORDER INFORMATION

Part Number	Package
VL83C11-QC	Plastic Leaded Chip Carrier (PLCC)

Note: Operating temperature range is 0°C to +70°C.

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ENHANCED SERIAL COMMUNICATIONS CONTROLLER (ESCC)

FEATURES

- Enhanced SCC functions support DMA
  - 14-bit byte counter
  - 19-bit wide FIFO
- Completely downward compatible with the NMOS 8530
- Two independent full-duplex channels
- Programmable clock factor
- Break generation and error detection
- Intelligent SDLC/HDLC
- Local loopback and auto echo modes
- Internal or external character synchronization
- Low power consuming CMOS

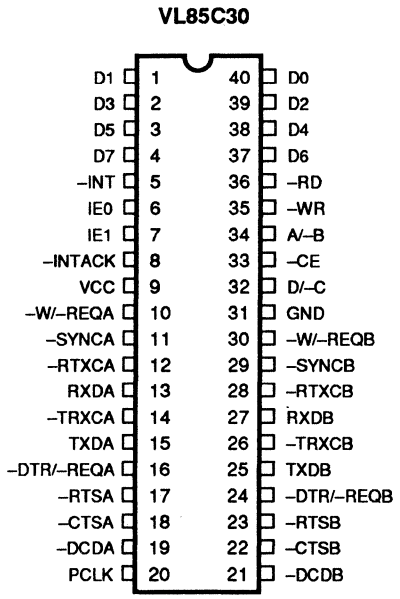
DESCRIPTION

The VL85C30 CMOS Enhanced Serial Communications Controller (ESCC) is a dual-channel, multi-protocol data communications peripheral designed for use with non-multiplexed buses. The ESCC can be software configured for a wide variety of serial communications applications. The device contains a variety of new, sophisticated internal functions, including all of the features of the NMOS 8530. In addition, the VL85C30 Enhanced SCC contains a 10 x 19-bit FIFO array and 14-bit byte counter. These features, in addition to the new higher clock frequency capabilities, allow the ESCC to be used with a direct memory access (DMA) controller.

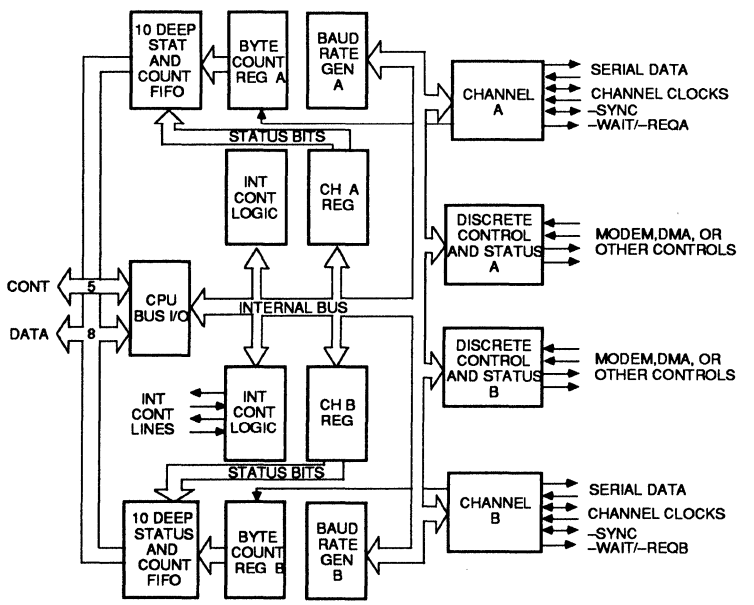
The ESCC handles asynchronous formats, such synchronous byte-oriented protocols as IBM Bisync, and such synchronous bit-oriented protocols as HDLC and IBM SDLC. This versatile device supports virtually any serial data transfer application (cassette, diskette, tape drives, etc.), including DMA.

The device can generate and check CRC codes in any synchronous mode and can be programmed to check data integrity in various modes. The ESCC also has facilities for modem controls in both channels, in addition to its Byte - Counting Register and FIFO in SDLC mode.

PIN DIAGRAM



BLOCK DIAGRAM



ORDER INFORMATION

Part Number	Clock Frequency	Package
VL85C30-8PC VL85C30-8QC	8 MHz	Plastic DIP Plastic Leaded Chip Carrier (PLCC)
VL85C30-10PC VL85C30-10QC	10 MHz	Plastic DIP Plastic Leaded Chip Carrier (PLCC)
VL85C30-12PC VL85C30-12QC	12 MHz	Plastic DIP Plastic Leaded Chip Carrier (PLCC)

Note: Operating temperature range is 0°C to +70°C.

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VLSI TECHNOLOGY, INC.

32-BIT RISC MICROPROCESSOR FAMILY

VL86C010 32-BIT RISC MICROPROCESSOR

FEATURES

- 32-bit internal architecture
- 32-bit external data bus
- 64M-byte linear address space
- Bus timing optimized for standard DRAM usage with page-mode operation
- 48M-byte/second bus bandwidth
- Simple/powerful instruction set providing an excellent high level language compiler target
- Hardware support for virtual memory systems
- Low interrupt latency for real-time application requirements
- Full CMOS implementation results in low power consumption
- 84-pin plastic leaded chip carrier (PLCC)

DESCRIPTION

The VL86C010 Acorn RISC Machine (ARM) is a full 32-bit general-purpose microprocessor designed using reduced instruction set computer (RISC) methodologies. The processor is targeted for the microcomputer, graphics, industrial and controller markets for use in stand-alone or embedded systems. Applications in which the processor is useful include laser printers, graphics engines, numerical control machines, or any other systems requiring fast real-time response to external interrupt sources and high processing throughput.

The VL86C010 features a 32-bit data bus, 27 registers of 32 bits each, a load-store architecture, a partially overlapping register set, 22.5 clocks worst-case interrupt latency, conditional instruction execution, a 26-bit linear address space and an average instruction execution rate of from five-to-six million instructions per second (MIPS). Additionally, the processor supports two addressing modes: program counter (PC) and base register relative modes. The ability to do pre- and post-indexing allows stacks and queues to be easily implemented in software. All instructions are 32 bits long (aligned on word boundaries), with register-to-register operations executing in one cycle. The two data types supported are 8-bit bytes and 32-bit words.

ORDER INFORMATION

Part Number	Clock Frequency	Package
VL86C010-10QC	10 MHz	Plastic Leaded Chip Carrier (PLCC)
VL86C010-12QC	12 MHz	Plastic Leaded Chip Carrier (PLCC)

Note: Operating temperature range is 0°C to +70°C.

VL86C110 RISC MEMORY CONTROLLER (MEMC)

FEATURES

- Drives up to 32 standard dynamic RAMs giving 4M bytes of real memory with 1M-bit devices
- Logical-to-physical address translation (32M-byte logical address space) supporting three protection levels:
  - Supervisor Mode
  - Operating System Mode
  - User Mode
- Uses fast page-mode DRAM accesses to maximize bandwidth from commodity memories
- Internal DMA address generators for video, cursor and sound data buffers
- Various ROM speeds supported (access times of 450, 325, and 200 ns)

DESCRIPTION

The memory controller (MEMC) acts as the interface between the ARM (Acorn RISC Machine) processor and other functions in the system. The four circuits in the RISC family: MEMC, ARM, VIDC (video controller), and IOC (I/O controller), can be used to implement a small computer system. MEMC uses a single clock input to derive timing information for the other components.

In addition to providing interface signals to the other controllers, MEMC generates all the control signals for several access times of read-only memory (ROM) plus high-resolution timing and refresh control for dynamic RAM (DRAM). The controller outputs can drive up to 32 memory devices directly in a wide variety of configurations using various architectures of standard DRAMs. A logical-to-physical address translator maps the 4M-byte physical memory into the 32M-byte logical address space with three levels of protection.

Address translation is performed by a simple 128 entry content-addressable memory (CAM). MEMC provides a descriptor entry for every page of physical memory which eliminates descriptor thrashing (address translation misses) from degrading system performance.

ORDER INFORMATION

Part Number	Bus Clock Frequency	Package
VL86C110-08QC	8 MHz	Plastic Leaded Chip Carrier (PLCC)

Note: Operating temperature range is 0°C to + 70°C.

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32-BIT RISC MICROPROCESSOR FAMILY

VL86C310 RISC VIDEO CONTROLLER (VIDC)

FEATURES

- Pixel rate selectable as 8, 12, 16, or 24 MHz
- Serializes data to 1-, 2-, 4-, or 8- bits per pixel
- 16 x 13-bit words - 4096 color look-up palette
- Three 4-bit DACs (one for each CRT gun)
- Fully programmable screen parameters
- Screen border in any of the 4096 possible colors
- Flexible cursor sprite
- High quality stereo sound generation

DESCRIPTION

The Video Controller (VIDC) accepts video data from DRAM under DMA control, serializes and passes it through a color look-up palette, and converts it to analog signals for driving the CRT guns. The chip also controls all the display timing parameters plus the position and pattern of the cursor sprite. In addition, the VIDC includes an exponential DAC and stereo image table for the generation of high quality sound from data in the DRAM.

The VIDC requests data from the RAM when required, and buffers it in one of three first-in, first-out memories (FIFOs). Note that the addressing of the data in RAM is controlled elsewhere in the system (usually in the VL86C110 Memory Controller, MEMC). Data is requested in blocks of four 32-bit words, allowing efficient use of page-mode DRAM without locking up the system data bus for long periods.

The VIDC is a highly programmable device, offering a very wide choice of display formats. The pixel rate can be selected in a range between 8 and 24 MHz and the data can be serialized to either 8-, 4-, 2-, or 1-bit per pixel. The horizontal timing parameters can be controlled to units of two pixels, and the vertical timing parameters can be controlled in units of a raster. The color look-up palette which drives the three on-chip DACs is 13 bits wide, offering a choice from 4096 colors or an external video source.

ORDER INFORMATION

Part Number	Clock Frequency	Package
VL86C310-08QC	8 MHz	Plastic Leaded Chip Carrier (PLCC)

Note: Operating temperature is 0°C to +70°C.

VL86C410 RISC I/O CONTROLLER (IOC)

FEATURES

- Power on reset control
- Four independent 16-bit programmable counters
  –Two timers
  –Two baud rate generators
- Bidirectional serial keyboard interface
- Six programmable bidirectional control pins
- Interrupt mask, request and status registers for –IRQ and –FIRQ
- 14 level triggered interrupt inputs
- Two edge triggered interrupt inputs
- Four programmable peripheral cycles
- ARM/IO bus interface control
- Expansion bus buffer control

DESCRIPTION

The VL86C410 Input/Output Controller (IOC) is designed to interface to the VL86C010/VL86C110/VL86C310 chip set to provide a unified view of interrupts and peripherals within an Acorn RISC Machine (ARM) based computer. It controls an 8-to-32 bit I/O data bus to which on-board peripherals and any I/O expansions are connected. It provides a set of internal functions, which are accessed without wait states, and programmable speed access to external peripherals.

The VL86C410 provides system level I/O with six programmable control pins and a full-duplex, bidirectional serial keyboard interface. To support system timing requirements, the VL86C410 contains four independent programmable counters. Two of these counters are used as baud rate generators. One is dedicated to the keyboard and the other controls the BAUD output pin to generate a free-running clock. The other two counters can be used to generate system timing events.

ORDER INFORMATION

Part Number	Clock Frequency	Package
VL86C410-08QC	8 MHz	Plastic Leaded Chip Carrier (PLCC)

Note: Operating temperature is 0°C to +70°C.

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VTC's LSP line gives you a whole range of analog solutions, for:

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- ☐ Data acquisition/conversion
- ☐ Signal transmission
- ☐ And special functions

The line includes a complete selection of *Op Amps* to 500MHz bandwidth . . . precision, high-speed, and fast settling, plus dual or quad.

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Flash Converters to 8 bits, 250MHz.

DACs to 12 bits.

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And *Operational Transconductance Amplifiers* like the new VA703 and VA713, which feature a broad loop bandwidth of 75MHz, and a high slew rate of 50V/μsec.

If your analog application requires high speed, high slew rate, low offsets, large power bandwidth, high output drive capability, fast conversion rates, and/or higher packaging density . . . then you should be specifying VTC's high-performance LSP ICs in your system!

What's more, these parts are specified with ±5V operation to help simplify your system power requirements, and reduce power consumption.

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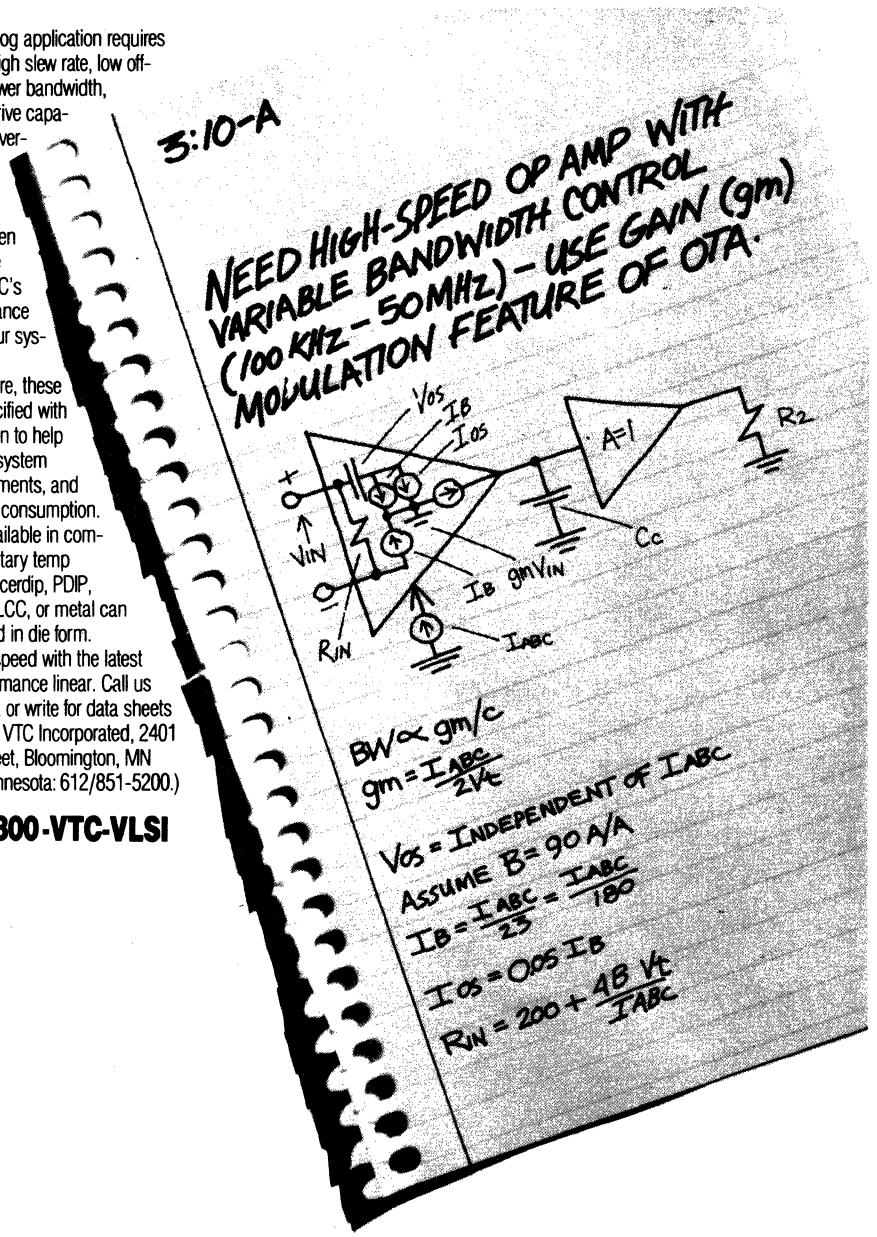
CALL 1-800-VTC-VLSI



VTC

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Operational Transconductance Amplifiers (OTA)

DEVICE	DESCRIPTION	PACKAGE*	SLEW RATE	BANDWIDTH	OFFSET Voltage	OFFSET Current	OUTPUT CURRENT	BIAS CURRENT	COMMENTS
VA703J	OTA	D,P,PO,T	50V/µs	75MHz	5mV	0.6µA	—	5µA	Commercial
VA703S	OTA	D,T,X	50V/µs	75MHz	3mV	0.6µA	—	5µA	Military
VA713J	OTA w/Buffer	D,P,PO,T	50V/µs	75MHz	5mV	0.6µA	20mA	5µA	Commercial
VA713S	OTA w/Buffer	D,T,X	50V/µs	75MHz	3mV	0.6µA	20mA	5µA	Military
VA2703J	Dual OTA	D,P,PO	50V/µs	75MHz	5mV	0.6µA	—	5µA	Commercial
VA2703S	Dual OTA	D	50V/µs	75MHz	3mV	0.6µA	—	5µA	Military
VA2713J	Dual OTA w/Buffer	D,P,PO	50V/µs	75MHz	5mV	0.6µA	20mA	5µA	Commercial
VA2713S	Dual OTA w/Buffer	D	50V/µs	75MHz	3mV	0.6µA	20mA	5µA	Military

Linear Amplifiers, Special Purpose

DEVICE	DESCRIPTION	PACKAGE*	COMMENTS
VA702J	Op Amp, Wideband, w/AGC	D,P,PO	450MHz Bandwidth
VA712J	Op Amp, Wideband, w/AGC	T	450MHz Bandwidth
VA712S	Op Amp, Wideband, w/AGC	T,X	450MHz Bandwidth
VA730J	Amplifier, Sample and Hold	D,DL	50MHz Sampling Frequency
VA730S	Amplifier, Sample and Hold	D,DL,X	50MHz Sampling Frequency

Data Converters

DEVICE	DESCRIPTION	PACKAGE*	COMMENTS
VC008J	8-Bit Flash A/D	D,DL	8-Bit A/D, 250MHz, Commercial
VC008S	8-Bit Flash A/D	D,DL,X	8-Bit A/D, 250MHz, Military
VC018J	8-Bit Flash A/D	D,DL	8-Bit A/D, 150MHz, Commercial
VC018S	8-Bit Flash A/D	D,DL,X	8-Bit A/D, 150MHz, Military
VC108J	8-Bit Video DAC	D,DL,PL,P	8-Bit DAC, 200MHz, Commercial
VC108K	8-Bit Video DAC	D,DL,PL,P	8-Bit DAC, 300MHz, Commercial
VC108S	8-Bit Video DAC	D,DL,X	8-Bit DAC, 250MHz Military
VC401J	V/F Converter	D,P,PO	0-20MHz Frequency Range, Commercial
VC401S	V/F Converter	D,X	0-20MHz Frequency Range, Military
VC512J	12-Bit DAC	D,P,PO,PL,DL	12-Bit DAC, 125ns Settling Time, Commercial
VC512S	12-Bit DAC	D,DL,X	12-Bit DAC, 125ns Settling Time, Military
VC594J	12-Bit A/D	D,P,PO,PL,DL	12-Bit A/D, 5µs Conversion Rate, Commercial
VC594K	12-Bit A/D	D,P,PO,PL,DL	12-Bit A/D, 2µs Conversion Rate, Commercial
VC594S	12-Bit A/D	D,DL,X	12-Bit A/D, 2µs Conversion Rate, Military

Comparators

DEVICE	DESCRIPTION	PACKAGE*	OFFSET Voltage	OFFSET Current	PROP DELAY	ENABLE PW	ENABLE Set-up/Hold	COMMENTS
VC7690J	Comparator,Very Fast	D,P,PO,T	5mV	5µA	1.9ns	—	—	Commercial
VC7690S	Comparator, Very Fast	D,T,X	5mV	5µA	2.0ns	—	—	Military
VC7695J	Comparator, Ultra Fast	D,P,PO,T,DL	5mV	5µA	1.9ns	2.0ns	1.0ns	Commercial
VC7695S	Comparator, Ultra Fast	D,T,DL,X	5mV	5µA	2.0ns	2.0ns	1.0ns	Military
VC7696J	TTL Comparator	D,P,PO,T,DL	3mV	5µA	6.0ns	2.0ns	2.0ns	Commercial
VC7696S	TTL Comparator	D,T,TL,X	3mV	5µA	6.5ns	2.0ns	2.0ns	Military
VC7697J	Dual Comparator, Ultra Fast	D,P,PO,DL	5mV	5µA	2.5ns	2.0ns	1.0ns	Commercial
VC7697S	Dual Comparator, Ultra Fast	D,DL	5mV	5µA	2.8ns	2.0ns	1.0ns	Military
VC7698J	Dual TTL Comparator	D,P,PO,DL	3mV	5µA	8.0ns	2.0ns	2.0ns	Commercial
VC7698S	Dual TTL Comparator	D,DL	3mV	5µA	8.5ns	2.0ns	2.0ns	Military

Video Amplifiers

DEVICE	DESCRIPTION	PACKAGE*	GAIN G1	GAIN G2	GAIN G3	BANDWIDTH G1	BANDWIDTH G2	BANDWIDTH G3	INPUT NOISE	PROP DELAY G1	PROP DELAY G2	PROP DELAY G3	COMMENTS
VA592J	Video Amplifier	D,P,PO,T	400	100	—	80MHz	100MHz	—	4µVrms	7.5ns	6.0ns	—	Commercial
VA592S	Video Amplifier	D,X,T	400	100	—	80MHz	100MHz	—	4µVrms	7.5ns	6.0ns	—	Military
VA733J	Video Amplifier	D,P,PO,T	400	100	10	95MHz	110MHz	140MHz	4µVrms	7.5ns	6.0ns	3.6ns	Commercial
VA733S	Video Amplifier	D,X,T	400	100	10	95MHz	110MHz	140MHz	4µVrms	7.5ns	6.0ns	3.6ns	Military

Buffer Amplifiers

DEVICE	DESCRIPTION	PACKAGE*	SLEW RATE	BANDWIDTH	OUTPUT OFFSET VOLTAGE	OUTPUT CURRENT	COMMENTS
VA003J	Unity Gain Buffer	D,P,PO,T	600V/µs	300MHz	15mV	±100mA	Commercial
VA003S	Unity Gain Buffer	D,X,T	600V/µs	300MHz	10mV	±100mA	Military
VA033J	Unity Gain Buffer	D,P,PO,T	1500V/µs	300MHz	15mV	±100mA	Commercial
VA033S	Unity Gain Buffer	D,X,T	1500V/µs	300MHz	10mV	±100mA	Military

Line Drivers

DEVICE	DESCRIPTION	PACKAGE*	COMMENTS
VS610	NTDS Driver/Receiver	D,P,DL,DK,X	MIL-STD-1397 TYPE B,C NTDS Driver/Receiver
VS620/VS621	10-bit Video Line Driver	PL	SMPTE RP-125 10-bit Video Driver

VTC

Linear Signal Processing

The linear signal processing (LSP) product line is part of the system solution for such applications as scientific and medical instrumentation, data acquisition, process control, and general signal processing on either side of the A/D and D/A conversion blocks.

VTC's unique processes couple high speed with close device matching along with laser trimming capabilities. LSP products include operational amplifiers, buffers, comparators, transconductance amplifiers, sample-hold and D-to-A and A-to-D converters.

As in all products offered by VTC, the emphasis is on performance and reliability. The devices are designed to fit applications where high performance, high slew rate, low offset, wide gain bandwidth and high output current capability is required.

Operational Amplifiers (All Parameters @ 25°C, V supplies = ±5V)

DEVICE	DESCRIPTION	PACKAGE	SLEW RATE	GAIN BANDWIDTH PRODUCT	OFFSET		OUTPUT CURRENT	BIAS CURRENT	COMMENTS
					Voltage	Current			
VA701J	Op Amp, Precision	D,P,PO,T	6V/µs	30MHz A_{CL} ≥1	400µV	150nA	50mA	200nA	Commercial
VA701K	Op Amp, Precision	D,P,PO,T,DL	6V/µs	30MHz A_{CL} ≥1	100µV	100nA	50mA	100nA	Commercial
VA701L	Op Amp, Precision	D,T,DL	6V/µs	30MHz A_{CL} ≥1	25µV	50nA	50mA	40nA	Military
VA701S	Op Amp, Precision	D,T,DL	6V/µs	30MHz A_{CL} ≥1	25µV	50nA	50mA	40nA	Military
VA705J	Op Amp, Precision, High-Speed	D,P,T,PO	30V/µs	25MHz A_{CL} ≥1	10mV	100nA	40mA	1100nA	Commercial
VA705K	Op Amp, Precision, High-Speed	D,P,T,PO	30V/µs	25MHz A_{CL} ≥1	5mV	50nA	50mA	900nA	Commercial
VA705L	Op Amp, Precision, High-Speed	D,P,T,PO	30V/µs	25MHz A_{CL} ≥1	2mV	25nA	50mA	900nA	Commercial
VA705S	Op Amp, Precision, High-Speed	D,T,X	30V/µs	25MHz A_{CL} ≥1	5mV	25nA	50mA	1100nA	Military
VA705T	Op Amp, Precision, High-Speed	D,T	30V/µs	25MHz A_{CL} ≥1	2mV	25nA	50mA	900nA	Military
VA706J	Op Amp, Fast Settling, High-Speed	D,P,T,PO	38V/µs	25MHz A_{CL} ≥1	20mV	120nA	40mA	1100nA	Commercial
VA706K	Op Amp, Fast Settling, High-Speed	D,P,T,PO	38V/µs	25MHz A_{CL} ≥1	10mV	120nA	50mA	1100nA	Commercial
VA706S	Op Amp, Fast Settling, High-Speed	D,T,X	38V/µs	25MHz A_{CL} ≥1	10mV	120nA	50mA	1100nA	Military
VA707J	Op Amp, Fast Settling, High-Speed	D,P,T,PO	80V/µs	300MHz A_{CL} ≥12	12mV	120nA	40mA	1100nA	Commercial
VA707K	Op Amp, Fast Settling, High-Speed	D,P,T,PO	80V/µs	300MHz A_{CL} ≥12	6mV	120nA	50mA	1100nA	Commercial
VA707S	Op Amp, Fast Settling, High-Speed	D,T,X	80V/µs	300MHz A_{CL} ≥12	6mV	120nA	50mA	1100nA	Military
VA708J	Op Amp, Fast Settling, High-Speed	D,P,T,PO	60V/µs	100MHz A_{CL} ≥3	12mV	120nA	40mA	1100nA	Commercial
VA708K	Op Amp, Fast Settling, High-Speed	D,P,T,PO	60V/µs	100MHz A_{CL} ≥3	6mV	120nA	50mA	1100nA	Commercial
VA708S	Op Amp, Fast Settling, High-Speed	D,T,X	60V/µs	100MHZ A_{CL} ≥3	6mV	120nA	50mA	1100nA	Military
VA711J	Op Amp, Precision	D,P,PO,T	18V/µs	100MHz A_{CL} ≥5	400µV	150nA	50mA	200nA	Commercial
VA711K	Op Amp, Precision	D,P,PO,T	18V/µs	100MHz A_{CL} ≥5	100µV	100nA	50mA	100nA	Commercial
VA711L	Op Amp, Precision	D,T,DL	18V/µs	100MHz A_{CL} ≥5	25µV	50nA	50mA	40nA	Military
VA711S	Op Amp, Precision	D,T,DL	18V/µs	100MHz A_{CL} ≥5	25µV	50nA	50mA	40nA	Military
VA721J	Op Amp, Precision	D,P,PO,T	100V/µs	450MHz A_{CL} ≥25	400µV	150nA	50mA	200nA	Commercial
VA721K	Op Amp, Precision	D,P,PO,T	100V/µs	450MHz A_{CL} ≥25	100µV	100nA	50mA	100nA	Commercial
VA721L	Op Amp, Precision	D,P,PO,T	100V/µs	450MHz A_{CL} ≥25	25µV	50nA	50mA	40nA	Commercial
VA721S	Op Amp, Precision	D,T,DL,X	100V/µs	450MHz A_{CL} ≥25	25µV	50nA	50mA	40nA	Military
VA2705J	Dual Op Amp	D,P,T	30V/µs	25MHz A_{CL} ≥1	12mV	50nA	40mA	1100nA	Commercial
VA2705K	Dual Op Amp	D,P,T	30V/µs	25MHz A_{CL} ≥1	6mV	100nA	50mA	900nA	Commercial
VA2705S	Dual Op Amp	D,T	30V/µs	25MHz A_{CL} ≥1	6mV	120nA	50mA	900nA	Military
VA2706J	Dual Op Amp	D,P,T	38V/µs	25MHz A_{CL} ≥1	20mV	120nA	40mA	1100nA	Commercial
VA2706S	Dual Op Amp	D,P	38V/µs	25MHz A_{CL} ≥1	12mV	120nA	50mA	1100nA	Military
VA2707J	Dual Op Amp	D,P,T	80V/µs	300MHz A_{CL} ≥12	12mV	120nA	40mA	1100nA	Commercial
VA2707K	Dual Op Amp	D,P,T	80V/µs	300MHz A_{CL} ≥12	6mV	120nA	50mA	1100nA	Commercial
VA2707S	Dual Op Amp	D,T	80V/µs	300MHz A_{CL} ≥12	6mV	120nA	50mA	1100nA	Military
VA2708J	Dual Op Amp	D,P,T	60V/µs	100MHz A_{CL} ≥3	12mV	120nA	40mA	1100nA	Commercial
VA2708K	Dual Op Amp	D,P,T	60V/µs	100MHz A_{CL} ≥3	6mV	120nA	50mA	1100nA	Commercial
VA2708S	Dual Op Amp	D,T	60V/µs	100MHz A_{CL} ≥3	6mV	50nA	50mA	1100nA	Military
VA2715J	Dual Op Amp w/Nulling	D,P	30V/µs	25MHZ A_{CL} ≥1	12mV	50nA	40mA	1100nA	Commercial
VA2715K	Dual Op Amp w/Nulling	D,P	30V/µs	25MHz A_{CL} ≥1	6mV	120nA	50mA	900nA	Commercial
VA2715S	Dual Op Amp w/Nulling	D	30V/µs	25MHz A_{CL} ≥1	6mV	120nA	50mA	900nA	Military
VA2716J	Dual Op Amp w/Nulling	D,P	38V/µs	25MHz A_{CL} ≥1	20mV	120nA	40mA	1100nA	Commercial
VA2716S	Dual Op Amp w/Nulling	D	38V/µs	25MHz A_{CL} ≥1	12mV	120nA	50mA	1100nA	Military
VA2717J	Dual Op Amp w/Nulling	D,P	80V/µs	300MHz A_{CL} ≥12	12mV	120nA	40mA	1100nA	Commercial
VA2717K	Dual Op Amp w/Nulling	D,P	80V/µs	300MHz A_{CL} ≥12	6mV	120nA	50mA	1100nA	Commercial
VA2717S	Dual Op Amp w/Nulling	D	80V/µs	300MHz A_{CL} ≥12	6mV	120nA	50mA	1100nA	Military
VA2718J	Dual Op Amp w/Nulling	D,P	60V/µs	100MHz A_{CL} ≥3	12mV	120nA	40mA	1100nA	Commercial
VA2718K	Dual Op Amp w/Nulling	D,P	60V/µs	100MHz A_{CL} ≥3	6mV	120nA	50mA	1100nA	Commercial
VA2718S	Dual Op Amp w/ Nulling	D	60V/µs	100MHz A_{CL} ≥3	6mV	120nA	40mA	1100nA	Military
VA4701J	Quad Op Amp, Precision	D,P,PO,T,DL	6V/µs	80MHz A_{CL} ≥1	500µV	150nA	50mA	200nA	Commercial
VA4701S	Quad Op Amp, Precision	D,T,DL	6V/µs	80MHz A_{CL} ≥1	400µV	100nA	50mA	100nA	Military
VA4705J	Quad Op Amp	D,P	30V/µs	25MHz A_{CL} ≥1	12mV	100nA	50mA	1100nA	Commercial
VA4705K	Quad Op Amp	D,P	30V/µs	25MHz A_{CL} ≥1	6mV	50nA	50mA	900nA	Commercial
VA4705S	Quad Op Amp	D	30V/µs	25MHz A_{CL} ≥1	6mV	50nA	50mA	900nA	Military
VA4706J	Quad Op Amp	D,P	38V/µs	25MHz A_{CL} ≥1	20mV	120nA	50mA	1100nA	Commercial
VA4706S	Quad Op Amp	D	38V/µs	25MHz A_{CL} ≥1	12mV	120nA	50mA	1100nA	Military
VA4707J	Quad Op Amp	D,P	80V/µs	300MHz A_{CL} ≥12	12mV	120nA	40mA	1100nA	Commercial
VA4707K	Quad Op Amp	D,P	80V/µs	300MHz A_{CL} ≥12	6mV	120nA	50mA	1100nA	Commercial
VA4707S	Quad Op Amp	D	80V/µs	300MHz A_{CL} ≥12	6mV	120nA	50mA	1100nA	Military
VA4708J	Quad Op Amp	D,P	60V/µs	100MHz A_{CL} ≥3	12mV	120nA	40mA	1100nA	Commercial
VA4708K	Quad Op Amp	D,P	60V/µs	100MHz A_{CL} ≥3	6mV	120nA	50mA	1100nA	Commercial
VA4708S	Quad Op Amp	D	60V/µs	100MHz A_{CL} ≥3	6mV	120nA	40mA	1100nA	Military
VA4711J	Quad Op Amp	D,P,PO,T,DL	18V/µs	100MHz A_{CL} ≥5	500µV	150nA	50mA	200nA	Commercial
VA4711S	Quad Op Amp	D,T,DL	18V/µs	100MHz A_{CL} ≥5	400µV	100nA	50mA	100nA	Military
VA4741J	Quad Op Amp	D,P,PO	2.7V/µs	5MHz A_{CL} ≥1	5mV	200nA	13mA	400nA	Commercial
VA4741S	Quad Op Amp	D	2.7V/µs	5MHz A_{CL} ≥1	5mV	200nA	13mA	400nA	Military
VA4742J	Quad Op Amp	D,P,PO	2.7V/µs	5MHz A_{CL} ≥1	5mV	200nA	13mA	400nA	Commercial
VA4742S	Quad Op Amp	D	2.7V/µs	5MHZ A_{CL} ≥1	5mV	200nA	13mA	400nA	Military

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DISK DRIVE READ/WRITE PREAMPLIFIERS

DEVICE	DAMPING RESISTOR OPTION	CHANNELS	POWER SUPPLY	INPUT NOISE	VOLTAGE GAIN (TYP)	PIN COUNT	PACKAGE
Ferrite Heads							
VM104		4	+6V,-4V	1.6nV/√Hz	35	24	F
VM115		5	+5V,-5V	2.5nV/√Hz	40	24	F
VM117		2,4,6	+5V,+12V	1.6nV/√Hz	100	18,22,24,28	P,D,F,PO
VM117R	X	2,4,6	+5V,+12V	1.6nV/√Hz	100	18,22,24,28	P,D,F,PO
VM217		6,8	+5V,+12V	1.6nV/√Hz	100	28,40,44	P,PL,TB
VM217R	X	6,8	+5V,+12V	1.6nV/√Hz	100	28,40,44	P,PL,TB
Center-Tapped Thin-Film Heads							
VM118		2,4,6	+5V,+12V	1.6nV/√Hz	100	18,22,24,28	P,PO
VM118R	X	2,4,6	+5V,+12V	1.6nV/√Hz	100	18,22,24,28	P,PO
VM218		6,8	+5V,+12V	1.6nV/√Hz	100	28,40,44	P,PL,TB
VM218R	X	6,8	+5V,+12V	1.6nV/√Hz	100	28,40,44	P,PL,TB
Thin-Film Heads							
VM214		4	+5V,-5V	1.1nV/√Hz	125	24	F
VM314		4	+5V,-5V	.6nV/√Hz	100	24	F

DISK DRIVE SERVO PREAMPLIFIERS

DEVICE	DESCRIPTION	POWER SUPPLY	INPUT NOISE	PACKAGE
VM101	Servo Preamp, Ferrite Head	-8.3V, or +10V	6nV/√Hz	D, PO
VM201	Servo Preamp, Ferrite Head, Low Noise	-8.3V, or +10V	1nV/√Hz	D, PO
VM216	Servo Preamp, Thin-film Head	-8.3V, or +12V	1nV/√Hz	D, PO

VTC

DISK DRIVE DATA RECOVERY

DEVICE	DESCRIPTION	POWER SUPPLY	CHARACTERISTICS	PACKAGE
VM305	Write/Servo Phase-Locked Oscillator	-5.2V or +5V	Data Rates from 10-48 Mbit/s	PO
VM443	Read Channel, Enhanced	+5V,+12V	RLL Compatible, BW = 30MHz	P, PL
VM5317/VM5327	Data Separator	+5V,+12V	Data Rates up to 22 Mbit/s, ECL	PL
VM5417/VM5427	Data Separator	+5V,+12V	Data Rates up to 22 Mbit/s, TTL	PL
VM5621	(2,7) Encoder/Decoder	+5V	Differential ECL Drivers	PL
VM5622	(2,7) Encoder/Decoder	+5V,-5V	Differential ECL Drivers	PL

TAPE DRIVE CIRCUITS

DEVICE	DESCRIPTION	CHARACTERISTICS	PACKAGE
VT210	Clock Synchronizer	Max Center Frequency = 2MHz, TTL Compatible	D
VT211	Write Driver	I_{WC} = 70mA p-p, I_{BIAS}= 40mA	D

VTC Incorporated

Advanced CMOS InterfaceLogic

VTC's advanced CMOS logic families offer state-of-the-art interfaces for the latest generations of microprocessor, memory, standard cell, and gate array systems.

All of the ACL products are fabricated by VTC using an advanced 1.2-micron, double-level metal CMOS 1 process and are packaged in plastic and ceramic dual in-line packages, small outline and leaded chip carrier packages with JEDEC standard pinouts.

High-Performance Interface

ACL from VTC means high-performance and high-quality bus interface logic. VTC's ACL products with their patented output structure offer the high drive (48 mA to 64 mA) required by VMEbus, Multibus and many other high-performance systems along with the popular speeds of FAST™ and ALS. Our ACL products are also latch-up free to 400 mA, have ESD protection greater than 2000 V and are fully characterized and specified. These features, along with low CMOS power, make VTC's ACL products ideal for systems requiring high-performance bus interface logic.

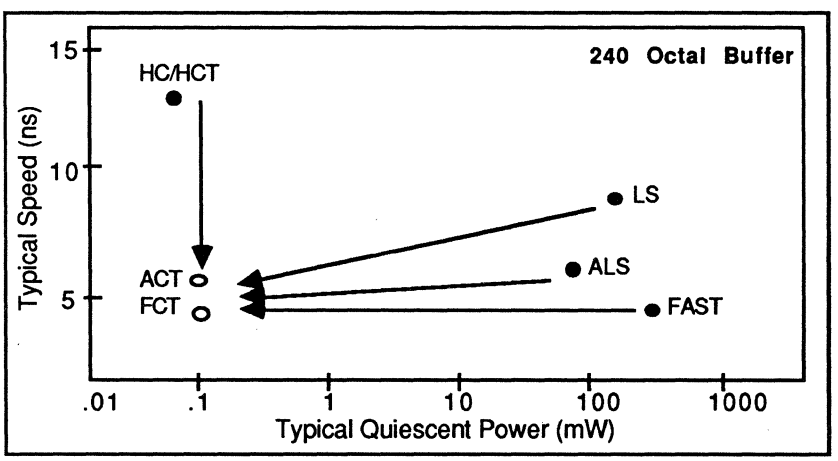
FCT

- CMOS Replacement for FAST™
- Upgrade for Systems using ALS, LS and HCT
- High Drive:
  IOL/IOH = 64/15 mA; Line Drivers and Transceivers
  IOL/IOH = 48/15 mA; Latches and Flip-flops
- Speed Equivalent to FAST, 4 to 5 ns Typical
- Low CMOS power, 50 µW Typical
- TTL Logic Levels
- Second-sourced by IDT
- MIL-STD-883, Ceramic DIP and LCC

ACT

- CMOS Replacement for ALS
- Upgrade for Systems using LS and HCT
- High Drive: IOL/IOH = 48/24 mA
- Speed Equivalent to ALS, 5 ns Typical
- Low CMOS Power, 50 µW Typical
- TTL Logic Levels
- MIL-STD-883, Ceramic DIP and LCC

ACL SPEED/POWER ADVANTAGE



VTC

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ACT FAMILY — EXAMPLE VTC PART NUMBER V74ACT240

FAMILY CROSSED TO	VTC ADVANTAGE	VENDOR	PART NUMBER EG.
ACT	Second Source	National GE/RCA	74ACT240 CD74ACT240
AHCT	Meet or Exceed Performance Upgrade by 10%	IDT Samsung Zytrex	IDT74AHCT240 KS74AHCT240 ZX74AHCT240
ALS	Equal Performance Dramatic Power Savings	†Texas Instruments †National †Mitsubishi	SN74ALS240A DM74ALS240 M74ALS240A
HCT	*System upgrade by 150%	Texas Instruments GE/RCA Hitachi Motorola National Signetics	SN74HCT240 CD74HCT240 HD74HCT240 MC74HCT240 MM74HCT240 74HCT240

VTC

FCT FAMILY — EXAMPLE VTC PART NUMBER V74FCT240

FAMILY CROSSED TO	VTC ADVANTAGE	VENDOR	PART NUMBER EG.
FCT	Second Source	IDT	IDT74FCT240
FAST™	Equal Performance Dramatic Power Savings	†Texas Instruments †Fairchild †Motorola †Signetics	SN74F240 74F240 MC74F240 74F240

FCT FAMILY — EXAMPLE VTC PART NUMBER V74FCT824A

FAMILY CROSSED TO	VTC ADVANTAGE	VENDOR	PART NUMBER EG.
39C	Equal Performance	IDT	IDT39C824
29XX	Equal Performance Dramatic Power Savings	†AMD	A29824

†These are bipolar components which can be replaced by functionally and performance equivalent CMOS.
**System upgrade refers to the clock rate attainable by substituting ACL parts. For instance a 6 MHz HC based system could be upgraded to a 18 MHz AC system.*

VTC Incorporated

Advanced CMOS InterfaceLogic

YOUR CHOICES IN HIGH-PERFORMANCE BUS INTERFACE LOGIC ARE REALLY STACKING UP.

And VTC was has them all. Now you have three ways to *enhance speed* and *reduce power* in your system, with direct pin-for-pin, part-for-part replacements.

ACT and now *FCT*—the latest addition to our family of advanced CMOS Logic (ACL) devices. And, with 50 parts in each, VTC gives you the *industry's largest selection* of 54/74 series ACL—in both DIP and surface-mount packages.

FCT gives you performance compatibility with FAST™ and 29800 parts.

ACT is a direct replacement for ALS.

All of them give you cool CMOS power. Dynamic power dissipation much lower than FAST and ALS, even at 75MHz. And remarkably low quiescent power—a reduction of 3 to 5 orders of magnitude over ALS.

What better way to start stacking the chips in your favor?

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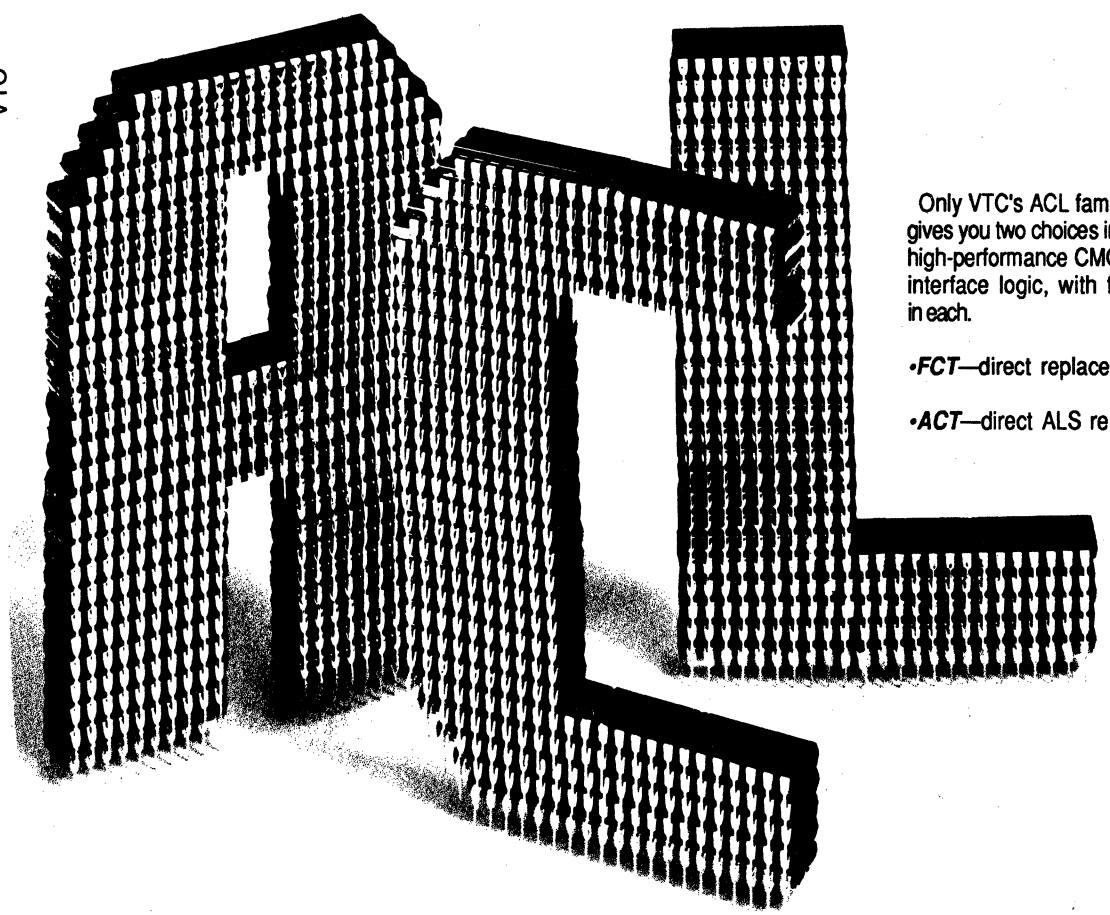
Largest Selection of 54/74Series ACL:

Buffers		*Transceivers*		*Flip-Flops*		*Latches*	
240	540	245	861	374	823	373	843
241	541	620	862	534	824	533	844
244	827	623	863	564	825	563	845
465	828	640	864	574	826	580	846
466		643		575	874	841	880
467		645		576	876	842	
478				577	878		
				821	879		

VTC



Only VTC's ACL family gives you two choices in high-performance CMOS bus interface logic, with fifty parts in each.

- ***FCT***—direct replacement for FAST™
- ***ACT***—direct ALS replacement

Fast is a trademark of Fairchild Semiconductor Corporation

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54/74FCT	54/74ACT	DESCRIPTION
54/74FCT240	54/74ACT240	Octal Buffers and Line Drivers
	54/74ACT241	Octal Buffers and Line Drivers
54/74FCT244	54/74ACT244	Octal Buffers and Line Drivers
54/74FCT245	54/74ACT245	Octal Bus Transceivers
54/74FCT373	54/74ACT373	Octal D-Type Transparent Latches
54/74FCT374	54/74ACT374	Octal D-Type Edge-Triggered Flip-Flops
	54/74ACT465	Octal Buffers and Line Drivers
	54/74ACT466	Octal Buffers and Line Drivers
	54/74ACT467	Octal Buffers and Line Drivers
	54/74ACT468	Octal Buffers and Line Drivers
54/74FCT533	54/74ACT533	Octal D-Type Transparent Latches
54/74FCT534	54/74ACT534	Octal D-Type Edge-Triggered Flip-Flops
	54/74ACT540	Octal Buffers and Line Drivers
	54/74ACT541	Octal Buffers and Line Drivers
	54/74ACT563	Octal D-Type Transparent Latches
	54/74ACT564	Octal D-Type Edge-Triggered Flip-Flops
54/74FCT573	54/74ACT573	Octal D-Type Transparent Latches
54/74FCT574	54/74ACT574	Octal D-Type Edge-Triggered Flip-Flops
	54/74ACT575	Octal D-Type Edge-Triggered Flip-Flops
	54/74ACT576	Octal D-Type Edge-Triggered Flip-Flops
	54/74ACT577	Octal D-Type Edge-Triggered Flip-Flops
	54/74ACT580	Octal D-Type Transparent Latches
	54/74ACT620	Octal Bus Transceivers
	54/74ACT623	Octal Bus Transceivers
54/74FCT640	54/74ACT640	Octal Bus Transceivers
	54/74ACT643	Octal Bus Transceivers
54/74FCT645	54/74ACT645	Octal Bus Transceivers
54/74FCT821A	54/74ACT821	10-Bit D-Type Edge-Triggered Flip-Flops
54/74FCT822A	54/74ACT822	10-Bit D-Type Edge-Triggered Flip-Flops
54/74FCT823A	54/74ACT823	9-Bit D-Type Edge-Triggered Flip-Flops
54/74FCT824A	54/74ACT824	9-Bit D-Type Edge-Triggered Flip-Flops
54/74FCT825A	54/74ACT825	Octal D-Type Edge-Triggered Flip-Flops
54/74FCT826A	54/74ACT826	Octal D-Type Edge-Triggered Flip-Flops
54/74FCT827A	54/74ACT827	10-Bit Buffers and Line Drivers
54/74FCT828A	54/74ACT828	10-Bit Buffers and Line Drivers
54/74FCT841A	54/74ACT841	10-Bit D-Type Transparent Latches
54/74FCT842A	54/74ACT842	10-Bit D-type Transparent Latches
54/74FCT843A	54/74ACT843	9-Bit D-type Transparent Latches
54/74FCT844A	54/74ACT844	9-Bit D-type Transparent Latches
54/74FCT845A	54/74ACT845	Octal D-type Transparent Latches
54/74FCT846A	54/74ACT846	Octal D-type Transparent Latches
54/74FCT861A	54/74ACT861	10-Bit Bus Transceivers
54/74FCT862A	54/74ACT862	10-Bit Bus Transceivers
54/74FCT863A	54/74ACT863	9-Bit Bus Transceivers
54/74FCT864A	54/74ACT864	9-Bit Bus Transceivers
	54/74ACT874	Dual 4-Bit D-Type Edge-Triggered Flip-Flops
	54/74ACT876	Dual 4-Bit D-Type Edge-Triggered Flip-Flops
	54/74ACT878	Dual 4-Bit D-Type Edge-Triggered Flip-Flops
	54/74ACT879	Dual 4-Bit D-Type Edge-Triggered Flip-Flops
	54/74ACT880	Dual 4-Bit D-Type Edge-Triggered Flip-Flops

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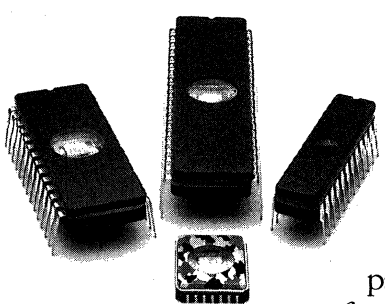
Waferscale Integration

New 256K to 1M bit EPROMs.
All Under 100ns.
All Available Now.

WSI puts performance into your hands. With a complete family of high-speed, non-volatile memory devices that let you realize the true zero-wait-state potential of today's high-end MPUs, DSPs, and embedded controllers.

WSI's L-Series CMOS EPROMs:
High density.
High performance.
High value.
WSI's new L-Series CMOS EPROMs are ideal for high-performance applications, including 16-MHz 68020 and 1750A-type systems. Available in 32K x 8 (WS27C256L), 64K x 8 (WS27C512L), and 128K x 8 (WS27C010L) architectures, WSI's L-Series NVMs open the realm of sub-100ns performance to everyone.



WSI's F-Series CMOS EPROMs:
Byte-wide.
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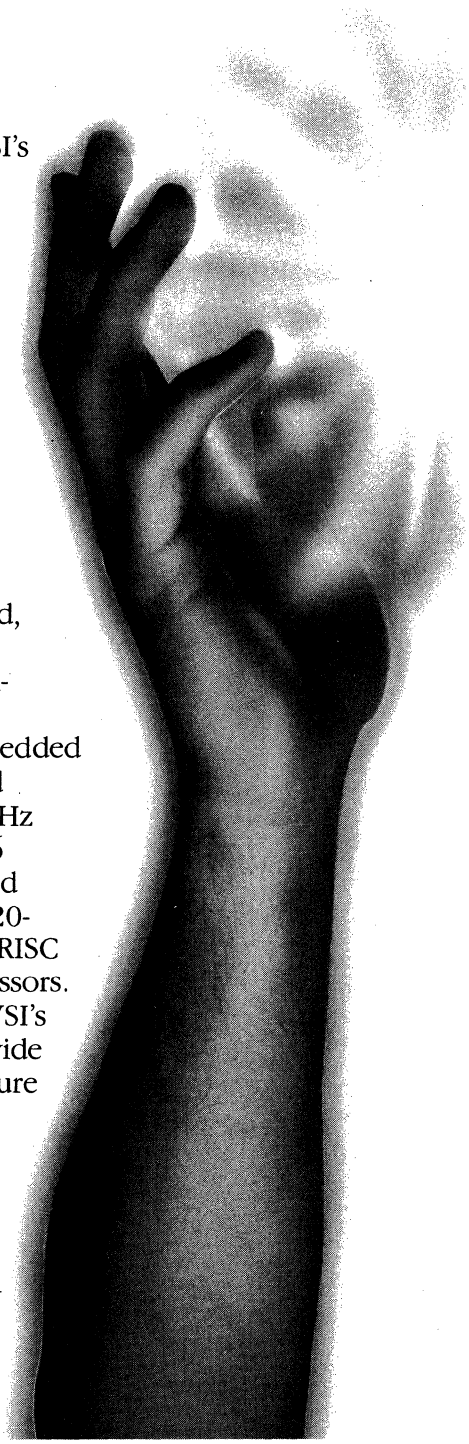
WSI's F-Series brings high-speed, high-density NVM to new-generation systems —including embedded controllers based on 12- and 16-MHz 80386/80376 MPUs, and 16- or 20-MHz RISC processors. And WSI's word-wide architecture lets you pack more performance into less board space.



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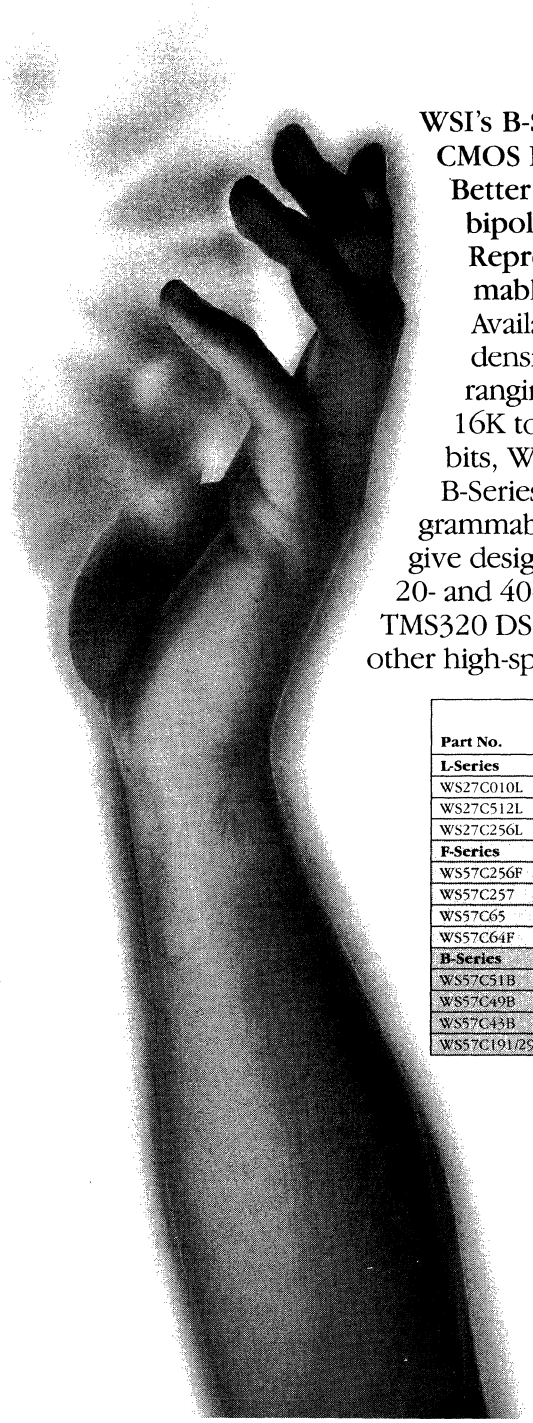
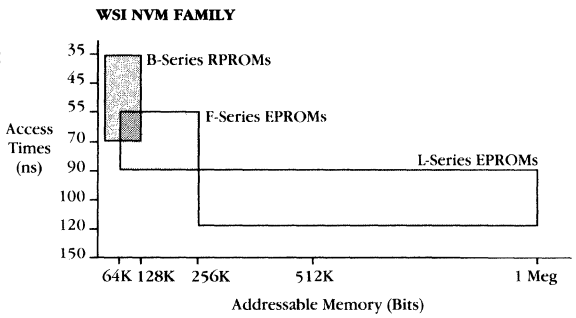
formance Memory signer's Hands.



WSI's B-Series CMOS RPROMs™: Better than bipolar. Reprogrammable, too.

Available in densities ranging from 16K to 128K bits, WSI's B-Series Reprogrammable PROMs give designers of 20- and 40-MHz TMS320 DSPs and other high-speed systems ultra-high performance. And they consume just a fraction of the power of their bipolar counterparts.



Feel the power of performance.

Whether your application is commercial or mil-spec, you can possess the power of WSI performance right now. Call today:

800/331-1030, extension 234

In California, call:

800/323-3939, extension 234.

Part No.	Fastest Commercial Speed	Fastest Military Speed	Type
L-Series			
WS27C010L	90ns	120ns	128K x 8 CMOS EPROM
WS27C512L	90ns	100ns	64K x 8 CMOS EPROM
WS27C256L	90ns	100ns	32K x 8 CMOS EPROM
F-Series			
WS57C256F	55ns	70ns	32K x 8 CMOS EPROM
WS57C257	55ns	70ns	16K x 16 CMOS EPROM
WS57C65	55ns	70ns	4K x 16 CMOS EPROM
WS57C64F	55ns	70ns	8K x 8 CMOS EPROM
B-Series			
WS57C51B	40ns	50ns	16K x 8 CMOS RPROM
WS57C49B	35ns	45ns	8K x 8 CMOS RPROM
WS57C43B	35ns	45ns	4K x 8 CMOS RPROM
WS57C191/291B	35ns	45ns	2K x 8 CMOS RPROM

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WSI's Programma

A new class of user-configurable products.

A higher standard of functionality, integration, and performance.

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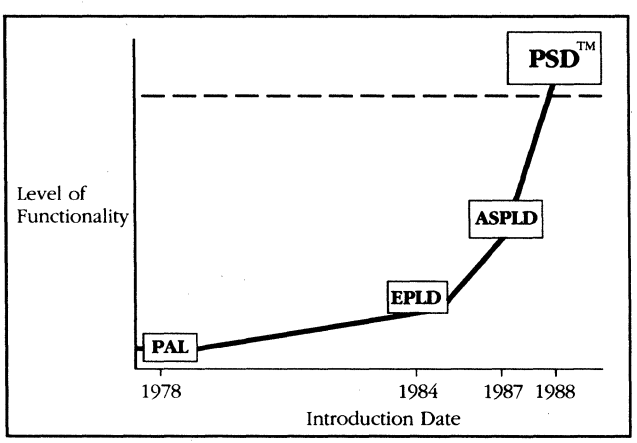
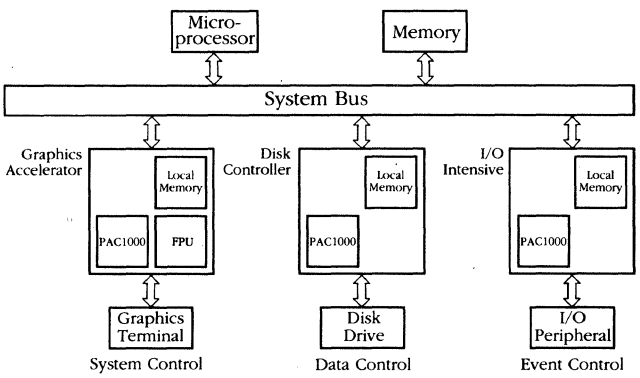
WSI's Programmable System Devices (PSD™) set a higher standard in functionality, integration, and performance. This new class of user-configurable, system-on-a-chip standard products goes beyond conventional programmable logic—combining programmable logic *and* memory into off-the-shelf, programmable one-chip systems. Each member of WSI's PSD product family integrates high-performance EPROM, SRAM and Logic, and each device can be readily configured on an IBM-PC® XT/AT or compatible with a familiar, "C"-like language.



WSI's PSD Products:
A major advance in user-configurability.

WSI's User-Configurable PAC1000.™ The New Standard in High-Speed Microcontrollers.

WSI's 16-bit PAC1000 User-Configurable, High-Performance Microcontroller is a single solution that's right for virtually every high-performance embedded system, data, or event control application.



PAC1000™ Embedded Control Applications

Available as a standard product, the PAC1000 Microcontroller can be user-configured both architecturally and functionally—a significant step beyond the logic-only configurability of PLDs. Through instructions written in a familiar "C"-like language, the PAC1000 device can be configured as a stand-alone microcontroller or as a microprocessor peripheral. And the function of each of the PAC1000 Microcontroller's bidirectional buses, I/O lines, and interrupt inputs can be redefined as needed by the system—as often as once every 50ns. No other stand-alone microcontroller comes close to the performance of WSI's PAC1000 system-on-a-chip. And configured as a microprocessor peripheral, the PAC1000 is the perfect interface between high-speed microprocessors and demanding real-time commercial and military controller applications. The PAC1000 Microcontroller already has been specified for graphics/imaging, communications, guidance systems, disk management, and many other applications.

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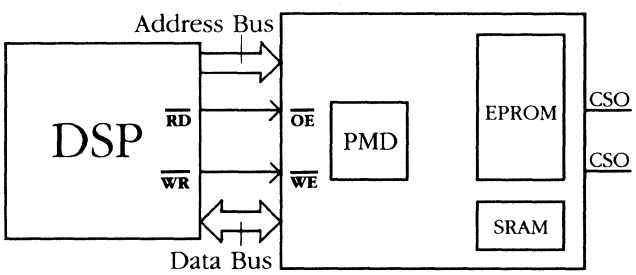
ble System Devices.

WSI's MAP168™ Mappable Memory
40ns Total Access Time. Zero Decode Delay.

Ideal for digital signal processor and other high-performance microprocessor designs, WSI's MAP168 Mappable Memory integrates a 128k bit EPROM program store, 32k bit SRAM data store, and programmable decode logic in a single, space-saving package. The MAP168 Mappable Memory is well-suited to either contiguous or split-mapped applications. WSI's menu-driven, high-level System Development Tools let you take full advantage of this extremely flexible, user-configurable circuit.



WSI-MAP168™
Mappable Memory

The MAP168 device's high-performance CMOS EPROM program store is subdivided into eight individually addressable blocks, and its integrated CMOS SRAM is similarly divided into two blocks. An on-chip Programmable Mapping Decoder (PMD) lets you map any block into any available address to create a virtually limitless combination of sequential and non-sequential memory sections. And the PMD completely decodes the address bus without slowing down the system, resulting in a total access time of only 40ns, including decode.

Simplified System Development

All of WSI's Programmable System Device products have been designed to cut system development time to the bone. All are system-on-a-chip standard products. Which means there's substantially less hardware to develop. And WSI's System Development Tools make configuring PSD products a fast, headache-free process.

WSI's easy-to-learn System Development Tools contain all the necessary programming hardware and software required to configure PSD products. Instructions are written in a menu-driven, familiar "C"-like language. And there's a complete functional simulator so you can test and debug your software quickly and easily.

WSI's System Development Tools run on the IBM-PC XT/AT (or compatible) platform. You can even use a laptop. All you need is DOS 3.1 or higher, and 640K of RAM. And most text editors are supported by the system.

WSI Puts Performance
Into Every Designer's Hands.

You can see, feel, and experience the advantages of WSI's Programmable System Devices right now. To put WSI performance into your hands, call today:

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Waferscale Integration

WD20C03A
Data Encryption Device

FEATURES

- CERTIFIED BY NATIONAL BUREAU OF STANDARDS
- TRANSFER RATE:
  UP TO 3.22 MBS WITH 5 MHZ CLOCK
  UP TO 5.10 MBS WITH 8 MHZ CLOCK
  UP TO 8.10 MBS WITH 10 MHZ CLOCK
- ENCRYPTS/DECRYPTS 64-BIT DATA WORDS USING 56-BIT KEY WORD
- ECB – ELECTRONIC CODE BOOK
  CBC – CIPHER BLOCK CHAINING
- SINGLE PORT 28-PIN PACKAGE
- COMMAND BIT PROGRAMMING VIA DAL BUS OR INPUT PINS
- PARITY CHECK ON KEY WORD LOADING
- STANDARD 8-BIT MICROPROCESSOR INTERFACE
- KEY STORED ON CHIP IS NOT EXTERNALLY ACCESSIBLE
- BATTERY BACK-UP MODE OF INTERNAL REGISTERS

APPLICATIONS

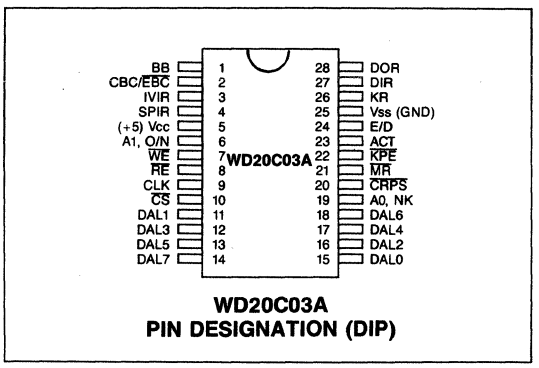
- SECURE BROKERAGE TRANSACTIONS
- ELECTRONIC FUNDS TRANSFERS
- SECURE BANKING/BUSINESS ACCOUNTING
- MAINFRAME COMMUNICATIONS
- REMOTE AND HOST COMPUTER COMMUNICATIONS

DESCRIPTION

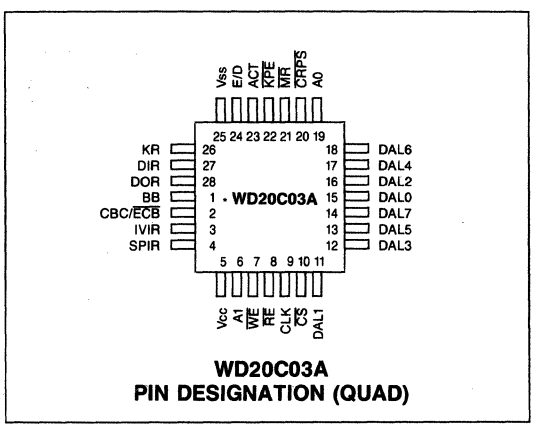
The Western Digital WD20C03A Data Encryption/Decryption device is designed to encrypt and decrypt 64-Bit blocks of data using the algorithm specified in the Federal Information Processing Data Encryption Standard (#46). This device encrypts a 64-Bit clear text word using a 56-Bit, user-specified key to produce a 64-Bit cipher text word. When reversed, the cipher text word is decrypted to produce the original clear text word.

The WD20C03A is fabricated using silicon gate, CMOS technology. All inputs and outputs are TTL compatible in all devices.

NOTE: This device cannot be shipped outside of the United States of America without authorization from the State Department and the Department of Defense.



WD20C03A
PIN DESIGNATION (DIP)



WD20C03A
PIN DESIGNATION (QUAD)

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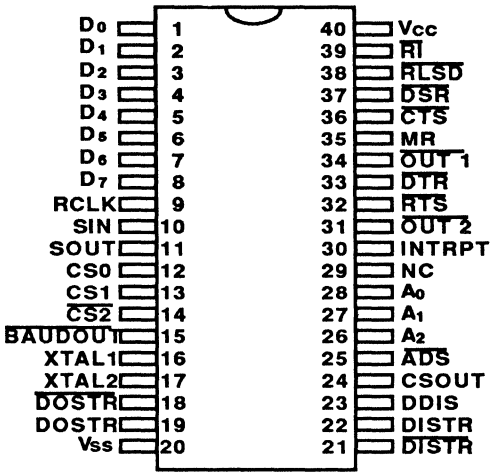
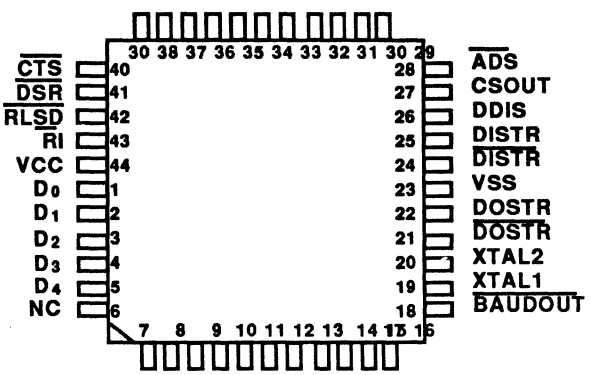
WD8250/82C50/16C450 ASYNCHRONOUS COMMUNICATIONS ELEMENT (ACE)

FEATURES

- Designed to be easily interfaced to most microprocessors (Z-80, 8088, 68000, etc.)
- Generating and stripping of Serial Async Control Bits (start, stop, parity)
- Full double buffering allows imprecise synchronization
- Independently controlled Transmit, Receive, Line Status, and data set Interrupts
- Programmable Baud Rate Generator allows division of any input Clock by 1 to (2^{16}-1) and generates the internal 16X Clock.
- Independent Receiver Clock input
- Modem interface capabilities
- Fully programmable Serial-Interface characteristics:
  - 5-, 6-, 7-, or 8-Bit Characters
  - Even, Odd, or No-Parity Bit Generation and Detection
  - 1-, 1 1/2-, or 2-Stop Bit Generation
  - Baud Rate Generation (DC to 56K Baud)**
- False Start Bit detector
- Complete status reporting capabilities
- Three-State TTL drive capabilities for bi-directional Data and Control bus
- Line break Generation and Detection
- Internal Diagnostic capabilities
  - Loopback Controls for Communications Link Fault Isolation
  - Break, Parity, Overrun, and Framing Error Simulation
- Full prioritized interrupt system controls
- Single +5 Volt Power Supply
- Low CMOS Power Dissipation



PIN DESIGNATION (DIP)



PIN DESIGNATION (Quad) *

DESCRIPTION

The WD8250/82C50/16C450 is a programmable Asynchonous Communication Element (ACE) in a 40-pin DIP or 44-pin Quad package. The device is fabricated in NMOS (WD8250) and CMOS (WD82C50 & WD16C450) silicon gate technology.

The ACE is a software-oriented device using a three-state 8-bit bi-directional data bus.

The ACE is used to convert parallel data to a serial format on the transmit side and to convert serial data to a parallel format on the receive side. The serial format, in order of transmission and reception, is a start bit, followed by five to eight data bits, a parity bit (if programmed) and one, one and one half (five bit format only) or two stop bits. The recommended data rate is 56K baud.*

Internal register enable the user to program various types of interrupts, modem controls, and character formats. The user can read the status of the ACE at any time monitoring word conditions, interrupts and modem status.

An additional feature of the ACE is a programmable Baud Rate Generator that is capable of dividing an internal XTAL or TTL signal clock by a division of up to 2^{16}-1.

The ACE is designated to work in either a polling or interrupt driven system, which is programmable by users' software controlling an internal register.

* Contact WD Sales Office for other Pin Outs.
** Contact WD Sales Office for exceeding this recommended maximum baud rate.

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WD1935A Synchronous Data Link Controller

FEATURES

- OFFERS COMPATIBILITY WITH MANY CURRENT COMMUNICATIONS STANDARDS, SUCH AS HDLC, SDLC, ADCCP, CCITT X.25 AND ISDN
- INCLUDES SDLC LOOP DATA LINK CAPABILITY
- PROVIDES DATA TRANSMISSION SPEEDS TO 4.0 MBPS
- ALLOWS ERROR CHECKING FOR CRC, UNDERRUN, OVERRUN, ABORTED OR INVALID FRAME ERRORS
- CONTAINS EXTENDABLE ADDRESS/CONTROL FIELD
- PERFORMS AUTOMATIC ZERO INSERTION AND DELETION
- USES SINGLE +5 VOLT POWER SOURCE
- 40 PIN DUAL-IN-LINE OR LEADED CHIP CARRIER FOR SMT
- PROVIDES ENHANCED DMA CAPABILITY/EOB OPTION
- ALLOWS VARIABLE CHARACTER LENGTH AND RESIDUAL CHARACTER CAPABILITY
- OFFERS PROGRAMMABLE MODEM CONTROL INTERRUPTS AND NRZI ENCODE/DECODE

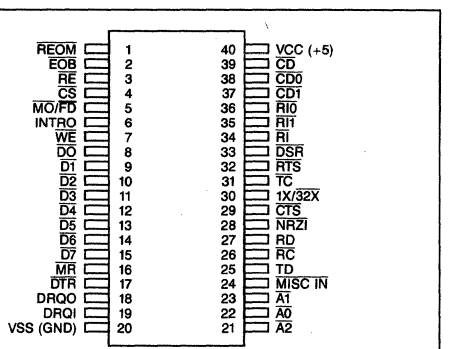
DESCRIPTION

The WD1935A is a programmable Synchronous Data Link Controller that facilitates the easy design of interfaces between a parallel digital system and a serial data communication channel and vice versa. This controller is capable of full and half duplex operation and is particularly suited to high speed applications.

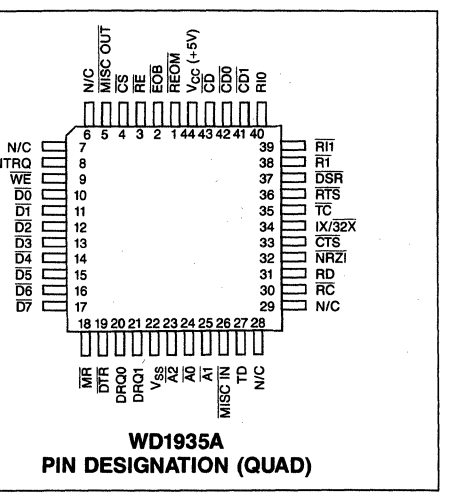
The 1935A is an NMOS/LSI device designed for bit-oriented SDLC, HDLC and other bit synchronous protocols. It is designed to be particularly efficient when used in DMA applications.

Applications include: computer to terminal communications, computer to modem interfacing, front end communications, message and packet switching, protocol converters, and communication test equipment.

The WD1935A is compatible with most eight bit microcomputers and can be connected directly to a microcomputer bus.



WD1935A
PIN DESIGNATION (DIP)



WD1935A
PIN DESIGNATION (QUAD)

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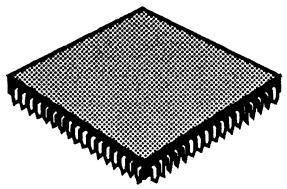
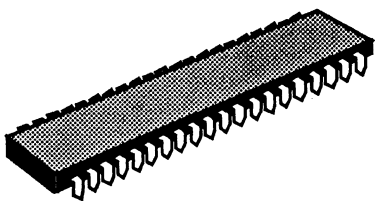
StarLAN HUB CONTROLLERS

WD83C503



StarLAN Mini-Hub Controller

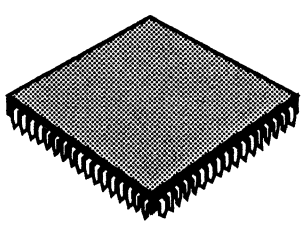
WD83C510A



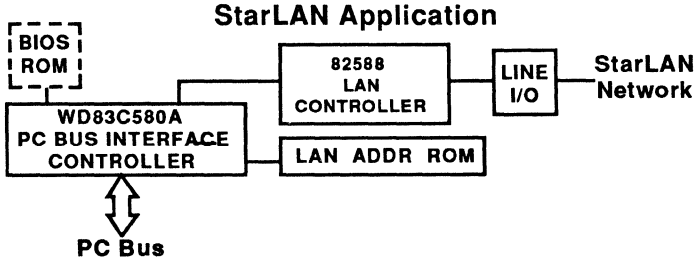
StarLAN Hub Controller

FEATURES	WD83C503	WD83C510A
• IEEE 802.3 1BASE5 StarLAN Compatible	X	X
• 1 MBPS Manchester Signal Regeneration	X	X
• Supports Hub Inputs	3	10
• Adds Hub Functions to StarLAN Station Adapters	X	
• Economical Repeater For StarLAN Network Extension	X	
• Cascadable For Larger Hubs Up To 40 Ports		X
• Allows 10 Hub Levels	X	X
• Automatic Detection Of Upper-Level Hub Presence	X	X
• Collision Detection And Signalling	X	X
• Ancillary Collision Detection Circuitry Input	X	X
• Carrier Sense Function	X	X
• Jabber Detection And Inhibit	X	X
• Built-In Network Diagnostic Functions	X	X
• Packaging	44-Pin PLCC	40-Pin DIP 44-Pin PLCC
• 5-Volt CMOS Technology	X	X

WD83C580A



StarLAN Application



FEATURES

- Handles PC Interrupt, DMA Functions And Data Bus Control For StarLAN Adapters
- Handles 82588 LAN Controller Interrupt, DMA, Chip Select And Reset
- Handles 82586 LAN Controller Interrupt, Channel Attention and Reset
- Supports BIOS ROM And LAN Address ROM
- Software-Controlled Wait State Insertion For PC Data Bus
- Handles Jumpers For I/O Base Address And DMA Configuration
- Internal Control And Status Register
- Integrates Typical SSI/MSI PC Bus Interface Logic
- 5-Volt CMOS Technology In 68-Pin PLCC

CM100/jlb

Western Digital

WESTERN DIGITAL

WD25C17 Enhanced Synchronous Data Link Controller

FEATURES:

- HDLC, SDLC, ADCCP, CCITT X.25, ISDN LAPD and SS7 capability
- Advanced CMOS technology
- SDLC loop mode capability
- Full/half duplex operation
- Up to 4.0 Mbps serial data rate
- Supports up to 8 logical channels for LAPD operation
- Programmable station address filtering
- Two receiver DMA channels and one transmitter DMA channel
- 8/16 bit DMA data bus to the memory buffer
- Two internal timers (T1 and T2)
- Programmable NRZI Encode/Decode option
- Digital Phase Locked Loop
- Full set of modem control signals
- Optional PCM Highway Interface supports from 32 to 128 time slots
- Programmable 16 Kbps rate adaption when used in PCM Interface Mode
- Up to 8K buffer length
- FLAG, ABORT and IDLE generation and detection
- Automatic FCS generation and checking
- Automatic Zero insertion and deletion
- Error detection on FCS error, transmitter underrun, receiver overrun, frame aborted and invalid frame (non-byte data and buffer length error)
- Generic CPU Host Interface
- Maintenance mode for self-testing
- TTL compatible I/O
- 68-pin package

APPLICATIONS:

- PBX and Central Offices switches
- Computer communications
- Terminal communications (POS, Teletex, Videotex, G IV FAX, etc.)
- Computer to modem interfacing
- Line controllers
- Front end communications
- Network processors
- Telecommunication switching networks
- Packet switching
- Data concentrators/Multiplexers
- Multidrop line systems
- Protocol converters/gateways

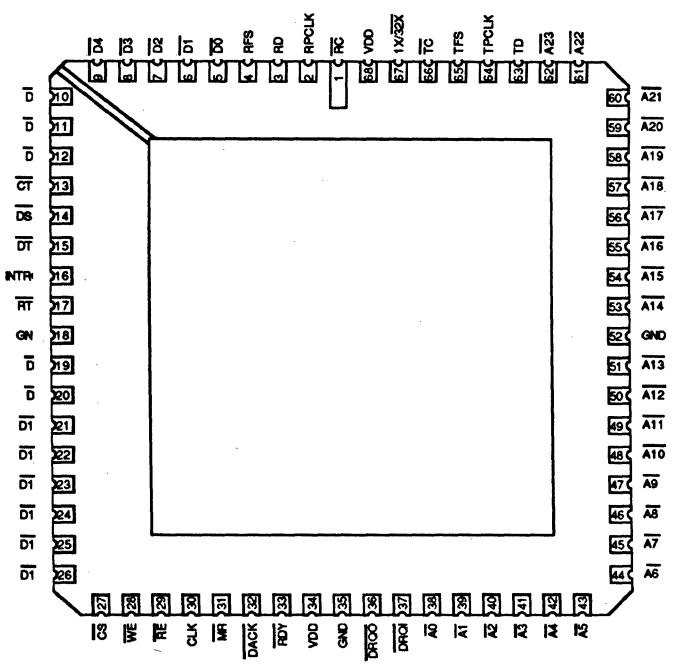


FIGURE 1: WD25C17 PIN DESIGNATION

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CM116/LB

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WD2512/2511A
X.25 Link Level Controllers

FEATURES

Managing the Communication Link

- HANDLES THE ENTIRE LINK LEVEL PROTOCOL OF CCITT X.25
- PROGRAMMABLE TIME OUT AND RETRANSMISSION PARAMETERS
- AUTOMATIC ERROR DETECTION AND DATA RETRANSMISSION
- AUTOMATIC FLOW CONTROL
- AUTOMATIC HANDLING OF ALL ADDRESS AND CONTROL FIELDS
- THE 2512 IS COMPATIBLE WITH THE 2511A
- BUILT-IN LOOPBACK TESTING
- CAN OPERATE AS A LAPB HALF-DUPLEX STATION

VLSI Design Provides Top Performance

- THE 2512 HAS TRANSMISSION SPEEDS AVAILABLE TO 2.048 MP/S
- THE 2511A HAS TRANSMISSION SPEEDS TO 1.1 MBPS
- BUILT-IN DUAL CHANNEL DMA
- ON CHIP BUFFER MANAGEMENT
- AVAILABLE IN 48-PIN DIP AND 68-PIN PLCC

WD2512 Extras

- SINGLE +5V SUPPLY
- LOWER POWER CONSUMPTION
- ENHANCED TO MEET THE DCNA GROUP IV FACSIMILE STANDARD FOR THE JAPANESE INS NETWORK

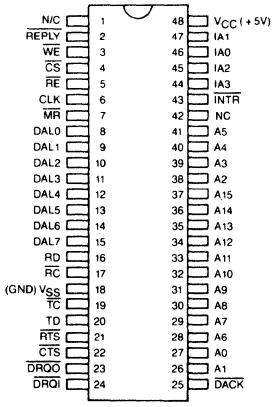
DESCRIPTION

The 2512 link level controller provides a low cost solution for managing data communication links for CCITT X.25, Group IV FAX, and teletex equipment. This controller was especially designed for packet switching networks. The design was based on a proven and certified implementation, the 2511A, the first complete implementation of the CCITT Recommendation X.25 LAPB protocol in a chip.

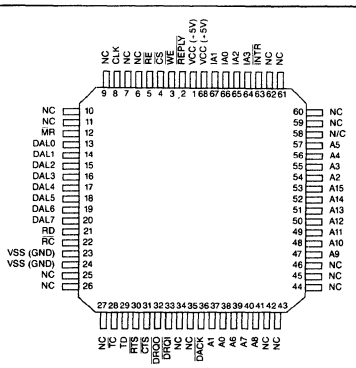
The 2512 is a NMOS LSI device which provides a unique solution for point-to-point communications.

It offloads the host by implementing the full link-layer protocol of the international standard recommendation X.25. This bit oriented, serial link controller automatically handles the transmission and reception of packets of data on two internal DMA channels, acknowledges the receipts of error free packets, and requests that lost or erroneous packets be retransmitted.

The host is interrupted after receiving an error free packet, after receiving acknowledgement of a transmitted packet, and after detecting certain error or abnormal conditions on the link.



WD2512 PIN DESIGNATION (DIP)
(Pin 42 on the 2511A has a V_{DD} (+12V) connection)



WD2512 PIN DESIGNATION (QUAD)
(for 2511A pin-out, contact WD)

Product specifications subject to change without notice.

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WESTERN DIGITAL

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WESTERN DIGITAL

Dual Enhanced Asynchronous Communications Element WD16C452/552

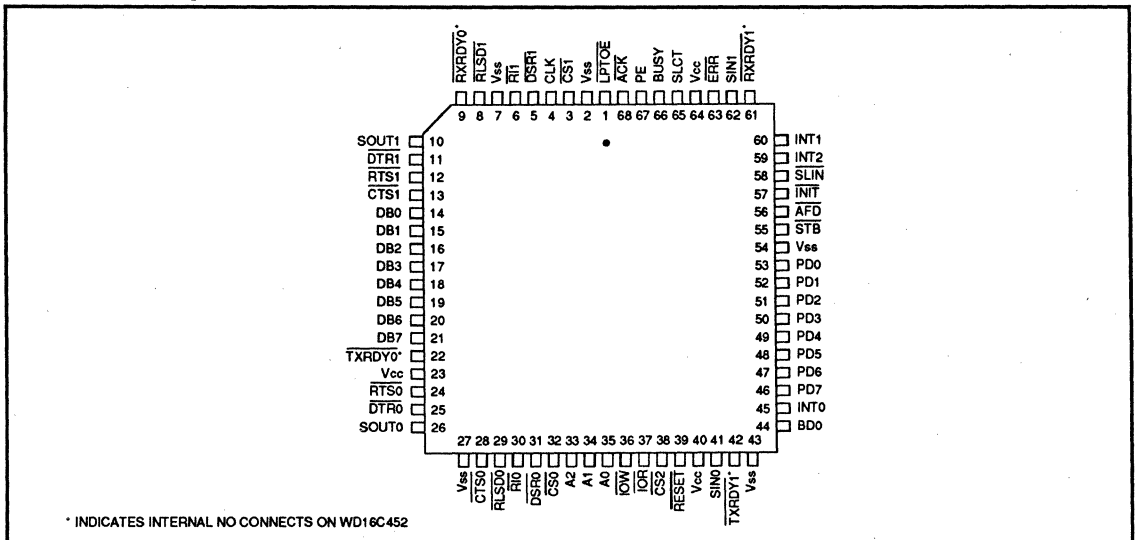
Features

- Two fully programmable serial I/O channels (dc to 512K Baud).
- THREE-STATE TTL drive capabilities for bi-directional data bus and control bus on each channel.
- Loopback controls for communications link fault isolation for each ACE.
- Line break generation and detection for each ACE.
- Complete status reporting capabilities.
- Generation and stripping of serial asynchronous data control bits (start, stop, parity).
- Programmable baud rate generators and modem control signals for each channel.
- Fully prioritized independent interrupt system controls for each channel.
- 16 byte FIFO buffers on both transmit and receive of each channel for CPU relief during high speed data transfer. †
- Programmable FIFO threshold Levels of 1, 4, 8, or 14 bytes on each channel. †
- Two modes of DMA signaling available for transfer of data characters to and from FIFO buffers. †
- Fully bi-directional Centronics compatible parallel port for direct printer interface.
- CMOS implementation for high speed and low power requirements.
- 68-pin QUAD package.

Description

The low power CMOS WD16C452/552 is a single device solution for serving two serial input/output ports simultaneously and one fully bi-directional parallel port for the IBM* PC, PC XT, PC AT*, PS/2*, and compatible systems. The parallel port is fully compatible to the Centronics printer port and IBM Serial/Parallel Adapter. Each Asynchronous Communications Element (ACE) is fully programmable. Each ACE in the WD16C552 is capable of buffering up to 16 bytes of data for transmission, and up to 16 bytes of data upon reception relieving the CPU of interrupt overhead. Buffering of data also allows greater latency time in interrupt servicing, which is vital in a multitasking environment. DMA signaling, between the internal FIFO buffers and host CPU, allows single or multiple character transfers. Each ACE has a maximum recommended data rate of 512K with a clock frequency of 8.0 MHz.

(*) IBM , PS/2, and AT are registered trademarks of International Business Machines Incorporated.
† The FIFO mode of operation is not available in the WD16C452.



WD16C452/552 PIN DESCRIPTION (PLCC)

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Enhanced X.25 Protocol Controller WD25C84

Features

- Complete support of CCITT, 1984 X.25 link procedure/LAPB.
- Supports single channel LAPD.
- XID frames capability.
- Data rates up to 3.1 Mbps.
- Automatic Error Detection and Data retransmission.
- Direct Memory Access for Transmit and Receive Channels.
- On-board buffer memory manager.
- Internal and External loop back mode for diagnostic purposes.
- 16 bits host Data bus and 24 bits host Address bus.
- Easily interfaces to 8086/80186 and 68000/68010 microprocessors.
- Fully TTL and CMOS compatible inputs/outputs.
- Advanced CMOS technology.
- 68 pin PLCC package.

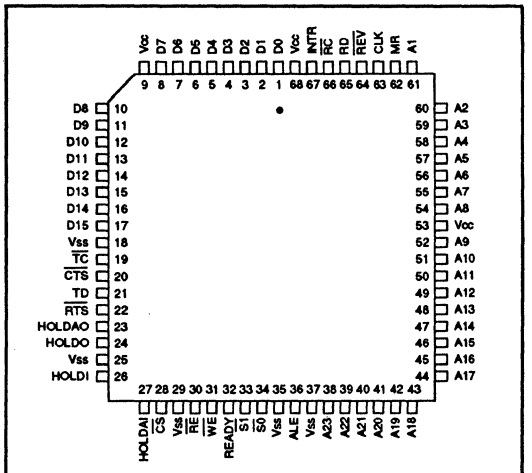
Description

The WD25C84 provides a low cost solution for the management and control of data communication links for CCITT 1984 X.25 and TELETEX applications.

This device is specially designed for packet switching networks and is based on Western Digital's extensive experience with Data Communications devices and X.25 controllers in particular.

The WD25C84 is a 68 pin device, fabricated using advanced 1.25 µm CMOS technology to provide the high speed and low power dissipation required in todays point-to-point Data Communications. It offloads the host by implementing the full link layer protocol of the international standard, the 1984 recommendation for the X.25/LAPB. It is a bit oriented Serial Link Controller which automatically handles the transmission and reception of data packets. The WD25C84 accomplishes this by using two internal, high speed DMA channels, acknowledges the reception of error free packets, and request that missing or erroneous packets be retransmitted. The host CPU will be interrupted by the WD25C84 after the reception of an error free packet, after receiving acknowledgement for a previously transmitted packet, and after detecting certain errors or abnormal conditions on the link. Interfacing to the 8086/80186 and the 68000/68010 architectures is easily accomplished by the WD25C84 device with the internal reversal of bytes within a word, before transferred to memory.

The WD25C84 has the ability to receive and transmit non-LAPB/LAPD frames using transparent modes. These transparent modes allow the device to pass through all frames or just those frames addressed to the individual node.



PIN DESIGNATION

Applications

The WD25C84 can be used on dedicated or switched lines whenever reliable error free communications are needed.

Useful applications:
- Modems
- Packet Switches
- PADs
- Statistical Multiplexers
- Teletex terminals
- Gateways
- Protocol converters
- Satellite communications
- Computer-to-Computer communications

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C98809
WD2110C 10/88 2.5M

WD83C690/WD83C691/WD83B692
WD Ethernet Chip Set

WD83C690 DESCRIPTION

The WD83C690 network interface controller implements the 802.3 protocol for networks such as Ethernet, Cheapernet, StarLAN, and IBM PC Network Baseband. The WD83C690 implements all Media Access Control layer functions for transmission and reception of data packets.

Two full duplex DMA channels have been integrated into the WD83C690 for data transfer from the WD83C690 to memory and memory to the host CPU.

The WD83C690 has internal codecs for Manchester and differential Manchester coding and decoding at data rates of 1 or 2 Mbps for implementation of StarLAN and IBM PC Network Baseband systems, respectively.

WD83C691 DESCRIPTION

The WD83C691 Ethernet data separator (EDS) provides Manchester data encoding and decoding functions for IEEE 802.3 Ethernet/Cheapernet type local area networks. The EDS interfaces the WD83C690 Network Interface Controller to the Ethernet transceiver. The differential line drivers can drive up to 50 meters of twisted pair AUI Ethernet transceiver cable.

The WD83C691 EDS is a complete Manchester encoder/decoder including ECL-like balanced drivers and receivers, on-board crystal oscillator, collision signal translator and loopback circuitry for diagnostics implementation.

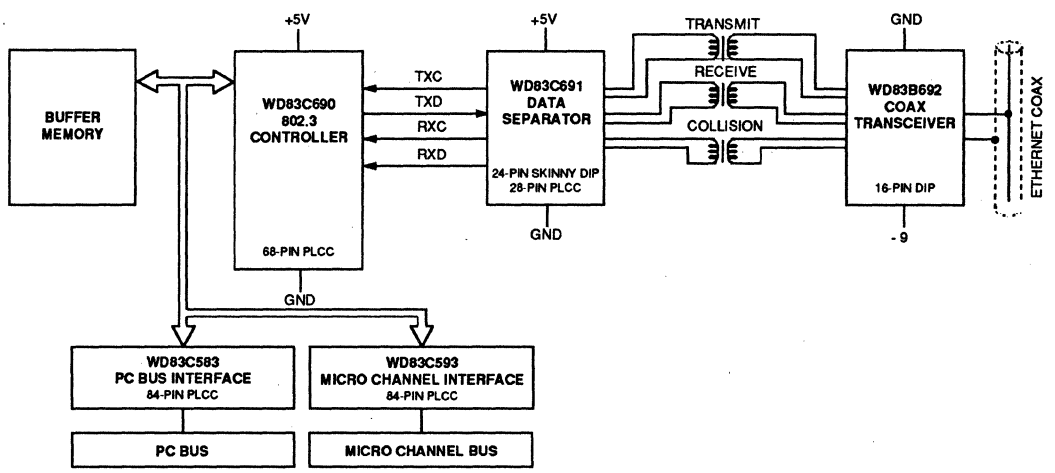
WD83B692 DESCRIPTION

The WD83B692 Ethernet Input/Output device (EIO) is used as a coaxial cable line driver/receiver for Ethernet and Cheapernet type local area networks.

In Ethernet applications, the EIO is part of the Media Attachment Unit (MAU) that connects directly to the coaxial transmission media and communicates with the Media Access Controller Unit (MAC) thru an Attachment Unit Interface (AUI) cable. In Cheapernet applications, the EIO device is embedded in the MAC with the transmission cable connected directly between MACs.

All Ethernet Chip Sets meet Ethernet II, IEEE 802.3 10BASE 5 and 10BASE2 specifications.

WD Ethernet Chip Set



- Implements a complete IEEE 802.3 compatible network node interface.
- 10 Mbps maximum data rates, CSMA/CD.
- High speed dual DMA controllers for efficient memory management.
- Provides Manchester data encoding and decoding with clock recovery.
- Low power CMOS technology used in the WD83C690 and WD83C691.

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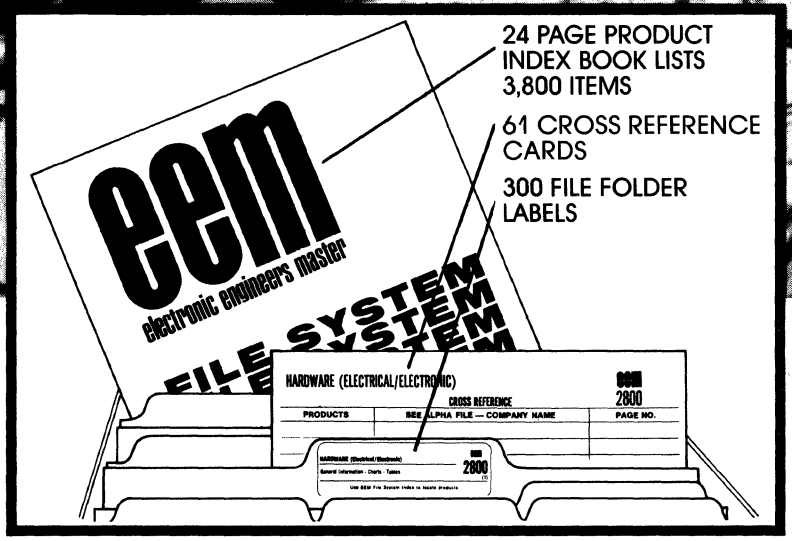

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Memory Overview

Since its founding, Xicor has developed and placed into production a wide range of system-alterable nonvolatile memory devices. These devices, manufactured with Xicor's proprietary state-of-the-art textured triple-poly floating gate process, are available in a variety of architectures (NOVRAM* and E^2PROM), interfaces (nibble-wide, byte-wide and serial), densities, and speeds. Xicor's success as an innovator and leader in system-alterable nonvolatile memory is affirmed with an *Electronic Product Magazine* Product of the Year award in 1980 and again in 1982 for the first 5-volt only NOVRAM and the first 5-volt only full featured E^2PROM, respectively.

Lower density E^2PROMs and NOVRAMs have been readily available for a number of years and have provided unique niche applications solutions. Serial devices have replaced DIP switches in a wide range of products that offer user selectable operating parameters. Nibble-wide and byte-wide NOVRAMs and E^2PROMs are being used in instrumentation and industrial control applications to store calibration data and control information. Communications equipment has implemented these same devices to store phone numbers in repertory dialers and antenna positioning equipment.

The list of first generation applications goes on at length; however, with the second generation represented by the X2864A, the direction of applications began to diverge. The higher density allowed practical usage of E^2PROMs in program and mass data storage. The advent of the X28256 has pushed this application usage even higher.

Xicor strives to serve the marketplace by providing next generation devices in existing product areas as evidenced by the X2864B and X2864H high speed 64K E^2PROMs. Similarly, the X24C16 and X24C04 maintain compatibility with the original X2404 but offer low power operation over a much wider V_{CC} range.

As designers have gained experience implementing the denser E^2PROM devices into system memories, they have given Xicor feedback on features they would like. Xicor has listened.

Xicor's response has been active. The issues addressed by the Xicor design team have been: faster read access time, faster write cycle time, denser memory devices and write protection mechanisms.

Xicor has also implemented added features via software control rather than "dedicated pin" hardware control for optional system use. Xicor is committed to providing solutions that neither hinder nor limit the system designer's imagination. The products and features shown in the data sheets in this data book illustrate Xicor's dedication to listening to you, the designer, in providing memory design solutions.

*NOVRAM is Xicor's nonvolatile static RAM device.

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NOVRAMs*

Part Number	Organization	Access Time	Power		Store Cycles	Temp. Range(s)	Package									
			Active	Standby			S	P	D	C	F1	F2	K	J	E	G
X2201A	1024 x 1	300 ns	60 mA	N/A	10,000	†			•							
X2210	64 x 4	300 ns	50 mA	N/A	10,000	†		•	•							
X2210/5	64 x 4	300 ns	50 mA	N/A	50,000	†		•	•							
X2210/10	64 x 4	300 ns	50 mA	N/A	100,000	†		•	•							
X2210I	64 x 4	300 ns	55 mA	N/A	10,000	I		•	•							
X2210I/5	64 x 4	300 ns	55 mA	N/A	50,000	I		•	•							
X2210I/10	64 x 4	300 ns	55 mA	N/A	100,000	I		•	•							
X2210M**	64 x 4	300 ns	55 mA	N/A	10,000	M			•							
X2210M/5**	64 x 4	300 ns	55 mA	N/A	50,000	M			•							
X2210M/10**	64 x 4	300 ns	55 mA	N/A	100,000	M			•							
X2212	256 x 4	300 ns	60 mA	N/A	10,000	†		•	•							
X2212/5	256 x 4	300 ns	60 mA	N/A	50,000	†		•	•							
X2212/10	256 x 4	300 ns	60 mA	N/A	100,000	†		•	•							
X2212I	256 x 4	300 ns	70 mA	N/A	10,000	I		•	•							
X2212I/5	256 x 4	300 ns	70 mA	N/A	50,000	I		•	•							
X2212I/10	256 x 4	300 ns	70 mA	N/A	100,000	I		•	•							
X2212M**	256 x 4	300 ns	70 mA	N/A	10,000	M			•							
X2212M/5**	256 x 4	300 ns	70 mA	N/A	50,000	M			•							
X2212M/10**	256 x 4	300 ns	70 mA	N/A	100,000	M			•							

N/A = Not Applicable

Key:
** = MIL-STD-883 Rev. C, Class B Compliant

† = Blank = Commercial = 0°C to +70°C
I = Industrial = −40°C to +85°C
M = Military = −55°C to +125°C

S = Plastic Small Outline Gull Wing
P = 18-Lead Plastic DIP
D = 18-Lead Cerdip
C = Side Braze
F1 = Ceramic Flat Pack for X2864A, X2864B, X2864H and X28C64
F2 = Ceramic Flat Pack for X28C256 and X28C256B
K = Ceramic Pin Grid Array
J = J-Hook Plastic Leaded Chip Carrier
E = Ceramic Leadless Chip Carrier (Solder Seal)
G = Ceramic Leadless Chip Carrier (Glass Frit Seal)

*NOVRAM is Xicor's nonvolatile static RAM device.

Reference and Package Guide to Xicor Nonvolatile Memories

NOVRAMs (Byte-Wide)

Part Number	Organization	Access Time	Power		Store Cycles	Temp. Range(s)	Package									
			Active	Standby			S	P	D	C	F1	F2	K	J	E	G
X2001-20	128 x 8	200 ns	80 mA	50 mA	100,000	†		●								
X2001-25	128 x 8	250 ns	80 mA	50 mA	100,000	†		●								
X2001	128 x 8	300 ns	80 mA	50 mA	100,000	†		●								
X2001I-20	128 x 8	200 ns	100 mA	65 mA	100,000	I		●								
X2001I-25	128 x 8	250 ns	100 mA	65 mA	100,000	I		●								
X2001I	128 x 8	300 ns	100 mA	65 mA	100,000	I		●								

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I = Industrial = −40°C to +85°C
M = Military = −55°C to +125°C

S = Plastic Small Outline Gull Wing
P = 24-Lead Plastic DIP
D = Cerdip
C = Side Braze
F1 = Ceramic Flat Pack for X2864A, X2864B, X2864H and X28C64
F2 = Ceramic Flat Pack for X28C256 and X28C256B
K = Ceramic Pin Grid Array
J = J-Hook Plastic Leaded Chip Carrier
E = Ceramic Leadless Chip Carrier (Solder Seal)
G = Ceramic Leadless Chip Carrier (Glass Frit Seal)

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NOVRAMs (Byte-Wide) (Continued)

Part Number	Organization	Access Time	Power		Store Cycles	Temp. Range(s)	Package									
			Active	Standby			S	P	D	C	F1	F2	K	J	E	G
X2004-20	512 x 8	200 ns	100 mA	55 mA	100,000	†			•					•	•	
X2004-25	512 x 8	250 ns	100 mA	55 mA	100,000	†			•					•	•	
X2004	512 x 8	300 ns	100 mA	55 mA	100,000	†			•					•	•	
X2004I-20	512 x 8	200 ns	120 mA	90 mA	100,000	I			•					•	•	
X2004I-25	512 x 8	250 ns	120 mA	90 mA	100,000	I			•					•	•	
X2004I	512 x 8	300 ns	120 mA	90 mA	100,000	I			•					•	•	
X2004M-25**	512 x 8	250 ns	120 mA	90 mA	100,000	M			•				•		•	•
X2004M**	512 x 8	300 ns	120 mA	90 mA	100,000	M			•				•		•	•

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E = 32-Pad Ceramic Leadless Chip Carrier (Solder Seal)
G = 32-Pad Ceramic Leadless Chip Carrier (Glass Frit Seal)

Reference and Package Guide to Xicor Nonvolatile Memories

SERIAL NOVRAMs

Part Number	Organization	CLK Frequency	Power			Store Cycles	Temp. Range(s)	Package									
			Active	Standby	Sleep			S	P	D	C	F1	F2	K	J	E	G
X2444	16 x 16	1 MHz	15 mA	10 mA	7 mA	100,000	†	•	•	•							
X2444I	16 x 16	1 MHz	25 mA	15 mA	10 mA	100,000	I	•	•	•							
X2444M**	16 x 16	1 MHz	25 mA	15 mA	10 mA	100,000	M		•	•							

Key:
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M = Military = −55°C to +125°C

S = 8-Lead Plastic Small Outline Gull Wing
P = 8-Lead Plastic DIP
D = 8-Lead Cerdip
C = Side Braze
F1 = Ceramic Flat Pack for X2864A, X2864B, X2864H and X28C64
F2 = Ceramic Flat Pack for X28C256 and X28C256B
K = Ceramic Pin Grid Array
J = J-Hook Plastic Leaded Chip Carrier
E = Ceramic Leadless Chip Carrier (Solder Seal)
G = Ceramic Leadless Chip Carrier (Glass Frit Seal)

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SERIAL E²PROMs

Part Number	Organization	Page Size (# Bytes)	CLK Frequency	Power		Temp. Range(s)	Package									
				Active	Standby		S	P	D	C	F1	F2	K	J	E	G
X2402	256 x 8	8	100 KHz	30 mA	25 mA	†	•	•	•							
X2402I	256 x 8	8	100 KHz	35 mA	30 mA	I	•	•	•							
X2402M	256 x 8	8	100 KHz	35 mA	30 mA	M			•							
X2404	512 x 8	8	100 KHz	30 mA	25 mA	†	•	•	•							
X2404I	512 x 8	8	100 KHz	35 mA	30 mA	I	•	•	•							
X2404M**	512 x 8	8	100 KHz	35 mA	30 mA	M			•							
X24C04	512 x 8	16	100 KHz	3 mA	100 μA	†	•	•	•							
X24C04I	512 x 8	16	100 KHz	3 mA	100 μA	I	•	•	•							
X24C04M	512 x 8	16	100 KHz	3 mA	100 μA	M			•							
X24C16	2048 x 8	16	100 KHz	3 mA	100 μA	†	•	•	•							
X24C16I	2048 x 8	16	100 KHz	3 mA	100 μA	I	•	•	•							
X24C16M**	2048 x 8	16	100 KHz	3 mA	100 μA	M			•							

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I = Industrial = −40°C to +85°C
M = Military = −55°C to +125°C

S = 14-Lead Plastic Small Outline Gull Wing
P = 8-Lead Plastic DIP
D = 8-Lead Cerdip
C = Side Braze
F1 = Ceramic Flat Pack for X2864A, X2864B, X2864H and X28C64
F2 = Ceramic Flat Pack for X28C256 and X28C256B
K = Ceramic Pin Grid Array
J = J-Hook Plastic Leaded Chip Carrier
E = Ceramic Leadless Chip Carrier (Solder Seal)
G = Ceramic Leadless Chip Carrier (Glass Frit Seal)

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4K E²PROMs

Part Number	Organization	Page Size (# Bytes)	Access Time	Power		Temp. Range(s)	Package									
				Active	Standby		S	P	D	C	F1	F2	K	J	E	G
X2804A-25	512 x 8	N/A	250 ns	80 mA	50 mA	†		•	•							
X2804A	512 x 8	N/A	300 ns	80 mA	50 mA	†		•	•							
X2804A-35	512 x 8	N/A	350 ns	80 mA	50 mA	†		•	•							
X2804A-45	512 x 8	N/A	450 ns	80 mA	50 mA	†		•	•							
X2804AI-25	512 x 8	N/A	250 ns	100 mA	60 mA	I		•	•							
X2804AI	512 x 8	N/A	300 ns	100 mA	60 mA	I		•	•							
X2804AI-35	512 x 8	N/A	350 ns	100 mA	60 mA	I		•	•							
X2804AI-45	512 x 8	N/A	450 ns	100 mA	60 mA	I		•	•							
X2804AM**	512 x 8	N/A	300 ns	100 mA	60 mA	M			•							
X2804AM-35**	512 x 8	N/A	350 ns	100 mA	60 mA	M			•							
X2804AM-45**	512 x 8	N/A	450 ns	100 mA	60 mA	M			•							

N/A = Not Applicable

Key:
** = MIL-STD-883 Rev. C, Class B Compliant

† = Blank = Commercial = 0°C to +70°C
I = Industrial = −40°C to +85°C
M = Military = −55°C to +125°C

S = Plastic Small Outline Gull Wing
P = 24-Lead Plastic DIP
D = 24-Lead Cerdip
C = Side Braze
F1 = Ceramic Flat Pack for X2864A, X2864B, X2864H and X28C64
F2 = Ceramic Flat Pack for X28C256 and X28C256B
K = Ceramic Pin Grid Array
J = J-Hook Plastic Leaded Chip Carrier
E = Ceramic Leadless Chip Carrier (Solder Seal)
G = Ceramic Leadless Chip Carrier (Glass Frit Seal)

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16K E²PROMs

Part Number	Organization	Page Size (# Bytes)	Access Time	Power		Temp. Range(s)	Package									
				Active	Standby		S	P	D	C	F1	F2	K	J	E	G
X2816AM**	2048 x 8	N/A	300 ns	140 mA	60 mA	M			•						•	
X2816AM-35**	2048 x 8	N/A	350 ns	140 mA	60 mA	M			•						•	
X2816AM-45**	2048 x 8	N/A	450 ns	140 mA	60 mA	M			•						•	

16K E²PROMs (Continued)

Part Number	Organization	Page Size (# Bytes)	Access Time	Power		Temp. Range(s)	Package									
				Active	Standby		S	P	D	C	F1	F2	K	J	E	G
X2816B-25	2048 x 8	16	250 ns	120 mA	60 mA	†		•	•				•	•	•	
X2816B	2048 x 8	16	300 ns	120 mA	60 mA	†		•	•				•	•	•	
X2816BI-25	2048 x 8	16	250 ns	140 mA	70 mA	I		•	•				•	•	•	
X2816BI	2048 x 8	16	300 ns	140 mA	70 mA	I		•	•				•	•	•	
X2816BM-25**	2048 x 8	16	250 ns	140 mA	70 mA	M			•				•		•	
X2816BM**	2048 x 8	16	300 ns	140 mA	70 mA	M			•				•		•	

N/A = Not Applicable

Key:
** = MIL-STD-883 Rev. C, Class B Compliant

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I = Industrial = −40°C to +85°C
M = Military = −55°C to +125°C

S = Plastic Small Outline Gull Wing
P = 24-Lead Plastic DIP
D = 24-Lead Cerdip
C = Side Braze
F1 = Ceramic Flat Pack for X2864A, X2864B, X2864H and X28C64
F2 = Ceramic Flat Pack for X28C256 and X28C256B
K = 28-Pin Ceramic Pin Grid Array
J = 32-Lead J-Hook Plastic Leaded Chip Carrier
E = 32-Pad Ceramic Leadless Chip Carrier (Solder Seal)
G = Ceramic Leadless Chip Carrier (Glass Frit Seal)

64K E²PROMs

Part Number	Organization	Page Size (# Bytes)	Access Time	Power		Temp. Range(s)	Package								
				Active	Standby		S	P	D	C	F1	F2	K	J	E	G
X2864A-25	8192 x 8	16	250 ns	140 mA	60 mA	†		•	•		•			•	•	•
X2864A	8192 x 8	16	300 ns	140 mA	60 mA	†		•	•		•			•	•	•
X2864A-35	8192 x 8	16	350 ns	140 mA	60 mA	†		•	•		•			•	•	•
X2864A-45	8192 x 8	16	450 ns	140 mA	60 mA	†		•	•		•			•	•	•
X2864AI-25	8192 x 8	16	250 ns	140 mA	70 mA	I		•	•		•			•	•	•
X2864AI	8192 x 8	16	300 ns	140 mA	70 mA	I		•	•		•			•	•	•
X2864AI-35	8192 x 8	16	350 ns	140 mA	70 mA	I		•	•		•			•	•	•
X2864AI-45	8192 x 8	16	450 ns	140 mA	70 mA	I		•	•		•			•	•	•
X2864AM-25**	8192 x 8	16	250 ns	140 mA	70 mA	M			•		•				•	•
X2864AM**	8192 x 8	16	300 ns	140 mA	70 mA	M			•		•				•	•
X2864AM-35**	8192 x 8	16	350 ns	140 mA	70 mA	M			•		•				•	•
X2864AM-45**	8192 x 8	16	450 ns	140 mA	70 mA	M			•		•				•	•

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S = Plastic Small Outline Gull Wing
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D = 28-Lead Cerdip
C = Side Braze
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K = Ceramic Pin Grid Array
J = 32-Lead J-Hook Plastic Leaded Chip Carrier
E = 32-Pad Ceramic Leadless Chip Carrier (Solder Seal)
G = 32-Pad Ceramic Leadless Chip Carrier (Glass Frit Seal)

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64K E²PROMs (Continued)

Part Number	Organization	Page Size (# Bytes)	Access Time	Power		Temp. Range(s)	Package									
				Active	Standby		S	P	D	C	F1	F2	K	J	E	G
X2864B-12	8192 x 8	32	120 ns	150 mA	80 mA	†		•	•		•		•	•	•	•
X2864B-15	8192 x 8	32	150 ns	150 mA	80 mA	†		•	•		•		•	•	•	•
X2864B-18	8192 x 8	32	180 ns	150 mA	80 mA	†		•	•		•		•	•	•	•
X2864BI-12	8192 x 8	32	120 ns	150 mA	80 mA	I		•	•		•		•	•	•	•
X2864BI-15	8192 x 8	32	150 ns	150 mA	80 mA	I		•	•		•		•	•	•	•
X2864BI-18	8192 x 8	32	180 ns	150 mA	80 mA	I		•	•		•		•	•	•	•
X2864BM-12**	8192 x 8	32	120 ns	150 mA	80 mA	M			•		•		•		•	•
X2864BM-15**	8192 x 8	32	150 ns	150 mA	80 mA	M			•		•		•		•	•
X2864BM-18**	8192 x 8	32	180 ns	150 mA	80 mA	M			•		•		•		•	•

64K E²PROMs (Continued)

Part Number	Organization	Page Size (# Bytes)	Access Time	Power		Temp. Range(s)	Package									
				Active	Standby		S	P	D	C	F1	F2	K	J	E	G
X2864H-70	8192 x 8	32	70 ns	150 mA	80 mA	†		•	•		•		•	•	•	•
X2864H-90	8192 x 8	32	90 ns	150 mA	80 mA	†		•	•		•		•	•	•	•
X2864HI-90	8192 x 8	32	90 ns	150 mA	80 mA	I		•	•		•		•	•	•	•
X2864HM-90**	8192 x 8	32	90 ns	150 mA	80 mA	M			•		•		•		•	•

Xicor

Key:
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S = Plastic Small Outline Gull Wing
P = 28-Lead Plastic DIP
D = 28-Lead Cerdip
C = Side Braze
F1 = 28-Lead Ceramic Flat Pack for X2864A, X2864B, X2864H and X28C64
F2 = Ceramic Flat Pack for X28C256 and X28C256B
K = 28-Pin Ceramic Pin Grid Array
J = 32-Lead J-Hook Plastic Leaded Chip Carrier
E = 32-Pad Ceramic Leadless Chip Carrier (Solder Seal)
G = 32-Pad Ceramic Leadless Chip Carrier (Glass Frit Seal)

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64K E²PROMs (Continued)

Part Number	Organization	Page Size (# Bytes)	Access Time	Power		Temp. Range(s)	Package									
				Active	Standby		S	P	D	C	F1	F2	K	J	E	G
X28C64-20	8192 x 8	64	200 ns	60 mA	200 µA	†		•	•		•		•	•	•	•
X28C64-25	8192 x 8	64	250 ns	60 mA	200 µA	†		•	•		•		•	•	•	•
X28C64	8192 x 8	64	300 ns	60 mA	200 µA	†		•	•		•		•	•	•	•
X28C64-35	8192 x 8	64	350 ns	60 mA	200 µA	†		•	•		•		•	•	•	•
X28C64I-20	8192 x 8	64	200 ns	60 mA	200 µA	I		•	•		•		•	•	•	•
X28C64I-25	8192 x 8	64	250 ns	60 mA	200 µA	I		•	•		•		•	•	•	•
X28C64I	8192 x 8	64	300 ns	60 mA	200 µA	I		•	•		•		•	•	•	•
X28C64I-35	8192 x 8	64	350 ns	60 mA	200 µA	I		•	•		•		•	•	•	•
X28C64M-20	8192 x 8	64	200 ns	60 mA	200 µA	M			•		•		•		•	•
X28C64M-25	8192 x 8	64	250 ns	60 mA	200 µA	M			•		•		•		•	•
X28C64M	8192 x 8	64	300 ns	60 mA	200 µA	M			•		•		•		•	•
X28C64M-35	8192 x 8	64	350 ns	60 mA	200 µA	M			•		•		•		•	•

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C = Side Braze
F1 = 28-Lead Ceramic Flat Pack for X2864A, X2864B, X2864H and X28C64
F2 = Ceramic Flat Pack for X28C256 and X28C256B
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J = 32-Lead J-Hook Plastic Leaded Chip Carrier
E = 32-Pad Ceramic Leadless Chip Carrier (Solder Seal)
G = 32-Pad Ceramic Leadless Chip Carrier (Glass Frit Seal)

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256K E²PROMs

Part Number	Organization	Page Size (# Bytes)	Access Time	Power		Temp. Range(s)	Package								
				Active	Standby		S	P	D	C	F1	F2	K	J	E	G
X28256-25	32768 x 8	64	250 ns	120 mA	60 mA	†		•	•					•	•	•
X28256	32768 x 8	64	300 ns	120 mA	60 mA	†		•	•					•	•	•
X28256-35	32768 x 8	64	350 ns	120 mA	60 mA	†		•	•					•	•	•
X28256I-25	32768 x 8	64	250 ns	120 mA	60 mA	I		•	•					•	•	•
X28256I	32768 x 8	64	300 ns	120 mA	60 mA	I		•	•					•	•	•
X28256I-35	32768 x 8	64	350 ns	120 mA	60 mA	I		•	•					•	•	•
X28256M-25**	32768 x 8	64	250 ns	120 mA	60 mA	M			•						•	•
X28256M**	32768 x 8	64	300 ns	120 mA	60 mA	M			•						•	•
X28256M-35**	32768 x 8	64	350 ns	120 mA	60 mA	M			•						•	•

Key:
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M = Military = −55°C to +125°C

S = Plastic Small Outline Gull Wing
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D = 28-Lead Cerdip
C = Side Braze
F1 = Ceramic Flat Pack for X2864A, X2864B, X2864H and X28C64
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K = Ceramic Pin Grid Array
J = 32-Lead J-Hook Plastic Leaded Chip Carrier
E = 32-Pad Ceramic Leadless Chip Carrier (Solder Seal)
G = 32-Pad Ceramic Leadless Chip Carrier (Glass Frit Seal)

256K E²PROMs (Continued)

Part Number	Organization	Page Size (# Bytes)	Access Time	Power		Temp. Range(s)	Package									
				Active	Standby		S	P	D	C	F1	F2	K	J	E	G
X28C256-20	32768 x 8	64	200 ns	60 mA	200 µA	†		•	•			•	•	•	•	•
X28C256-25	32768 x 8	64	250 ns	60 mA	200 µA	†		•	•			•	•	•	•	•
X28C256	32768 x 8	64	300 ns	60 mA	200 µA	†		•	•			•	•	•	•	•
X28C256-35	32768 x 8	64	350 ns	60 mA	200 µA	†		•	•			•	•	•	•	•
X28C256I-20	32768 x 8	64	200 ns	60 mA	200 µA	I		•	•			•	•	•	•	•
X28C256I-25	32768 x 8	64	250 ns	60 mA	200 µA	I		•	•			•	•	•	•	•
X28C256I	32768 x 8	64	300 ns	60 mA	200 µA	I		•	•			•	•	•	•	•
X28C256I-35	32768 x 8	64	350 ns	60 mA	200 µA	I		•	•			•	•	•	•	•
X28C256M-20**	32768 x 8	64	200 ns	60 mA	200 µA	M			•			•	•		•	•
X28C256M-25**	32768 x 8	64	250 ns	60 mA	200 µA	M			•			•	•		•	•
X28C256M**	32768 x 8	64	300 ns	60 mA	200 µA	M			•			•	•		•	•
X28C256M-35**	32768 x 8	64	350 ns	60 mA	200 µA	M			•			•	•		•	•

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** = MIL-STD-883 Rev. C, Class B Compliant

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I = Industrial = −40°C to +85°C
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S = Plastic Small Outline Gull Wing
P = 28-Lead Plastic DIP
D = 28-Lead Cerdip
C = Side Braze
F1 = Ceramic Flat Pack for X2864A, X2864B, X2864H and X28C64
F2 = 28-Lead Ceramic Flat Pack for X28C256 and X28C256B
K = 28-Pin Ceramic Pin Grid Array
J = 32-Lead J-Hook Plastic Leaded Chip Carrier
E = 32-Pad Ceramic Leadless Chip Carrier (Solder Seal)
G = 32-Pad Ceramic Leadless Chip Carrier (Glass Frit Seal)

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256K E²PROMs (Continued)

Part Number	Organization	Page Size (# Bytes)	Access Time	Power		Temp. Range(s)	Package									
				Active	Standby		S	P	D	C	F1	F2	K	J	E	G
X28C256B-15	32768 x 8	64	150 ns	60 mA	200 μA	†		•	•			•	•	•	•	•
X28C256B-18	32768 x 8	64	180 ns	60 mA	200 μA	†		•	•			•	•	•	•	•
X28C256BI-15	32768 x 8	64	150 ns	60 mA	200 μA	I		•	•			•	•	•	•	•
X28C256BI-18	32768 x 8	64	180 ns	60 mA	200 μA	I		•	•			•	•	•	•	•
X28C256BM-15	32768 x 8	64	150 ns	60 mA	200 μA	M			•			•	•		•	•
X28C256BM-18	32768 x 8	64	180 ns	60 mA	200 μA	M			•			•	•		•	•

Key:
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I = Industrial = −40°C to +85°C
M = Military = −55°C to +125°C

S = Plastic Small Outline Gull Wing
P = 28-Lead Plastic DIP
D = 28-Lead Cerdip
C = Side Braze
F1 = Ceramic Flat Pack for X2864A, X2864B, X2864H and X28C64
F2 = 28-Lead Ceramic Flat Pack for X28C256 and X28C256B
K = 28-Pin Ceramic Pin Grid Array
J = 32-Lead J-Hook Plastic Leaded Chip Carrier
E = 32-Pad Ceramic Leadless Chip Carrier (Solder Seal)
G = 32-Pad Ceramic Leadless Chip Carrier (Glass Frit Seal)

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1M E²PROMs

Part Number	Organization	Page Size (# Bytes)	Access Time	Power		Temp. Range(s)	Package									
				Active	Standby		S	P	D	C	F1	F2	K	J	E	G
X28C010	131072 x 8	128	200 ns	80 mA	500 μA	†, I, M			•	•						

Key:
** = MIL-STD-883 Rev. C, Class B Compliant

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I = Industrial = −40°C to +85°C
M = Military = −55°C to +125°C

S = Plastic Small Outline Gull Wing
P = Plastic DIP
D = 32-Lead Cerdip
C = 32-Lead Side Braze
F1 = Ceramic Flat Pack for X2864A, X2864B, X2864H and X28C64
F2 = Ceramic Flat Pack for X28C256 and X28C256B
K = Ceramic Pin Grid Array
J = J-Hook Plastic Leaded Chip Carrier
E = Ceramic Leadless Chip Carrier (Solder Seal)
G = Ceramic Leadless Chip Carrier (Glass Frit Seal)

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1MEGABIT E²PROM MODULES

Part Number	Organization	Page Size (# Bytes)	Access Time	Power		Temp. Range(s)
				Active	Standby	
XM28C010-25	131072 x 8	64	250 ns	70 mA	800 μA	†
XM28C010	131072 x 8	64	300 ns	70 mA	800 μA	†
XM28C010I-25	131072 x 8	64	250 ns	70 mA	800 μA	I
XM28C010I	131072 x 8	64	300 ns	70 mA	800 μA	I
XM28C010M-25***	131072 x 8	64	250 ns	70 mA	800 μA	M
XM28C010M***	131072 x 8	64	300 ns	70 mA	800 μA	M

Key:
*** = High Rel product comprised of MIL-STD-883 Rev. C, Class B components

† = Blank = Commercial = 0°C to +70°C
I = Industrial = −40°C to +85°C
M = Military = −55°C to +125°C

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E²POTENTIOMETERs

Part Number	Minimal Resistance	Wiper Increments	Maximum Resistance	Temp. Range(s)	Package									
					S	P	D	C	F1	F2	K	J	E	G
X9102	40Ω	10Ω	1 KΩ	†	•	•	•							
X9103	40Ω	101Ω	10 KΩ	†	•	•	•							
X9503	40Ω	505Ω	50 KΩ	†	•	•	•							
X9104	40Ω	1010Ω	100 KΩ	†	•	•	•							
X9102I	40Ω	10Ω	1 KΩ	I	•	•	•							
X9103I	40Ω	101Ω	10 KΩ	I	•	•	•							
X9503I	40Ω	505Ω	50 KΩ	I	•	•	•							
X9104I	40Ω	1010Ω	100 KΩ	I	•	•	•							
X9102M	40Ω	10Ω	1 KΩ	M		•	•							
X9103M	40Ω	101Ω	10 KΩ	M		•	•							
X9503M	40Ω	505Ω	50 KΩ	M		•	•							
X9104M	40Ω	1010Ω	100 KΩ	M		•	•							

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I = Industrial = −40°C to +85°C
M = Military = −55°C to +125°C

S = 14-Lead Plastic Small Outline Gull Wing
P = 8-Lead Plastic DIP
D = 8-Lead Cerdip
C = Side Braze
F1 = Ceramic Flat Pack for X2864A, X2864B, X2864H and X28C64
F2 = Ceramic Flat Pack for X28C256 and X28C256B
K = Ceramic Pin Grid Array
J = J-Hook Plastic Leaded Chip Carrier
E = Ceramic Leadless Chip Carrier (Solder Seal)
G = Ceramic Leadless Chip Carrier (Glass Frit Seal)

For complete data sheet specifications and ordering information, please refer to the Xicor 1988 Data Book Stock No. 100-080. For additional product availability check with your local Xicor sales representative.

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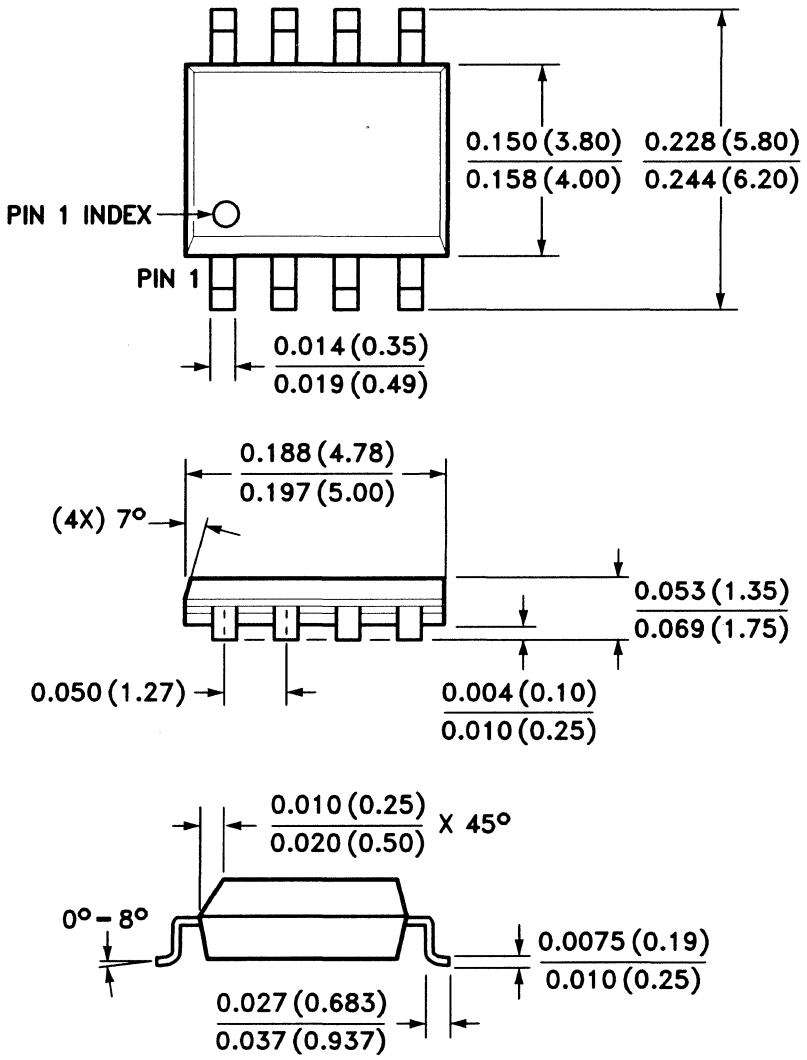
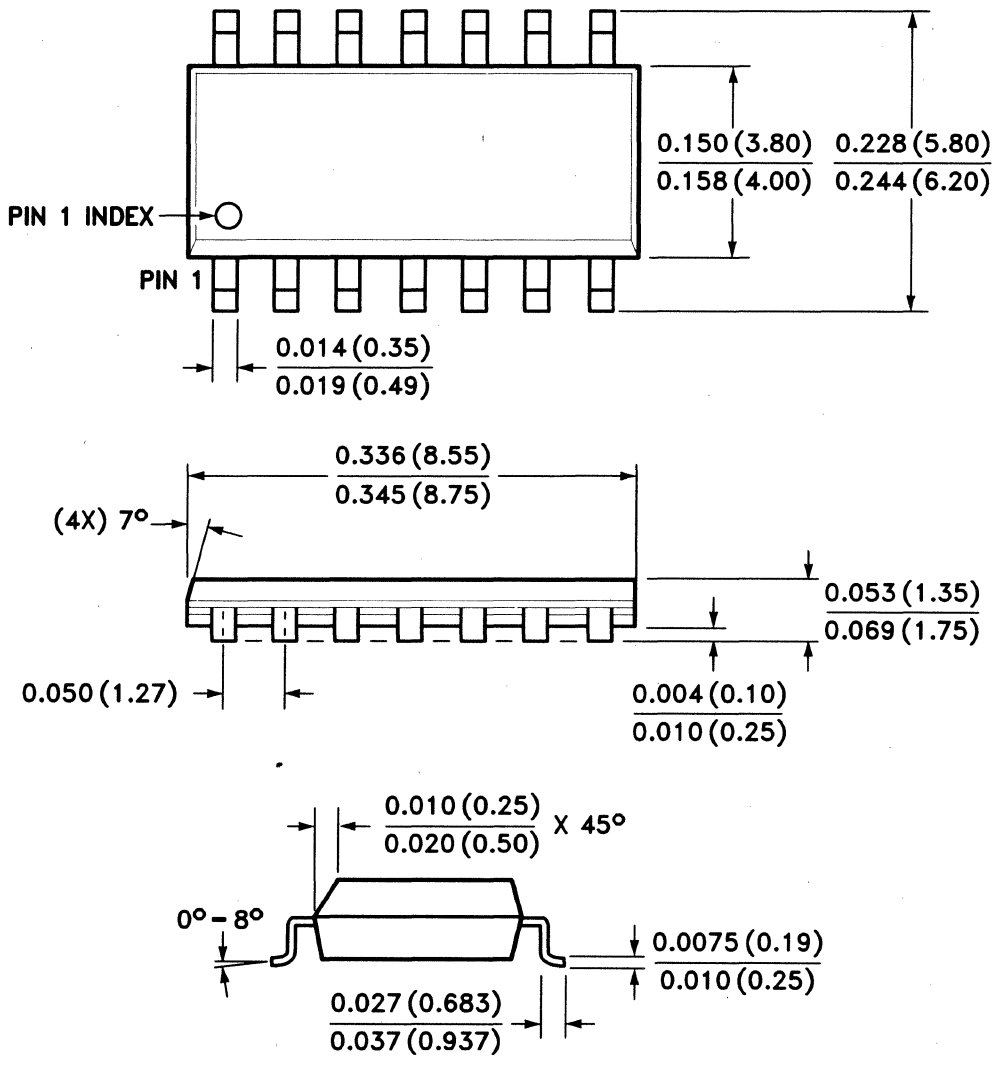
8-LEAD PLASTIC SMALL OUTLINE GULL WING PACKAGE TYPE S



PSE008

NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

14-LEAD PLASTIC SMALL OUTLINE GULL WING PACKAGE TYPE S



PSE014

NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

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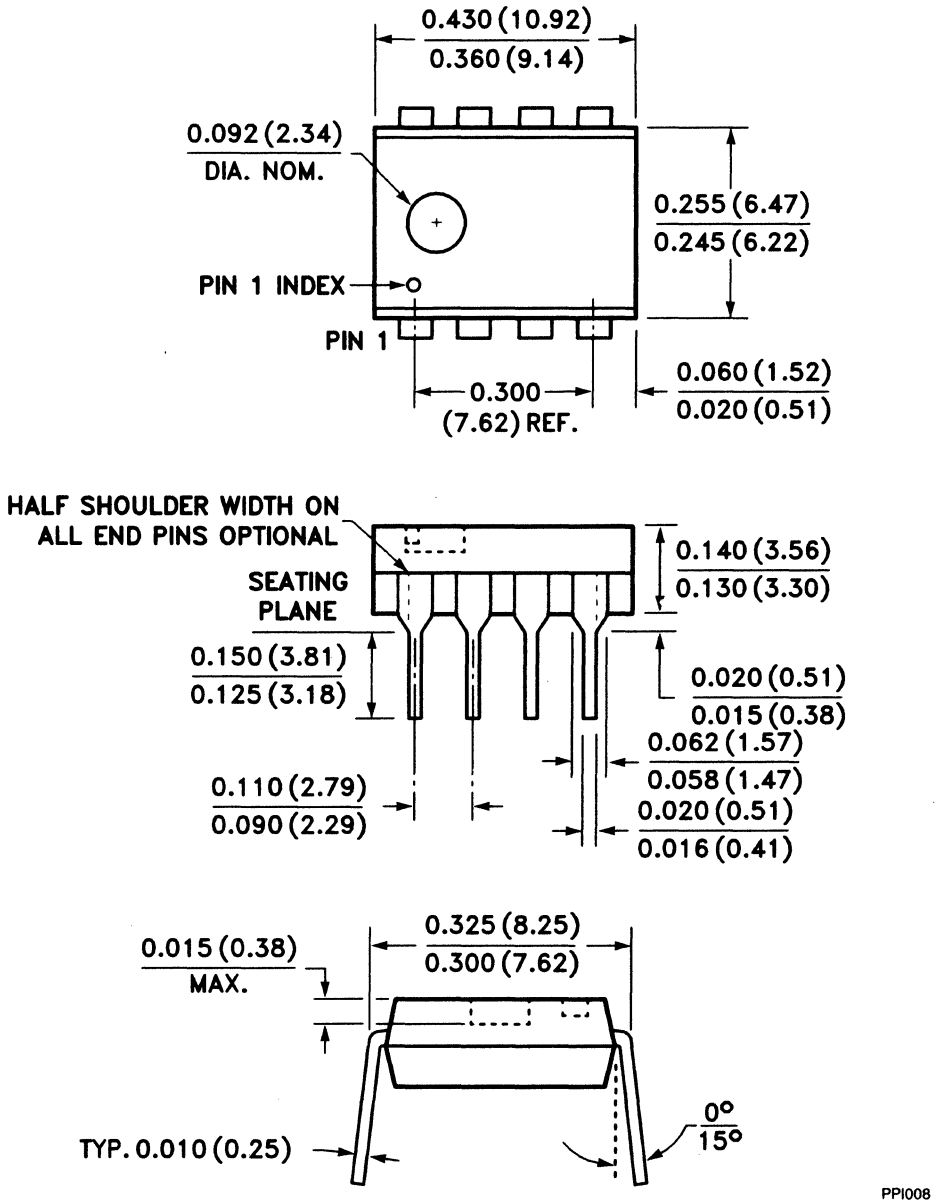
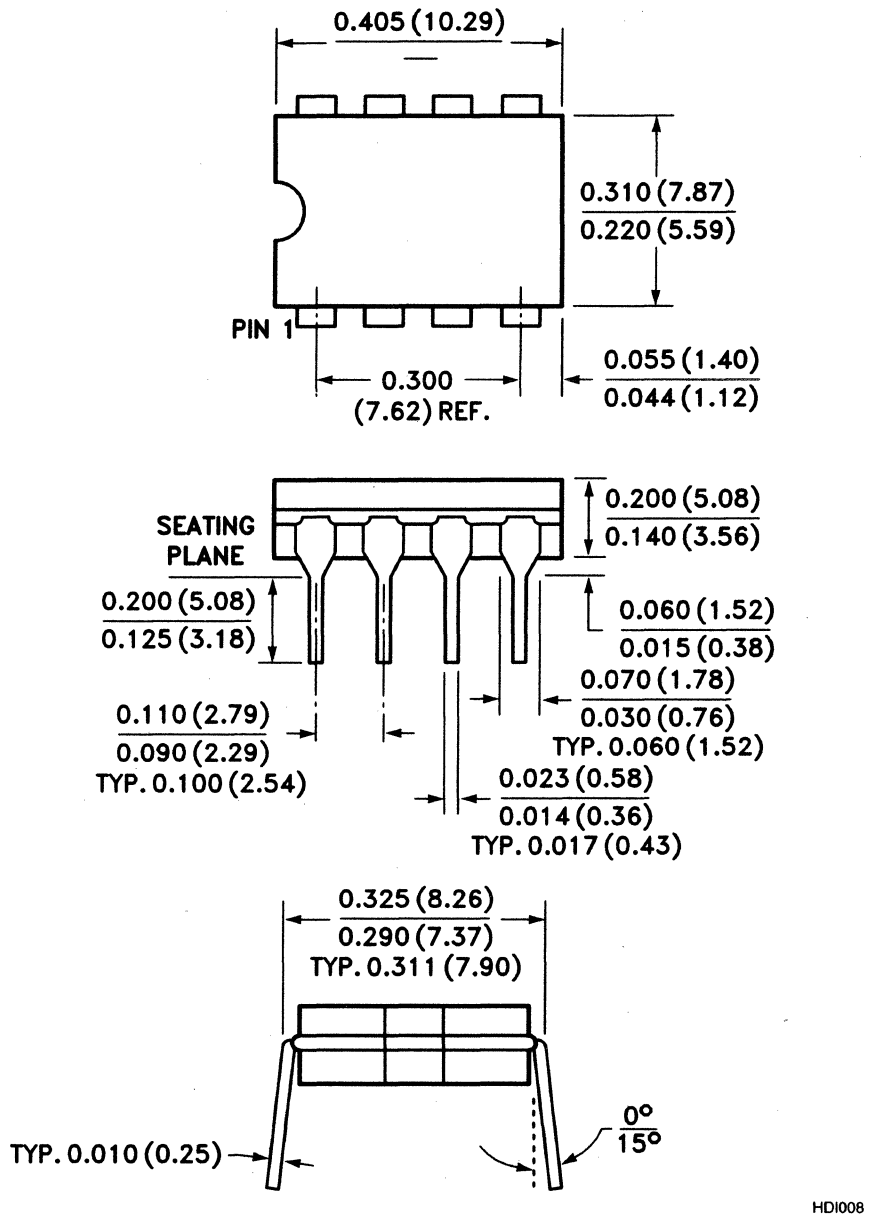
8-LEAD PLASTIC DUAL IN-LINE PACKAGE TYPE P



PPI008

NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

8-LEAD HERMETIC DUAL IN-LINE PACKAGE TYPE D



NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

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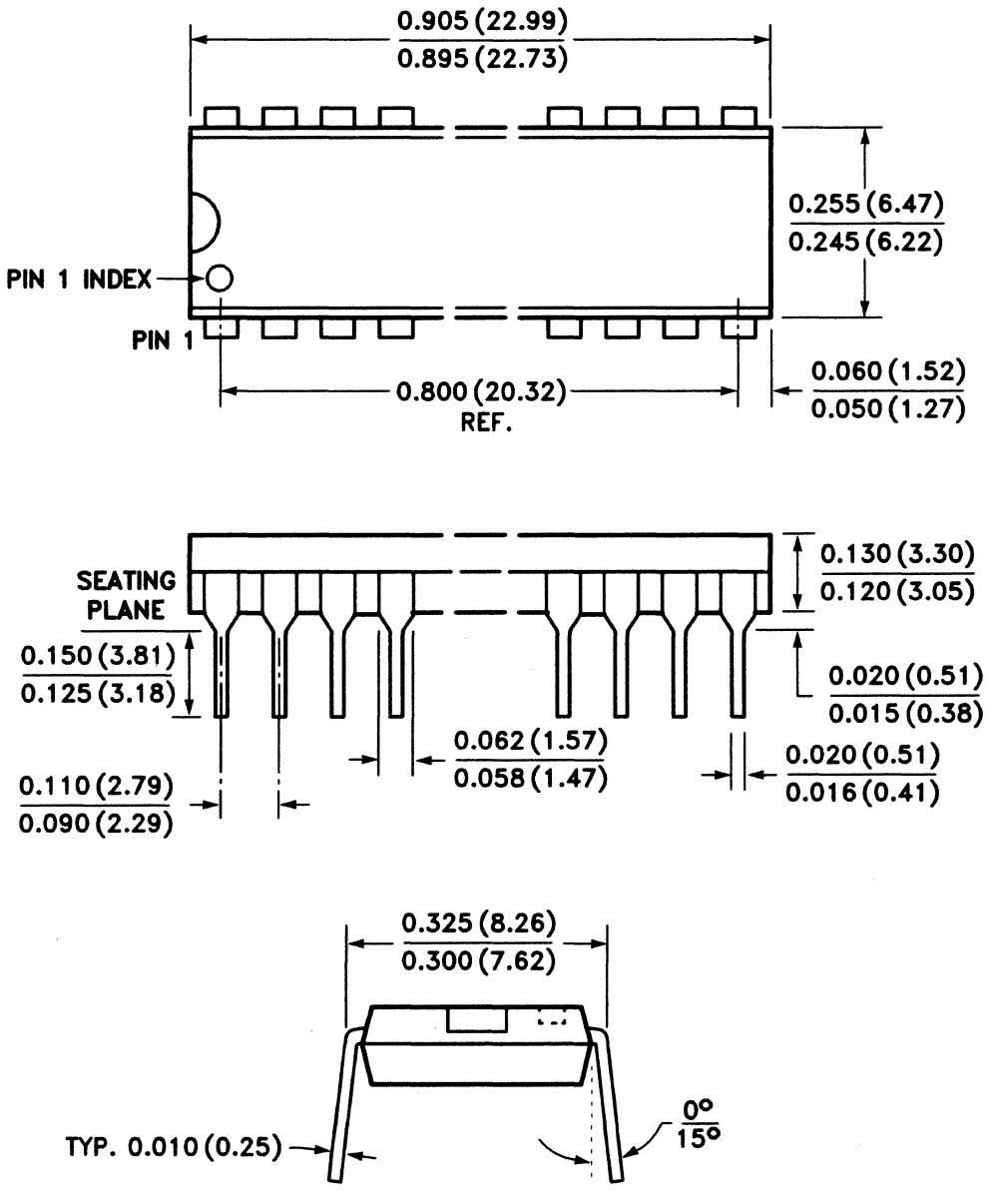
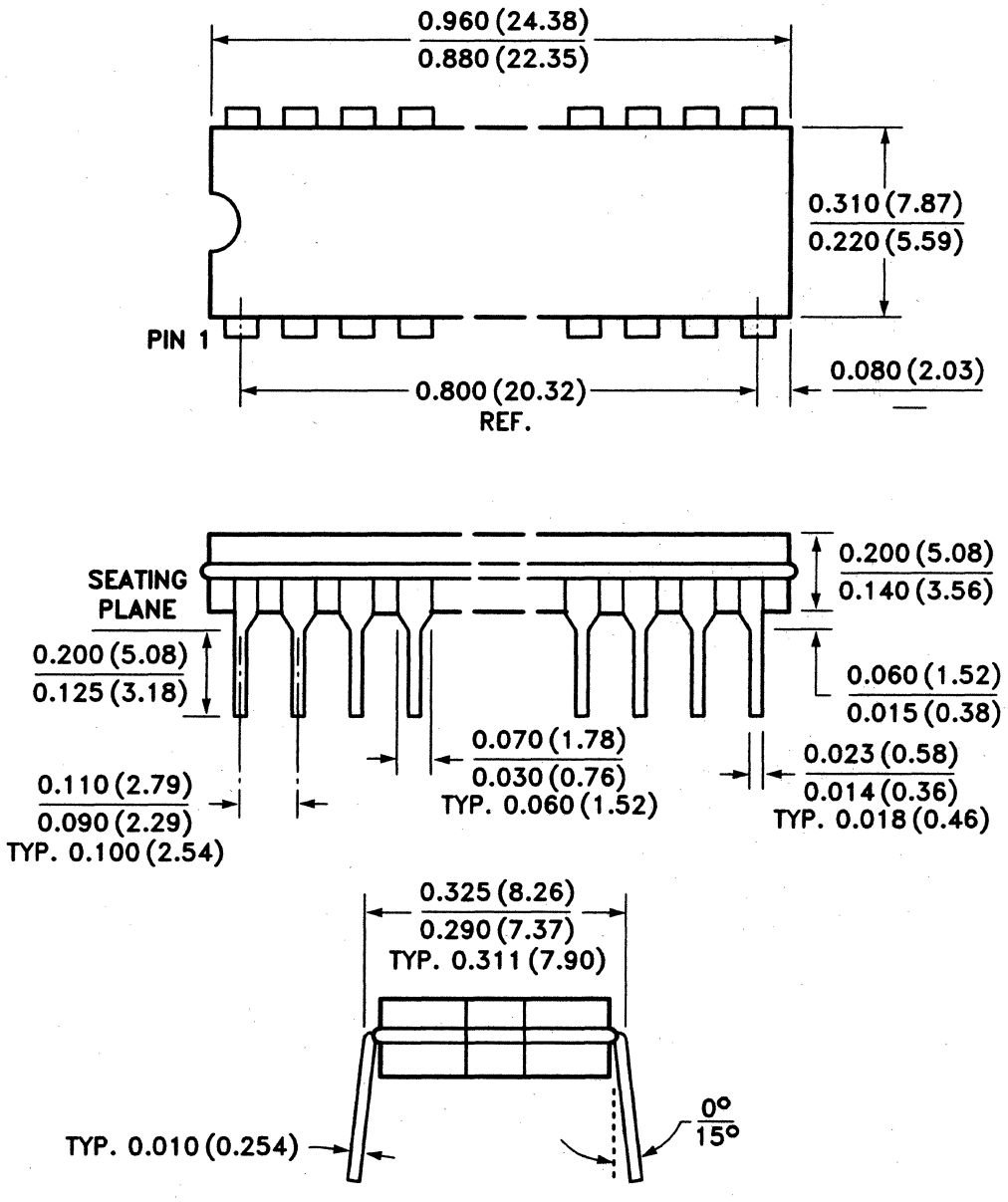
18-LEAD PLASTIC DUAL IN-LINE PACKAGE TYPE P



PPI018

NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

18-LEAD HERMETIC DUAL IN-LINE PACKAGE TYPE D



HDI018

NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

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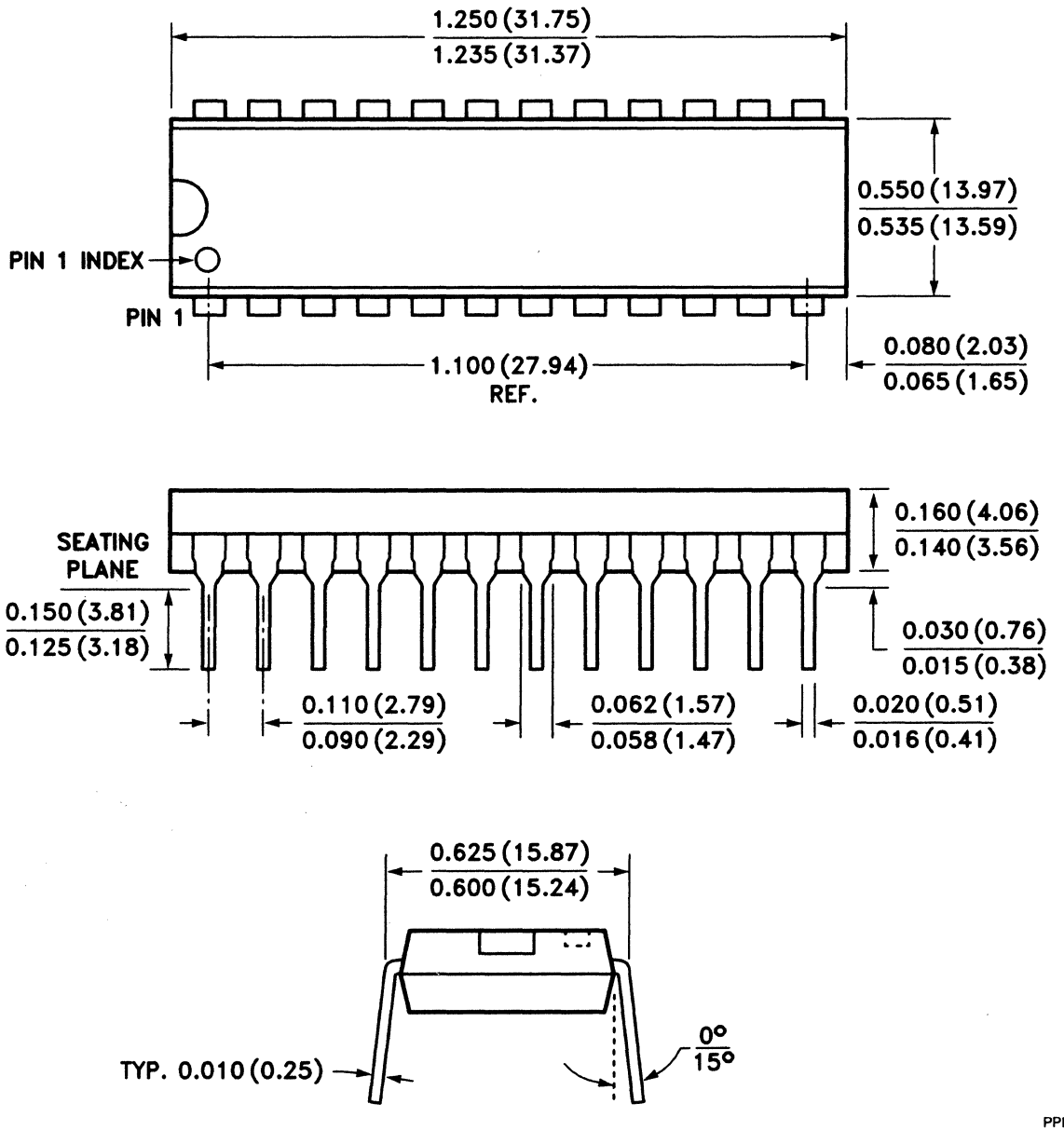
24-LEAD PLASTIC DUAL IN-LINE PACKAGE TYPE P



PPI024

NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

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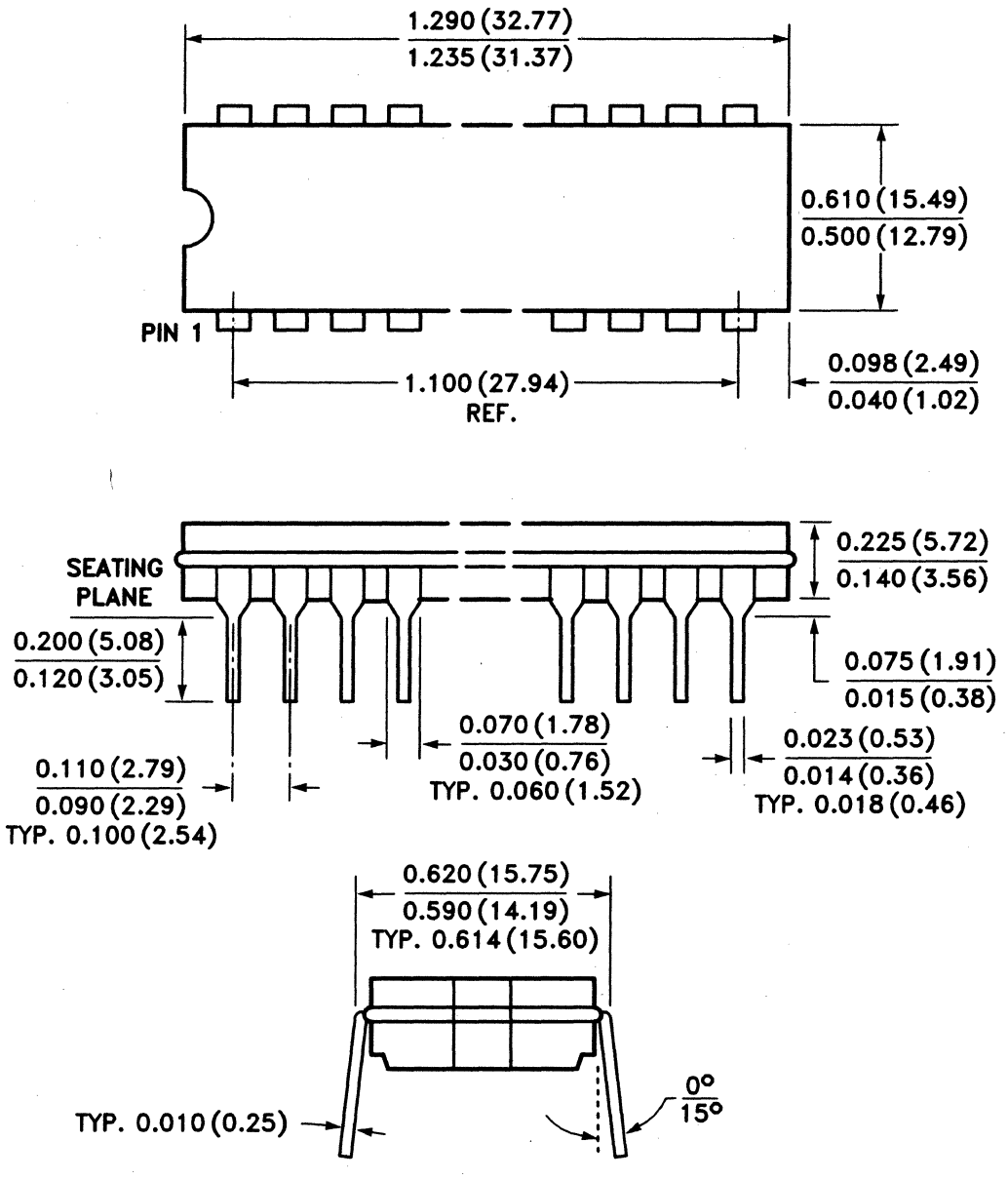
24-LEAD HERMETIC DUAL IN-LINE PACKAGE TYPE D



HDI024

NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

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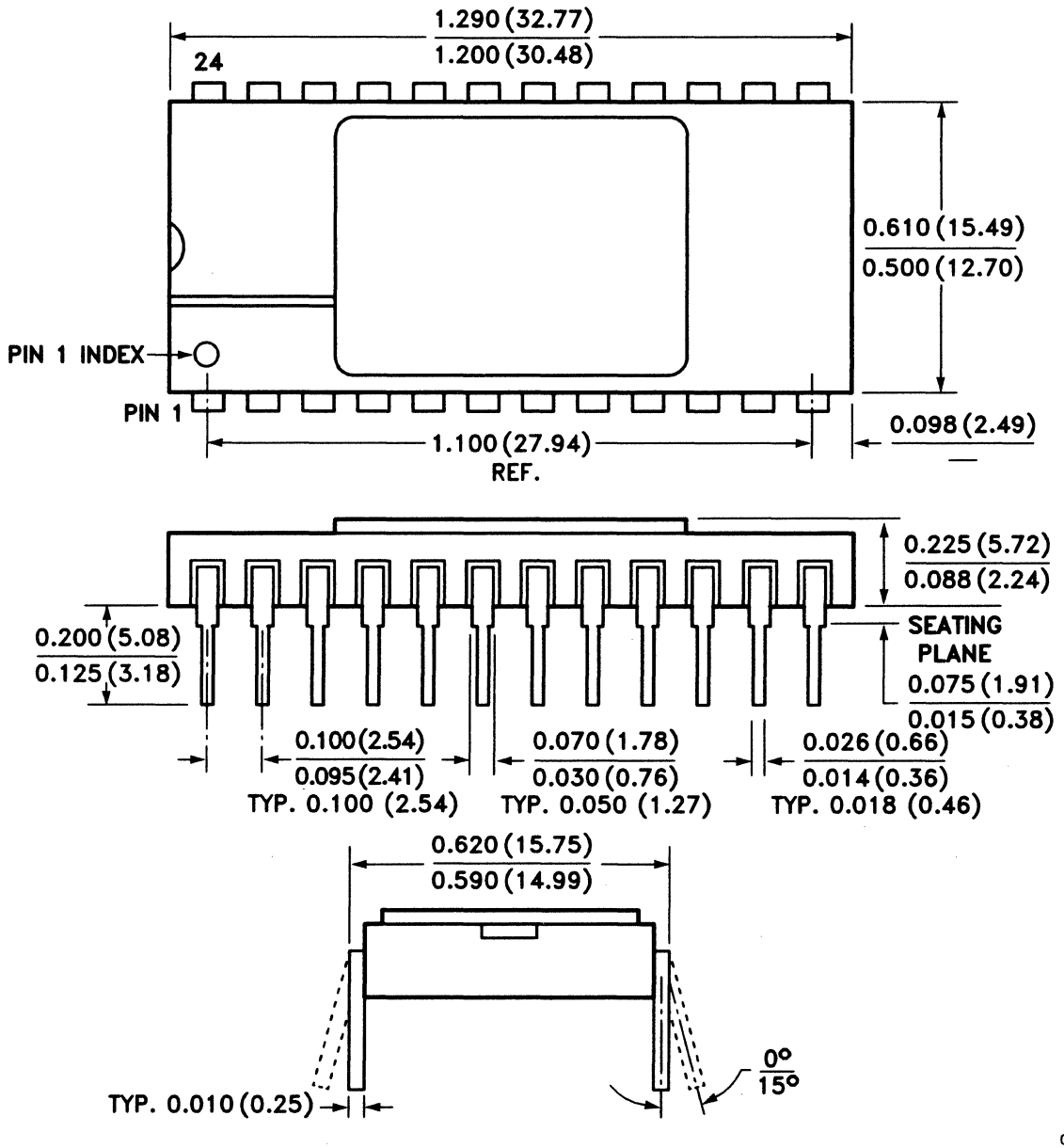
24-LEAD SIDE BRAZE PACKAGE TYPE C



0CJ024

NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

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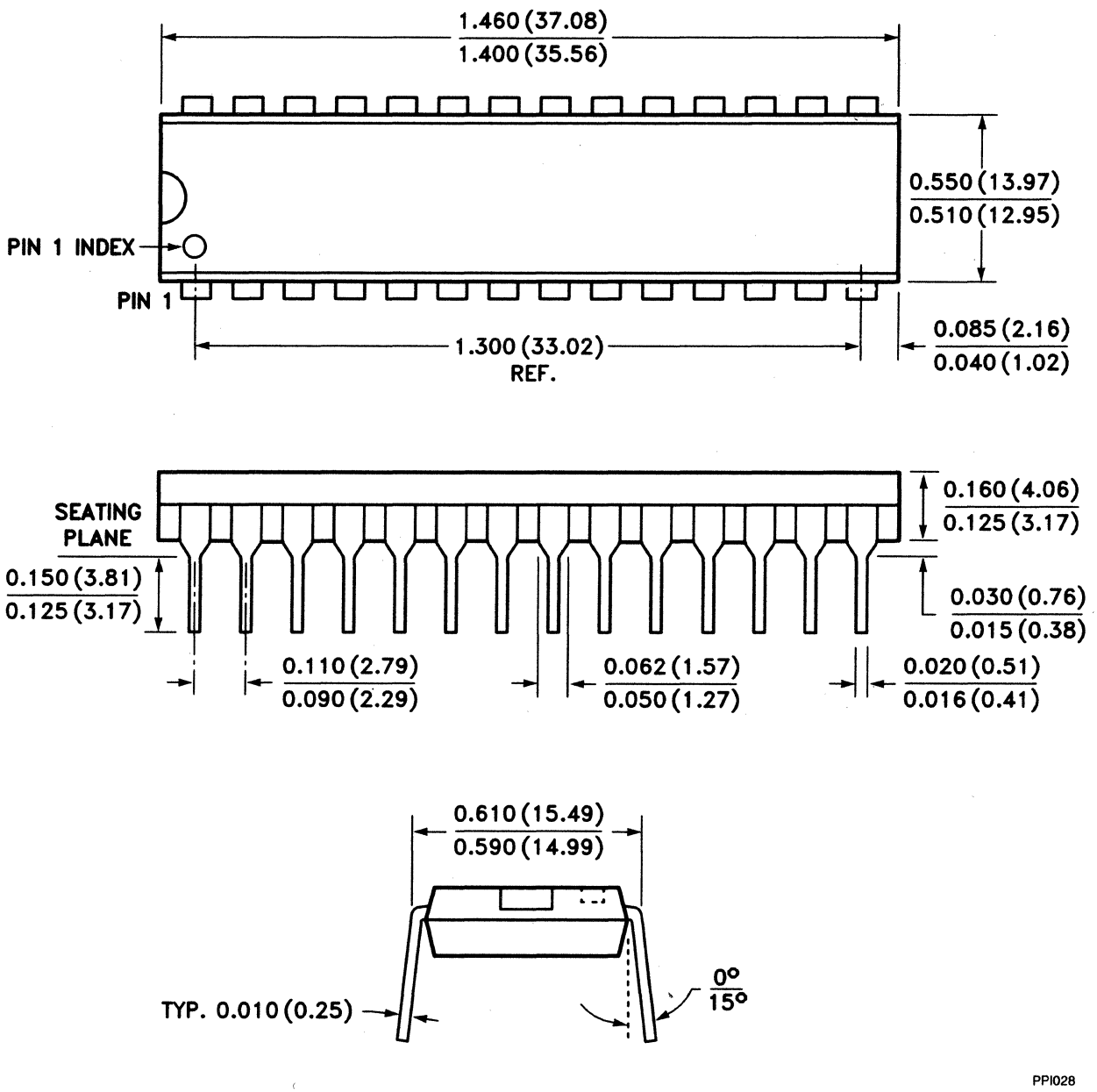
28-LEAD PLASTIC DUAL IN-LINE PACKAGE TYPE P



PPI028

NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

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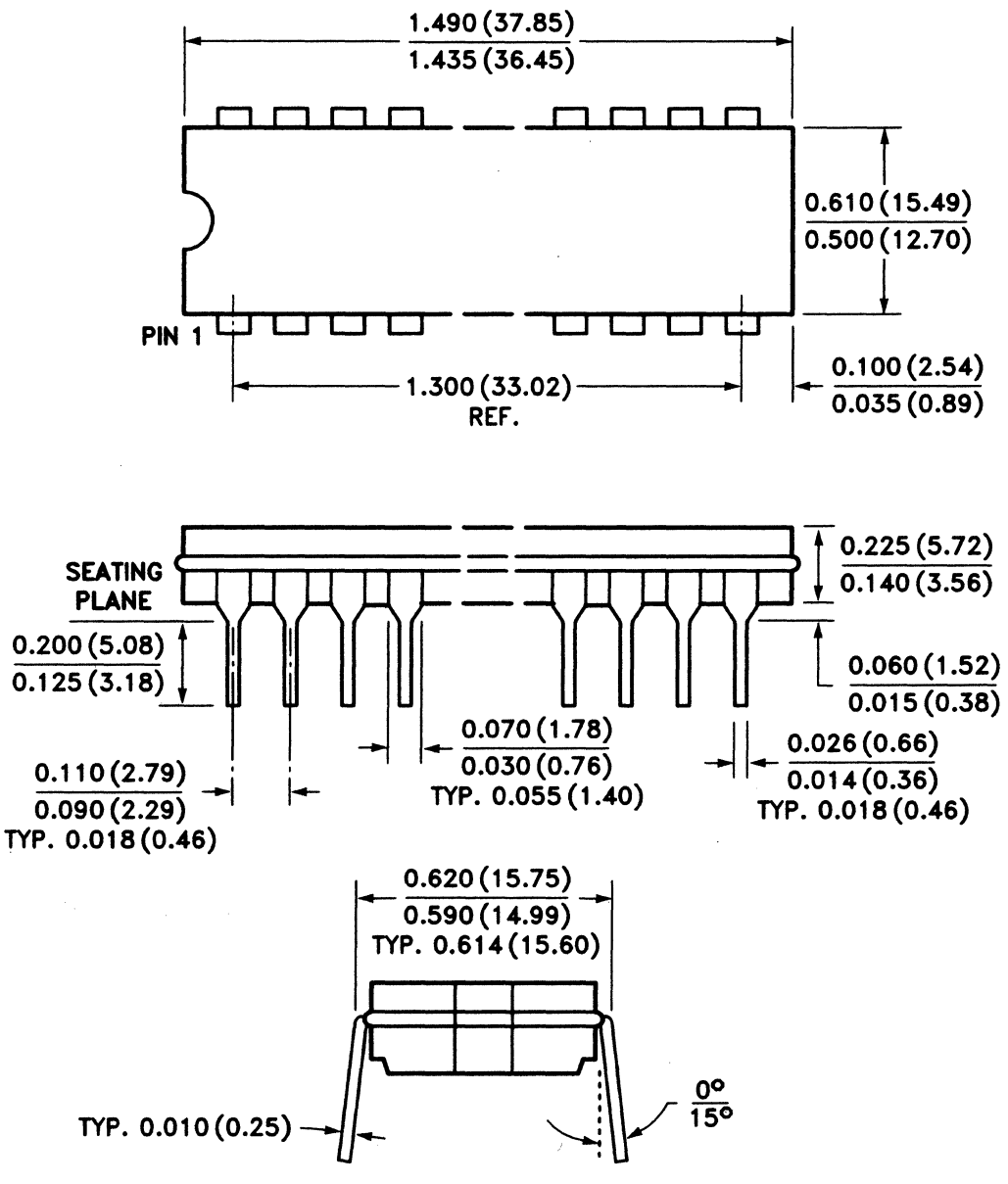
28-LEAD HERMETIC DUAL IN-LINE PACKAGE TYPE D

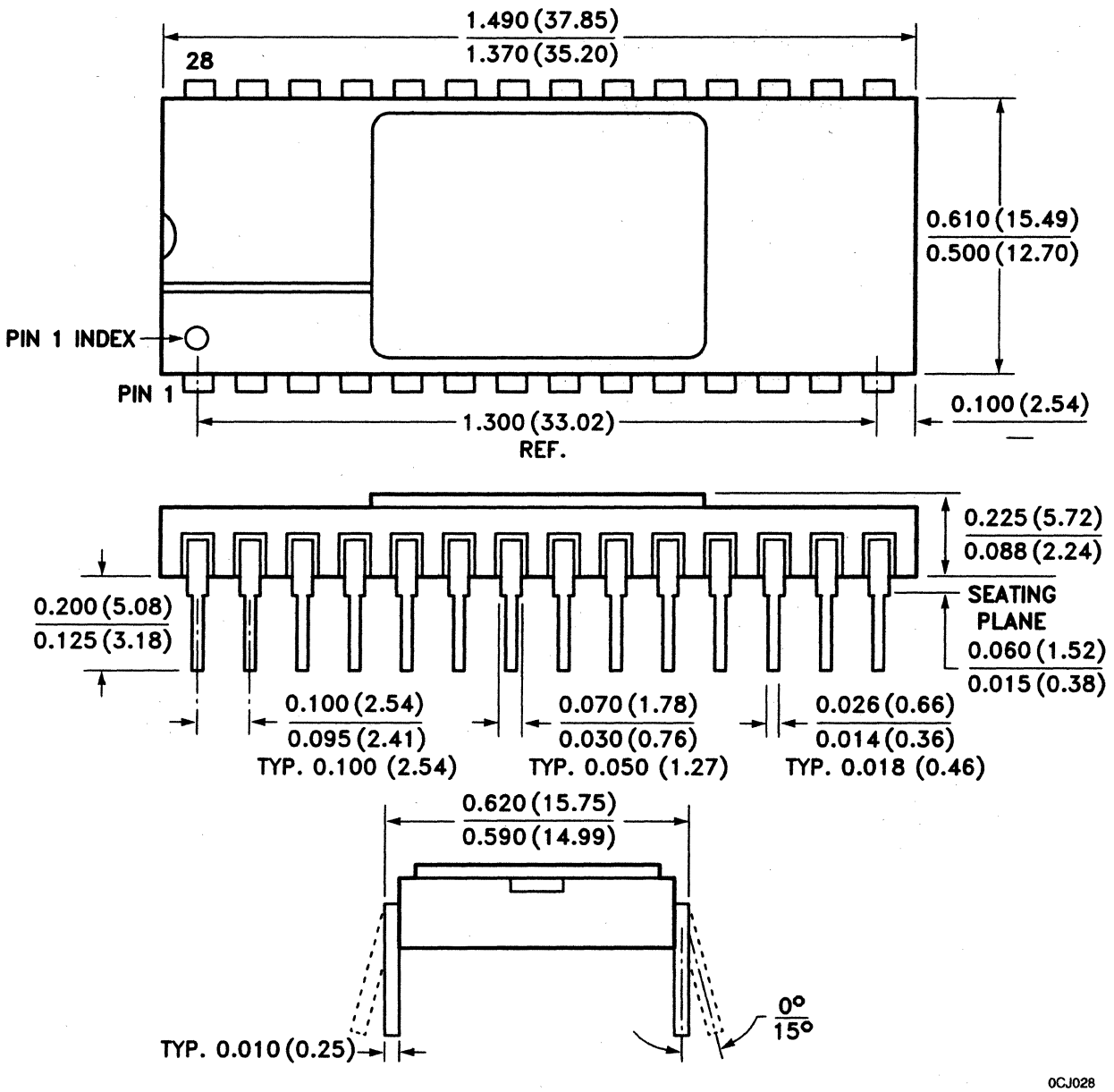


HDI028

NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

Xicor

28-LEAD SIDE BRAZE PACKAGE TYPE C



NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

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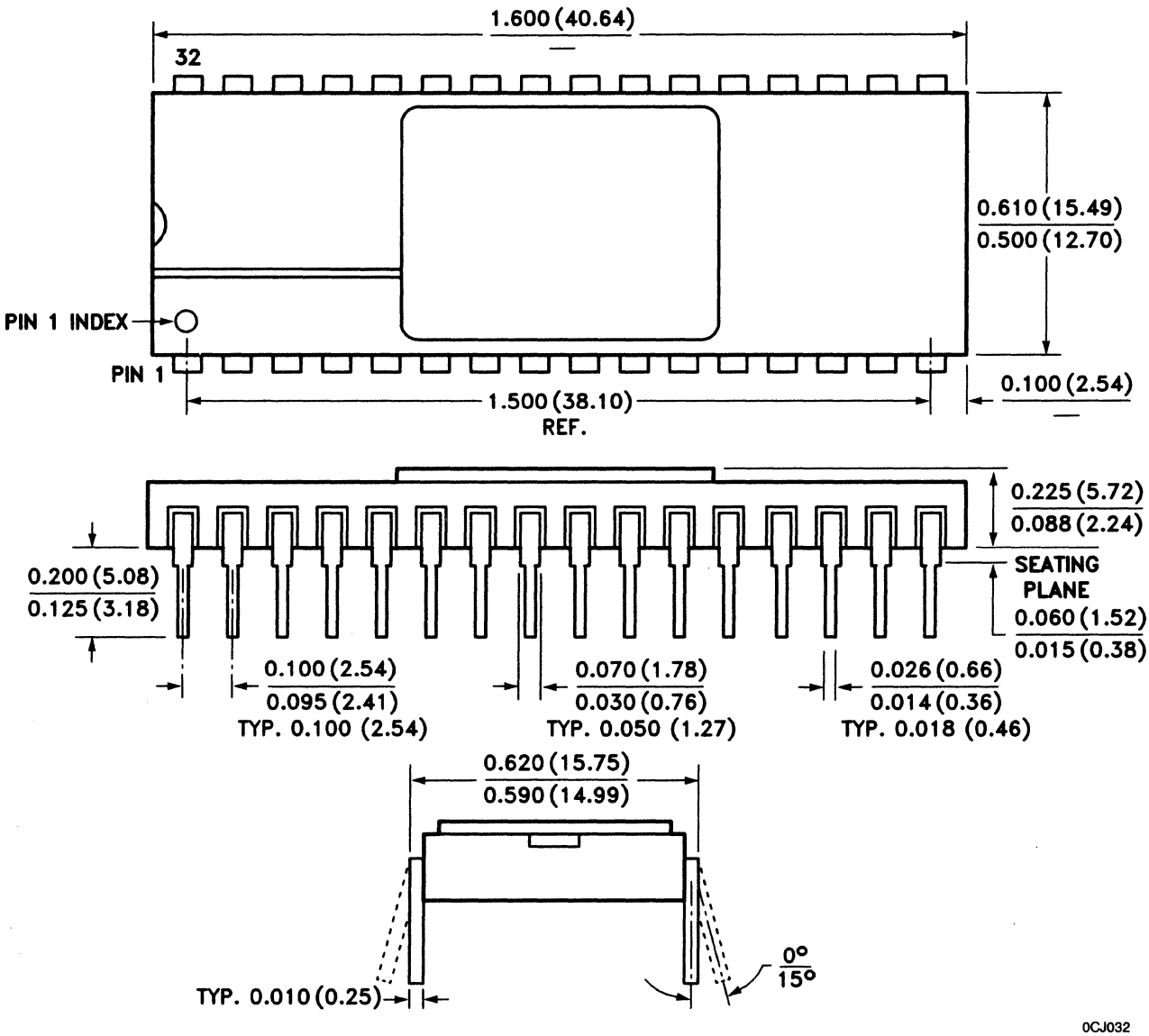
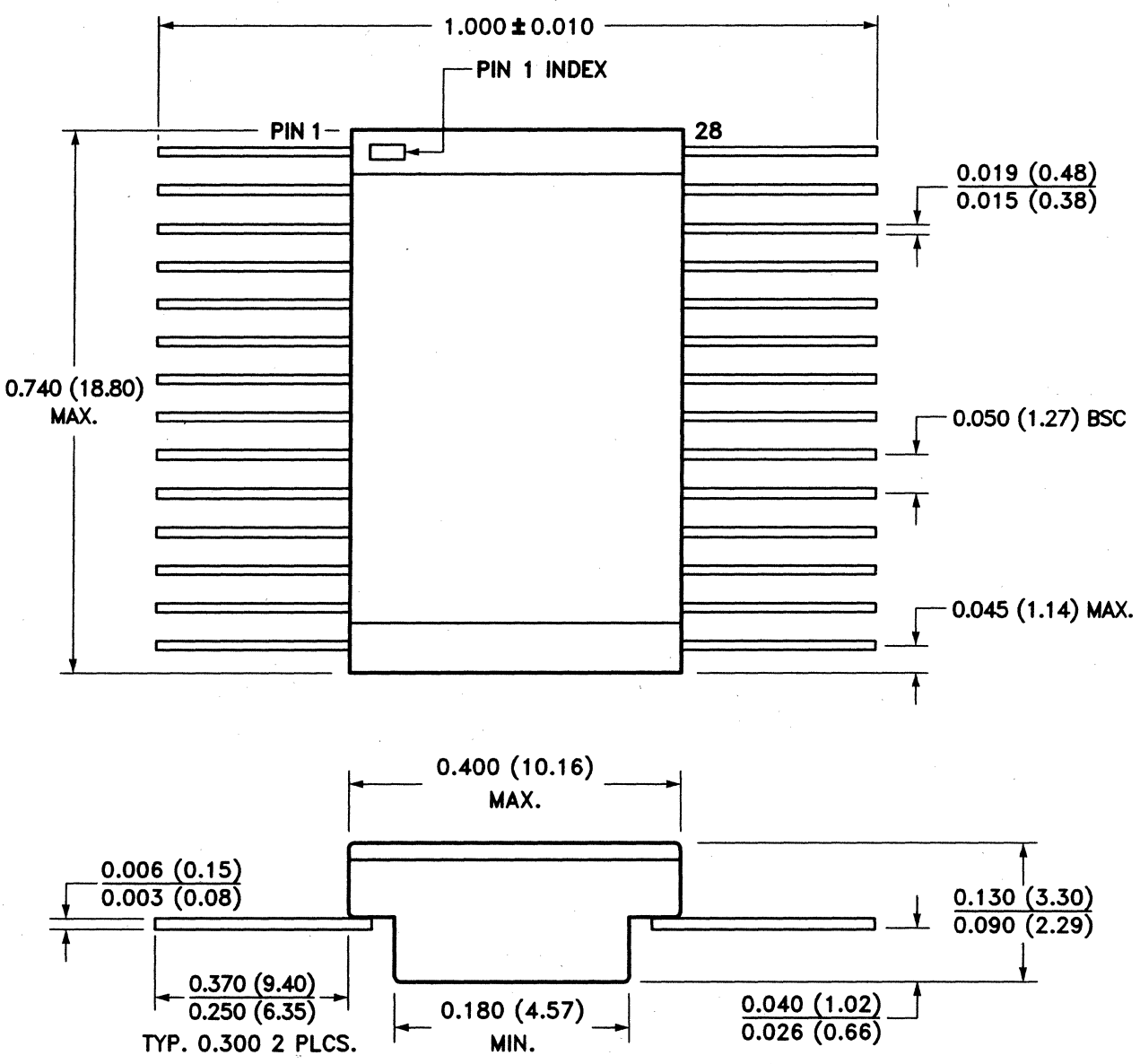
32-LEAD SIDE BRAZE PACKAGE TYPE C



Xicor

NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

28-LEAD CERAMIC FLAT PACK TYPE F1



NOTES:

1. ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

2. CASE OUTLINE FOR X2864A, X2864B, X2864H AND X28C64

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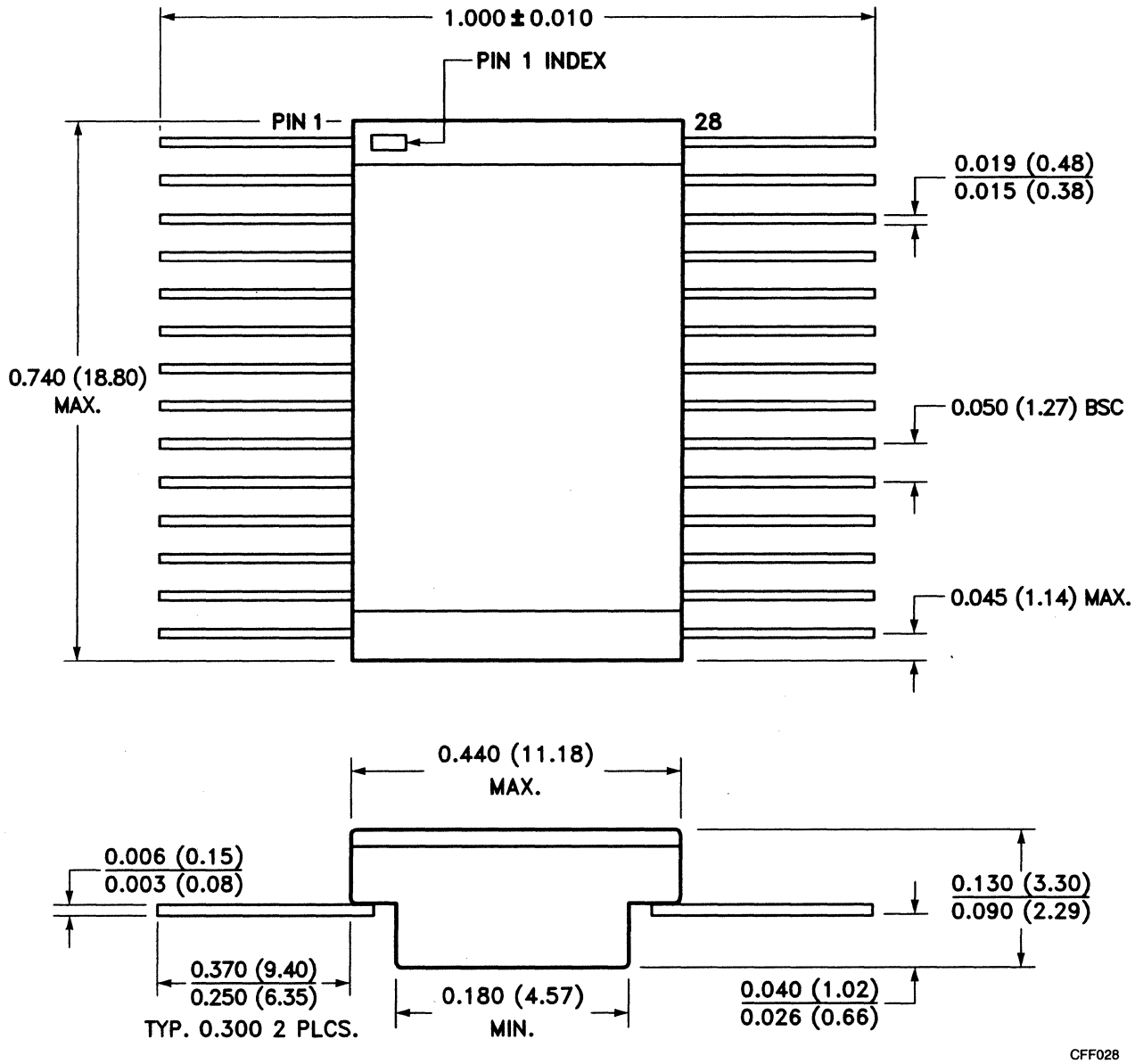
28-LEAD CERAMIC FLAT PACK TYPE F2



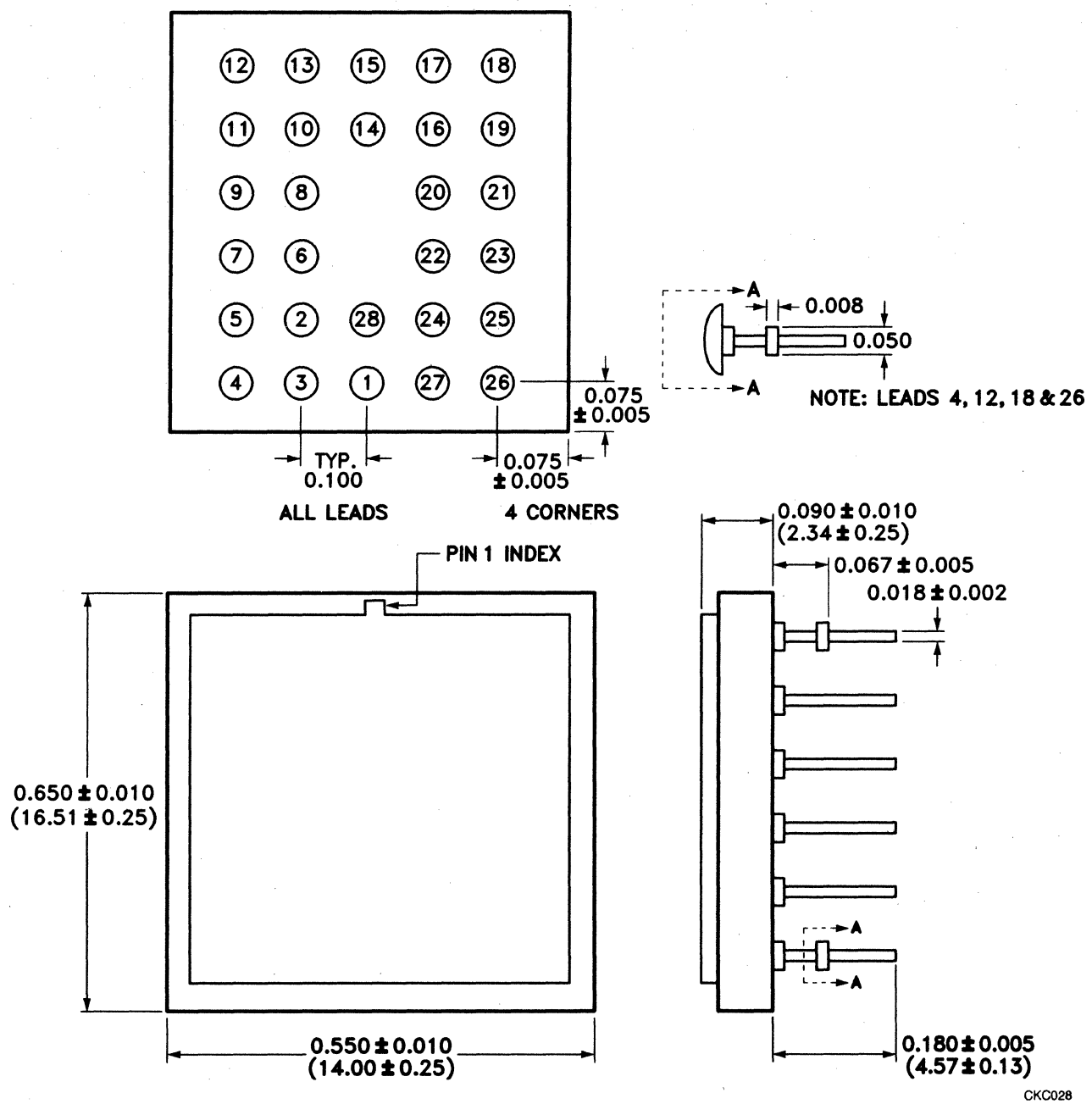
Xicor

NOTES:

1. ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

2. CASE OUTLINE FOR X28C256 AND X28C256B

28-PIN CERAMIC PIN GRID ARRAY PACKAGE TYPE K



NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

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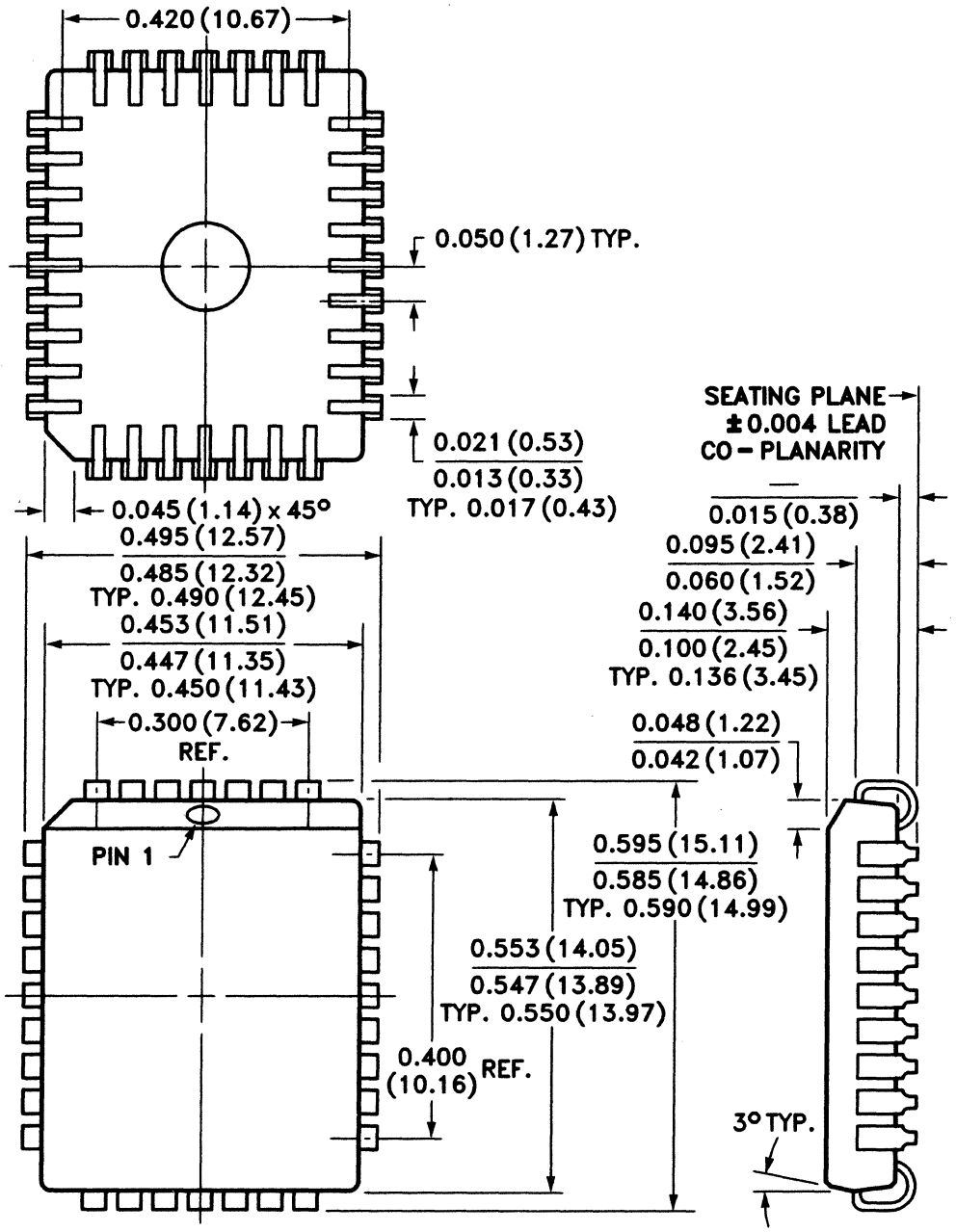
32-LEAD PLASTIC LEADED CHIP CARRIER PACKAGE TYPE J

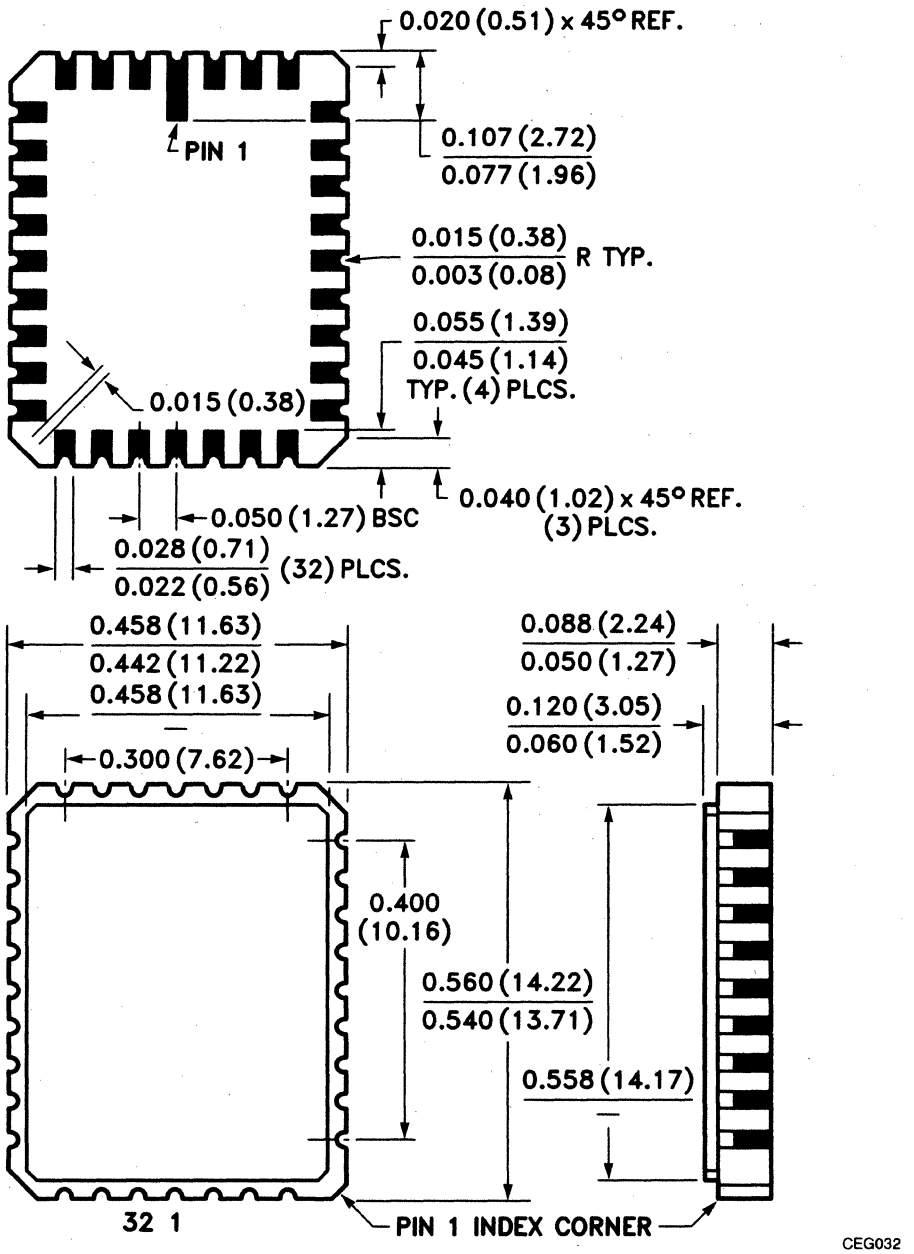


PJG032

NOTES:

1. ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
2. DIMENSIONS WITH NO TOLERANCE FOR REFERENCE ONLY

32-PAD CERAMIC LEADLESS CHIP CARRIER PACKAGE TYPE E



NOTES:

1. ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

2. TOLERANCE: ±1% NLT ±0.005 (0.127)

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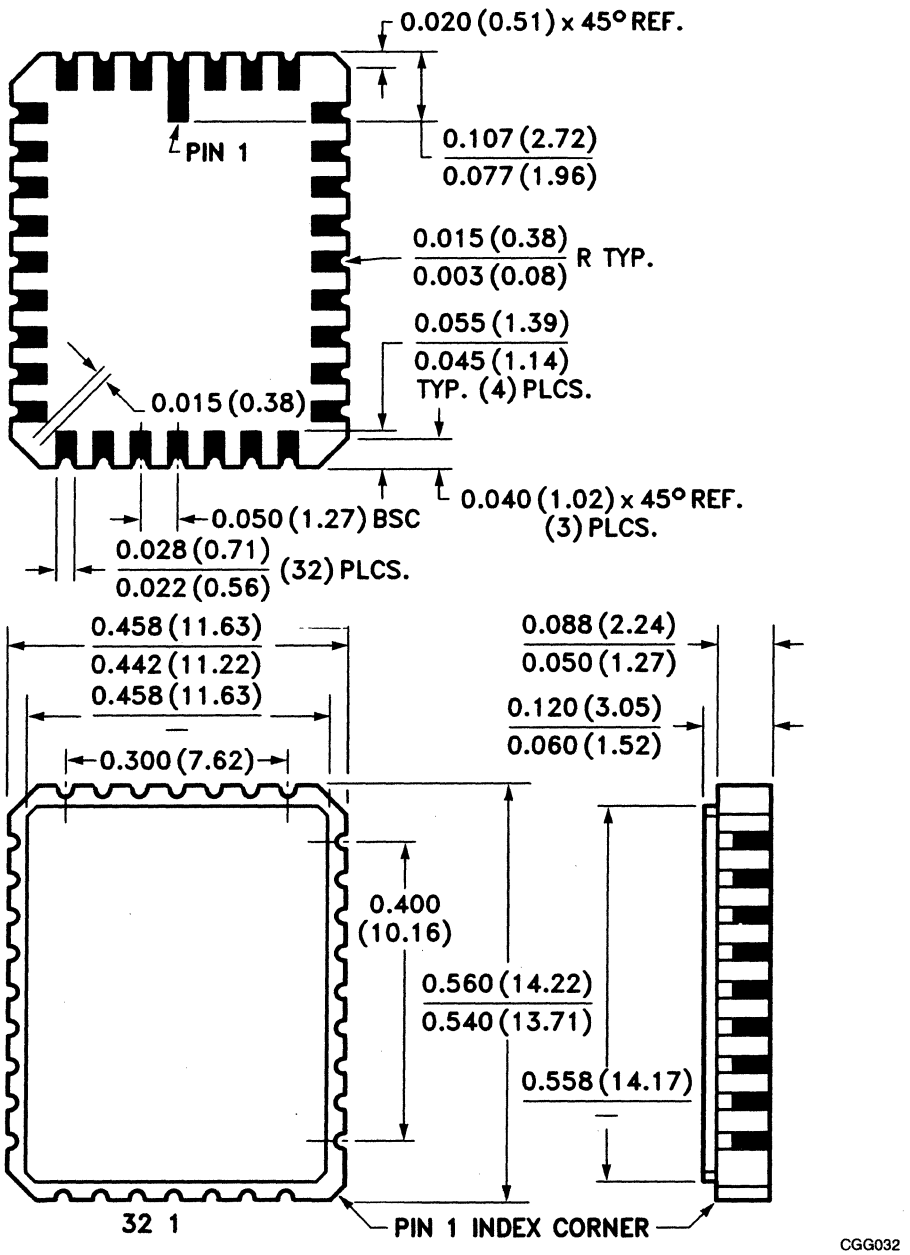
32-PAD CERAMIC LEADLESS CHIP CARRIER (GLASS FRIT SEAL) PACKAGE TYPE G



NOTES:

1. ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
2. TOLERANCE: ±1% NLT ±0.005 (0.127)
3. FOR EXTENDED STORAGE TEMPERATURE ENVIRONMENTS

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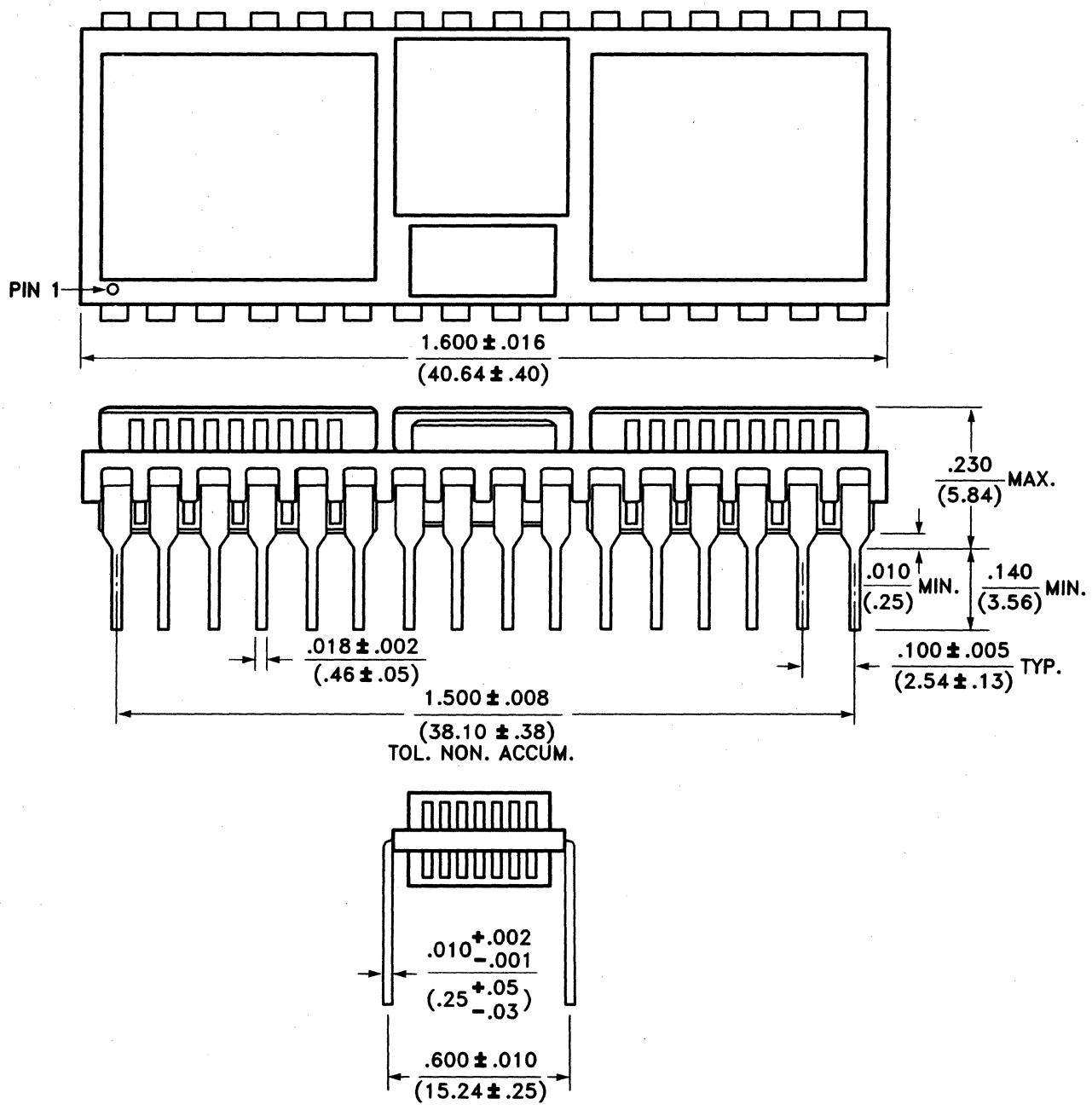
32-PIN DUAL-IN-LINE PACKAGE
CERAMIC LEADLESS CHIP CARRIERS
ON SIDE BRAZED CERAMIC SUBSTRATE



CEAA32

NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

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256 Bit	Commercial Industrial	X2210 X2210I	64 x 4 Bit

Nonvolatile Static RAM

FEATURES

- **Single 5V Supply**
- **Fully TTL Compatible**
- **Infinite E²PROM Array Recall, RAM Read and Write Cycles**
- **Access Time of 300 ns Max.**
- **Nonvolatile Store Inhibit: V_{CC} = 3V Typical**
- **100 Year Data Retention**
- **JEDEC Standard 18-Pin Package**

DESCRIPTION

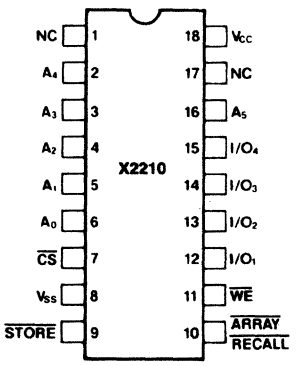
The Xicor X2210 is a 64 x 4 NOVRAM* featuring a high-speed static RAM overlaid bit-for-bit with a nonvolatile E²PROM. The X2210 is fabricated with the same reliable N-channel floating gate MOS technology used in all Xicor 5V nonvolatile memories. The X2210 features the JEDEC approved pinout for 4-bit-wide memories, compatible with industry standard RAMs.

The NOVRAM design allows data to be easily transferred from RAM to E²PROM (store) and from E²PROM to RAM (recall). The store operation is completed in 10 ms or less and the recall is typically completed in 1 μs.

Xicor NOVRAMs are designed for unlimited write operations to RAM, either from the host or recalls from E²PROM. The E²PROM array is designed for a minimum 10,000 store cycles. Data retention is specified to be greater than 100 years.

*NOVRAM is Xicor's nonvolatile static RAM device.

PIN CONFIGURATION

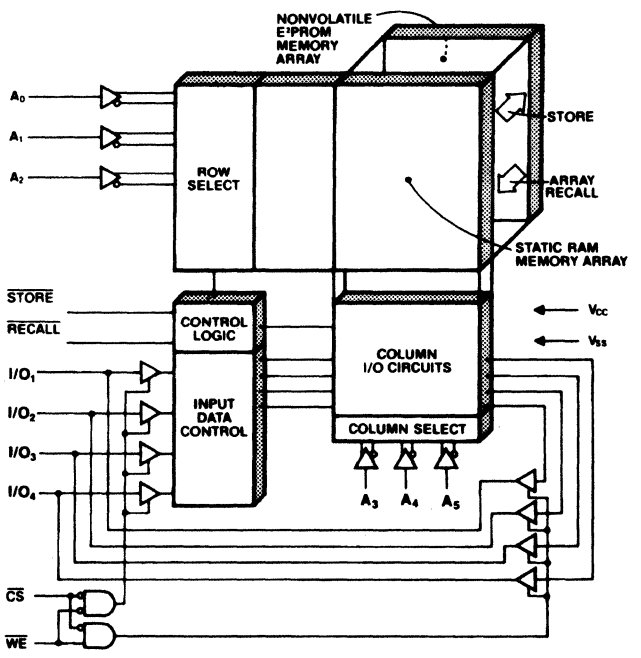


0045-1

PIN NAMES

A_0–A_5	Address Inputs
I/O_1–I/O_4	Data Inputs/Outputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{ARRAY\ RECALL}$	Array Recall
$\overline{STORE}$	Store
V_{CC}	+5V
V_{SS}	Ground
NC	No Connect

FUNCTIONAL DIAGRAM



0045-2

Xicor

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Characteristics subject to change without notice

Nonvolatile Static RAM

FEATURES

- **Single 5V Supply**
- **Fully TTL Compatible**
- **Infinite E²PROM Array Recall, RAM Read and Write Cycles**
- **Access Time of 300 ns Max.**
- **Nonvolatile Store Inhibit: V_{CC} = 3V Typical**
- **100 Year Data Retention**
- **JEDEC Standard 18-Pin Package**

DESCRIPTION

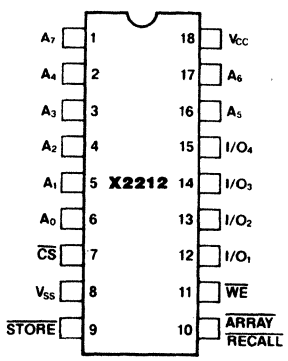
The Xicor X2212 is a 256 x 4 NOVRAM* featuring a high-speed static RAM overlaid bit-for-bit with a nonvolatile E²PROM. The X2212 is fabricated with the same reliable N-channel floating gate MOS technology used in all Xicor 5V nonvolatile memories. The X2212 features the JEDEC approved pinout for 4-bit-wide memories, compatible with industry standard RAMs.

The NOVRAM design allows data to be easily transferred from RAM to E²PROM (store) and from E²PROM to RAM (recall). The store operation is completed in 10 ms or less and the recall is typically completed in 1 μs.

Xicor NOVRAMs are designed for unlimited write operations to RAM, either from the host or recalls from E²PROM. The E²PROM array is designed for a minimum 10,000 store cycles. Data retention is specified to be greater than 100 years.

*NOVRAM is Xicor's nonvolatile static RAM device.

PIN CONFIGURATION

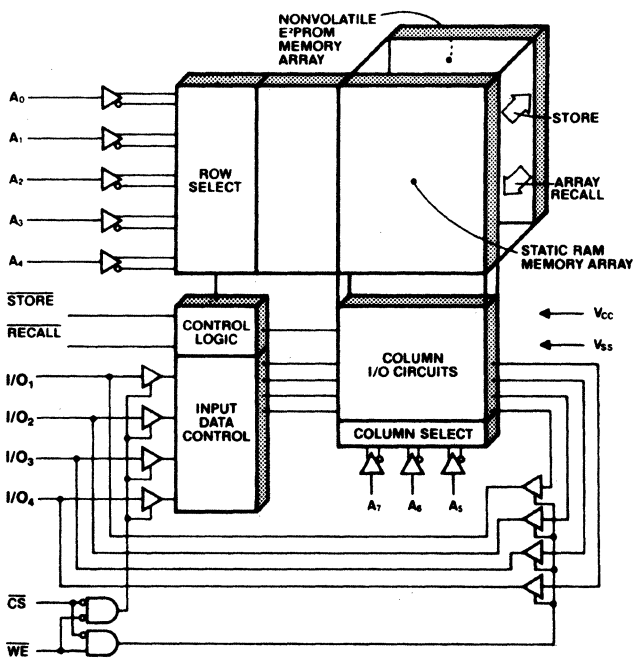


0058-1

PIN NAMES

A_0–A_7	Address Inputs
I/O_1–I/O_4	Data Inputs/Outputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{ARRAY\ RECALL}$	Array Recall
$\overline{STORE}$	Store
V_{CC}	+5V
V_{SS}	Ground
NC	No Connect

FUNCTIONAL DIAGRAM



0058-2

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1K	Commercial Industrial	X2001 X2001I	128 x 8 Bit

Nonvolatile Static RAM

FEATURES

- **Nonvolatile Data Integrity**
- **Automatic Store Timing**
- **Store and Array Recall Combined on One Line ($\overline{NE}$)**
- **Enhanced Store Protection**
- **Infinite E²PROM Array Recall, and RAM Read and Write Cycles**
- **Single 5V Supply**
- **100 Year Data Retention**
- **Fast Access Time: 200 ns Max.**
- **Automatic Recall on Power-Up**
- **JEDEC Approved Byte-Wide Pinout**

DESCRIPTION

The Xicor X2001 is a byte-wide NOVRAM* featuring a high-speed static RAM overlaid bit-for-bit with a nonvolatile electrically erasable PROM (E²PROM). The X2001 is fabricated with the same reliable N-channel floating gate MOS technology used in all Xicor 5V programmable nonvolatile memories. The X2001 features the JEDEC approved pinout for byte-wide memories, compatible with industry standard RAMs, ROMs, EPROMs and E²PROMs.

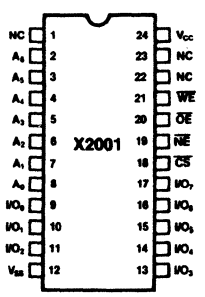
The NOVRAM design allows data to be easily transferred from RAM to E²PROM (store) and E²PROM to RAM (recall). With $\overline{NE}$ LOW, these functions are performed in the same manner as RAM read and write operations. The store operation is completed in 10 ms or less and the recall operation is completed in 5 μs or less.

Xicor NOVRAMs are designed for unlimited write operations to RAM, either from the host or recalls from E²PROM, and a minimum 100,000 store operations to the E²PROM. Data retention is specified to be greater than 100 years.

*NOVRAM is Xicor's nonvolatile static RAM device.

Xicor

PIN CONFIGURATION

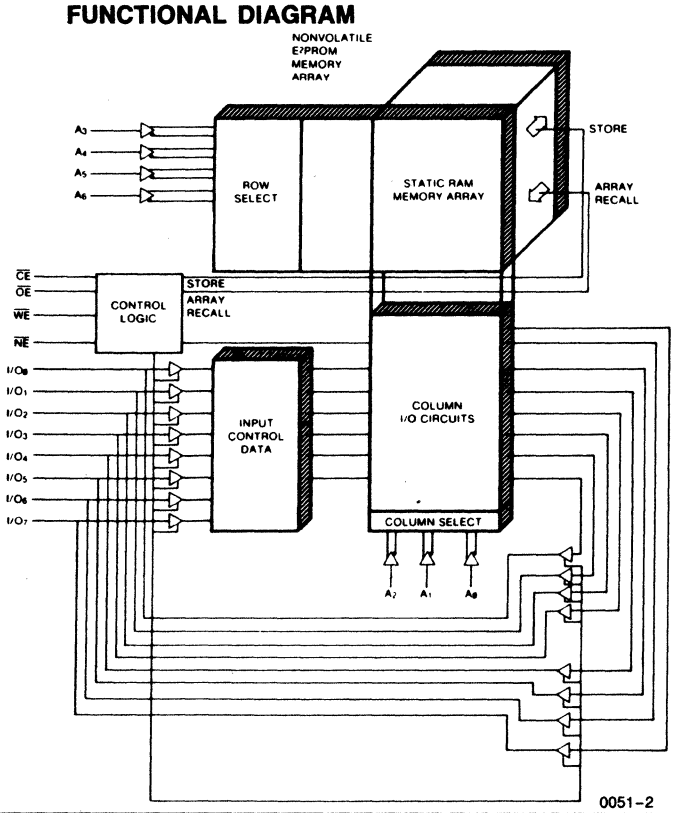


0051-1

PIN NAMES

A_0–A_6	Address Inputs
I/O_0–I/O_7	Data Inputs/Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
$\overline{NE}$	Nonvolatile Enable
V_{CC}	+5V
V_{SS}	Ground
NC	No Connect

FUNCTIONAL DIAGRAM



0051-2

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Characteristics subject to change without notice

4K Commercial Industrial X2004 X2004I 512 x 8 Bit

Nonvolatile Static RAM

FEATURES

- **Nonvolatile Data Integrity**
- **Automatic Store Timing**
- **Store and Array Recall Combined on One Line ($\overline{NE}$)**
- **Enhanced Store Protection**
- **Infinite E²PROM Array Recall, and RAM Read and Write Cycles**
- **Single 5V Supply**
- **100 Year Data Retention**
- **Fast Access Time: 200 ns Max.**
- **Automatic Recall on Power-Up**
- **JEDEC Approved Byte-Wide Pinout**

DESCRIPTION

The Xicor X2004 is a byte-wide NOVRAM* featuring a high-speed static RAM overlaid bit-for-bit with a nonvolatile electrically erasable PROM (E²PROM). The X2004 is fabricated with the same reliable N-channel floating gate MOS technology used in all Xicor 5V programmable nonvolatile memories. The X2004 features the JEDEC approved pinout for byte-wide memories, compatible with industry standard RAMs, ROMs, EPROMs and E²PROMs.

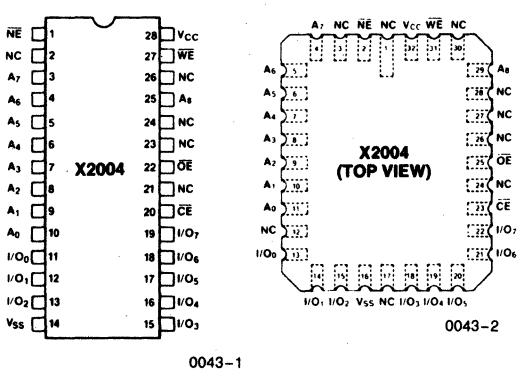
The NOVRAM design allows data to be easily transferred from RAM to E²PROM (store) and E²PROM to RAM (recall). With $\overline{NE}$ LOW, these functions are performed in the same manner as RAM read and write operations. The store operation is completed in 10 ms or less and the recall operation is completed in 5 μs or less.

Xicor NOVRAMs are designed for unlimited write operations to RAM, either from the host or recalls from E²PROM, and a minimum 100,000 store operations to the E²PROM. Data retention is specified to be greater than 100 years.

*NOVRAM is Xicor's nonvolatile static RAM device.

Xicor

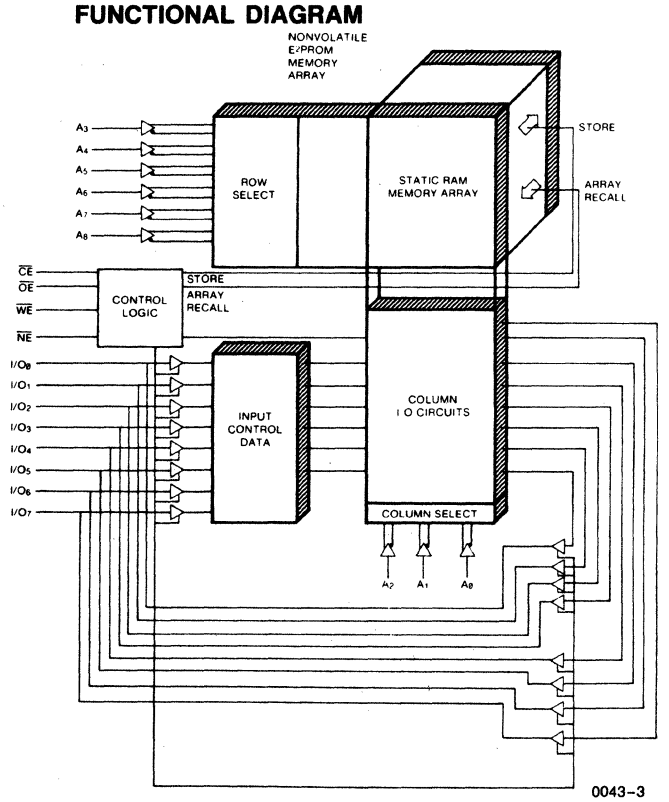
PIN CONFIGURATIONS



PIN NAMES

A_0–A_8	Address Inputs
I/O_0–I/O_7	Data Inputs/Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
$\overline{NE}$	Nonvolatile Enable
V_{CC}	+5V
V_{SS}	Ground
NC	No Connect

FUNCTIONAL DIAGRAM



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256 Bit	Commercial Industrial	X2444 X2444I	16 x 16 Bit

Nonvolatile Static RAM

FEATURES

- **Ideal for use with Single Chip Microcomputers**
  - **—Static Timing**
  - **—Minimum I/O Interface**
  - **—Serial Port Compatible (COPS™, 8051)**
  - **—Easily Interfaces to Microcontroller Ports**
  - **—Minimum Support Circuits**
- **Software and Hardware Control of Nonvolatile Functions**
  - **—Maximum Store Protection**
- **TTL Compatible**
- **16 x 16 Organization**
- **Low Power Dissipation**
  - **—Active Current: 15 mA Typical**
  - **—Store Current: 8 mA Typical**
  - **—Standby Current: 6 mA Typical**
  - **—Sleep Current: 5 mA Typical**
- **8 Pin Mini-DIP Package**

DESCRIPTION

The Xicor X2444 is a serial 256 bit NOVRAM* featuring a static RAM configured 16 x 16, overlaid bit for bit with a nonvolatile E^2PROM array. The X2444 is fabricated with the same reliable N-channel floating gate MOS technology used in all Xicor 5V nonvolatile memories.

The Xicor NOVRAM design allows data to be transferred between the two memory arrays by means of software commands or external hardware inputs. A store operation (RAM data to E^2PROM) is completed in 10 ms or less and a recall operation (E^2PROM data to RAM) is completed in 2.5 μs or less.

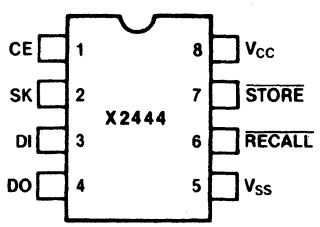
Xicor NOVRAMs are designed for unlimited write operations to RAM, either from the host or recalls from E^2PROM and a minimum 100,000 store operations. Data retention is specified to be greater than 100 years.

*NOVRAM is Xicor's nonvolatile static RAM device.

COPS™ is a trademark of National Semiconductor Corp.

Xicor

PIN CONFIGURATION

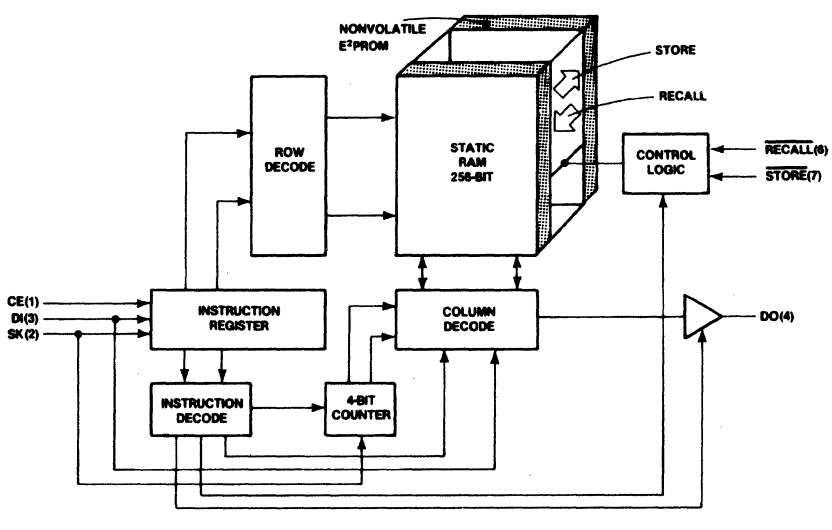


0042-1

PIN NAMES

CE	Chip Enable
SK	Serial Clock
DI	Serial Data In
DO	Serial Data Out
$\overline{\text{RECALL}}$	Recall
$\overline{\text{STORE}}$	Store
V_{CC}	+5V
V_{SS}	Ground

FUNCTIONAL DIAGRAM



0042-2

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Characteristics subject to change without notice

PRELIMINARY INFORMATION

2K Commercial Industrial X2402 X2402I 256 x 8 Bit

Electrically Erasable PROM

TYPICAL FEATURES

- Internally Organized 256 x 8
- 2 Wire Serial Interface
- Provides Bidirectional Data Transfer Protocol
- Eight Byte Page Write Mode
  —Minimizes Total Write Time Per Byte
- Self Timed Write Cycle
  —Typical Write Cycle Time of 5 ms
- Data Retention Greater Than 100 Years
- 8 Pin Mini-DIP Package

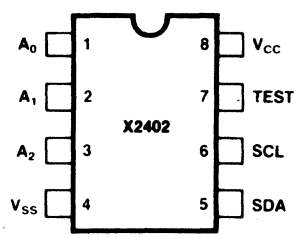
DESCRIPTION

The X2402 is a 2048 bit serial E²PROM, internally organized as one 256 x 8 page. The X2402 is fabricated with the same reliable N-channel floating gate MOS technology used in all Xicor 5V programmable nonvolatile memories.

The X2402 features a serial interface and software protocol allowing operation on a two wire bus.

Xicor E²PROMs are designed and tested for applications requiring extended endurance. Refer to RR504 for further endurance information. Data retention is specified to be greater than 100 years.

PIN CONFIGURATION

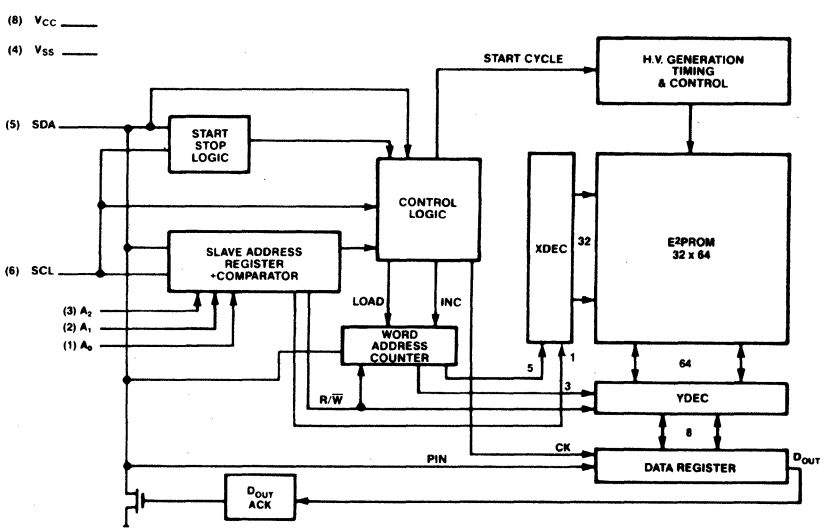


0035-1

PIN NAMES

1 to 3	A_0 to A_2 Address Inputs
4	V_{SS}
5	SDA Serial Data
6	SCL Serial Clock
7	**Test Input → to V_{SS}**
8	V_{CC}

FUNCTIONAL DIAGRAM



0035-2

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4K	Commercial Industrial	X2404 X2404I	512 x 8 Bit

Electrically Erasable PROM

TYPICAL FEATURES

- **Internally Organized as Two Pages**
  —Each 256 x 8
- **2 Wire Serial Interface**
- **Provides Bidirectional Data Transfer Protocol**
- **Eight Byte Page Write Mode**
  —Minimizes Total Write Time Per Byte
- **Self Timed Write Cycle**
  —Typical Write Cycle Time of 5 ms
- **Data Retention Greater Than 100 Years**
- **8 Pin Mini-DIP Package**

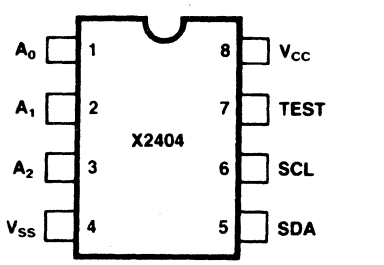
DESCRIPTION

The X2404 is a 4096 bit serial E²PROM, internally organized as two 256 x 8 pages. The X2404 is fabricated with the same reliable N-channel floating gate MOS technology used in all Xicor 5V programmable nonvolatile memories.

The X2404 features a serial interface and software protocol allowing operation on a two wire bus.

Xicor E²PROMs are designed and tested for applications requiring extended endurance. Refer to RR504 for further endurance information. Data retention is specified to be greater than 100 years.

PIN CONFIGURATION

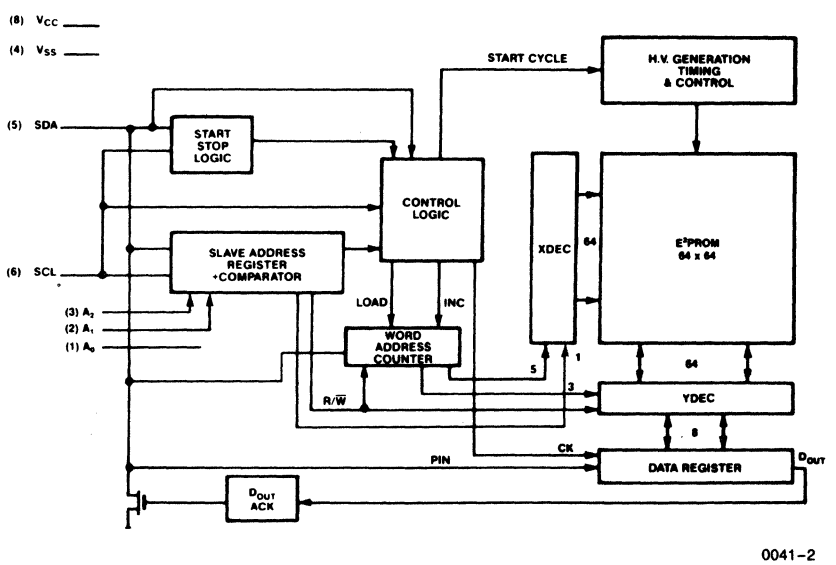


0041-1

PIN NAMES

1 to 3	A_0 to A_2 Address Inputs
4	V_{SS}
5	SDA Serial Data
6	SCL Serial Clock
7	**Test Input → to V_{SS}**
8	V_{CC}

FUNCTIONAL DIAGRAM



0041-2

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Characteristics subject to change without notice

ADVANCED INFORMATION

4K Commercial Industrial X24C04 X24C04I 512 x 8 Bit

Electrically Erasable PROM

TYPICAL FEATURES

- **Low Power CMOS**
  - **—2 mA Active Current Typical**
  - **—60 μA Standby Current Typical**
- **Internally Organized as Two Pages**
  - **—Each 256 x 8**
- **2 Wire Serial Interface**
- **Provides Bidirectional Data Transfer Protocol**
- **Sixteen Byte Page Write Mode**
  - **—Minimizes Total Write Time Per Byte**
- **Self Timed Write Cycle**
  - **—Typical Write Cycle Time of 5 ms**
- **Data Retention Greater Than 100 Years**
- **8 Pin Mini-DIP Package**

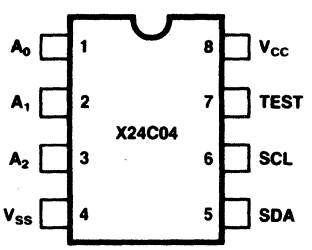
DESCRIPTION

The X24C04 is a CMOS 4096 bit serial E^2PROM, internally organized as two 256 x 8 pages. The X24C04 features a serial interface and software protocol allowing operation on a two wire bus.

Xicor E^2PROMs are designed and tested for applications requiring extended endurance. Data retention is specified to be greater than 100 years.

Xicor

PIN CONFIGURATION

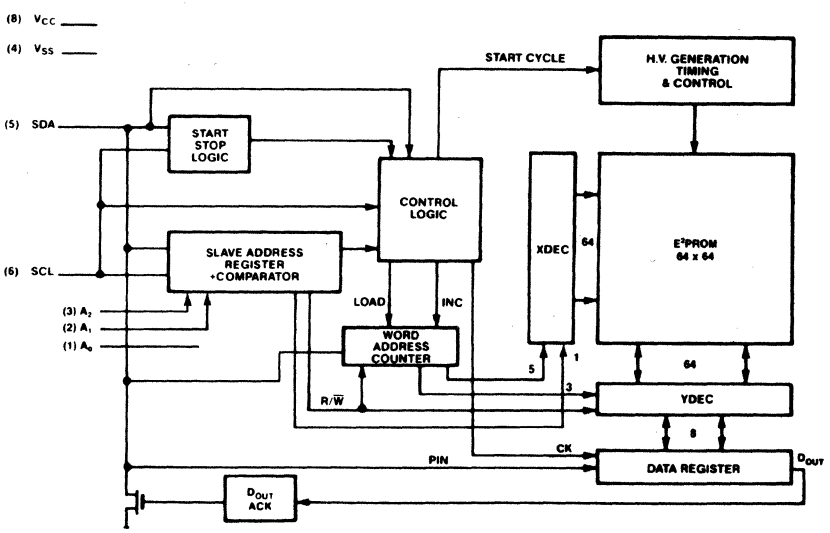


0046-1

PIN NAMES

1 to 3	A_0 to A_2 Address Inputs
4	V_{SS}
5	SDA Serial Data
6	SCL Serial Clock
7	**Test Input → to V_{SS}**
8	V_{CC}

FUNCTIONAL DIAGRAM



0046-2

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PRELIMINARY INFORMATION

16K	Commercial Industrial	X24C16 X24C16I	2048 x 8 Bit

Electrically Erasable PROM

TYPICAL FEATURES

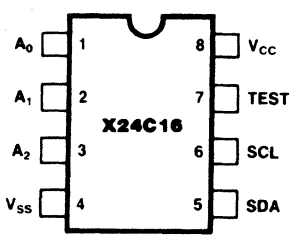
- **Low Power CMOS**
  - **—2 mA Active Current Typical**
  - **—60 μA Standby Current Typical**
- **Internally Organized as Eight Pages**
  - **—Each 256 x 8**
- **2 Wire Serial Interface**
- **Provides Bidirectional Data Transfer Protocol**
- **Sixteen Byte Page Write Mode**
  - **—Minimizes Total Write Time Per Byte**
- **Self Timed Write Cycle**
  - **—Typical Write Cycle Time of 5 ms**
- **Data Retention Greater Than 100 Years**
- **8 Pin Mini-DIP Package**

DESCRIPTION

The X24C16 is a CMOS 16,384 bit serial E²PROM, internally organized as eight 256 x 8 pages. The X24C16 features a serial interface and software protocol allowing operation on a two wire bus.

Xicor E²PROMs are designed and tested for applications requiring extended endurance. Data retention is specified to be greater than 100 years.

PIN CONFIGURATION

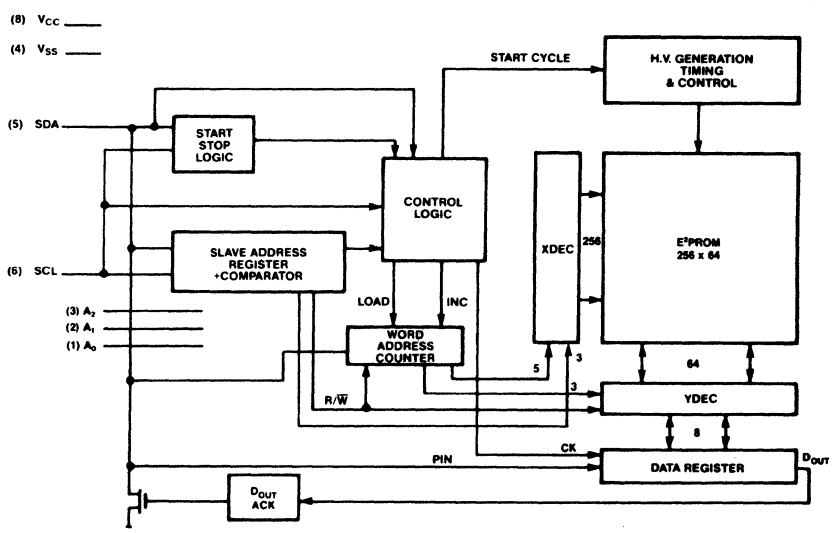


0038-1

PIN NAMES

1 to 3	A_0 to A_2 Address Inputs
4	V_{SS}
5	SDA Serial Data
6	SCL Serial Clock
7	**Test Input → to V_{SS}**
8	V_{CC}

FUNCTIONAL DIAGRAM



0038-2

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Electrically Erasable PROM

FEATURES

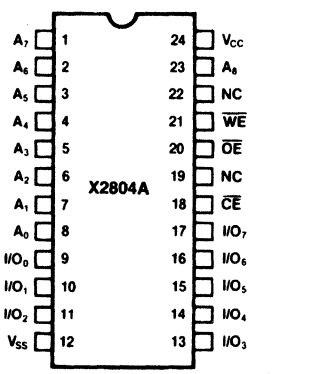
- **Simple Byte Write Operation**
  - **—No High Voltages Necessary**
  - **—Single TTL Level $\overline{WE}$ Signal Modifies Data**
  - **—Internally Latched Address and Data**
  - **—Self Timed Write**
  - **—Noise Protected $\overline{WE}$ Pin**
- **Reliable N-Channel Floating Gate MOS Technology**
- **Single 5V Supply**
- **Byte Write Time: 10 ms Max.**
- **Fast Access Time: 250 ns Max.**
- **Low Power Dissipation**
  - **—Active Current: 80 mA Max.**
  - **—Standby Current: 50 mA Max.**

DESCRIPTION

The Xicor X2804A is a 512 x 8 E²PROM, fabricated with the same reliable N-channel floating gate MOS technology used in all Xicor 5V programmable nonvolatile memories. The X2804A is compatible with the JEDEC approved pinout for byte-wide memories.

Xicor E²PROMs are designed and tested for applications requiring extended endurance. Refer to Device Operation for further endurance information. Data retention is specified to be greater than 100 years.

PIN CONFIGURATION

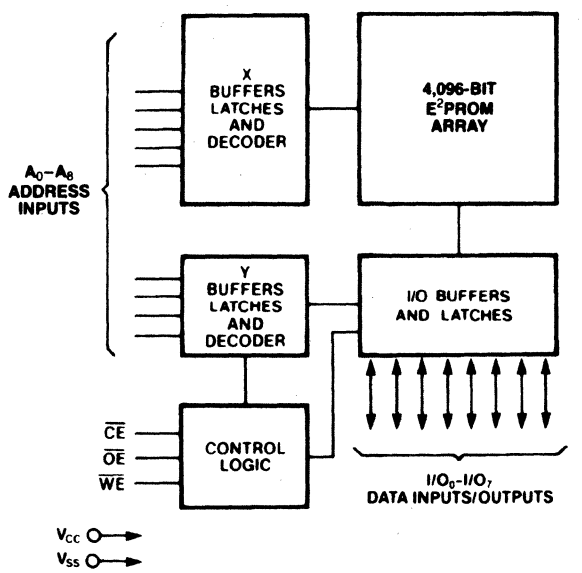


0044-1

PIN NAMES

A_0–A_8	Address Inputs
I/O_0–I/O_7	Data Input/Output
$\overline{WE}$	Write Enable
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
V_{CC}	+5V
V_{SS}	Ground
NC	No Connect

FUNCTIONAL DIAGRAM



0044-2

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16K Commercial Industrial X2816B X2816BI 2048 x 8 Bit

Electrically Erasable PROM

FEATURES

- 250 ns Access Time
- High Performance Advanced NMOS Technology
- Fast Write Cycle Times
  - —16-Byte Page Write Operation
  - —Byte or Page Write Cycle: 5 ms Typical
  - —Complete Memory Rewrite: 640 ms Typical
  - —Effective Byte Write Cycle Time of 300 μs Typical
- $\overline{\text{DATA}}$ Polling
  - —Allows User to Minimize Write Cycle Time
- Simple Byte and Page Write
  - —Single TTL Level $\overline{\text{WE}}$ Signal
  - —Internally Latched Address and Data
  - —Automatic Write Timing
- JEDEC Approved Byte-Wide Pinout

DESCRIPTION

The Xicor X2816B is a 2K x 8 E²PROM, fabricated with an advanced, high performance N-channel floating gate MOS technology. Like all Xicor programmable nonvolatile memories it is a 5V only device. The X2816B features the JEDEC approved pinout for byte-wide memories, compatible with industry standard RAMs, ROMs and EPROMs.

The X2816B supports a 16-byte page write operation, typically providing a 300 μs/byte write cycle, enabling the entire memory to be written in less than 640 ms. The X2816B also features $\overline{\text{DATA}}$ Polling, a system software support scheme used to indicate the early completion of a write cycle.

Xicor E²PROMs are designed and tested for applications requiring extended endurance. Data retention is specified to be greater than 100 years.

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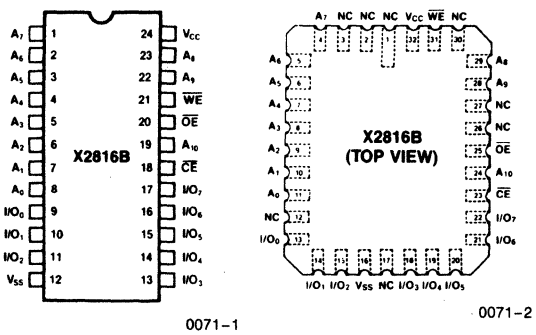
PIN CONFIGURATIONS

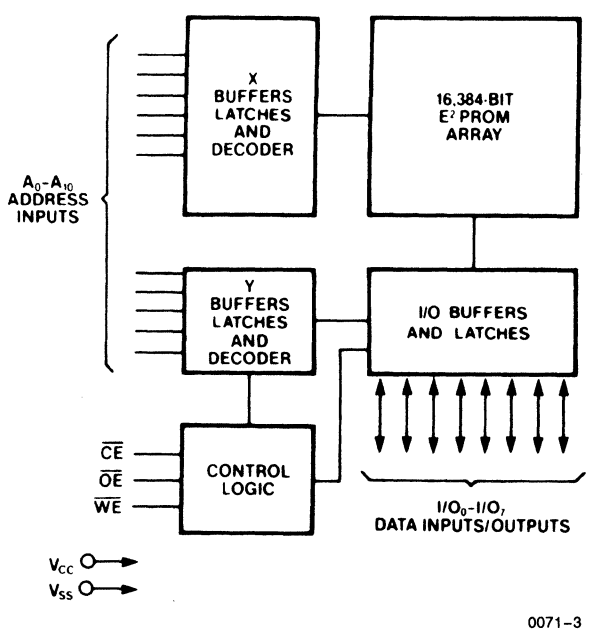


0071-1 0071-2

PIN NAMES

A_0–A_{10}	Address Inputs
I/O_0–I/O_7	Data Input/Output
$\overline{WE}$	Write Enable
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
V_{CC}	+5V
V_{SS}	Ground
NC	No Connect

FUNCTIONAL DIAGRAM



0071-3

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Electrically Erasable PROM

FEATURES

- 250 ns Access Time
- Fast Write Cycle Times
  - —16-Byte Page Write Operation
  - —Byte or Page Write Cycle: 5 ms Typical
  - —Complete Memory Rewrite: 2.6 Sec. Typical
  - —Effective Byte Write Cycle Time of 300 μs Typical
- $\overline{\text{DATA}}$ Polling
  - —Allows User to Minimize Write Cycle Time
- Simple Byte and Page Write
  - —Single TTL Level $\overline{\text{WE}}$ Signal
  - —Internally Latched Address and Data
  - —Automatic Write Timing
- JEDEC Approved Byte-Wide Pinout

DESCRIPTION

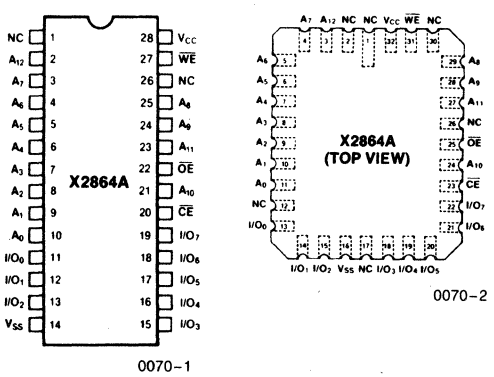
The Xicor X2864A is a 8K x 8 E²PROM, fabricated with the same reliable N-channel floating gate MOS technology used in all Xicor 5V programmable nonvolatile memories. The X2864A features the JEDEC approved pinout for byte-wide memories, compatible with industry standard RAMs, ROMs and EPROMs.

The X2864A supports a 16-byte page write operation, effectively providing a 300 μs/byte write and enabling the entire memory to be written in less than 2.6 seconds. The X2864A also features $\overline{\text{DATA}}$ Polling, a system software support scheme used to indicate the early completion of a write cycle.

Xicor E²PROMs are designed and tested for applications requiring extended endurance. Refer to Device Operation for further endurance information. Data retention is specified to be greater than 100 years.

Xicor

PIN CONFIGURATIONS



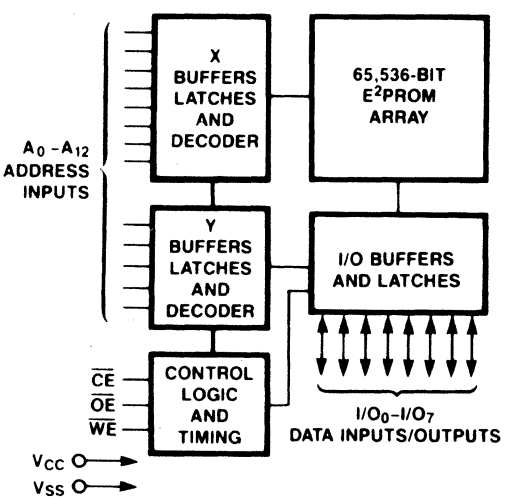
0070-1

0070-2

PIN NAMES

A_0–A_{12}	Address Inputs
I/O_0–I/O_7	Data Input/Output
$\overline{\text{WE}}$	Write Enable
$\overline{\text{CE}}$	Chip Enable
$\overline{\text{OE}}$	Output Enable
V_{CC}	+5V
V_{SS}	Ground
NC	No Connect

FUNCTIONAL DIAGRAM



0070-3

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64K Commercial Industrial X2864B X2864BI 8192 x 8 Bit

Electrically Erasable PROM

TYPICAL FEATURES

- 120 ns Access Time
- High Performance Scaled NMOS Technology
- Fast Write Cycle Times
  - —32-Byte Page Write Operation
  - —Byte or Page Write Cycle: 3 ms Typical
  - —Complete Memory Rewrite: 750 ms Typical
  - —Effective Byte Write Cycle Time of 95 μs Typical
- $\overline{\text{DATA}}$ Polling
  - —Allows User to Minimize Write Cycle Time
- Simple Byte and Page Write
  - —Single TTL Level $\overline{\text{WE}}$ Signal
  - —Internally Latched Address and Data
  - —Automatic Write Timing
- JEDEC Approved Byte-Wide Pinout

DESCRIPTION

The Xicor X2864B is a 8K x 8 E²PROM, fabricated with an advanced, high performance N-channel floating gate MOS technology. Like all Xicor programmable nonvolatile memories it is a 5V only device. The X2864B features the JEDEC approved pinout for byte-wide memories, compatible with industry standard RAMs, ROMs and EPROMs.

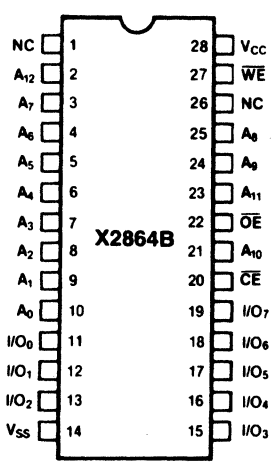
The X2864B supports a 32-byte page write operation, effectively providing a 95 μs/byte write cycle and enabling the entire memory to be written in less than 750 ms. The X2864B also features $\overline{\text{DATA}}$ Polling, a system software support scheme used to indicate the early completion of a write cycle.

Xicor E²PROMs are designed and tested for applications requiring extended endurance. Data retention is specified to be greater than 10 years.

Xicor

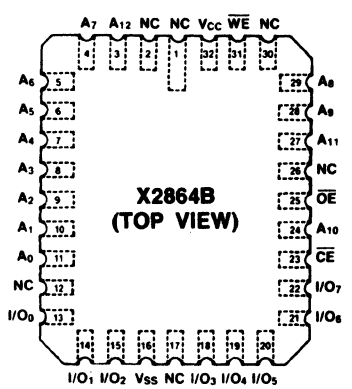
PIN CONFIGURATIONS

PLASTIC CERDIP FLAT PACK



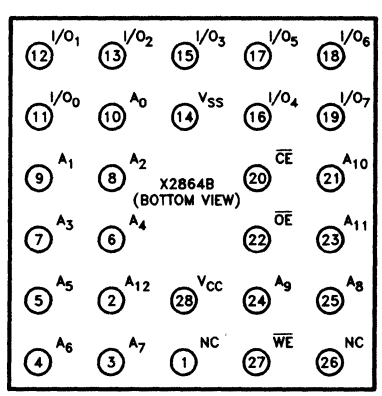
0031-1

PLCC LCC



0031-2

PGA



0031-11

PIN NAMES

A_0–A_{12}	Address Inputs
I/O_0–I/O_7	Data Input/Output
$\overline{\text{WE}}$	Write Enable
$\overline{\text{CE}}$	Chip Enable
$\overline{\text{OE}}$	Output Enable
V_{CC}	+5V
V_{SS}	Ground
NC	No Connect

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64K Commercial Industrial X2864H X2864HI 8192 x 8 Bit

Electrically Erasable PROM

TYPICAL FEATURES

- 70 ns Access Time
- High Performance Scaled NMOS Technology
- Fast Write Cycle Times
  - —32-Byte Page Write Operation
  - —Byte or Page Write Cycle: 3 ms Typical
  - —Complete Memory Rewrite: 750 ms Typical
  - —Effective Byte Write Cycle Time of 95 μs Typical
- $\overline{\text{DATA}}$ Polling
  - —Allows User to Minimize Write Cycle Time
- Simple Byte and Page Write
  - —Single TTL Level $\overline{\text{WE}}$ Signal
  - —Internally Latched Address and Data
  - —Automatic Write Timing
- JEDEC Approved Byte-Wide Pinout

DESCRIPTION

The Xicor X2864H is a high speed 8K x 8 E²PROM, fabricated with Xicor's proprietary, high performance, N-channel floating gate MOS technology. Like all Xicor programmable nonvolatile memories it is a 5V only device. The X2864H features the JEDEC approved pinout for byte-wide memories, compatible with industry standard RAMs, ROMs, and EPROMs.

The X2864H supports a 32-byte page write operation, effectively providing a 95 μs/byte write cycle and enabling the entire memory to be written in less than 750 ms. The X2864H also features $\overline{\text{DATA}}$ Polling, a system software support scheme used to indicate the early completion of a write cycle.

Xicor E²PROMs are designed and tested for applications requiring extended endurance. Data retention is specified to be greater than 10 years.

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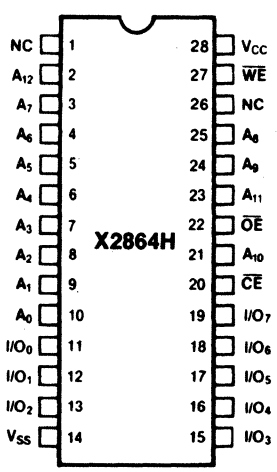
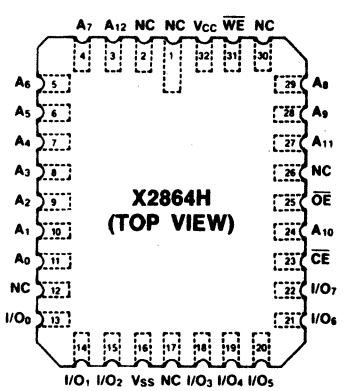
PIN CONFIGURATIONS

PLASTIC CERDIP FLAT PACK



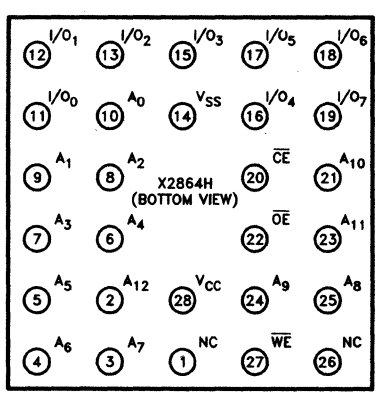
0034-1

PLCC LCC



0034-2

PGA



0034-9

PIN NAMES

A_0–A_{12}	Address Inputs
I/O_0–I/O_7	Data Input/Output
$\overline{\text{WE}}$	Write Enable
$\overline{\text{CE}}$	Chip Enable
$\overline{\text{OE}}$	Output Enable
V_{CC}	+5V
V_{SS}	Ground
NC	No Connect

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ADVANCED INFORMATION

64K Commercial Industrial X28C64 X28C64I 8K x 8 Bit

Electrically Erasable PROM

FEATURES

- LOW Power CMOS
  - —60 mA Active Current Max.
  - —200 μA Standby Current Max.
- Fast Write Cycle Times
  - —64-Byte Page Write Operation
  - —Byte or Page Write Cycle: 5 ms Typical
  - —Complete Memory Rewrite: 0.625 Sec. Typical
  - —Effective Byte Write Cycle Time: 78 μs Typical
- Software Data Protection
- End of Write Detection
  - —$\overline{\text{DATA}}$ Polling
  - —Toggle Bit
- Simple Byte and Page Write
  - —Single TTL Compatible $\overline{\text{WE}}$ Signal
  - —Internally Latched Address and Data
  - —Automatic Write Timing
- JEDEC Approved Byte-Wide Pinout

DESCRIPTION

The Xicor X28C64 is a 8K x 8 E^2PROM, fabricated with Xicor's proprietary, high performance, floating gate CMOS technology. Like all Xicor programmable nonvolatile memories the X28C64 is a 5V only device. The X28C64 features the JEDEC approved pinout for byte-wide memories, compatible with industry standard RAMs.

The X28C64 supports a 64-byte page write operation, effectively providing a 78 μs/byte write cycle and enabling the entire memory to be typically written in 0.625 seconds. The X28C64 also features $\overline{\text{DATA}}$ Polling, a system software support scheme used to indicate the early completion of a write cycle. In addition, the X28C64 includes a user-optional software data protection mode that further enhances Xicor's hardware write protect capability.

Xicor E^2PROMs are designed and tested for applications requiring extended endurance. Data retention is specified to be greater than 10 years.

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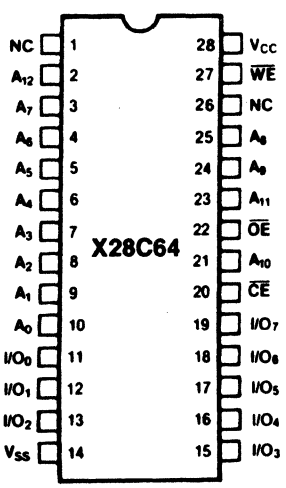
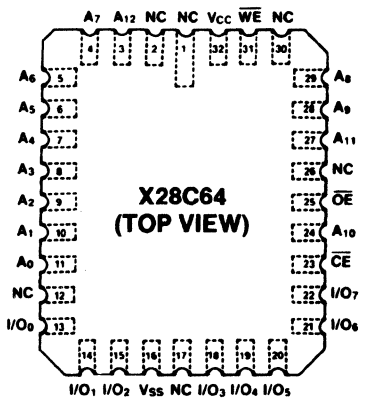
PIN CONFIGURATIONS

PLASTIC
CERDIP
FLAT PACK



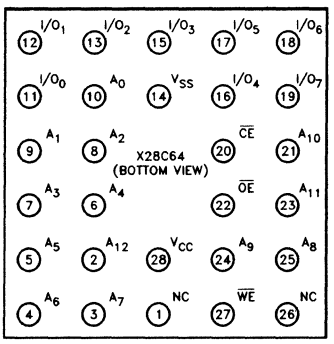
0101-1

PLCC
LCC



0101-2

PGA



0101-3

PIN NAMES

A_0–A_{12}	Address Inputs
I/O_0–I/O_7	Data Input/Output
$\overline{\text{WE}}$	Write Enable
$\overline{\text{CE}}$	Chip Enable
$\overline{\text{OE}}$	Output Enable
V_{CC}	+5V
V_{SS}	Ground
NC	No Connect

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PRELIMINARY INFORMATION

256K Commercial Industrial X28256 X28256I 32K x 8 Bit

Electrically Erasable PROM

FEATURES

- 250 ns Access Time
- Fast Write Cycle Times
  - —64-Byte Page Write Operation
  - —Byte or Page Write Cycle: 5 ms Typical
  - —Complete Memory Rewrite: 2.5 Sec. Typical
  - —Effective Byte Write Cycle Time: 78 μs Typical
- Software Data Protection
- End of Write Detection
  - —$\overline{\text{DATA}}$ Polling
  - —Toggle Bit
- Simple Byte and Page Write
  - —Single TTL Level $\overline{\text{WE}}$ Signal
  - —Internally Latched Address and Data
  - —Automatic Write Timing
- Upward Compatible with X2864A
- JEDEC Approved Byte-Wide Pinout

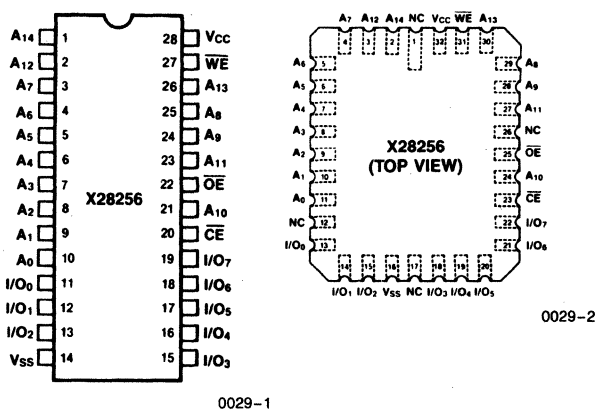
DESCRIPTION

The Xicor X28256 is a 32K x 8 E²PROM, fabricated with Xicor's proprietary, high performance, N-channel floating gate MOS technology. Like all Xicor programmable nonvolatile memories the X28256 is a 5V only device. The X28256 features the JEDEC approved pinout for byte-wide memories, compatible with industry standard RAMs.

The X28256 supports a 64-byte page write operation, effectively providing a 78 μs/byte write cycle and enabling the entire memory to be typically written in less than 2.5 seconds. The X28256 also features $\overline{\text{DATA}}$ Polling, a system software support scheme used to indicate the early completion of a write cycle. In addition, the X28256 includes a user-optional software data protection mode that further enhances Xicor's hardware write protect capability.

Xicor E²PROMs are designed and tested for applications requiring extended endurance. Data retention is specified to be greater than 10 years.

PIN CONFIGURATIONS



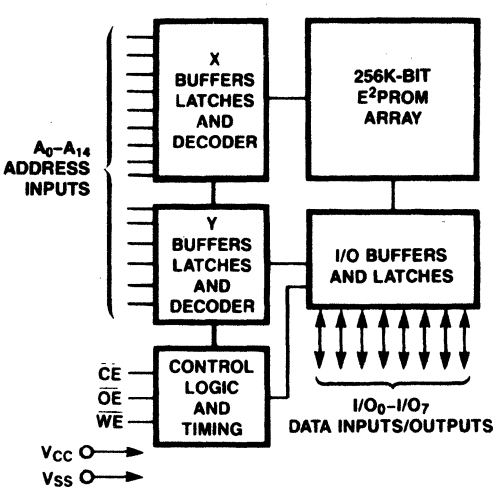
0029-1

0029-2

PIN NAMES

A_0–A_{14}	Address Inputs
I/O_0–I/O_7	Data Input/Output
$\overline{WE}$	Write Enable
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
V_{CC}	+5V
V_{SS}	Ground
NC	No Connect

FUNCTIONAL DIAGRAM



0029-3

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Xicor®

256K | **Commercial** / **Industrial** | **X28C256** / **X28C256I** | **32K x 8 Bit**

Electrically Erasable PROM

FEATURES

- **LOW Power CMOS**
  - **—60 mA Active Current Max.**
  - **—200 μA Standby Current Max.**
- **Fast Write Cycle Times**
  - **—64-Byte Page Write Operation**
  - **—Byte or Page Write Cycle: 5 ms Typical**
  - **—Complete Memory Rewrite: 2.5 Sec. Typical**
  - **—Effective Byte Write Cycle Time: 78 μs Typical**
- **Software Data Protection**
- **End of Write Detection**
  - **—$\overline{\text{DATA}}$ Polling**
  - **—Toggle Bit**
- **Simple Byte and Page Write**
  - **—Single TTL Compatible $\overline{\text{WE}}$ Signal**
  - **—Internally Latched Address and Data**
  - **—Automatic Write Timing**
- **Upward Compatible with X2864A**
- **JEDEC Approved Byte-Wide Pinout**

DESCRIPTION

The Xicor X28C256 is a 32K x 8 E²PROM, fabricated with Xicor's proprietary, high performance, floating gate CMOS technology. Like all Xicor programmable nonvolatile memories the X28C256 is a 5V only device. The X28C256 features the JEDEC approved pinout for byte-wide memories, compatible with industry standard RAMs.

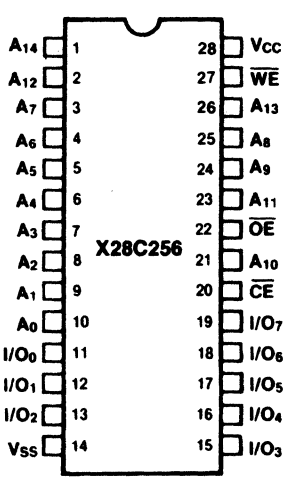
The X28C256 supports a 64-byte page write operation, effectively providing a 78 μs/byte write cycle and enabling the entire memory to be typically written in less than 2.5 seconds. The X28C256 also features $\overline{\text{DATA}}$ Polling, a system software support scheme used to indicate the early completion of a write cycle. In addition, the X28C256 includes a user-optional software data protection mode that further enhances Xicor's hardware write protect capability.

Xicor E²PROMs are designed and tested for applications requiring extended endurance. Data retention is specified to be greater than 10 years.

Xicor

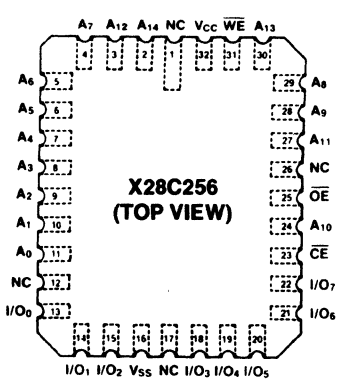
PIN CONFIGURATIONS

PLASTIC CERDIP FLAT PACK



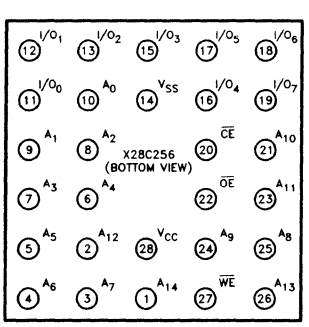
0067-1

PLCC LCC



0067-2

PGA



0067-21

PIN NAMES

A_0–A_{14}	Address Inputs
I/O_0–I/O_7	Data Input/Output
$\overline{\text{WE}}$	Write Enable
$\overline{\text{CE}}$	Chip Enable
$\overline{\text{OE}}$	Output Enable
V_{CC}	+5V
V_{SS}	Ground
NC	No Connect

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PRELIMINARY INFORMATION

256K Commercial Industrial X28C256B X28C256BI 32K x 8 Bit

Electrically Erasable PROM

FEATURES

- 150 ns Access Time
- LOW Power CMOS
  - —60 mA Active Current Max.
  - —200 μA Standby Current Max.
- Fast Write Cycle Times
  - —64-Byte Page Write Operation
  - —Byte or Page Write Cycle: 5 ms Typical
  - —Complete Memory Rewrite: 2.5 Sec. Typical
  - —Effective Byte Write Cycle Time: 78 μs Typical
- Software Data Protection
- End of Write Detection
  - —$\overline{\text{DATA}}$ Polling
  - —Toggle Bit
- Simple Byte and Page Write
  - —Single TTL Compatible $\overline{\text{WE}}$ Signal
  - —Internally Latched Address and Data
  - —Automatic Write Timing
- Upward Compatible with X2864A
- JEDEC Approved Byte-Wide Pinout

DESCRIPTION

The Xicor X28C256B is a 32K x 8 E^2PROM, fabricated with Xicor's proprietary, high performance, floating gate CMOS technology. Like all Xicor programmable nonvolatile memories the X28C256B is a 5V only device. The X28C256B features the JEDEC approved pinout for byte-wide memories, compatible with industry standard RAMs.

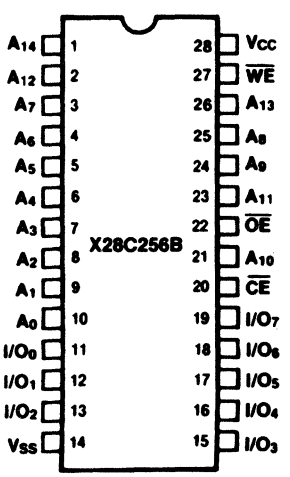
The X28C256B supports a 64-byte page write operation, effectively providing a 78 μs/byte write cycle and enabling the entire memory to be typically written in less than 2.5 seconds. The X28C256B also features $\overline{\text{DATA}}$ Polling, a system software support scheme used to indicate the early completion of a write cycle. In addition, the X28C256B includes a user-optional software data protection mode that further enhances Xicor's hardware write protect capability.

Xicor E^2PROMs are designed and tested for applications requiring extended endurance. Data retention is specified to be greater than 10 years.

Xicor

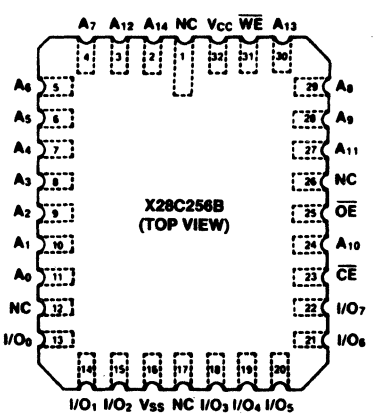
PIN CONFIGURATIONS

PLASTIC CERDIP



0098-1

PLCC LCC



0098-2

PIN NAMES

A_0–A_{14}	Address Inputs
I/O_0–I/O_7	Data Input/Output
$\overline{\text{WE}}$	Write Enable
$\overline{\text{CE}}$	Chip Enable
$\overline{\text{OE}}$	Output Enable
V_{CC}	+5V
V_{SS}	Ground
NC	No Connect

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ADVANCED INFORMATION

Xicor®

1M	Commercial Industrial	X28C010 X28C010I	128K x 8 Bit

Electrically Erasable PROM

FEATURES

- Low Power CMOS
  - —50 mA Active Current Max.
  - —500 μA Standby Current Max.
- High Speed Page Write Operation
- Fast Write Cycle Times
  - —256-Byte Page Size
  - —Byte or Page Write Cycle: 5 ms Typical
  - —Complete Memory Rewrite: 2.5 Sec.
  - —Effective Byte Write Cycle Time: 19 μs
- End of Write Detection
  - —$\overline{DATA}$ Polling
  - —Toggle Bit Testing
    - —Accommodates Multiprocessor Applications
- JEDEC Approved Software Data Protection
- JEDEC Approved Byte-Wide Pinout for DIPs

DESCRIPTION

The Xicor X28C010 is a 128K x 8 E²PROM, fabricated with Xicor's proprietary, high performance, floating gate CMOS technology. Like all Xicor programmable nonvolatile memories the X28C010 is a 5V only device. The X28C010 features the JEDEC approved pinout for byte-wide memories, compatible with industry EPROMs.

The X28C010 supports a 256-byte page write operation, effectively providing a 19 μs/byte write cycle and enabling the entire memory to be written in less than 2.5 seconds. The X28C010 also features $\overline{DATA}$ Polling and Toggle Bit test, system software support schemes used to indicate the early completion of a write cycle. In addition, the X28C010 supports the JEDEC approved Software Data Protection option.

Xicor E²PROMs are designed and tested for applications requiring extended endurance. Data retention is specified to be greater than 10 years.

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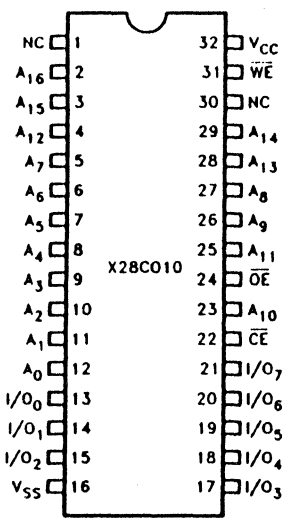
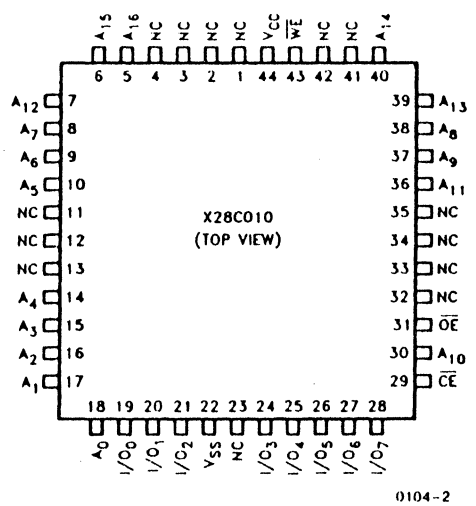
PIN CONFIGURATIONS

SIDE BRAZE



0104-1

LCC



0104-2

PIN NAMES

A_0–A_{16}	Address Inputs
I/O_0–I/O_7	Data Input/Output
$\overline{WE}$	Write Enable
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
V_{CC}	+5V
V_{SS}	Ground
NC	No Connect

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PRELIMINARY INFORMATION

1Megabit Module XM28C010 128K x 8 Bit

Electrically Erasable PROM

FEATURES

- High Density 1Megabit (128K x 8) E²PROM Module
- Access Time of 250 ns at −55°C to +125°C
- Base Memory Component: Xicor CMOS X28C256
- JEDEC Standard 32-Pin 600 Mil Wide Ceramic Side Braze Package
- Pin Compatible with the X28C010 1Megabit Monolithic CMOS E²PROM
- Fast Write Cycle Times Supported by:
  - —Internal Program Cycle 10 ms Max.
  - —64-Byte Page
  - —$\overline{\text{DATA}}$ Polling
  - —Toggle Status Bit
- High Rel Module Available with:
  - —100% MIL-STD-883 Compliant Components
  - —100% Screening and MIL-STD-883 Processing of Modules
- Software Data Protection

DESCRIPTION

The XM28C010 is a high density 1Megabit E²PROM comprised of four X28C256 32K x 8 LCCs mounted on a co-fired multilayered ceramic substrate. The XM28C010 is configured 128K x 8 bit and features the JEDEC approved pinout for byte-wide memories, compatible with the monolithic X28C010.

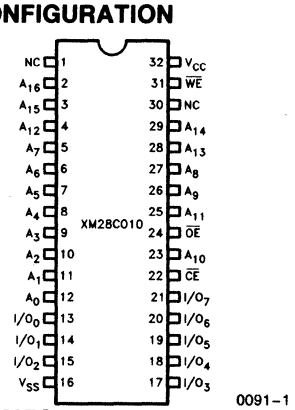
The XM28C010 is available in commercial, industrial and military temperature ranges. The military temperature range module is built with MIL-STD-883 Class B microcircuit components. In addition, after being assembled all High Rel modules undergo 100% screening.

The XM28C010 supports a 64-byte page write operation, this, combined with $\overline{\text{DATA}}$ Polling or Toggle Bit testing, effectively provides a 78 μs/byte write cycle, enabling the module memory array to be rewritten in 10 seconds.

The XM28C010 will also support Software Data Protection, a user-optional method of protecting data during power transitions.

The XM28C010 provides the same high endurance and data retention as the base memory components.

PIN CONFIGURATION

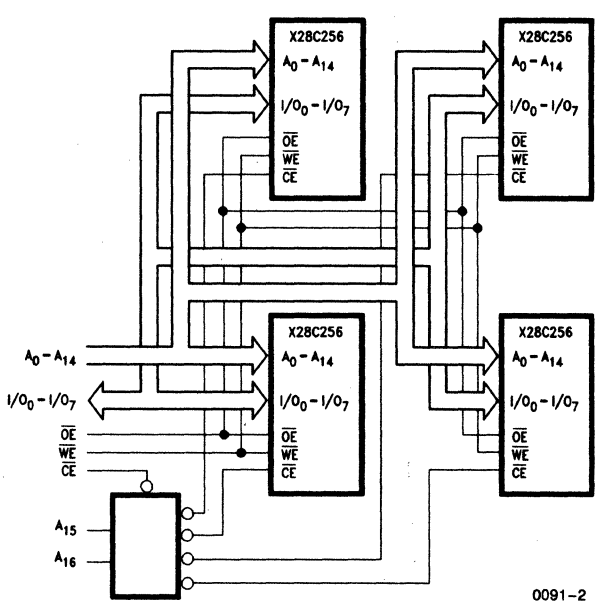


0091-1

PIN NAMES

A_0–A_{16}	Address Inputs
I/O_0–I/O_7	Data Input/Output
$\overline{WE}$	Write Enable
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
V_{CC}	+5V
V_{SS}	Ground
NC	No Connect

FUNCTIONAL DIAGRAM



0091-2

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PRELIMINARY INFORMATION

Commercial X9MME
Industrial X9MMEI

E²POT™ Digitally Controlled Potentiometer

FEATURES

- Solid State Reliability
- Single Chip MOS Implementation
- Three Wire TTL Control
- Operates From Standard 5V Supply
- 99 Resistive Elements
  - —Temperature Compensated
  - —±20% End to End Resistance Range
- 100 Wiper Tap Points
  - —Wiper Position Digitally Controlled
  - —Wiper Position Stored in Nonvolatile Memory Then Automatically Recalled on Power-Up
- 100 Year Wiper Position Retention
- 8 Pin Mini-DIP Package
- 14 Pin SOIC Package

DESCRIPTION

The Xicor X9MME is a solid state nonvolatile potentiometer and is ideal for digitally controlled resistance trimming.

The X9MME is a resistor array composed of 99 resistive elements. Between each element and at either end are tap points accessible to the wiper element. The position of the wiper element on the array is controlled by the $\overline{CS}$, U/$\overline{D}$, and $\overline{INC}$ inputs. The position of the wiper can be stored in nonvolatile memory and is recalled upon a subsequent power-up.

The resolution of the X9MME is equal to the maximum resistance value divided by 99. As an example; for the X9503 (50 KΩ) each tap point represents 505Ω.

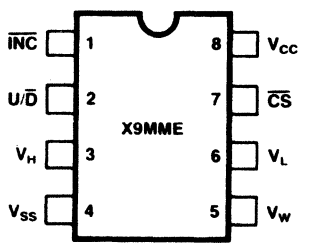
Xicor E² products are designed and tested for applications requiring extended endurance. Refer to Xicor reliability reports for further endurance information.

E²POT™ is a trademark of Xicor, Inc.

Xicor

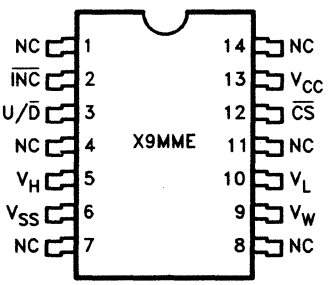
PIN CONFIGURATIONS

PLASTIC



0039-1

SOIC



0039-12

PIN NAMES

V_H	High Terminal of Pot
V_W	Wiper Terminal of Pot
V_L	Low Terminal of Pot
V_{SS}	Ground
V_{CC}	System Power
U/$\overline{D}$	Up/Down Control
$\overline{INC}$	Wiper Movement Control
$\overline{CS}$	Chip Select for Wiper Movement/Storage
NC	No Connect

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Quality is maintained automatically in the semiconductor photolithography clean room at the TI Sherman, Texas plant. Computers and robotics help produce reliable products here and in TI's other manufacturing facilities worldwide.

Quality is a way of life for more than 76,000 Texas Instruments employees around the world.

Good companies worldwide are achieving ever-higher quality levels. So, today, it is the rate of improvement versus competition that determines quality leadership. Quality leadership, in turn, determines success in the marketplace.

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Since inventing the integrated circuit thirty years ago, Texas Instruments has competed successfully against the world's toughest competition. World-class quality is key to continuing that success into the 21st Century. Our commitment to that end is absolute and total.

TEXAS INSTRUMENTS

SCICM

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